MPM3901

60V, 1A, Synchronous Step-Down Power Module with an Integrated Inductor, AEC-Q100 Qualified

DESCRIPTION

The MPM3901 is an easy-to-use, fully integrated, fixed-frequency, synchronous step-down power module with a built-in inductor and power MOSFETs. It can achieve up to 1A of continuous output current (I_{OUT}) with peak current control for excellent transient response.

The wide 4.5V to 60V input voltage (V_{IN}) range accommodates a variety of step-down applications in 12V and 24V automotive battery input environments. The 2µA shutdown-mode quiescent current (I_Q) makes the MPM3901 ideal for battery-powered applications.

The MPM3901 employs advanced asynchronous modulation (AAM) mode to achieve high efficiency during light-load conditions by scaling down the frequency to reduce switching and gate driver losses.

Standard features include built-in soft start (SS), enable (EN) control, and power good (PG) indication. A high duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPM3901 provides over-current protection (OCP) with valley current detection to avoid current runaway. The device also provides short-circuit protection (SCP) with hiccup mode, input under-voltage lockout (UVLO), and automatic recovery thermal protection.

With internal compensation, the MPM3901 offers a very compact solution with a minimal number of readily available, standard external components. It is available in a QFN-19 (4mmx6mm) package with wettable flanks.

FEATURES

- **Designed for Automotive Applications**
  - 4.5V to 40V Continuous Operating Input Voltage (V_{IN}) Range
  - Up to 60V Input Transient Voltage for Automotive Load Dump
  - Up to 1A of Continuous Output Current (I_{OUT})
  - Low-Dropout Mode

FEATURES *(continued)*

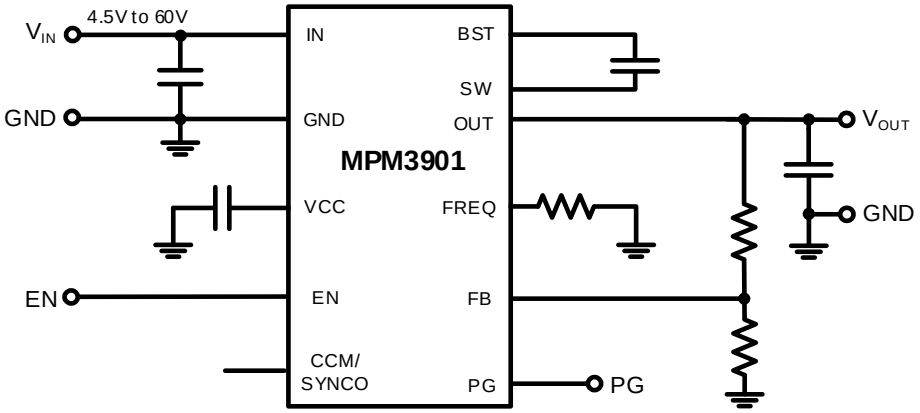
  - 90ns Minimum On Time (t_{ON_MIN})
  - Operating T_J from -40°C to +150°C
  - Available in AEC-Q100 Grade 1
- **Increases Battery Life**
  - 2µA Low Shutdown Mode Current
  - 40µA Quiescent Current (I_Q)
  - Selectable AAM Mode or FCCM at Light Loads
- **High Performance for Improved Thermals:**
  - 250mΩ/45mΩ Internal Power MOSFETs
  - Available in a QFN-19 (4mmx6mm) Package with Wettable Flanks
- **Optimized for EMC/EMI**
  - Integrated Power Inductor
  - Configurable f_{SW} Up to 2.2MHz
  - CISPR 25 Class 5 Compliant
- **Additional Features**
  - High-Efficiency Synchronous Mode Control
  - 180° Out-of-Phase SYNCO Clock
  - Feedback (FB) Tolerance: 1% at Room Temperature, 2% at Full Temperature
  - Internal 0.45ms Soft Start (SS)
  - Power Good (PG) Indicator
  - Over-Current Protection (OCP)
  - SCP with Hiccup Mode
  - Thermal Shutdown
- **Functional Safety System Design Capability**
  - MPSafe™-Compatible: Functional Safety Supporting Document Available

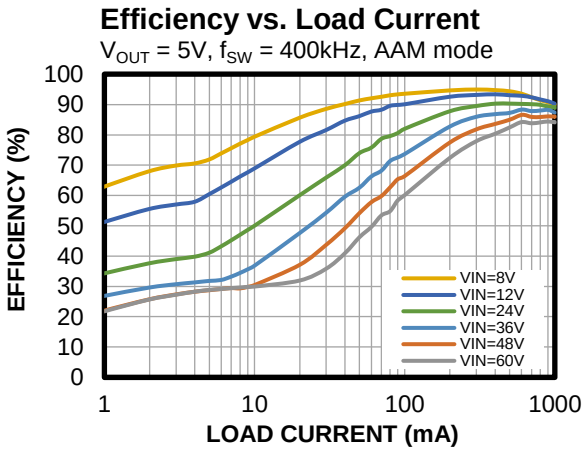
MPSafe™ FuSa Compatible

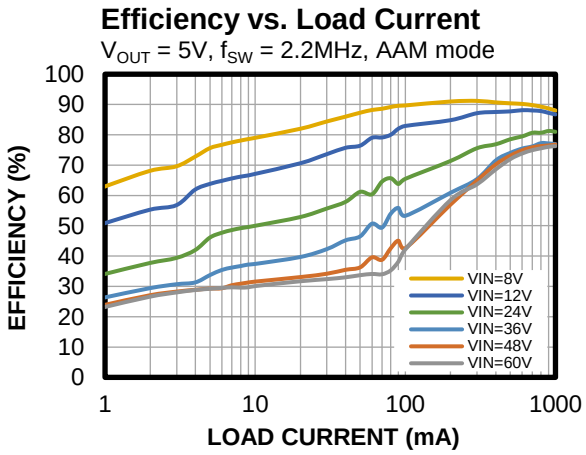
APPLICATIONS

- Automotive Infotainment
- Automotive Lamps and LEDs
- Automotive Motor Control

TYPICAL APPLICATION







ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPM3901GQWE***	QFN-19 (4mmx6mm)	*See Below*	3
MPM3901GQWE-AEC1***			

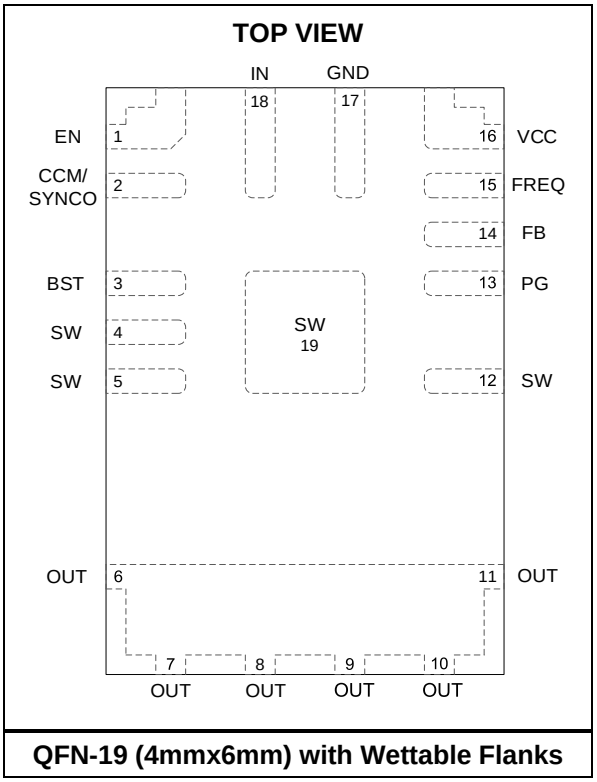
* For Tape & Reel, add suffix -Z (e.g. MPM3901GQWE-AEC1-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flanks

TOP MARKING

MPSYWW
MP3901
LLLLLL
ME

MPS: MPS prefix
Y: Year code
WW: Week code
MP3901: Part number
LLLLLL: Lot number
M: Module
E: Wettable flanks

PACKAGE REFERENCE



QFN-19 (4mmx6mm) with Wettable Flanks

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable.** Pull the EN pin above 1.45V to turn on the device. Float the pin or pull EN below 1.12V to turn off the device.
2	CCM/ SYNCO	**Mode selection or synchronization output.** To configure the converter for continuous conduction mode (CCM), connect the CCM pin to GND via a 10kΩ to 300kΩ resistor. Float the pin to force the converter to enter advanced asynchronous modulation (AAM) mode under light-load conditions. To configure the device for the synchronization output, use the SYNCO pin to output an out-of-phase 180° clock to the other devices.
3	BST	**Bootstrap.** Connect a capacitor between the BST and SW pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
4, 5, 12, 19	SW	**Switch output.** The SW pin is the output of the internal MOSFETs.
6, 7, 8, 9, 10, 11	OUT	**Power output.** Connect the load to the OUT pin. An output capacitor (C_{OUT}) is required.
13	PG	**Power good indicator.** PG is an open-drain pin that requires connecting a pull-up resistor to the power source. If the output voltage (V_{OUT}) is within 90% to 109.5% of the nominal voltage, then PG is pulled up to the power source; if V_{OUT} exceeds 116% or drops below 84% of the nominal voltage, then PG goes low.
14	FB	**Feedback point.** The FB pin is the negative input of the error amplifier (EA). Connect FB to the tap of an external resistor divider between the output and GND to set the regulation voltage. In addition, power good and under-voltage lockout (UVLO) circuits use FB to monitor V_{OUT}.
15	FREQ	**Configurable switching frequency.** Connect a resistor between FREQ and GND to set the switching frequency (f_{SW}).
16	VCC	**Internal bias supply.** The VCC pin supplies power to the internal control circuit and gate drivers. A decoupling capacitor exceeding 1µF is required to be connected to ground, placed close to VCC.
17	GND	**IC ground.** Connect the GND pin to larger copper areas and the negative terminals of the input capacitor (C_{IN}) and C_{OUT}.
18	IN	**Input supply.** The IN pin supplies all power to the converter. Place a decoupling capacitor to ground, as close as possible to the IC, to reduce switching spikes.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{OUT} .....-0.3V to +65V
V_{SW} .....-0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 5.5V
All other pins .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-19 (4mmx6mm) 3.69W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (3)
Charged-device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Continuous supply voltage (V_{IN}).....4.5V to 40V
Output voltage (V_{OUT}).....1V to 12V
Load current range .....0A to 1A
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-19 (4mmx6mm)
JESD51-7.....29.1.....3.5..°C/W (5)
EVM3901-QW-00A.....33.9.....°C/W (6)

Ψ_{JT}

QFN-19 (4mmx6mm)
JESD51-7.....4...°C/W (5)
EVM3901-QW-00A…….....6.9..°C/W (6)

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom, and the Ψ_{JT} value shows the characterization parameter from the junction-to-case top.
6) Measured on an MPS standard EVB, a 2oz copper thickness, 4-layer PCB (8.3cmx8.3cm). The Ψ_{JT} value shows the characterization parameter from the junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply and Under-Voltage Lockout (UVLO)						
Supply quiescent current	I_Q	No load, V_{FB} = 0.85V, AAM mode		40	65	µA
Supply shutdown current	I_{SD}	V_{EN} = 0V		2	5	µA
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_RISING}$		3.8	4	4.2	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		3.3	3.5	3.7	V
V_{IN} UVLO hysteresis threshold	$V_{IN\_UVLO\_HYS}$			500		mV
Output and Regulation						
Regulated feedback (FB) reference voltage	V_{REF}	T_J = 25°C	0.792	0.8	0.808	V
		T_J = -40°C to +125°C	0.784	0.8	0.816	V
FB input current	I_{FB}	V_{FB} = 0.85V		10	50	nA
MOSFETs, Inductor, and Frequency						
HS-FET on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V, T_J = 25°C	150	250	350	mΩ
		V_{BST} - V_{SW} = 5V, T_J = -40°C to +125°C	100	250	500	
LS-FET on resistance	$R_{DS(ON)\_LS}$	T_J = 25°C	30	45	60	mΩ
		T_J = -40°C to +125°C	20	45	90	
SW leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 0V or 60V		0.1	30	µA
Inductor DC resistance (7)	R_L			305		mΩ
Inductance (7)	L			10		µH
Switching frequency	f_{SW}	R_{FREQ} = 76.8kΩ	300	400	500	kHz
		R_{FREQ} = 28kΩ	750	1000	1250	kHz
		R_{FREQ} = 12.1kΩ	1850	2200	2650	kHz
Minimum on time (8)	t_{ON_MIN}			90		ns
Minimum off time (8)	t_{OFF_MIN}			100		ns
Power Good (PG)						
PG current sink capacity	V_{PG_SINK}	Sink 4mA			300	mV
PG deglitch time	$t_{PG\_DEGLITCH}$	Rising edge		70		µs
		Falling edge		25		µs
PG leakage current	I_{PG_LKG}			10	1000	nA
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	88	90	92	% of V_{REF}
		V_{FB} falling	107	109.5	112	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	82	84	86	
		V_{FB} rising	114	116	118	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable (EN)						
EN input rising threshold	V_{EN_RISING}		1.38	1.45	1.52	V
EN input falling threshold	$V_{EN\_FALLING}$		1.05	1.12	1.19	V
EN threshold hysteresis	V_{EN_HYS}			330		mV
EN input current	I_{EN}	V_{EN} = 2V		0.7		µA
EN turn-off delay	t_{EN_DELAY}		5			µs
Bootstrap (BST)						
V_{BST} - V_{SW} UVLO threshold				1.4	2.5	V
V_{BST} - V_{SW} UVLO hysteresis				60		mV
Soft Start (SS) and VCC						
Soft-start time	t_{SS}			0.45		ms
VCC regulator	V_{CC}	I_{CC} = 0mA	4.6	4.8	5	V
Protections						
Peak current limit	I_{PEAK_LIMIT}	20% duty cycle	1.4	1.95	2.5	A
Valley current limit	I_{VALLEY_LIMIT}		1.4			A
Zero-current detection (ZCD) threshold	I_{ZCD}	AAM mode	-100	140	+300	mA
Negative current limit	I_{LIMIT_NEG}	FCCM	-2	-1.3	-0.8	A
Thermal shutdown (8)	T_{SD}	Rising temperature		170		°C
Thermal shutdown hysteresis (8)	T_{SD_SYS}			25		°C

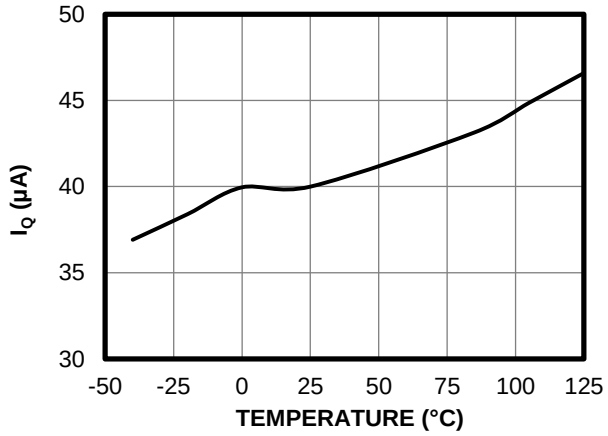
Notes:

7) Not tested in production. Guaranteed by manufacturer.
8) Derived from the bench characterization. Not tested in production.

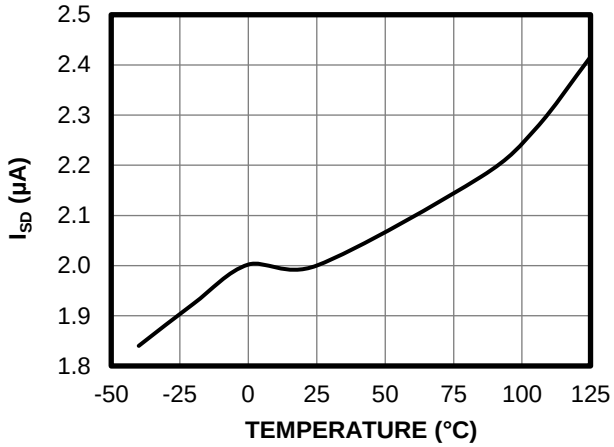
TYPICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

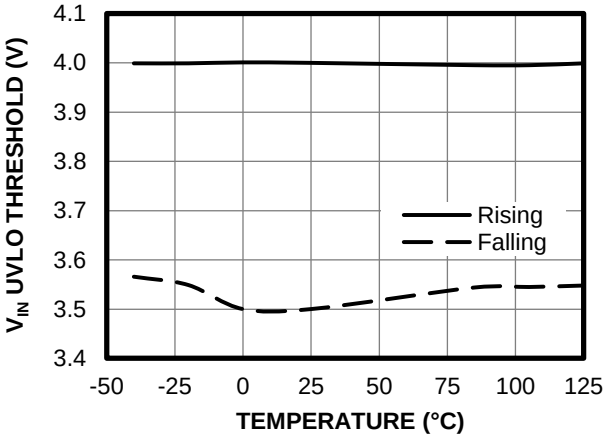
Quiescent Current vs. Temperature



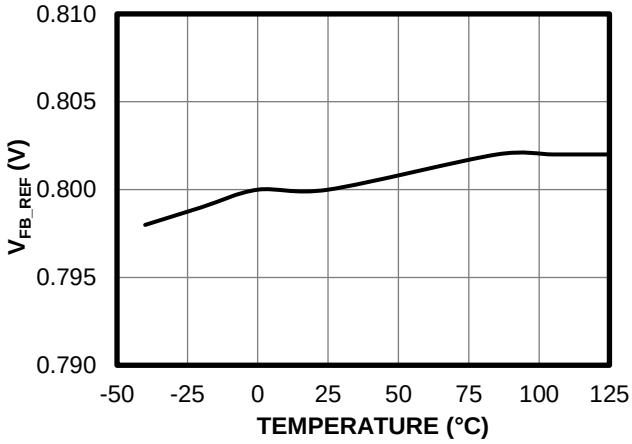
Shutdown Current vs. Temperature



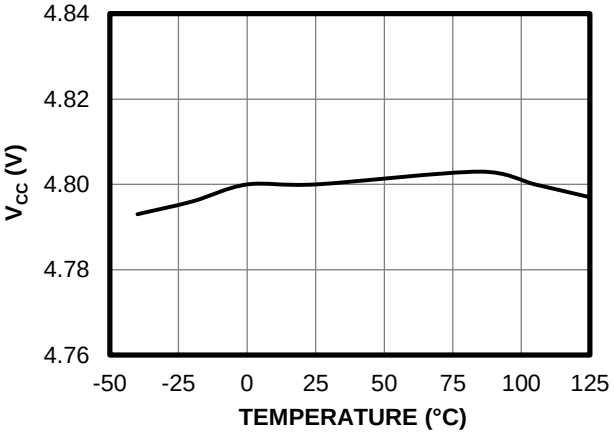
V_{IN} UVLO Threshold vs. Temperature



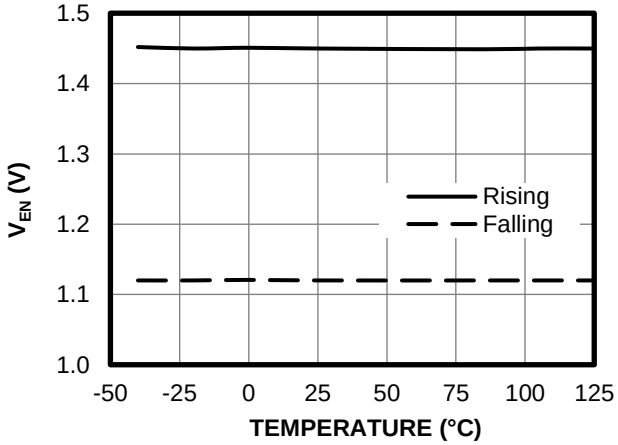
Feedback Reference Voltage vs. Temperature



VCC Voltage vs. Temperature



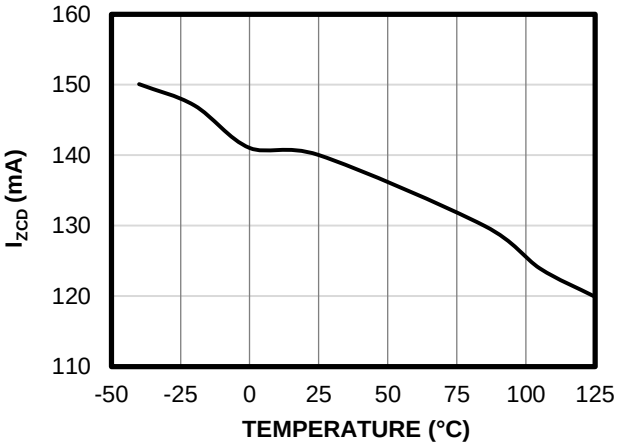
EN Threshold vs. Temperature



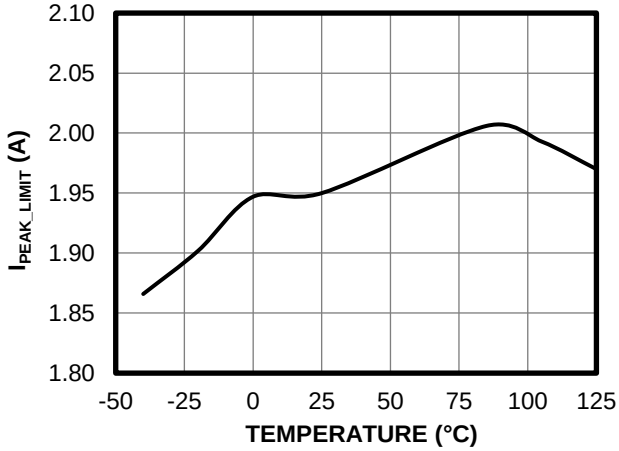
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

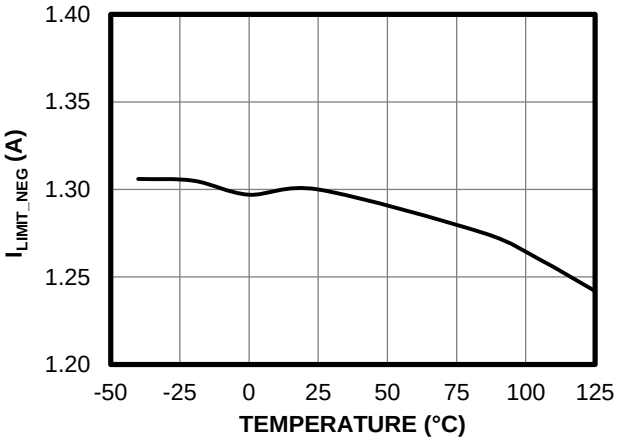
ZCD Threshold vs. Temperature



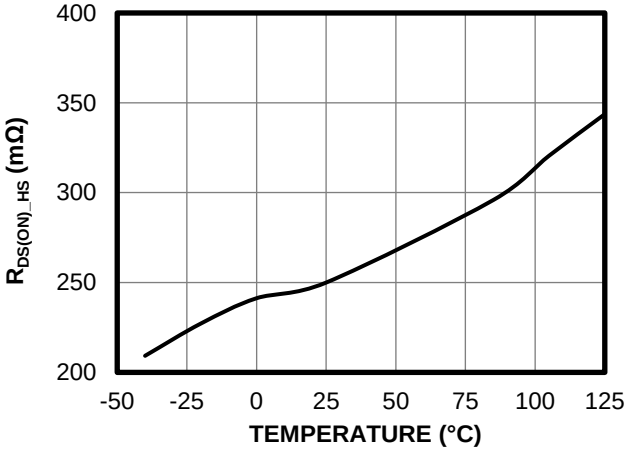
Peak Current Limit vs. Temperature



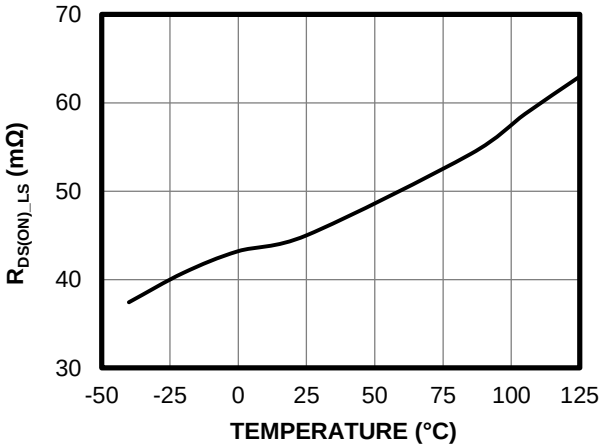
Negative Current Limit vs. Temperature



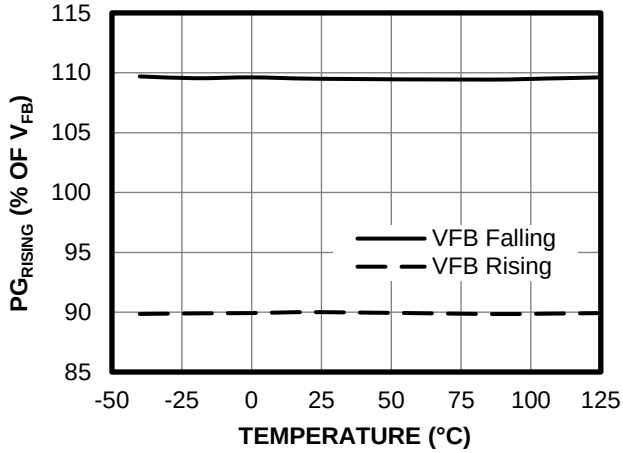
HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature



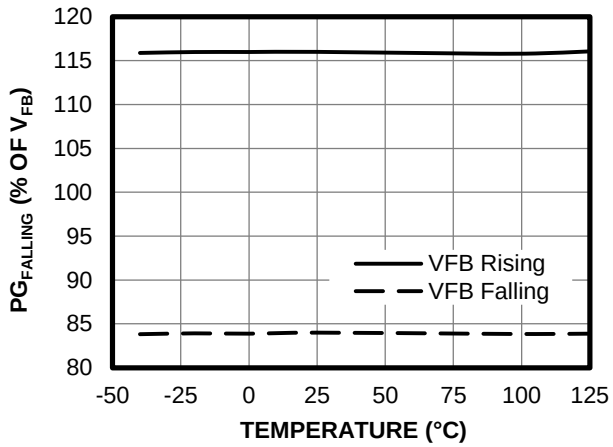
PG Rising Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

PG Falling Threshold vs. Temperature

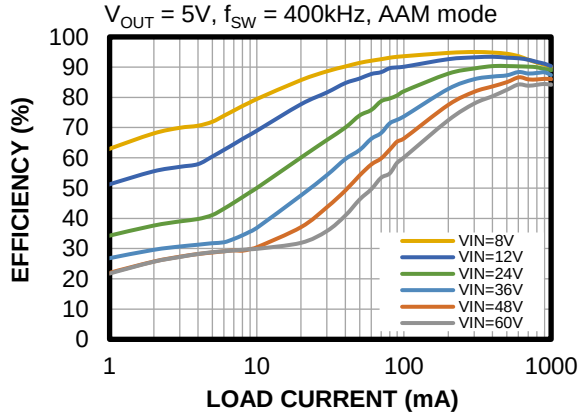


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode, T_A = 25°C, unless otherwise noted.

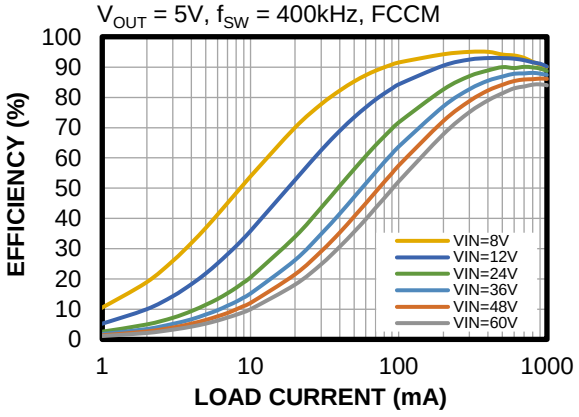
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode



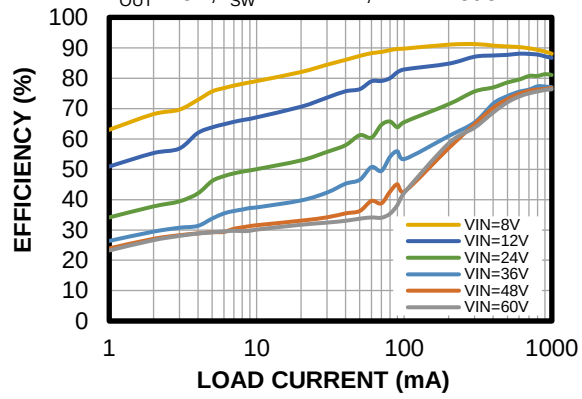
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 400kHz, FCCM



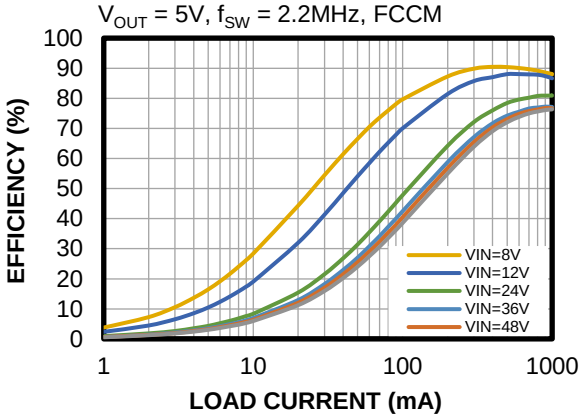
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 2.2MHz, AAM mode



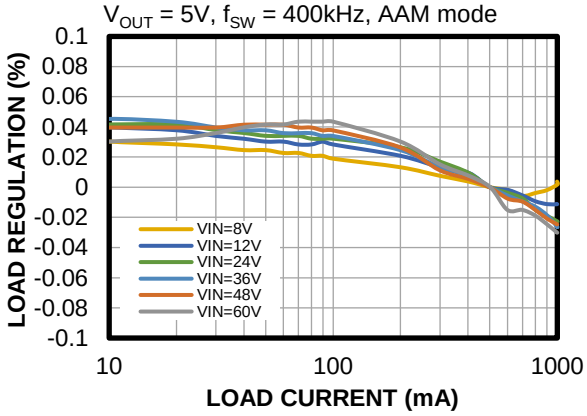
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 2.2MHz, FCCM



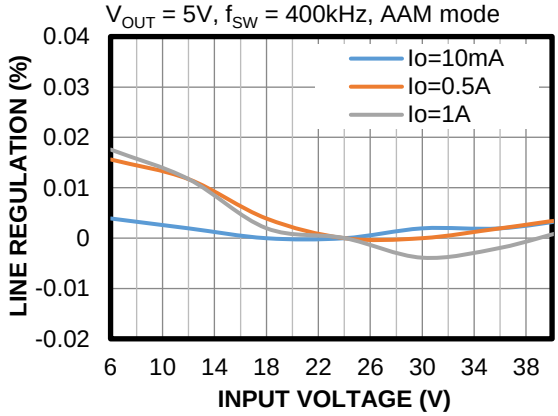
Load Regulation

V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode



Line Regulation

V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode

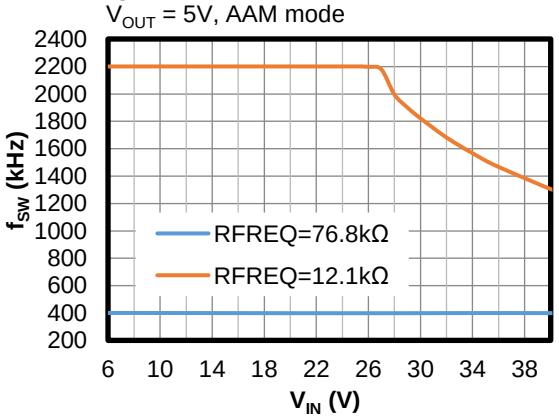


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode, T_A = 25°C, unless otherwise noted.

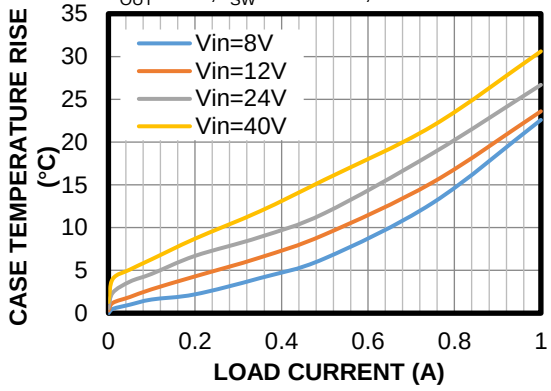
f_{SW} vs. V_{IN}

V_{OUT} = 5V, AAM mode



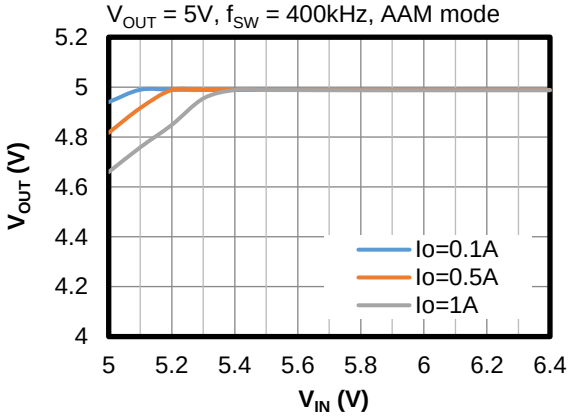
Case Temperature Rise vs. Load Current

V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode



Low-Dropout Mode vs. Input Voltage

V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode

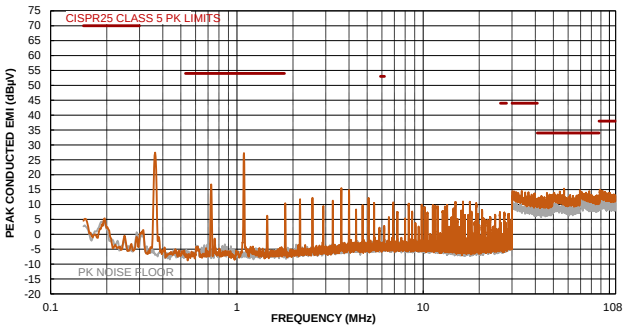


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode, T_A = 25°C, unless otherwise noted. (9)

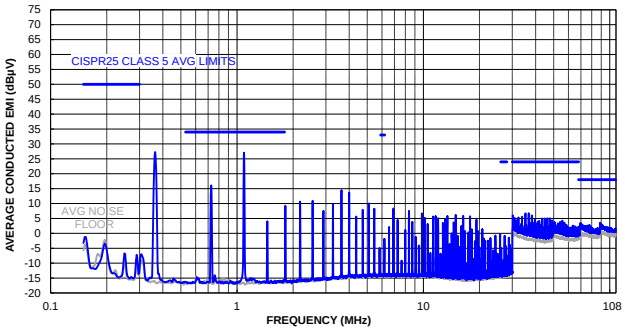
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



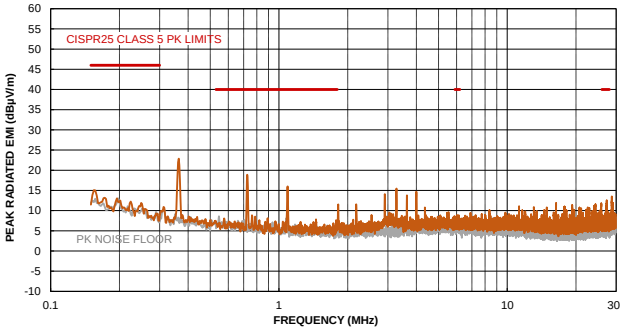
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



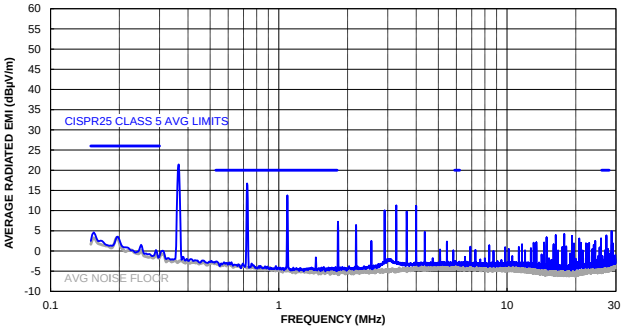
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



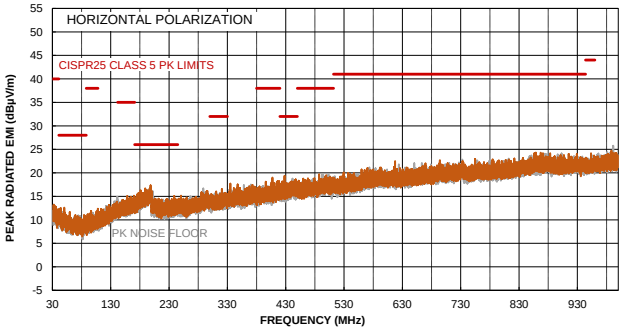
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



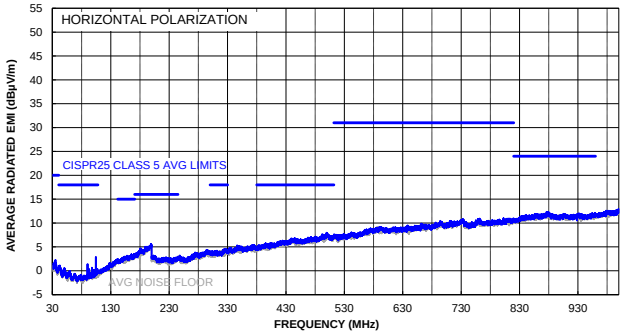
CISPR 25 Class 5 Peak Radiated Horizontal

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Horizontal

Horizontal, 30MHz to 1GHz

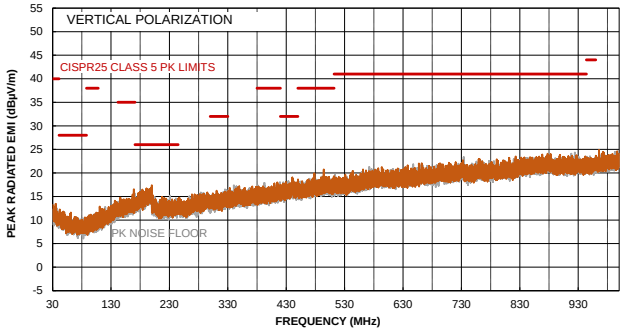


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, AAM mode, T_A = 25°C, unless otherwise noted. (9)

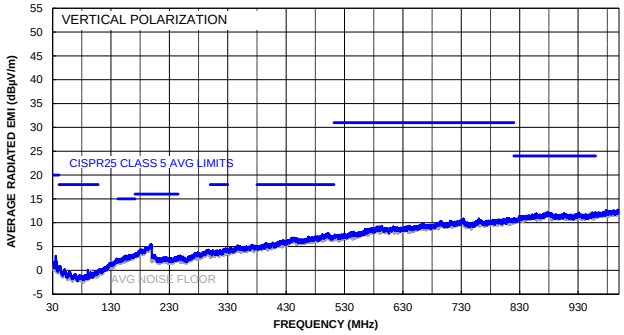
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

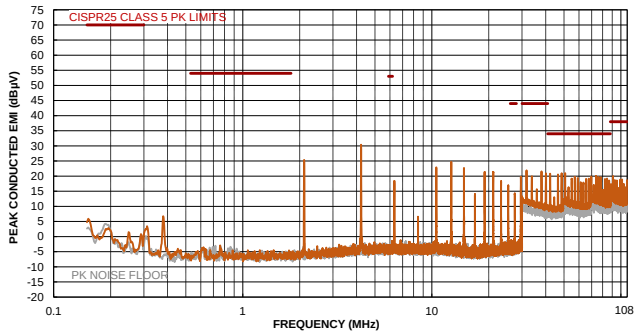
9) The EMC test results are based on the application circuit with an EMI filter (see Figure 11 on page 32) and tested on the EVM3901-QW-00A.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (10)

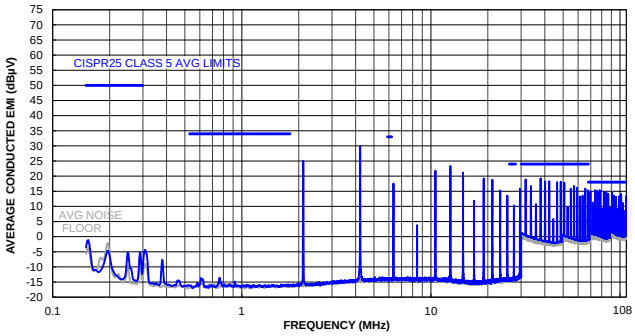
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



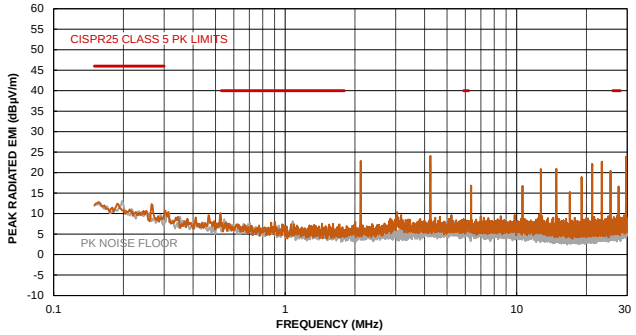
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



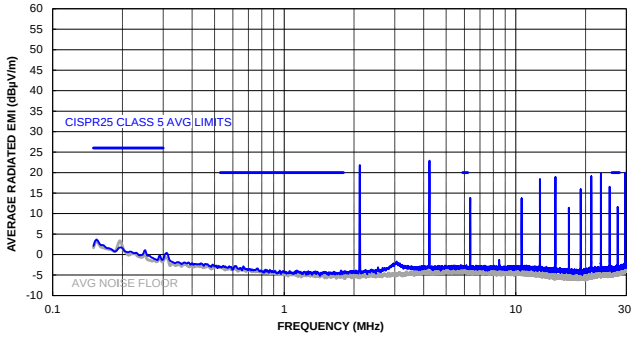
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



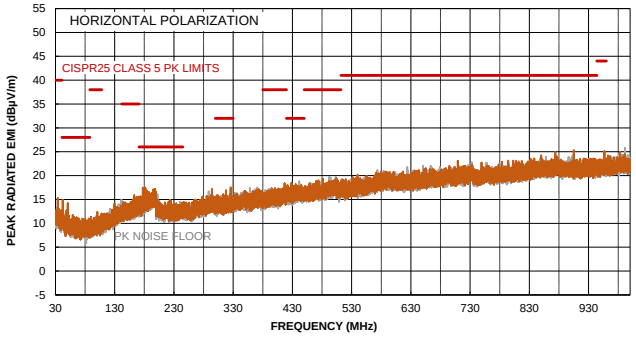
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



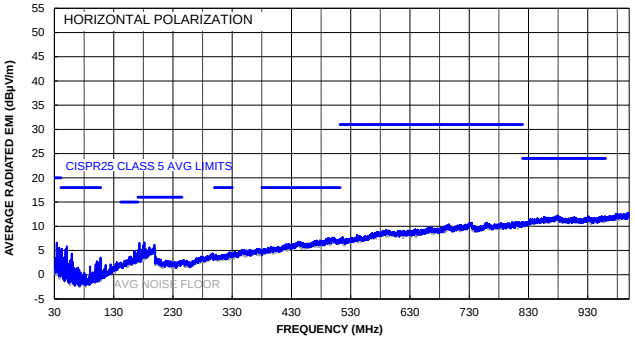
CISPR 25 Class 5 Peak Radiated Horizontal

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Horizontal

Horizontal, 30MHz to 1GHz

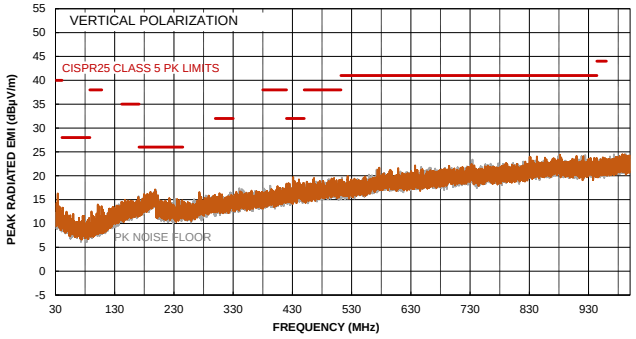


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (10)

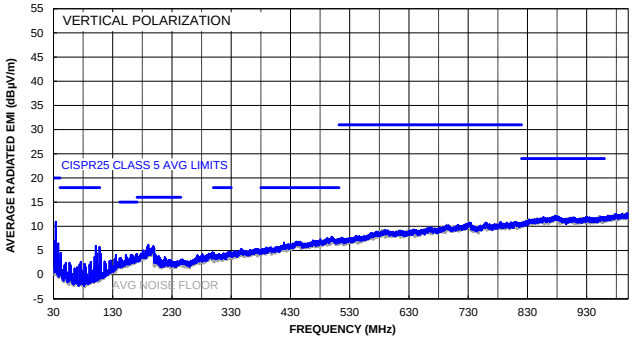
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

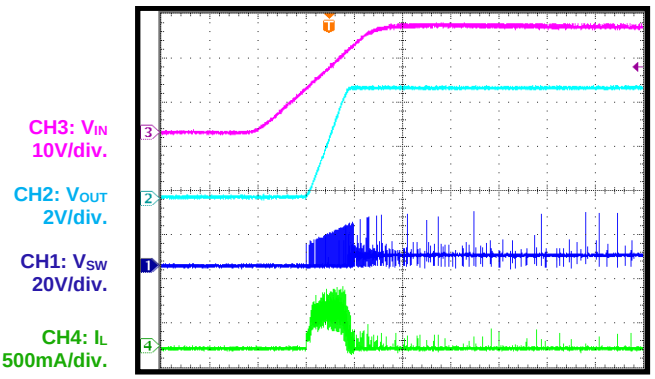
9) The EMC test results are based on the application circuit with an EMI filter (see Figure 12 on page 32) and tested on the EVM3901-QW-00A.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

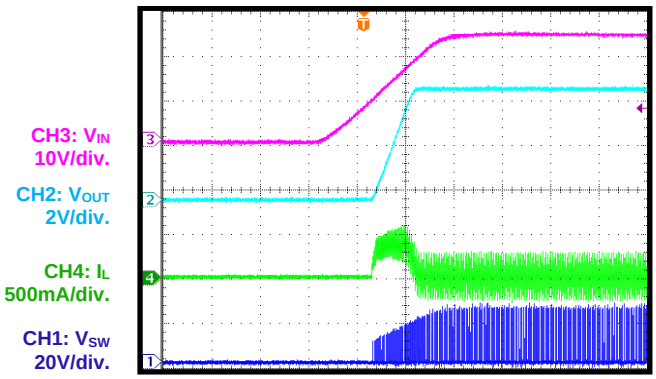
Start-Up through VIN

I_{OUT} = 0A, AAM mode



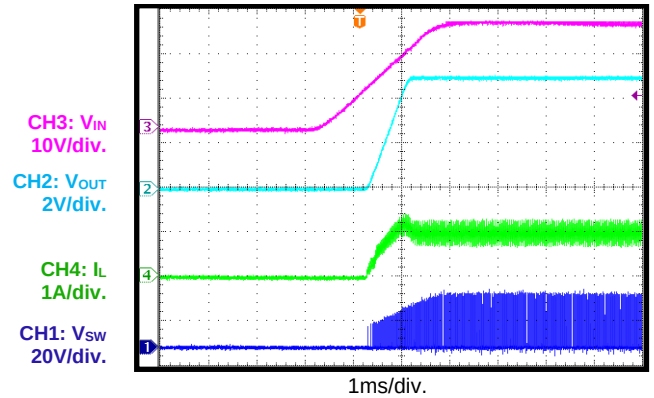
Start-Up through VIN

I_{OUT} = 0A, FCCM



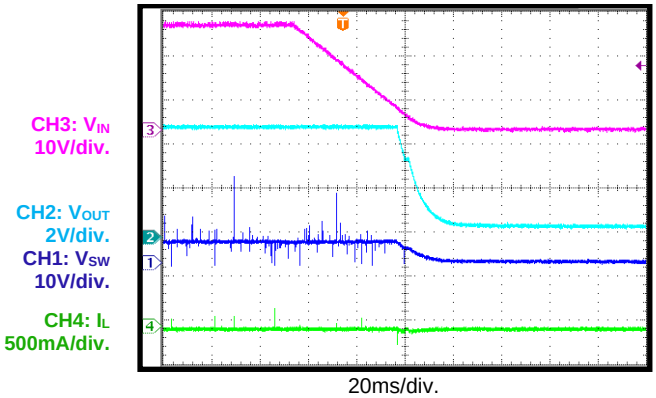
Start-Up through VIN

I_{OUT} = 1A



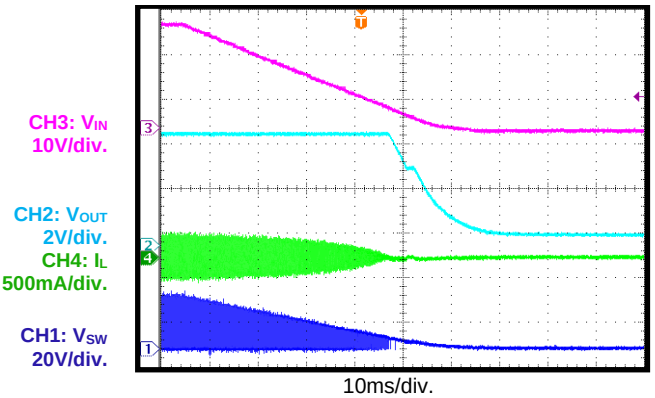
Shutdown through VIN

I_{OUT} = 0A, AAM mode



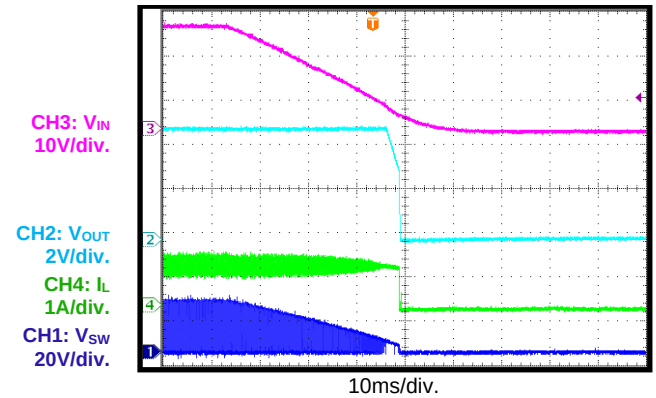
Shutdown through VIN

I_{OUT} = 0A, FCCM



Shutdown through VIN

I_{OUT} = 1A

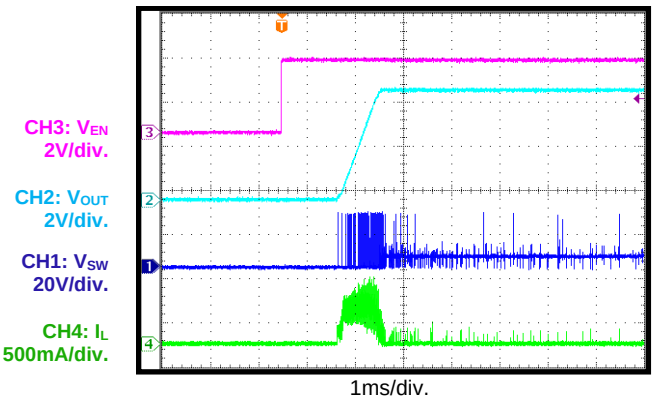


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

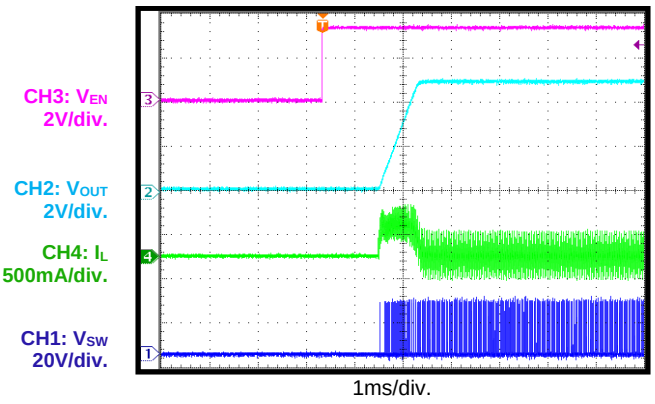
Start-Up through EN

I_{OUT} = 0A, AAM mode



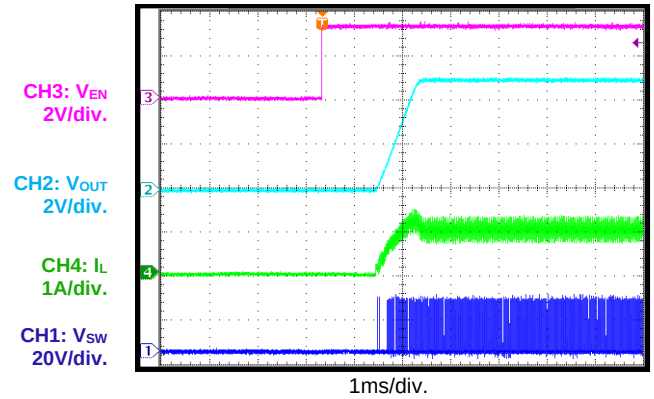
Start-Up through EN

I_{OUT} = 0A, FCCM



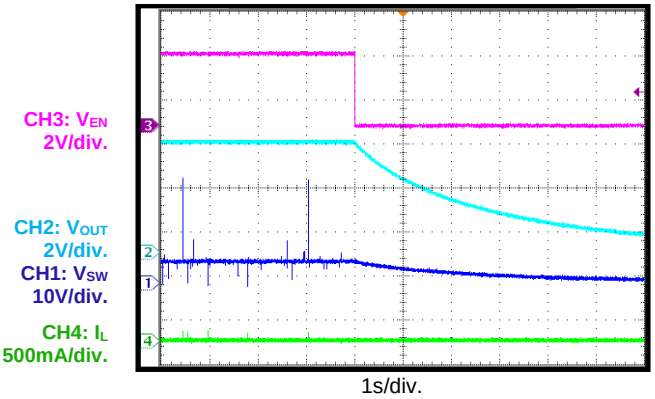
Start-Up through EN

I_{OUT} = 1A



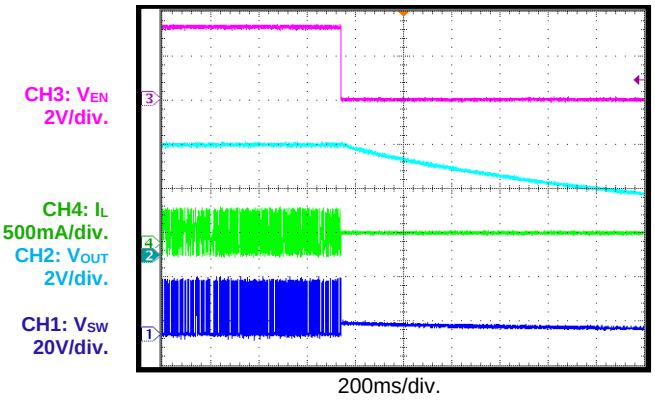
Shutdown through EN

I_{OUT} = 0A, AAM mode



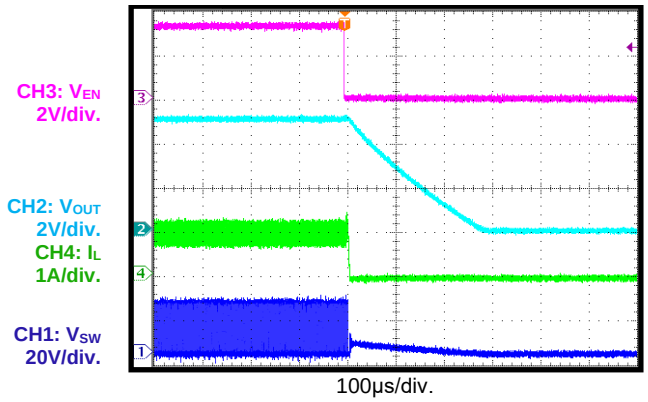
Shutdown through EN

I_{OUT} = 0A, FCCM



Shutdown through EN

I_{OUT} = 1A

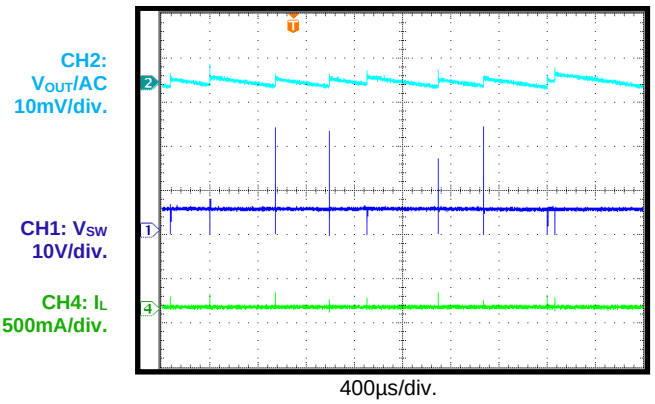


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

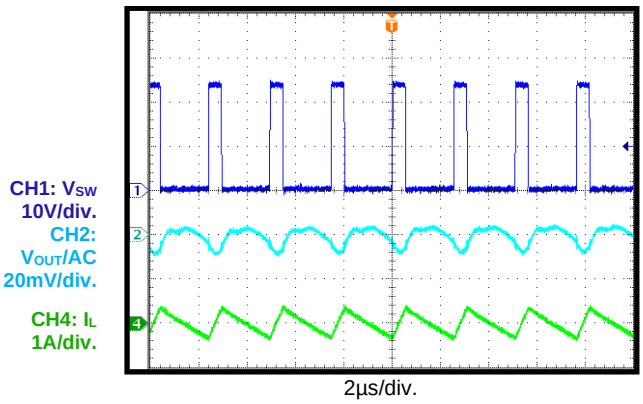
Output Ripple

I_{OUT} = 0A, AAM mode



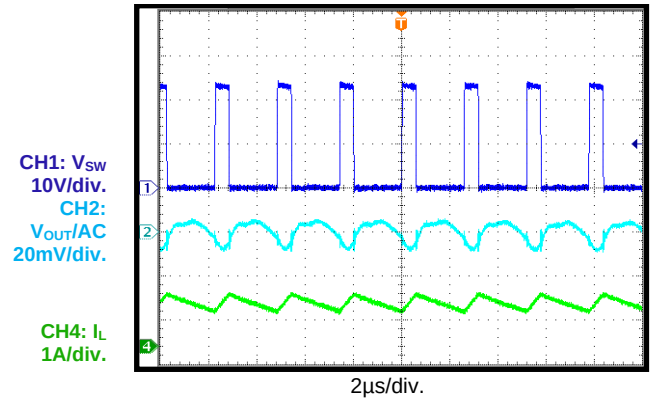
Output Ripple

I_{OUT} = 0A, FCCM



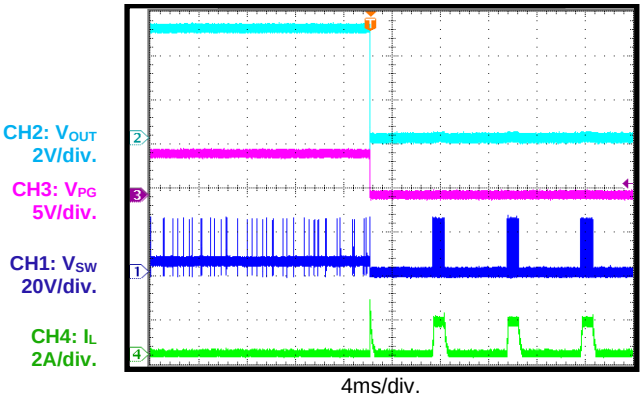
Output Ripple

I_{OUT} = 1A



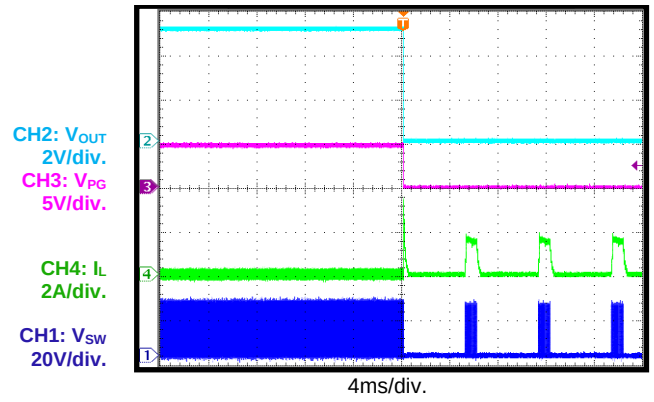
SCP Entry

I_{OUT} = 0A, AAM mode



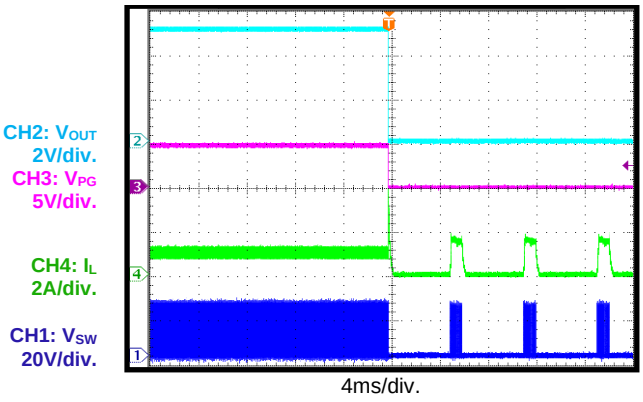
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

I_{OUT} = 1A

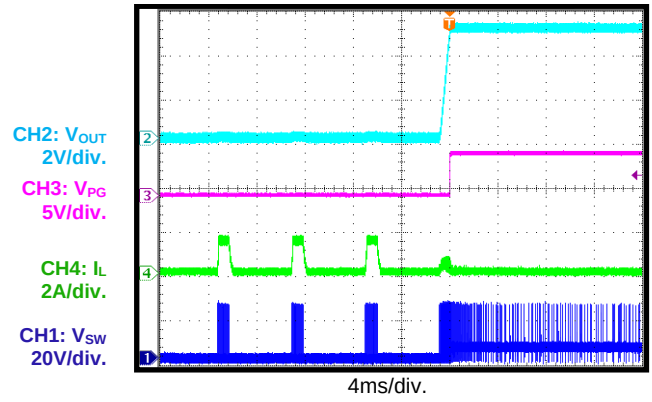


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

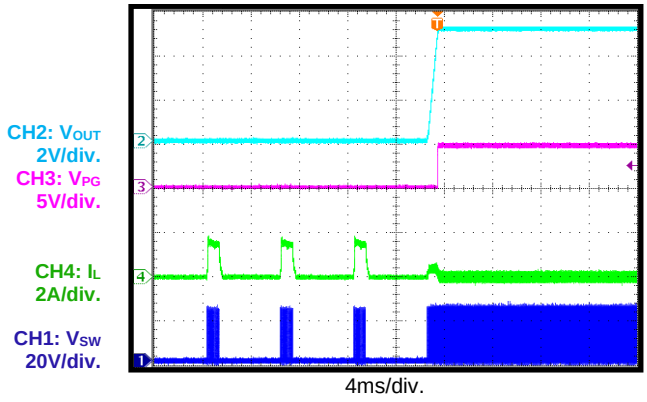
SCP Recovery

I_{OUT} = 0A, AAM mode



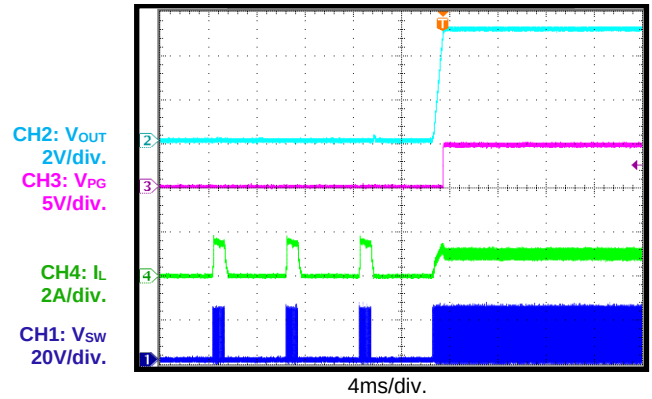
SCP Recovery

I_{OUT} = 0A, FCCM

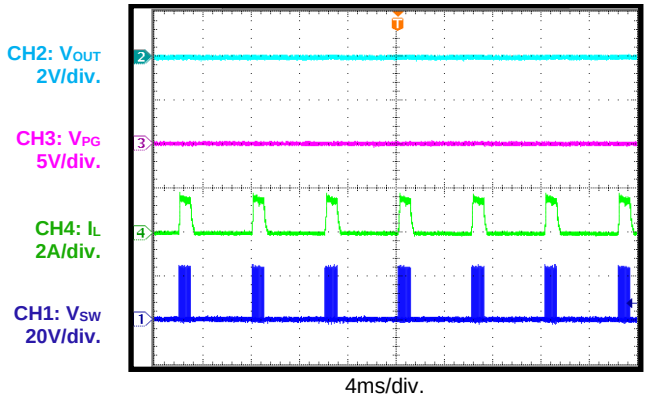


SCP Recovery

I_{OUT} = 1A

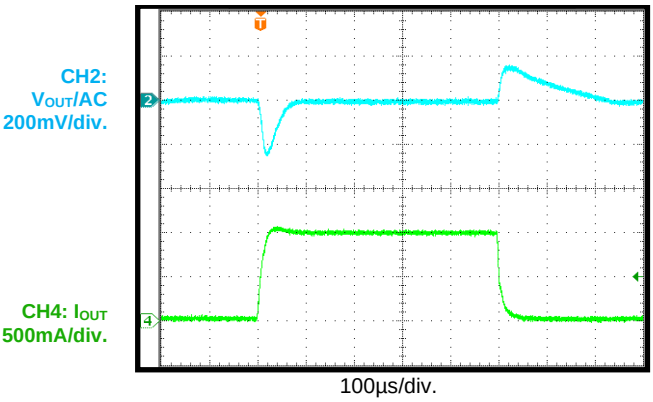


SCP Steady State



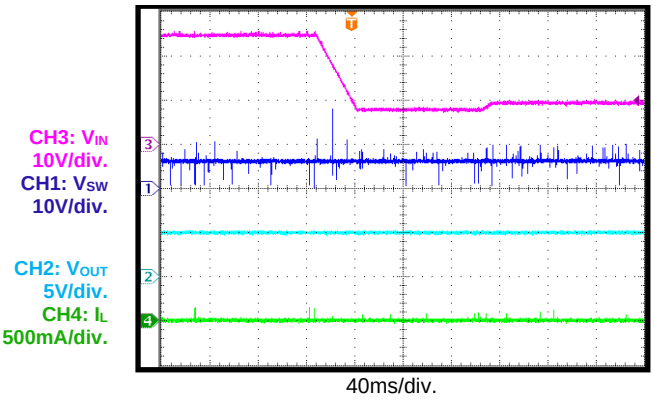
Load Transient

I_{OUT} = 0A to 1A, AAM mode



Cold Crank

V_{IN} = 24V to 4V to 5V, I_{OUT} = 0A

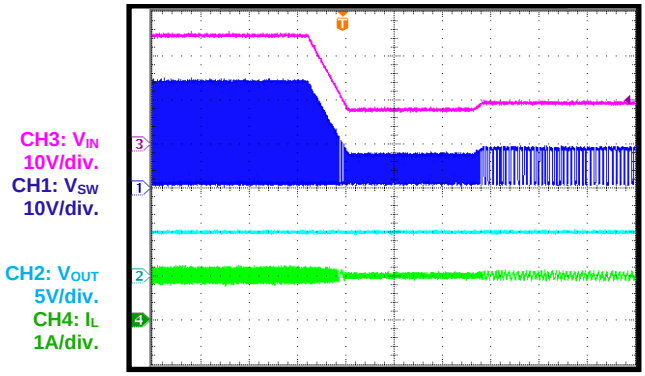


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

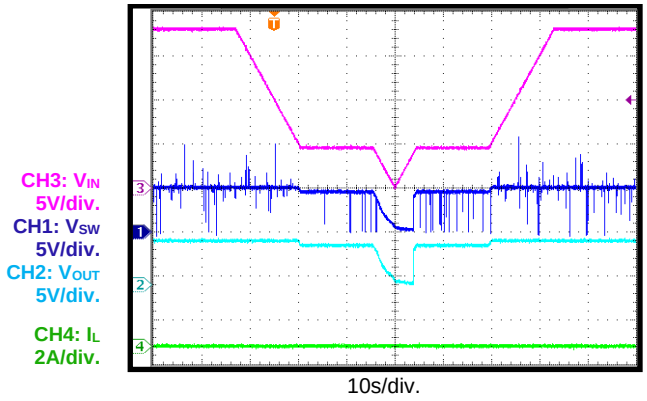
Cold Crank

V_{IN} = 24V to 4V to 5V, I_{OUT} = 1A



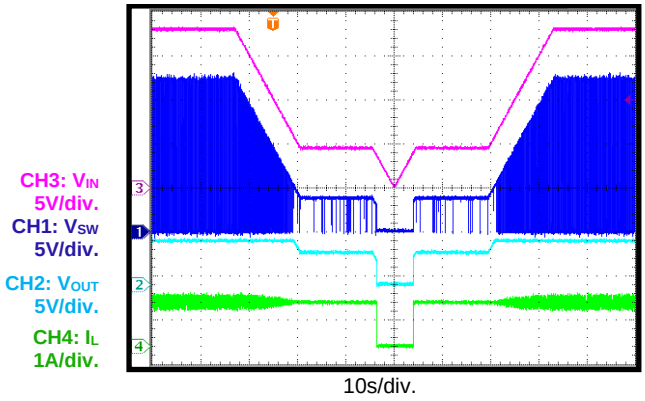
V_{IN} Ramping Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V,
I_{OUT} = 0A



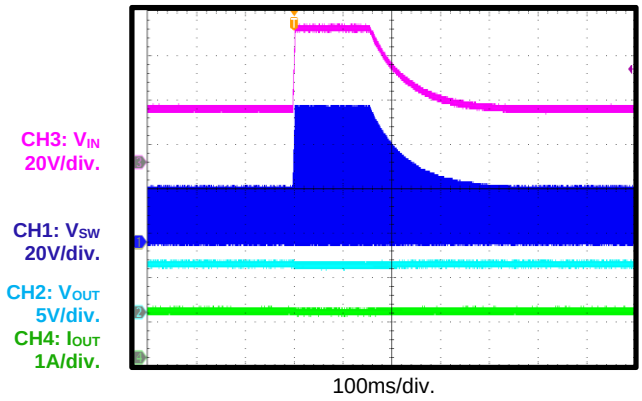
V_{IN} Ramping Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V,
I_{OUT} = 1A



Load Dump

V_{IN} = 24V to 60V to 24V, I_{OUT} = 1A



FUNCTIONAL BLOCK DIAGRAM

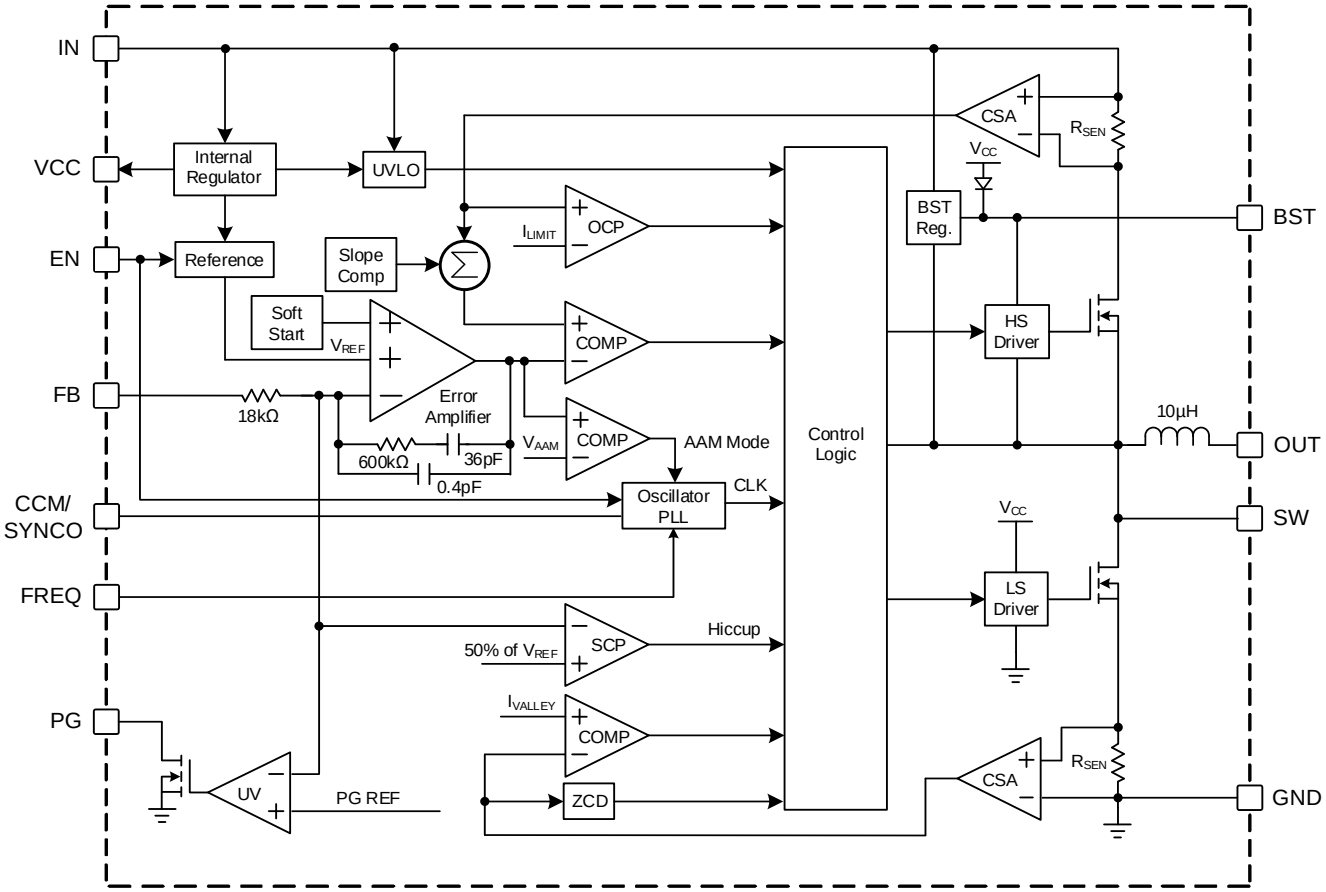


Figure 1: Functional Block Diagram

OPERATION

The MPM3901 is a synchronous, rectified, step-down switch-mode power module with built-in power MOSFETs and an integrated inductor. The module can operate across a wide input voltage (V_{IN}) range up to 60V with ≤40V continuous voltage across a lifetime. It can also achieve up to 1A of continuous output current (I_{OUT}), with excellent load and line regulation across a -40°C to +125°C ambient temperature (T_A) range. Figure 1 on page 22 shows the functional block diagram.

Pulse-Width Modulation (PWM) Control

At moderate-to-high output currents, the MPM3901 operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}).

An internal clock initiates a pulse-width modulation (PWM) cycle. At the clock's rising edge, the high-side MOSFET (HS-FET) turns on, and the inductor current (I_L) rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}), which is the output of the internal error amplifier (EA). V_{COMP} is based on the difference between the output feedback (FB) voltage (V_{FB}) and internal high-precision reference voltage. V_{COMP} determines the amount of energy to be transferred to the load. A higher load current creates a higher V_{COMP}. Once the HS-FET is on, it remains on for at least 90ns.

When the HS-FET is off, the low-side MOSFET (LS-FET) turns on immediately and remains on until the next clock starts. During this time, I_L flows through the LS-FET. Once the LS-FET is on, it remains on for at least 100ns before the next cycle starts. To avoid shoot-through, a dead time (DT) is inserted to prevent the HS-FET and LS-FET from turning on simultaneously.

If the current in the HS-FET does not reach the value set by COMP within one PWM period, then the HS-FET remains on and skips a turn-off operation.

Light-Load Operation

The MPM3901 provides configurable forced continuous conduction mode (FCCM) and light-load advanced asynchronous modulation (AAM) mode, which can be set by the CCM/SYNCO pin. FCCM maintains a constant switching frequency (f_{SW}) and smaller output ripple. However, FCCM also has low efficiency under light-load conditions, while AAM mode achieves high efficiency (see Figure 2).

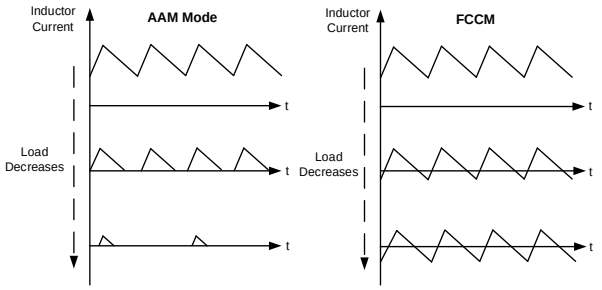


Figure 2: AAM Mode and FCCM

To force the device to enter FCCM, connect the CCM/SYNCO pin to GND using a 10kΩ to 300kΩ resistor. In FCCM, the converter works with a fixed frequency across a no-load to full-load range. Float CCM/SYNCO to force the device to enter AAM mode under light-load conditions. The device cannot change modes during operation, meaning the mode must be selected before start-up.

When AAM mode is enabled, f_{SW} is scaled down according to V_{COMP} under light-load conditions. The MPM3901 first enters asynchronous operation while I_L approaches 0A at light loads. If the load further decreases or is at no load, V_{COMP} drops below the internally set AAM voltage (V_{AAM}). The MPM3901 then enters sleep mode and consumes a low quiescent current (I_Q) to improve light-load efficiency.

In sleep mode, the internal clock is blocked, meaning the MPM3901 skips some pulses. V_{FB} is below the reference voltage (V_{REF}), resulting in V_{COMP} to ramp up until it exceeds V_{AAM}. Then the internal clock resets and the crossover time is used as the next clock's benchmark. This control scheme helps the device achieve high efficiency by scaling down the frequency to reduce switching and gate driver losses.

As I_{OUT} increases at light loads, V_{COMP} and f_{SW} rise. If I_{OUT} exceeds the critical level set by V_{COMP}, then the MPM3901 enters discontinuous conduction mode (DCM) or continuous conduction mode (CCM), which has constant f_{SW}.

Enable (EN)

The MPM3901 can be enabled or disabled via a remote enable (EN) signal that is referenced to ground. The remote EN control operates with a positive logic that is compatible with popular logic devices.

Positive logic indicates that when V_{IN} exceeds the under-voltage lockout (UVLO) threshold (about 4V), the converter is enabled by pulling the EN pin above 1.45V. Pull the EN pin below 1.12V to disable the MPM3901. An internal resistor (R_{EN}) connected between the EN and GND pins allows EN to be floated, which shuts down the chip (where R_{EN} is 2.8MΩ when EN is on, and R_{EN} is 1.8MΩ when EN is off).

Synchronization Output (SYNCO)

The MPM3901 provides a SYNCO pin. During start-up, SYNCO remains low and quickly outputs a 180° phase-shift clock to the internal oscillator once soft start (SS) is ready. SYNCO's falling edge is a 180° phase shift to the internal oscillator's rising edge. This function allows two devices to operate at the same frequency, but 180° out of phase reduces the total input current ripple. This allows for a smaller input bypass capacitor to be used.

Internal Regulator

A 4.8V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates across the full V_{IN} range. When V_{IN} exceeds 4.8V, the regulator's output is in full regulation. A lower V_{IN} results in lower V_{OUT}. The regulator is enabled when V_{IN} exceeds its UVLO threshold and EN is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

Configurable Frequency and Foldback

The MPM3901's f_{SW} is configured via an external frequency resistor (R_{FREQ}), which should be placed between the FREQ and GND pins, as close as possible to the device. Select a proper R_{FREQ}, which can be calculated with Equation (1):

$$R_{FREQ}\ (M\Omega) = \frac{30}{f_{SW}\ (kHz)} \quad (1)$$

R_{FREQ} may require fine-tuning with a bench test.

Figure 3 shows the f_{SW} vs. R_{FREQ} curve.

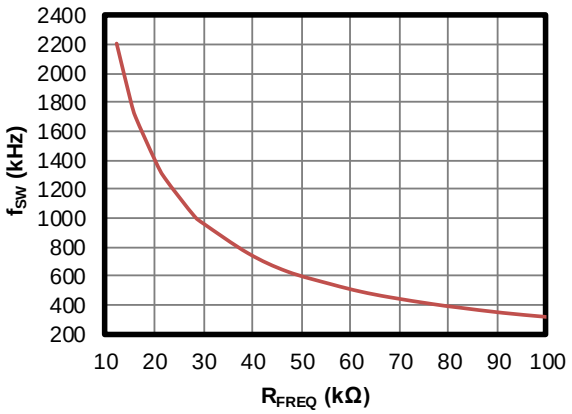


Figure 3: f_{SW} vs. R_{FREQ}

It is not possible to use a high f_{SW} with a high V_{IN} since the minimum on time (t_{ON_MIN}) required for the HS-FET is limited. The MPM3901's control loop automatically sets the maximum possible f_{SW} up to the set frequency, which also reduces excessive power loss in the IC. V_{OUT} is regulated by varying the duration of the HS-FET's turn-off time, which results in an automatic reduction of f_{SW}.

Compliance with the HS-FET's t_{ON_MIN} is guaranteed. An advantage of this method is that the device works at the desired f_{SW} as long as possible, and a correction is only made at high V_{IN}. For the f_{SW} vs. V_{IN} curve, see the Typical Performance Characteristics section on page 12, where R_{FREQ} is 12.1kHz.

Internal Soft Start (SS)

To avoid overshoot during start-up, the MPM3901 has built-in soft start (SS) that ramps up V_{OUT} at a controlled slew rate when the EN pin goes high. When the SS voltage (V_{SS}) is below the internal reference (V_{REF}), V_{SS} overrides V_{REF} as the EA reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. At this point, SS finishes, and the MPM3901 enters steady state.

The SS time (t_{SS}) is internally set to 0.45ms. When V_{OUT} is shorted to GND, V_{FB} is pulled low, then V_{SS} is discharged. The part soft starts again once it returns to the normal state.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, the output has a pre-biased voltage and neither the HS-FET nor LS-FET turns on until V_{SS} exceeds V_{FB}. This capability is only available when the device is set to AAM mode.

Power Good (PG) Indicator

The MPM3901 provides power good (PG) indication. The PG pin is the open drain of a MOSFET. It should be connected to a voltage source through a resistor (e.g. 100kΩ). If V_{IN} is present, the MOSFET turns on, making the PG pin to be pulled to GND before SS is ready. PG goes high if V_{OUT} is within 90% to 109.5% of the nominal voltage after a 70μs deglitch. PG goes low if V_{OUT} exceeds 116% or drops below 84% of the nominal voltage after a 25μs deglitch.

Under-Voltage Lockout (UVLO) Protection

The MPM3901 provides input UVLO to ensure reliable output power. Assuming the EN pin is active, the MPM3901 starts up when V_{IN} exceeds its UVLO rising threshold ($V_{IN\_UVLO\_RISING}$). The device is powered off when V_{IN} drops below its UVLO falling threshold ($V_{IN\_UVLO\_FALLING}$). This function prevents the device from operating at an insufficient voltage. It is a non-latch protection.

Over-Current Protection (OCP)

The MPM3901 provides a peak current limit (I_{PEAK_LIMIT}) of 1.95A. Once I_L reaches I_{PEAK_LIMIT}, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and I_L decreases. The HS-FET does not turn on again until I_L drops below the valley current limit. This protection prevents I_L from running away and damaging the components.

Short-Circuit Protection (SCP)

If a short-circuit condition occurs, the MPM3901 reaches its current limit immediately. Meanwhile, V_{OUT} drops until V_{FB} falls below 50% of V_{REF}, which is considered an output dead short. Short-circuit protection (SCP) with hiccup mode is triggered to periodically restart the part.

In hiccup mode, the MPM3901 disables its output power stage and slowly discharges the SS capacitor (C_{SS}), then initiates SS. If the short-circuit condition remains after SS ends, then the device repeats this operation until the short circuit is removed, and the output returns to the regulated level. This protection mode significantly reduces the average short-circuit current to alleviate thermal issues and protect the regulator.

Negative Current Protection

The MPM3901 provides a -1.3A negative current limit (I_{LIMIT_NEG}). Once I_L reaches the current limit, the LS-FET immediately turns off and then the HS-FET turns on. I_{LIMIT_NEG} prevents the negative current dropping too low and damaging the components.

Thermal Shutdown

The MPM3901 provides thermal protection by monitoring the IC temperature internally. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature (T_J) exceeds the threshold (typically 170°C), then the whole chip shuts down. This is a non-latch protection. There is a 25°C hysteresis. Once T_J drops to about 145°C, the device resumes normal operation by initiating SS.

Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor (C_{BST}) powers the floating HS-FET driver. There are two methods to charge C_{BST} (see Figure 4).

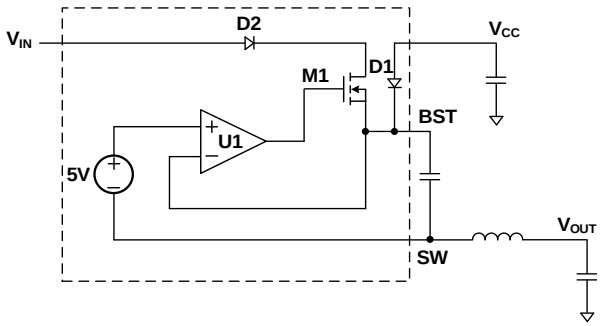


Figure 4: Internal Bootstrap Charging Circuit

The first method uses the main charging circuit from V_{CC} through a diode. When the HS-FET is on, the SW pin voltage (V_{SW}) is about equal to V_{IN} but exceeds V_{CC}, and C_{BST} is not charged. The optimal charging period occurs when the LS-FET is on, and the difference between V_{CC} and V_{SW} is largest. When there is no current in the inductor, V_{SW} is equal to V_{OUT}, meaning V_{CC} can only charge C_{BST} when V_{OUT} is very small.

The second method uses the auxiliary charging circuit from V_{IN}. When the difference between V_{BST} and V_{SW} is below the internal 5V BST regulator, a N-channel MOSFET pass transistor (M1) turns on to charge C_{BST}. The charging current is much smaller compared to the current from VCC; however, as long as V_{IN} exceeds V_{SW}, C_{BST} can be charged. This function is useful in sleep mode when there is not always a switch.

Low-Dropout Operation (BST Refresh)

To improve dropout, the MPM3901 is designed to operate at close to 100% duty cycle as long as the BST-to-SW voltage (V_{BST-SW}) exceeds 1.4V. When V_{BST-SW} drops below 1.34V, the HS-FET turns off using a UVLO circuit, which allows the LS-FET to conduct and refresh the charge on C_{BST}. When V_{IN} drops, the HS-FET remains on and close to 100% duty cycle to maintain output regulation until V_{BST-SW} drops below 1.34V.

Since the supply current sourced from C_{BST} is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. The means the switching regulator's effective duty cycle is high.

The effective duty cycle during the regulator's dropout is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts up first to generate a stable V_{REF} and reference current, then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank start-up glitches. When the SS block is enabled, it holds its SS output low to ensure the circuitries are ready, then slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} UVLO, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to the FB pin sets V_{OUT}. The FB resistor (R1, also called R_{FB}) cannot be too large or small to achieve stability and dynamic response. Choose R1 to be about 40kΩ. R2 can then be estimated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8} - 1} \quad (2)$$

Figure 5 shows the recommended T-type feedback network.

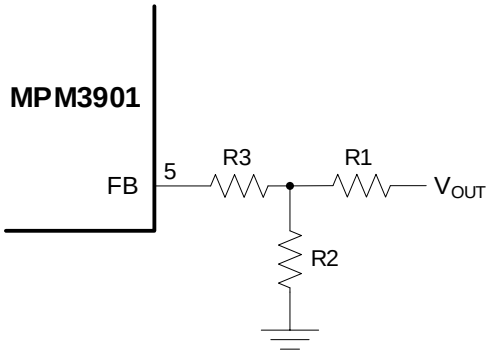


Figure 5: Feedback Network

R3 and R1 set the loop bandwidth. A higher R3 and R1 indicates a lower bandwidth. To ensure loop stability, it is strongly recommended to limit the bandwidth below 1/10 of f_{SW} and not exceed 100kHz.

The calculated resistance may require fine-tuning via bench testing. Table 1 shows the recommended feedback resistor divider values for common V_{OUT} values. Apply check loop analysis before using the device in application and adjust R3 for loop stability if necessary.

Table 1: Resistances for Typical V_{OUT}

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
3.3	41.2	13
5	41.2	7.68

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply the AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended because of their low ESR and small temperature coefficients. Other capacitors, such as Y5V and Z5U, should not be used since they lose too much capacitance with the frequency, temperature, and bias voltage.

Place C_{IN} as close to the IN pin as possible. For most applications, a 22µF capacitor is sufficient. For higher V_{OUT}, use a 47µF capacitor to improve system stability. To maintain a small solution size, choose a properly sized capacitor that has a voltage rating compliant with the input specifications.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating, which should not exceed the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (3):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (4):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality ceramic capacitor (0.1µF), placed as close to the IC as possible. C_{IN} determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system design, choose C_{IN} to meet the specifications.

The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Ceramic capacitors with low ESR are recommended for small size and low output voltage ripple. Electrolytic and polymer capacitors may also be used. The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

Where R_{ESR} is the equivalent series resistance of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

Another consideration for C_{OUT} is the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve a desired overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (10):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUT\_MAX} / V_{OUT})^2 - 1)} \quad (10)$$

Where V_{OUT_MAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitances required for ripple and overshoot, choose the larger capacitance.

The characteristics of C_{OUT} also affect the stability of the regulation system. The MPM3901 can be optimized for a wide range of capacitances and ESR values.

V_{IN} Under-Voltage Lockout (UVLO)

The MPM3901 provides an internal, fixed UVLO threshold. The rising threshold is 4V, while the falling threshold is about 3.5V. For applications that require a higher UVLO threshold, place an external resistor divider between the EN and IN pins to obtain a higher equivalent UVLO threshold. Figure 6 shows the adjustable UVLO threshold using an EN divider when EN is rising.

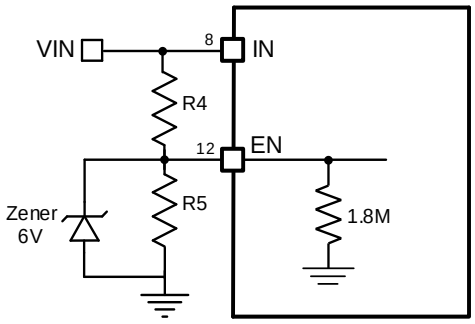


Figure 6: Adjustable UVLO Threshold Using the EN Divider when EN Is Rising

Figure 7 shows the adjustable UVLO threshold using an EN divider when EN is falling.

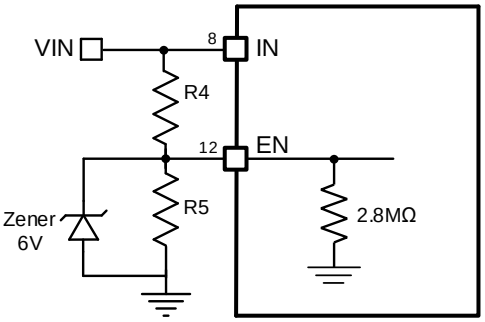


Figure 7: Adjustable UVLO Threshold Using the EN Divider when EN Is Falling

If the EN pin is connected to VIN through a resistor, add a 6V Zener diode between EN and GND.

$V_{IN\_UVLO\_RISING}$ when EN is rising can be calculated with Equation (11):

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R4}{1.8M\Omega \,//\, R5}) \times V_{EN\_RISING} \quad (11)$$

Where V_{EN_RISING} is 1.45V.

$V_{IN\_UVLO\_FALLING}$ when EN is falling can be calculated with Equation (12):

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R4}{2.8M\Omega \,//\, R5}) \times V_{EN\_FALLING} \quad (12)$$

Where $V_{EN\_FALLING}$ is 1.12V.

When selecting R4, ensure it is large enough to limit the current flowing into the EN pin below 100μA.

Bootstrap (BST) Resistor and Capacitor

A resistor R_{BST} in series with C_{BST} can reduce the SW rising rate and voltage spikes. This improves EMI performance and reduces voltage stress at a high V_{IN}. A higher resistance is better for reducing SW spikes but compromises efficiency. To make a tradeoff between EMI and efficiency, it is recommended to maintain R_{BST} below 20Ω. The recommended C_{BST} is between 0.1μF and 1μF.

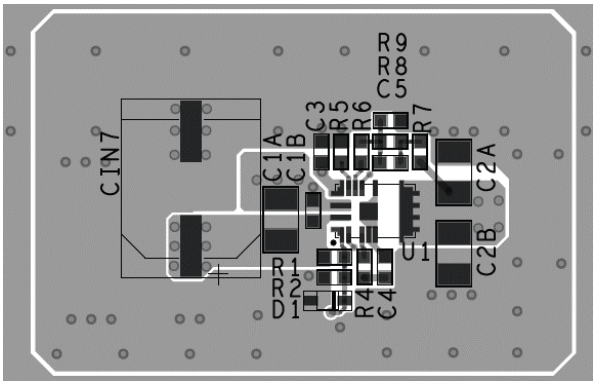
PCB Layout Guidelines (11)

An optimized PCB layout is very important for proper operation. A 4-layer layout is strongly recommended to achieve improved thermal performance. For the best results, refer to Figure 8 and follow the guidelines below:

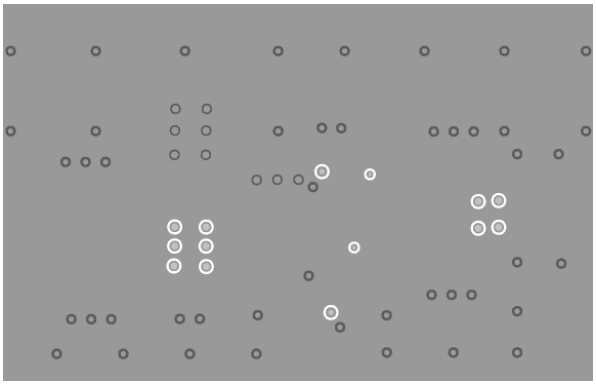
1. Place the high-current paths (GND, IN, and SW) very close to the device using short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to the IN and GND pins as possible to minimize high-frequency noise.
4. Place the T-type FB resistors as close as possible to the FB pin to ensure that the trace connected to the FB pin is as short as possible.
5. Route SW and BST away from sensitive analog areas, such as FB.
6. Use multiple vias to connect the power planes to the mid-layers.

Note:

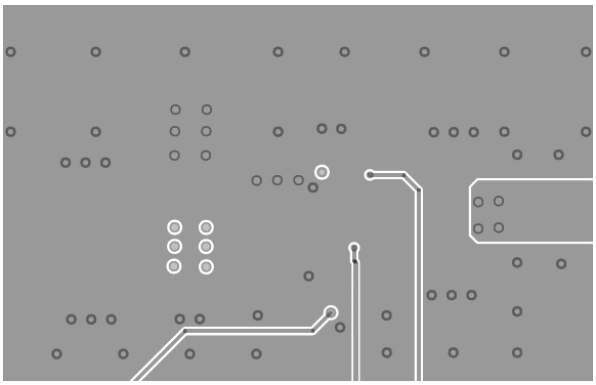
10) The recommended PCB layout is based on Figure 11 on page 32.



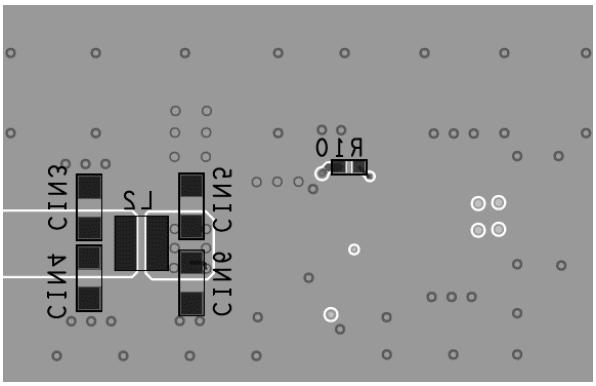
Top Silk and Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

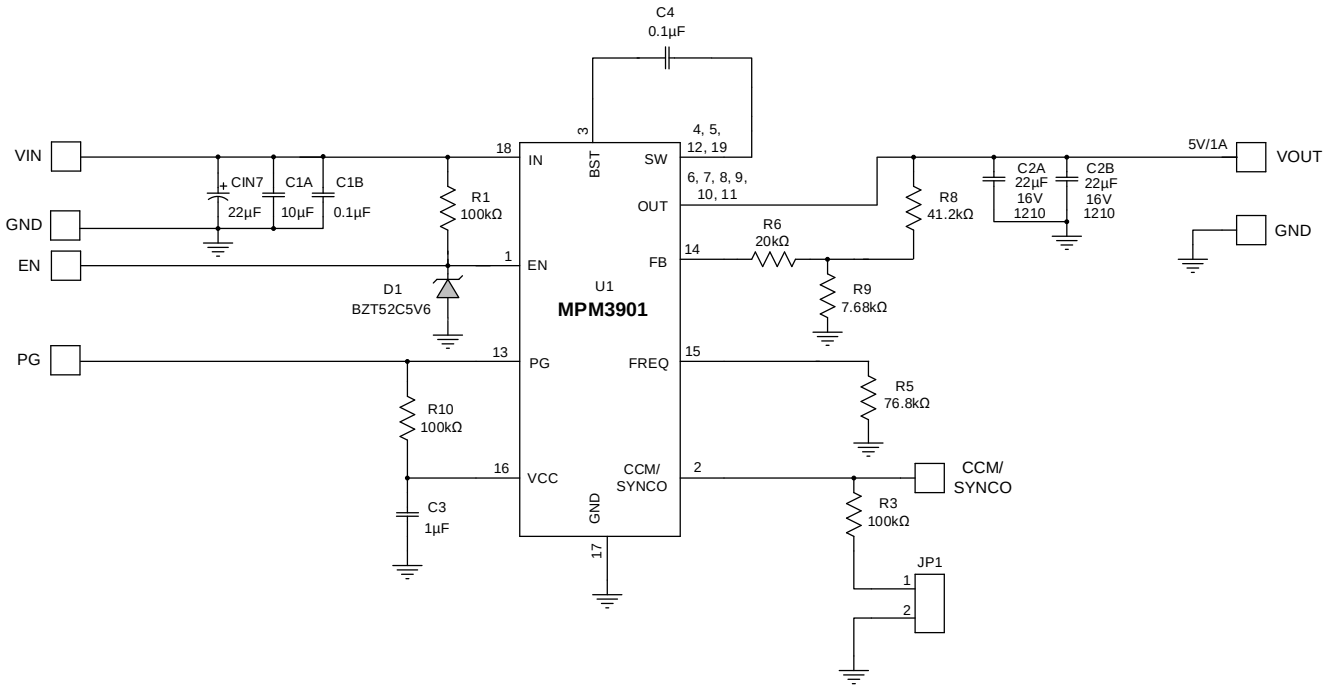


Figure 9: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 400kHz)

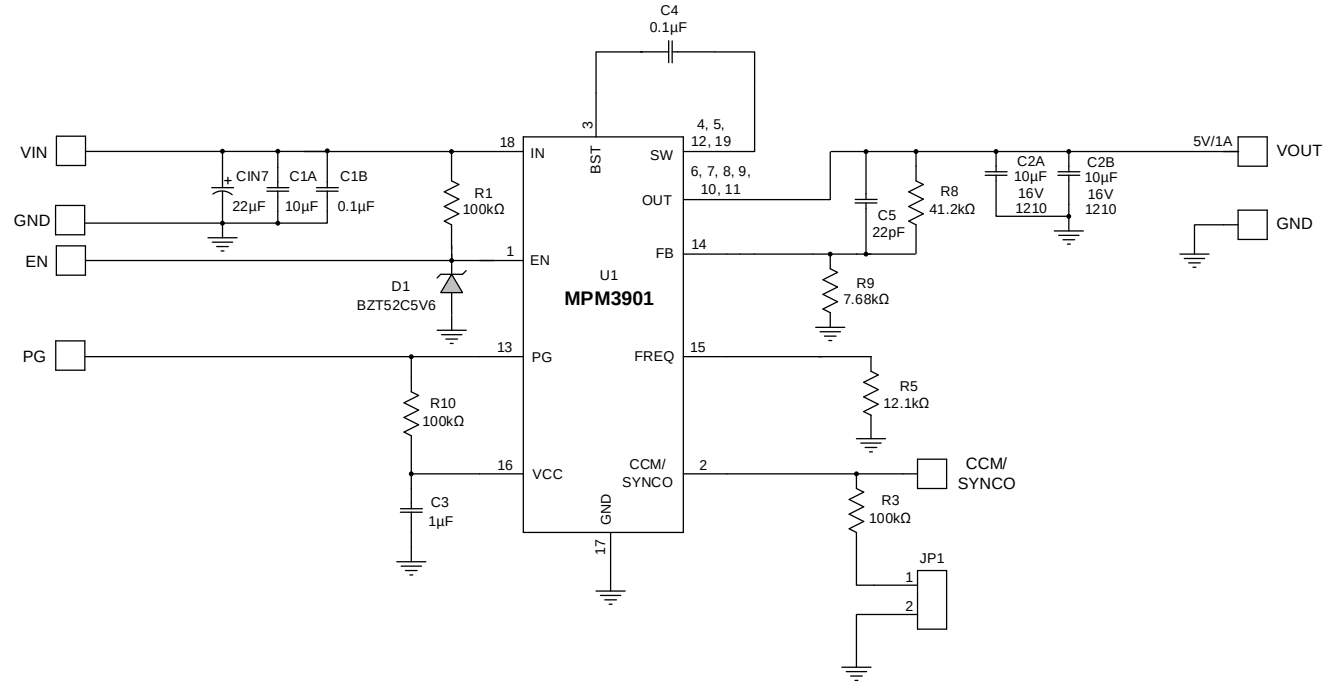


Figure 10: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

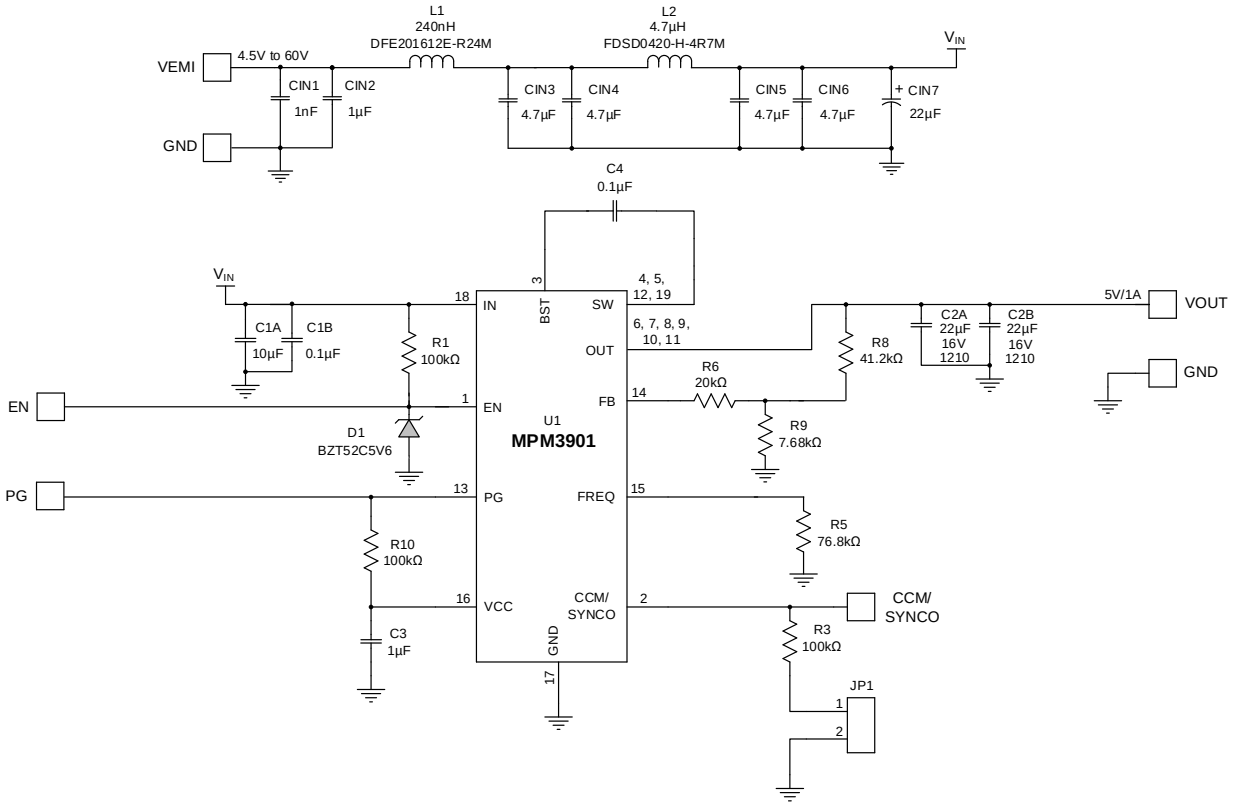


Figure 11: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 400kHz with EMI Filters)

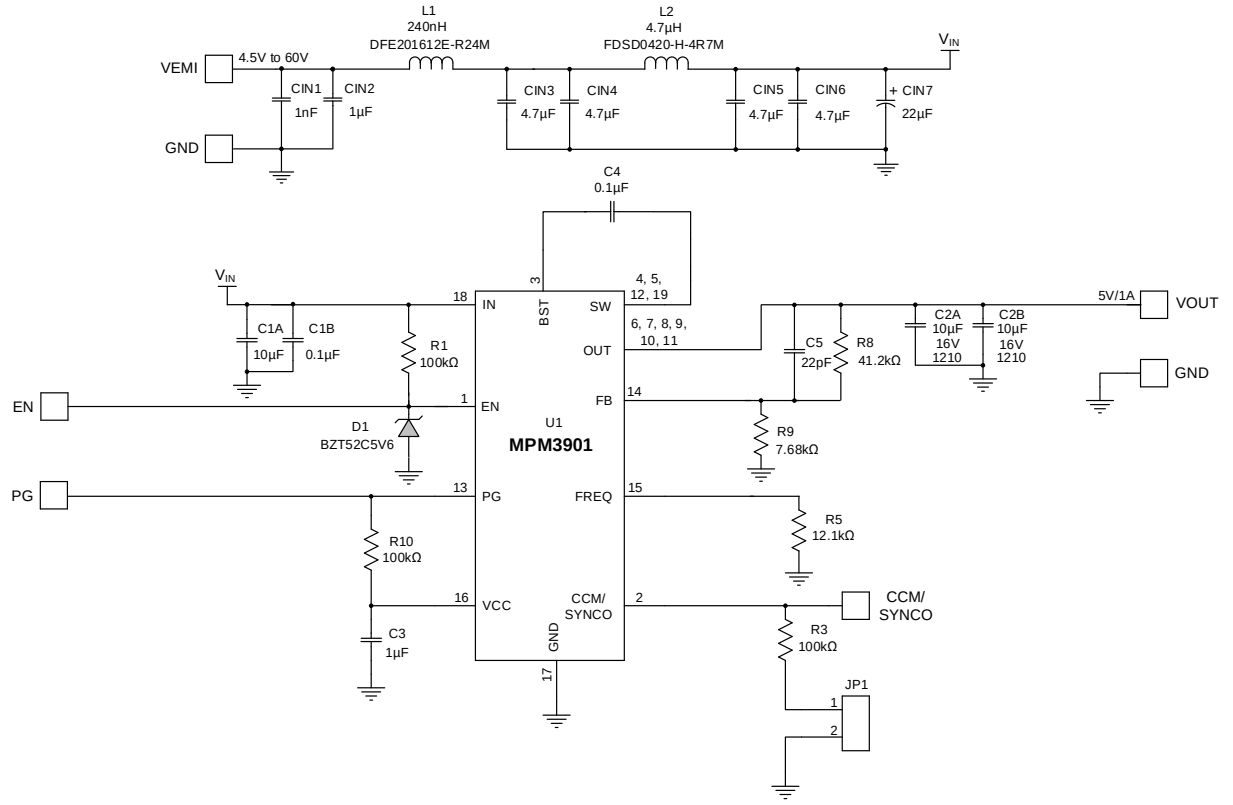
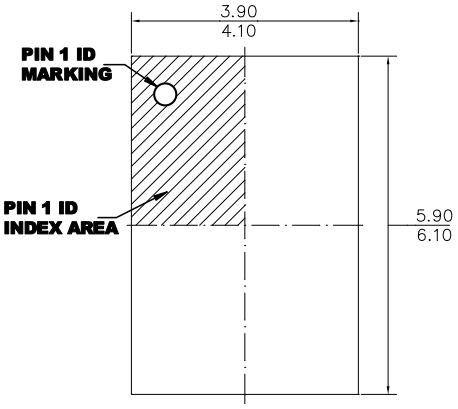


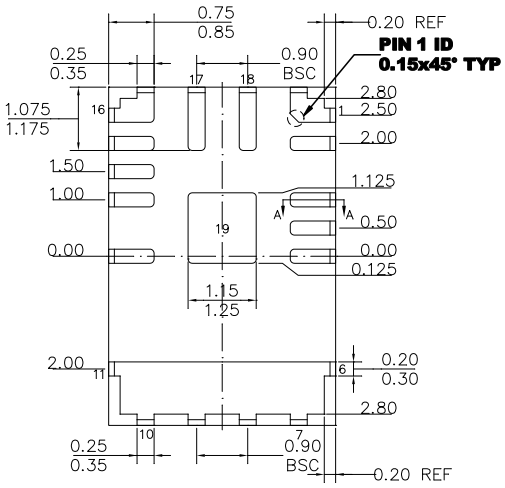
Figure 12: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filters)

PACKAGE INFORMATION

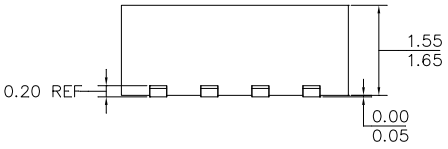
QFN-19 (4mmx6mm)
Wettable Flanks



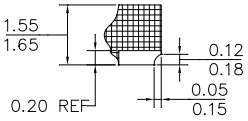
TOP VIEW



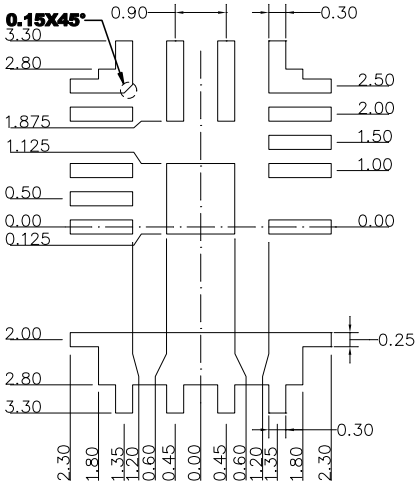
BOTTOM VIEW



SIDE VIEW



SECTION A-A

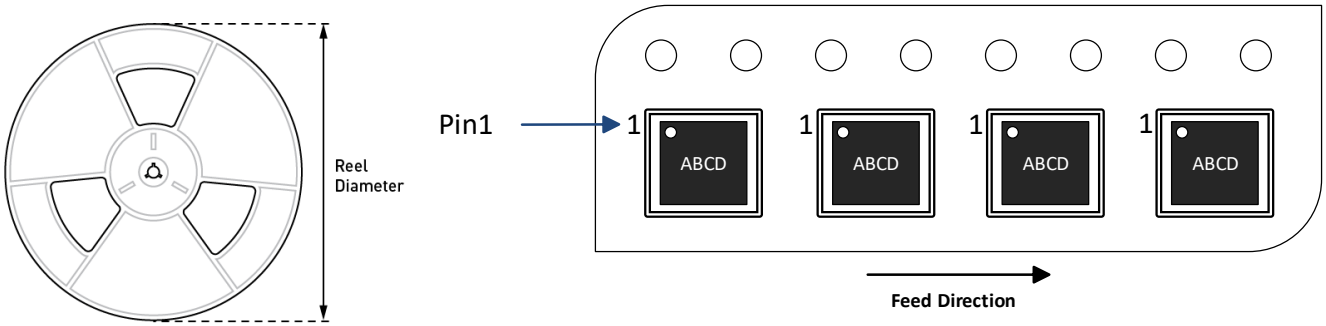


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3901GQWE-Z	QFN-19 (4mmx6mm)	5000	N/A	N/A	13in	12mm	8mm
MPM3901GQWE-AEC1-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/30/2024	Initial Release	-