MP8639

16V, 6A, Fully Integrated, Low-I_Q, Synchronous Step-Down Converter

DESCRIPTION

The MP8639 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. It offers an ultra-compact solution that can achieve up to 6A of continuous output current (I_{OUT}) and 7.5A of peak I_{OUT} (I_{OUT_PEAK}) across a wide 4.5V to 16V input voltage (V_{IN}) range.

MPS's proprietary switching loss reduction technique and internal, low on resistance ($R_{DS(ON)}$) power MOSFETs allow the device to operate at high efficiency across the entire I_{OUT} load range.

Adaptive constant-on-time (COT) control provides fast transient response and eases loop stabilization. The DC auto-tune loop and remote differential sense provide good load and line regulation.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MP8639 requires a minimal number of standard external components, and is available in a QFN-11 (2mmx2mm) package.

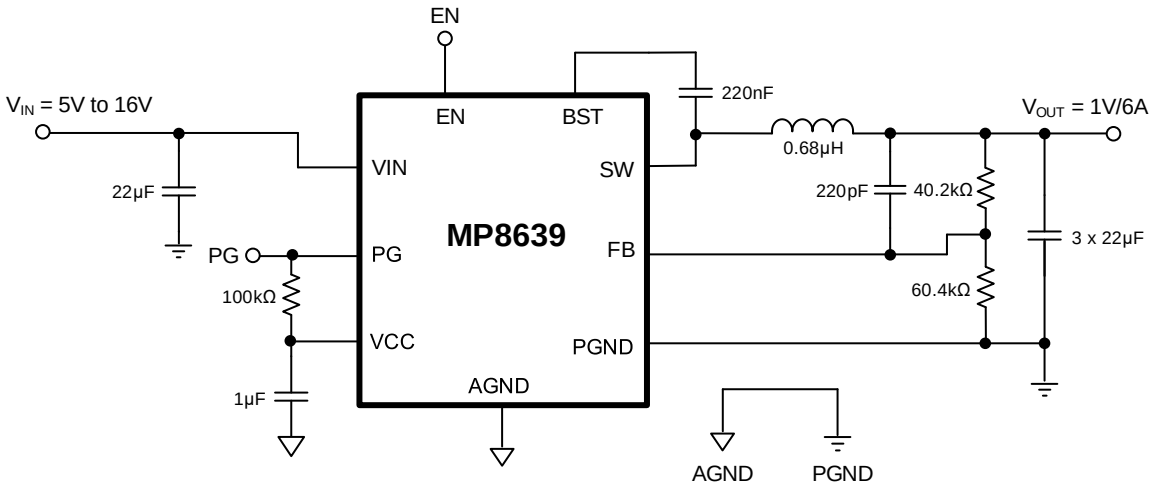
FEATURES

- Wide 4.5V to 16V Operating Input Voltage (V_{IN}) Range
- 6A Continuous Output Current (I_{OUT})
- 7.5A Peak I_{OUT} (I_{OUT_PEAK})
- Low 105μA Quiescent Current (I_Q)
- Adaptive Constant-On-Time (COT) Control for Fast Transient Response
- DC Auto-Tune Loop and Remote Differential Sense
- Low On Resistance ($R_{DS(ON)}$) Internal Power MOSFETs
- MPS Proprietary Switching Loss Reduction Technique
- Stable with POSCAP and Ceramic Capacitors
- 1% Accurate Reference Voltage (V_{REF})
- Internal Soft Start (SS)
- Output Discharge
- Over-Current Protection (OCP)
- Over-Voltage Protection (OVP)
- Under-Voltage Protection (UVP)
- Thermal Shutdown
- Available in a QFN-11 (2mmx2mm) Package

APPLICATIONS

- Telecom and Networking Systems
- Servers, Cloud Computing, and Storage
- Base Stations
- General-Purpose Point-of-Load (PoL)
- 12V Distribution Power Systems
- High-End TVs
- Game Consoles and Graphic Cards

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8639GG	QFN-11 (2mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP8639GG-Z).

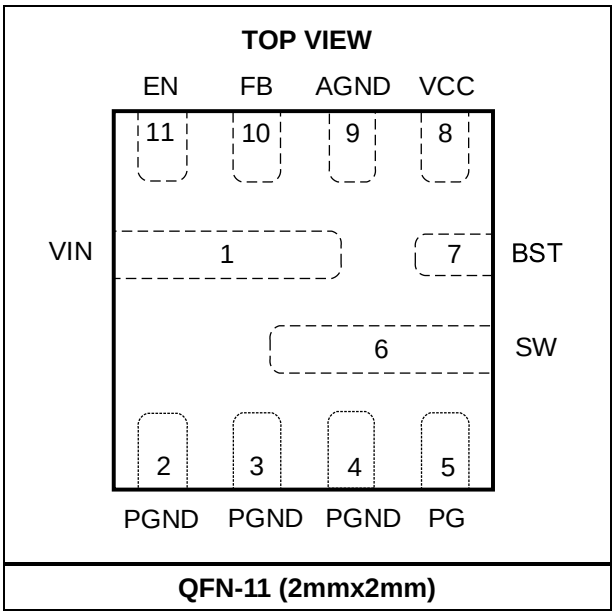
TOP MARKING

NTY

LLLL

NT: Product code of MP8639GG
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-11 (2mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** The VIN pin supplies power to the internal MOSFETs and converter. The MP8639 operates from a 4.5V to 16V input voltage (V_{IN}) rail. An input capacitor (C_{IN}) is required to decouple the input rail. Connect VIN using wide PCB traces and multiple vias, and with at least two layers for the input trace.
2, 3, 4	PGND	**Power ground.** Connect the PGND pin using wide PCB traces and multiple vias.
5	PG	**Power good (PG) output.** The PG pin is an open-drain output. If the output voltage (V_{OUT}) exceeds 95% or drops below 105% of the nominal voltage, PG is pulled high. It is recommended to connect the PG and VCC pins together.
6	SW	**Switch output.** Connect the SW pin to the inductor and the bootstrap (BST) capacitor (C_{BST}) using short, wide PCB traces. During the pulse-width modulation (PWM) mode on time (t_{ON}), the high-side MOSFET (HS-FET) pulls SW up to V_{IN}. During the PWM mode off time (t_{OFF}), the inductor current (I_L) pulls SW negative. The low-side MOSFET (LS-FET) on resistance ($R_{DS(ON)\_LS}$) and the internal diode fix this negative voltage.
7	BST	**Bootstrap (BST).** Connect a capacitor between the SW and BST pins to form a floating supply across the HS-FET driver.
8	VCC	**Internal 3V3 VCC voltage (V_{CC}) low-dropout (LDO) output.** The VCC pin provides power to the driver and control circuits. Decouple VCC using a >1µF, ceramic decoupling capacitor placed as close to VCC as possible. Ceramic capacitors with X7R or X5R dielectrics are recommended due to their stable temperature characteristics.
9	AGND	**Signal logic ground.** The AGND pin is the Kelvin connection to PGND.
10	FB	**Feedback (FB).** Set V_{OUT} using an external resistor divider connected between the output and AGND, which is tapped to FB. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. In addition, keep the FB trace far away from the SW node.
11	EN	**Enable (EN).** The EN pin is a digital input that turns the converter on and off. Pull EN high to turn the converter on; pull EN low to turn the converter off. For automatic start-up, connect the EN and VIN pins via a voltage resistor divider. The EN voltage (V_{EN}) should not exceed 4.5V. Do not float EN.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{SW} (DC) ..... -1V to V_{IN}
V_{SW} (25ns)..... -3.6V to +28V (2)
V_{BST} ..... V_{SW} + 4.5V
I_{EN}..... 100µA
All other pins ..... -0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (3)
QFN-11 (2mmx2mm) 1.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... Passed ±2kV
Charged device model (CDM) ..... Passed ±2kV

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.5V to 16V
Output voltage (V_{OUT}) ..... 0.6V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-11 (2mmx2mm) ..... 80 ..... 16 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured using a differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	V_{EN} = 3.3V, V_{FB} = 0.62V		105	130	µA
Shutdown current	I_{SD}	V_{EN} = 0V			1	µA
High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET)						
HS-FET on resistance (6)	$R_{DS(ON)\_HS}$			36		mΩ
LS-FET on resistance	$R_{DS(ON)\_LS}$			12		mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	µA
Current Limit						
LS-FET valley current limit	I_{LIMIT_LS}		6.5	7.5	9.5	A
Switching Frequency and Minimum Off Time						
Switching frequency	f_{SW}			750		kHz
On time	t_{ON}		-15		+15	% of t_{ON}
Minimum on time (6)	t_{ON_MIN}			50		ns
Minimum off time (6)	t_{OFF_MIN}			220		ns
Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)						
OVP threshold	V_{OVP}	V_{FB}	125	130	135	% of V_{REF}
UVP threshold 1	V_{UVP-1}	V_{FB}	70	75	80	% of V_{REF}
UVP threshold 1 hold-off time (6)	t_{UVP-1}	V_{OUT} = 60% of V_{REF}		32		µs
UVP threshold 2	V_{UVP-2}	V_{FB}	45	50	55	% of V_{REF}
Reference Voltage (V_{REF}) and Soft Start (SS)						
Reference voltage	V_{REF}		594	600	606	mV
Soft-start time (6)	t_{SS}	EN is pulled up to PG	1.4	1.85	2.3	ms
Enable (EN) and Under-Voltage Lockout (UVLO) Protection						
EN rising threshold	V_{EN_RISING}		1.1	1.25	1.4	V
EN hysteresis	V_{EN_HYS}			150		mV
EN current	I_{EN}	V_{EN} = 3.3V		5		µA
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_RISING}$			4.35	4.48	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			550		mV
VCC Regulator						
VCC voltage	V_{CC}		3.5	3.65	3.8	V
VCC load regulation	V_{CC_REG}	I_{VCC} = 5mA		5		%
Power Good (PG)						
Rising PG voltage (V_{PG}) (good)	$V_{PG\_RISING\_GOOD}$	V_{OUT} rising		95		% of V_{REF}
Falling V_{PG} (fault)	$V_{PG\_FALLING\_FAULT}$	V_{OUT} falling		90		% of V_{REF}
Rising V_{PG} (fault)	$V_{PG\_RISING\_FAULT}$	V_{OUT} rising		115		% of V_{REF}
Falling V_{PG} (good)	$V_{PG\_FALLING\_GOOD}$	V_{OUT} falling		105		% of V_{REF}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
PG low to high delay	t_{DELAY_PG}			1	10	µs
EN low to PG low delay	$t_{DELAY\_EN-PG\_LOW}$				1	µs
PG sink current capability	V_{PG_SINK}	4mA sink			0.4	V
Thermal Protection						
Thermal shutdown (6)	T_{SD}			150		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			25		°C

Note:

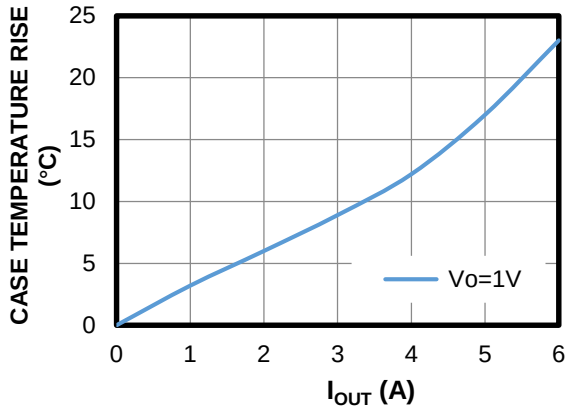
6) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 6.6mΩ, f_{SW} = 750kHz, T_J = 25°C, unless otherwise noted.

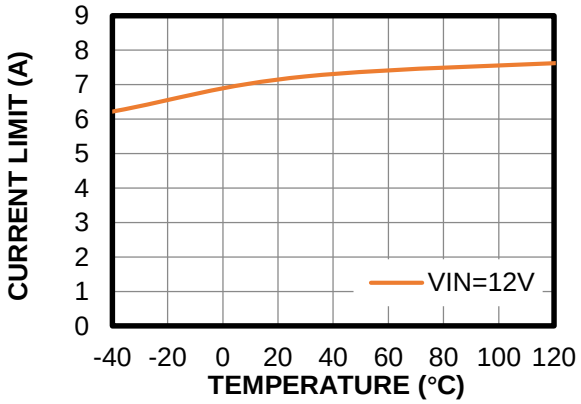
Case Temperature Rise vs. Output Current

V_{OUT} = 1V, f_{SW} = 750kHz, L = 0.68µH, DCR = 3.1mΩ, R_{BST} = 0Ω, C_{OUT} = 3 x 22µF



Current Limit vs. Temperature

V_{IN} = 12V, V_{OUT} = 1V

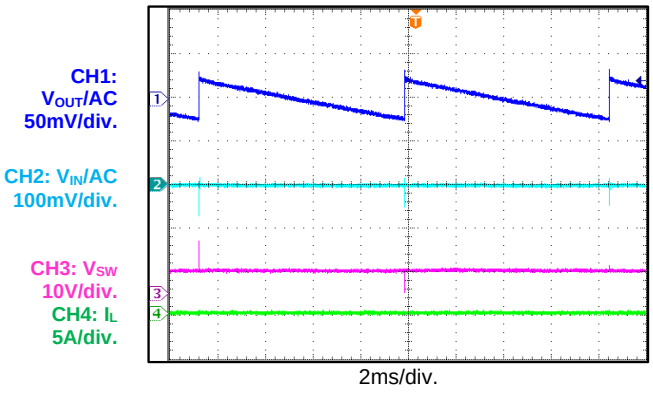


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, f_{SW} = 750kHz, T_J = 25°C, unless otherwise noted.

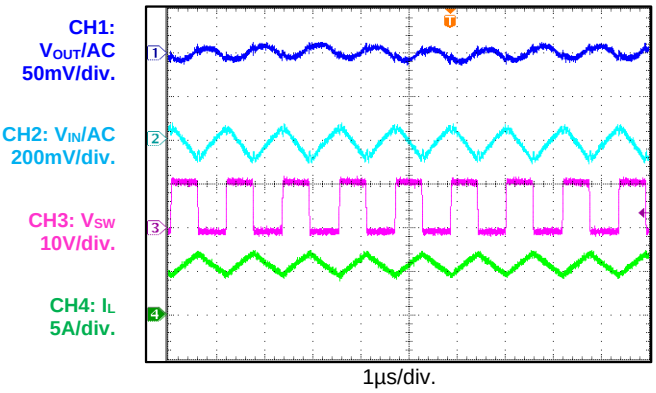
Input and Output Voltage Ripple

V_{OUT} = 5V, I_{OUT} = 0A



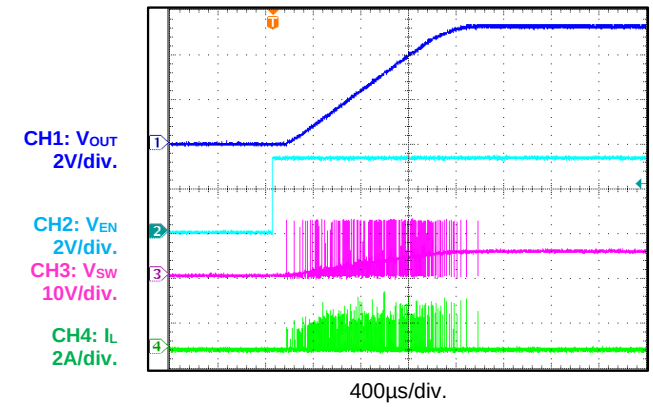
Input and Output Voltage Ripple

V_{OUT} = 5V, I_{OUT} = 6A



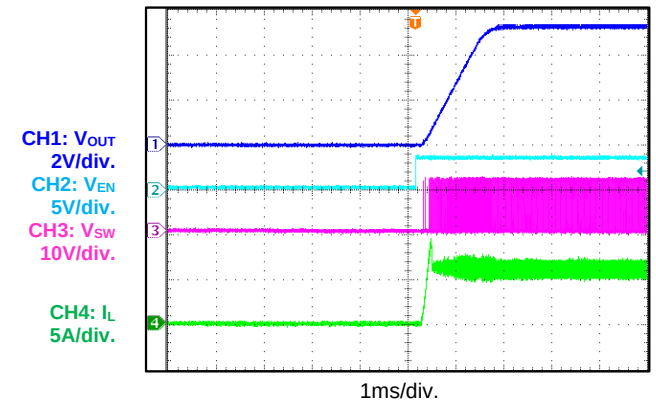
Start-Up through EN

V_{OUT} = 5V, I_{OUT} = 0A



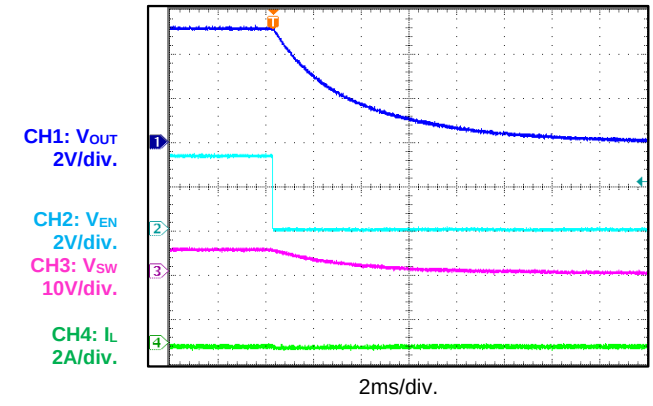
Start-Up through EN

V_{OUT} = 5V, I_{OUT} = 6A



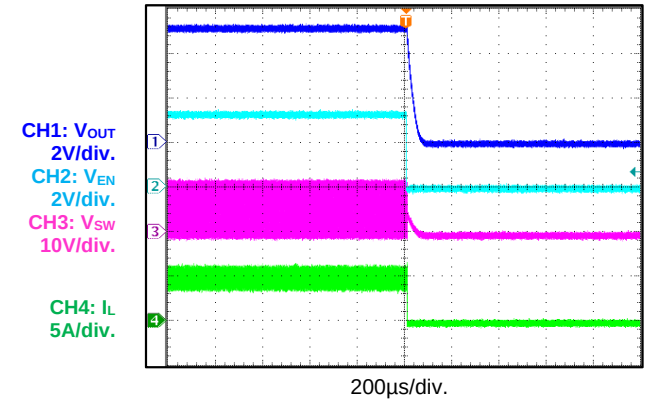
Shutdown through EN

V_{OUT} = 5V, I_{OUT} = 0A



Shutdown through EN

V_{OUT} = 5V, I_{OUT} = 6A

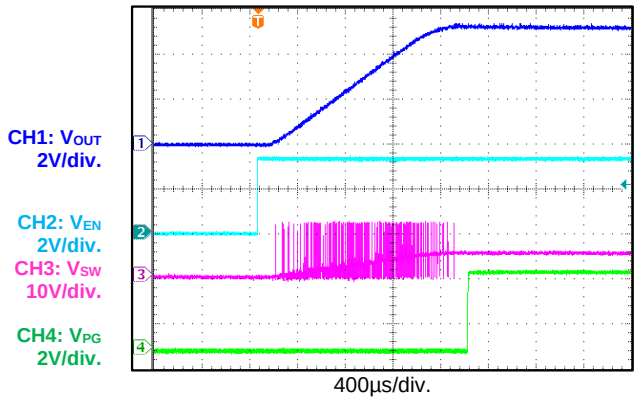


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, f_{SW} = 750kHz, T_J = 25°C, unless otherwise noted.

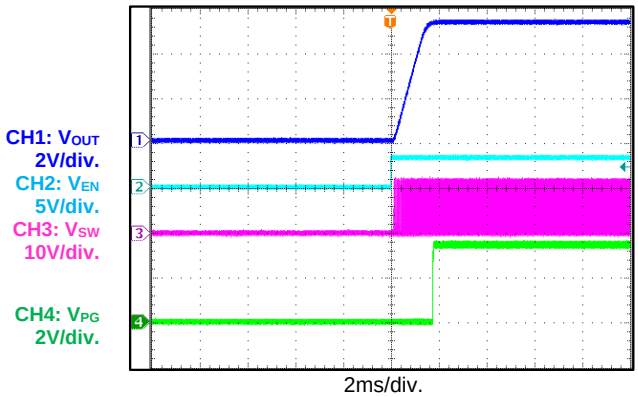
PG Start-Up through EN

V_{OUT} = 5V, I_{OUT} = 0A



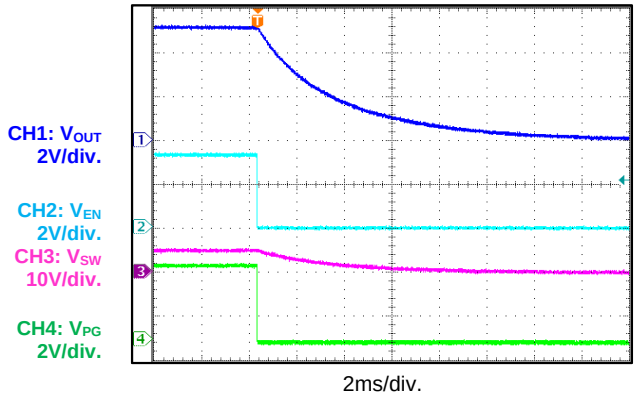
PG Start-Up through EN

V_{OUT} = 5V, I_{OUT} = 6A



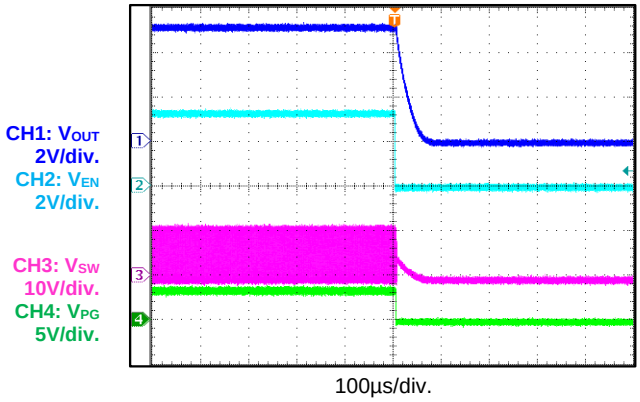
PG Shutdown through EN

V_{OUT} = 5V, I_{OUT} = 0A



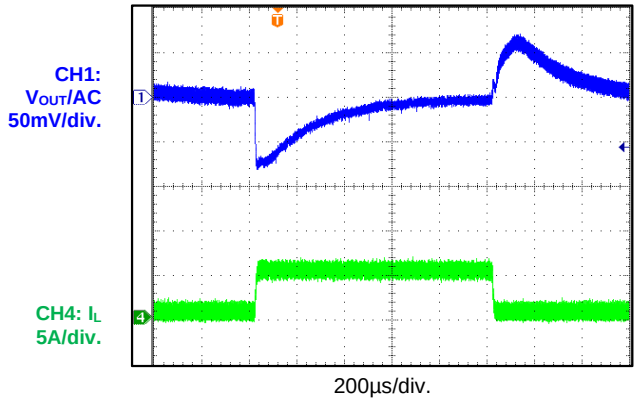
PG Shutdown through EN

V_{OUT} = 5V, I_{OUT} = 0A



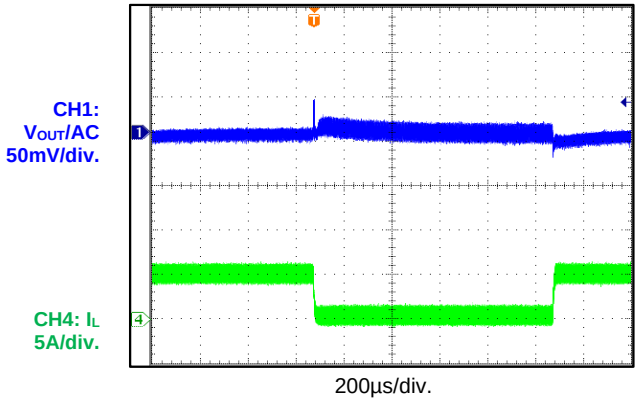
Load Transient Response

V_{OUT} = 5V, I_{OUT} = 0.6A to 5.4A, 1.6A/µs,
C_{OUT} = 5 x 22µF



Load Transient Response

V_{OUT} = 1V, I_{OUT} = 0.6 - 5.4A, 1.6A/µs,
C_{OUT} = 5 x 22µF

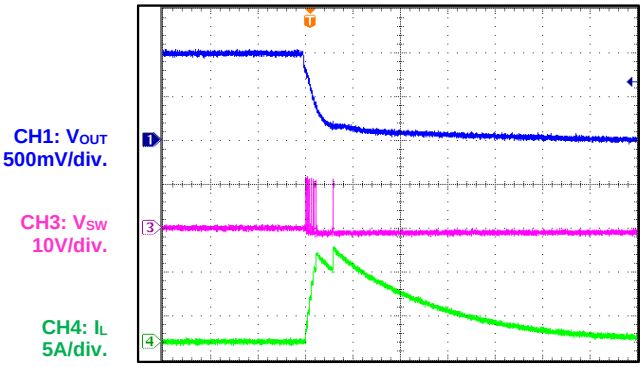


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, f_{SW} = 750kHz, T_J = 25°C, unless otherwise noted.

Short-Circuit Protection

V_{IN} = 12V, V_{OUT} = 1V



FUNCTIONAL BLOCK DIAGRAM

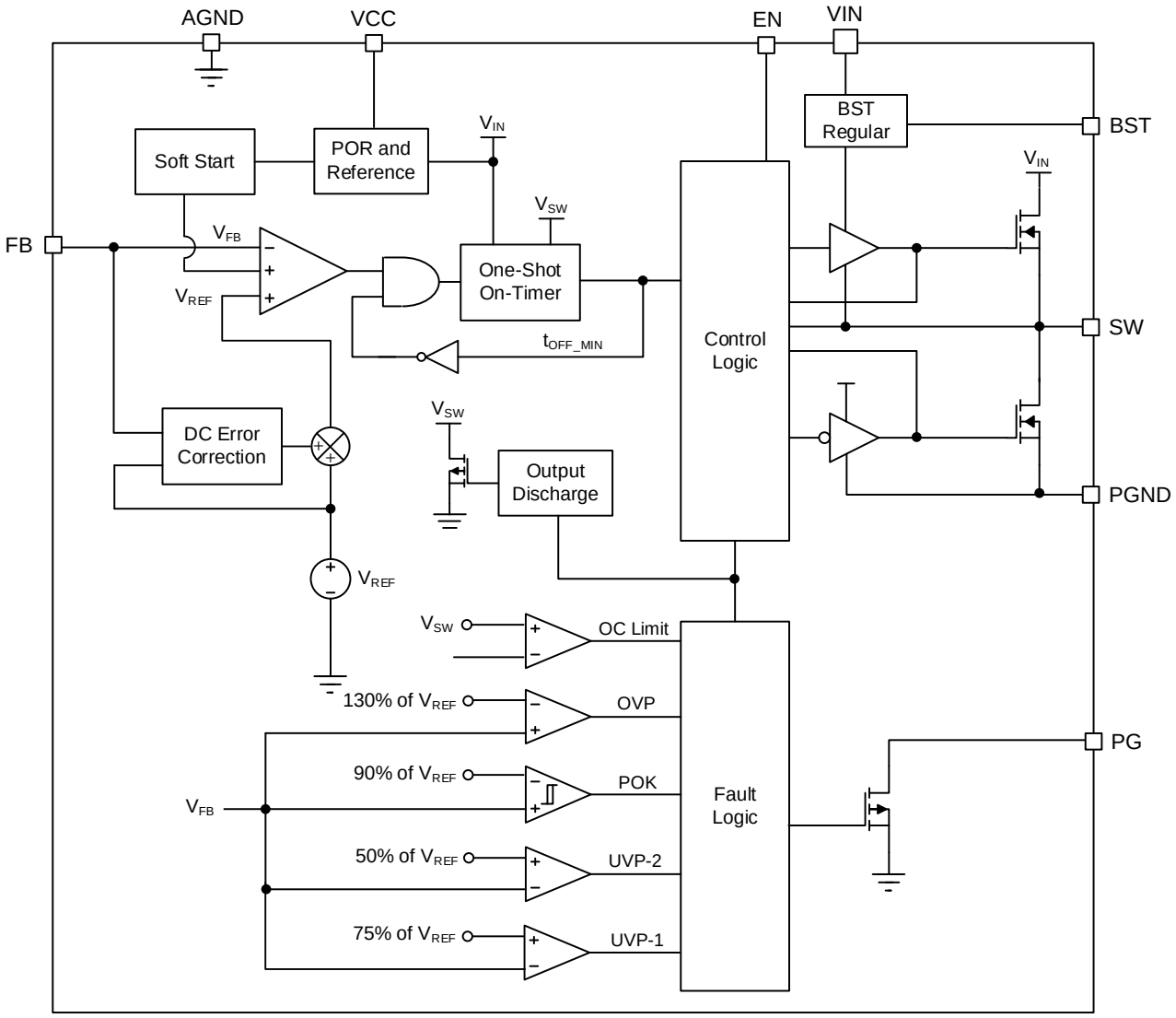


Figure 1: Functional Block Diagram

OPERATION

The MP8639 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each PWM cycle, the high-side MOSFET (HS-FET) turns on once the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage (V_{OUT}). The on time (t_{ON}) is determined by the input voltage (V_{IN}) and V_{OUT} to maintain a constant switching frequency (f_{SW}) across the entire V_{IN} range.

After t_{ON} elapses, the HS-FET turns off. Once V_{FB} drops below V_{REF}, the HS-FET turns on again. The converter regulates V_{OUT} by repeating this operation. The integrated low-side MOSFET (LS-FET) turns on once the HS-FET turns off to minimize conduction loss. If the HS-FET and LS-FET turn on at the same time, a dead short occurs between the input and GND. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off time (t_{OFF}) and LS-FET t_{ON}, and vice versa.

COT control with internal compensation provides stable operation, even if ceramic output capacitors (C_{OUT}) are used. Internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

In continuous conduction mode (CCM), the output current (I_{OUT}) is high and the inductor current (I_L) exceeds 0A (see Figure 2).

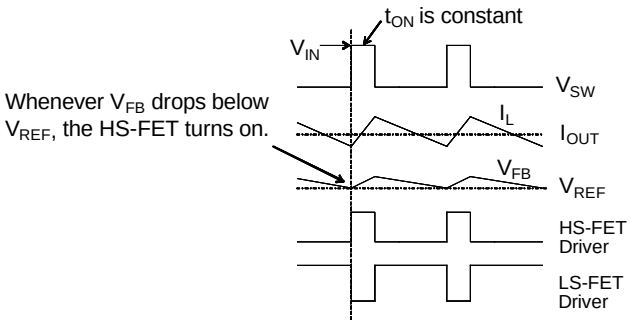


Figure 2: CCM during Heavy-Load Operation

If V_{FB} drops below V_{REF}, then the HS-FET turns on for a fixed interval that is determined by the one-shot on-timer. If the HS-FET turns off, then the LS-FET turns on until the next period begins. f_{SW} remains fairly constant during CCM. This is also called pulse-width modulation (PWM) mode.

Light-Load Operation

I_L decreases as the load decreases. Once I_L reaches 0A, the IC transitions from CCM to discontinuous conduction mode (DCM) (see Figure 3).

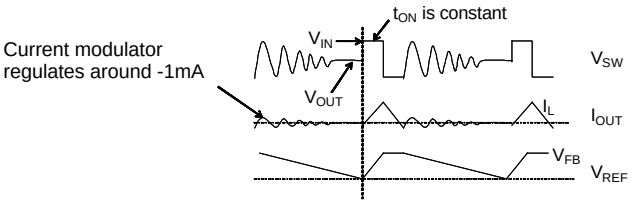


Figure 3: DCM during Light-Load Operation

If V_{FB} drops below V_{REF}, then the HS-FET turns on for a fixed interval that is determined by the one-shot on-timer. If the HS-FET turns off, then the LS-FET turns on until I_L reaches 0A.

In DCM, V_{FB} should not reach V_{REF} while I_L approaches 0A. The LS-FET driver switches to a high impedance (Hi-Z) state once I_L reaches 0A. A current modulator takes control of the LS-FET and limits I_L below -1mA. C_{OUT} discharges to ground slowly through the LS-FET, improving light-load efficiency. Under light-load conditions, the HS-FET does not turn on as frequently as it does under heavy-load conditions. This is called pulse-skip mode (PSM).

Under light-load or no-load conditions, V_{OUT} drops slowly to reduce f_{SW} and improve efficiency at light loads.

As I_{OUT} increases, the current modulator's regulation time shortens. The HS-FET turns on more frequently and f_{SW} increases. I_{OUT} reaches its critical level ($I_{OUT\_CRITICAL}$) once the current modulator time reaches 0s.

$I_{OUT\_CRITICAL}$ can be calculated using Equation (1):

$$I_{OUT\_CRITICAL} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once I_{OUT} exceeds $I_{OUT\_CRITICAL}$. After entering PWM mode, f_{SW} remains fairly constant across the entire I_{OUT} range.

Jitter and Feedback (FB) Ramp

If noise in the V_{FB} ripple propagates a delay to the HS-FET driver, then jitter can occur in both PWM mode and PSM.

Figure 4 shows jitter in PWM mode.

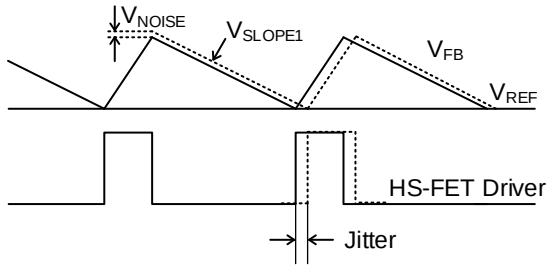


Figure 4: Jitter in PWM Mode

Figure 5 shows jitter in PSM.

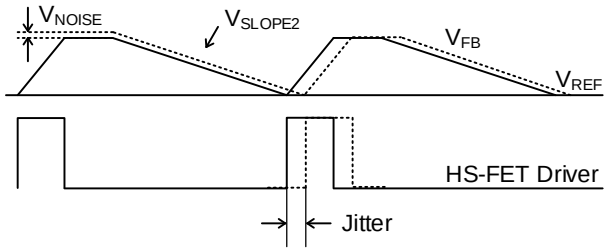


Figure 5: Jitter in PSM

Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope. As a result, jitter in DCM is typically larger than jitter in CCM. However, the V_{FB} ripple does not directly affect noise immunity.

External Ramp Compensation

The MP8639 can typically support use of a ceramic C_{OUT} without an external ramp. However, the internal ramp may not be sufficient to stabilize the system, or the jitter may be too large. In these cases, external ramp compensation is required. See the Application Information section on page 17 for more details.

Enable (EN) Control

The enable (EN) pin can enable and disable the IC. Pull EN high to turn the converter on; pull EN low to turn the converter off. Do not float EN.

For automatic start-up, pull EN up to VIN via a voltage resistor divider. Use the pull-up resistance (R_{UP}, from VIN to EN) and the pull-down resistance (R_{DOWN}, from EN to ground) to determine the automatic start-up voltage (V_{IN_START}). V_{IN_START} can be calculated using Equation (2):

$$V_{IN\_START} = 1.25 \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} (V) \quad (2)$$

For example, if R_{UP} = 150kΩ and R_{DOWN} = 51kΩ, then set V_{IN_START} to 4.92V.

It is recommended to connect a 10nF ceramic capacitor between EN and ground to avoid noise.

If EN is controlled via an external logic signal, then the EN voltage (V_{EN}) should be below 4.5V.

Power Good (PG)

The MP8639 has a power good (PG) output to indicate whether the buck converter's V_{OUT} is ready. PG is the MOSFET's open drain, and should be connected to V_{CC} or another voltage source via a 100kΩ resistor. When V_{IN} is applied, the MOSFET turns on and PG is pulled to GND before soft start (SS) is ready. Once V_{FB} reaches 95% of V_{REF}, PG is pulled high within 5µs.

If V_{FB} drops to 85% of V_{REF} or exceeds 115% of V_{REF}, then PG is pulled low.

Soft Start (SS)

The MP8639 employs SS to ensure smooth V_{OUT} during start-up. If V_{EN} goes high, then the internal V_{REF} ramps up slowly to ensure that V_{OUT} ramps up slowly as well. Once V_{REF} reaches its target value, SS completes and the device enters steady state operation (see Figure 6 on page 15).

If the output is pre-biased to a certain voltage during start-up, then the IC disables the HS-FET and LS-FET switching until V_{REF} exceeds the sensed V_{OUT}.

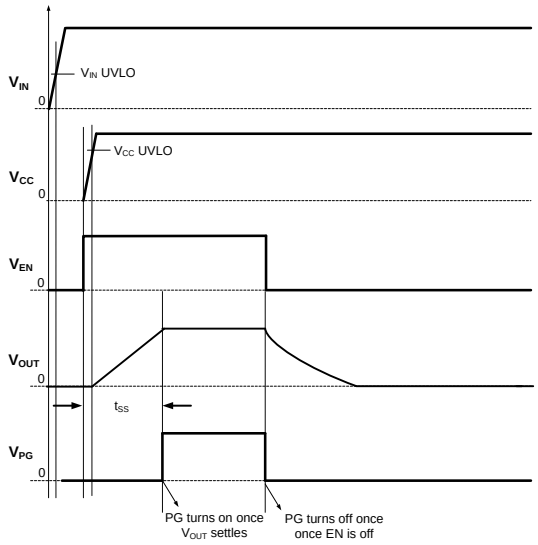


Figure 6: Start-Up and Shutdown Power Sequence

Over-Current Protection (OCP)

The MP8639 has cycle-by-cycle over-current protection (OCP). The current limit circuit employs a valley current-sensing algorithm. The MP8639 uses the LS-FET on resistance ($R_{DS(ON)\_LS}$) as a current-sensing element. If the current-sense signal magnitude exceeds the current limit threshold, then the PWM comparator cannot start a new PWM cycle, even if V_{FB} is below V_{REF}. Figure 7 shows the detailed operation of the valley current limit.

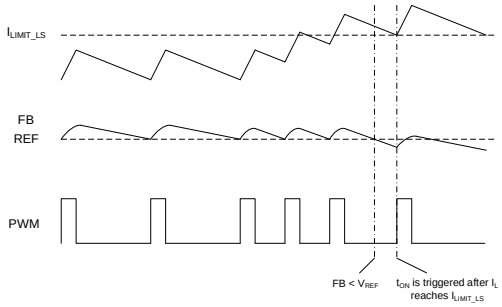


Figure 7: Valley Current Limit Control

Since the comparison occurs during the LS-FET t_{ON}, the over-current (OC) trip level sets the I_L valley threshold (I_{LIMIT_LS}).

The maximum load current (I_{LOAD_MAX}) at the OC threshold (I_{OC}) can be calculated using Equation (3):

$$I_{OC} = I_{LIMIT} + \frac{\Delta I_L}{2} \quad (3)$$

I_{OC} limits I_L and does not latch off. If an OC fault occurs, then the current to the load exceeds the current to C_{OUT}, and V_{OUT} typically drops. Eventually the current crosses the under-voltage protection (UVP) threshold and latches off. Fault latching can be reset by pulling EN low or cycling the power on VIN.

Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The MP8639 monitors the FB resistor divider to detect over-voltage (OV) and under-voltage (UV) conditions. If V_{FB} exceeds 130% of the target voltage, then the over-voltage protection (OVP) comparator output goes high. The circuit latches as the HS-FET turns off and the LS-FET turns on. This functions as a -2A current source.

To protect the MP8639 from damage, there is an absolute OVP on V_{OUT}. If V_{FB} is between 50% and 75% of V_{REF}, then the UVP threshold 1 comparator output goes high. If V_{FB} remains in this range for about 50µs, then the MP8639 latches off, which latches the HS-FET off and the LS-FET on. The LS-FET remains on until I_L reaches 0A. During this period, the valley current limit helps control I_L.

When V_{FB} drops below 50% of V_{REF}, the UVP threshold 2 comparator output goes high. After the comparator and logic delay, the MP8639 latches off, which latches the HS-FET off and the LS-FET on. The LS-FET remains on until I_L reaches 0A. Fault latching can be reset by driving EN low or cycling the power on VIN.

Under-Voltage Lockout (UVLO) Protection

The MP8639 has two under-voltage lockout (UVLO) protections: 3.2V V_{CC} UVLO and 4.35V V_{IN} UVLO. The MP8639 starts up once V_{CC} and V_{IN} exceed their respective UVLO thresholds. If either V_{CC} or V_{IN} drops below their UVLO falling threshold (2.8V and 3.2V, respectively), then the IC shuts down. Both V_{CC} UVLO and V_{IN} UVLO are non-latch protections.

If an application requires a higher UVLO, use EN to adjust V_{IN} UVLO via two external resistors (see Figure 8 on page 16).

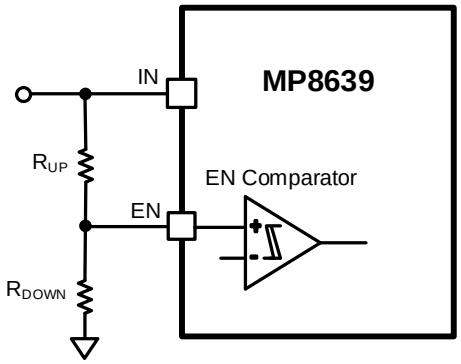


Figure 8: Adjustable UVLO Protection

Thermal Shutdown

The IC's junction temperature (T_J) is internally monitored. If T_J exceeds the thermal shutdown threshold (typically 150°C), then the converter shuts down. Once T_J drops to about 125°C, a new SS is initiated and the device resumes normal operation. There is a hysteresis of about 25°C. Thermal shutdown is a non-latch protection.

Output Discharge

If the controller is turned off by a protection function, such as UVP, OCP, OVP, UVLO, or thermal shutdown, then the MP8639 discharges all outputs. The output discharge resistor is typically 6Ω.

APPLICATION INFORMATION

Setting the Output Voltage without an External Ramp

The MP8639 does not require ramp compensation for applications where POSCAP or ceramic capacitors are used as C_{OUT}. V_{OUT} can then be set by the feedback (FB) resistors, R1 and R2 (see Figure 9).

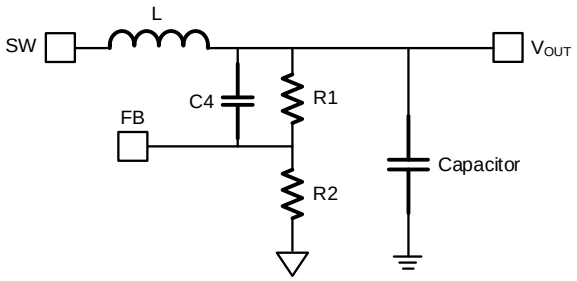


Figure 9: Simplified Circuit without External Ramp Compensation

Choose a value for R2. Consider that a small R2 can lead to considerable quiescent current (I_Q) loss, while a large R2 can make FB sensitive to noise. It is recommended to choose R2 to be between 5kΩ and 100kΩ. If V_{OUT} is low (1.05V), choose a larger R2. If V_{OUT} is high, choose a smaller R2. Considering the V_{OUT} ripple, R1 can be calculated using Equation (4):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (4)$$

A feed-forward capacitor (C4) improves the transient response. C4 can be set between 100pF and 1nF. A larger-value C4 improves transient response but results in more noise sensitivity.

Setting the Output Voltage with an External Ramp

If the system is not stable enough or the jitter is too large when ceramic capacitors are used, then an external voltage ramp should be added to FB via R4 and C4.

Since an internal ramp is already added to the system, a 1MΩ R4 and 220pF C4 ramp are sufficient. V_{OUT} is influenced by R1, R2, and R4 (see Figure 10).

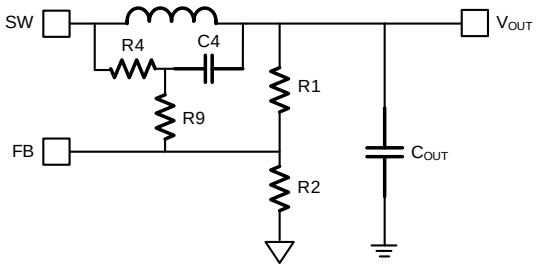


Figure 10: Simplified Circuit with External Ramp Compensation

Choose a reasonable R2 since a small R2 value can lead to considerable I_Q loss, while a large R2 value can make FB sensitive to noise. R2 is recommended to be between 5kΩ and 100kΩ. If V_{OUT} is low (1.05V), choose a larger R2. If V_{OUT} is high, choose a smaller R2. R1 can then be calculated using Equation (5):

$$R1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \times R2 \quad (5)$$

R9 is typically 0Ω and can be set to create a pole to reduce noise. R9 can be calculated using Equation (6):

$$R9 = \frac{1}{2\pi \times C4 \times 2f_{SW}} \quad (6)$$

Choose R9 to be between 1kΩ and 100Ω to reduce its influence on the ramp.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. Place the ceramic input capacitors (C_{IN}) as close to VIN as possible for the best performance. Capacitors with X5R and X7R ceramic dielectrics are recommended due to their stability amid temperature fluctuations.

The capacitors must also have a ripple current rating exceeding the converter's maximum input ripple current (I_{CIN}). I_{CIN} can be estimated using Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated using Equation (8):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of I_{LOAD_MAX}.

C_{IN} determines the converter V_{IN} ripple (ΔV_{IN}). If there is ΔV_{IN} requirement in the system, choose C_{IN} to meet the relevant specifications.

ΔV_{IN} can be estimated using Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be estimated using Equation (10):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (10)$$

Selecting the Output Capacitor

C_{OUT} is required to maintain the DC V_{OUT}. It is recommended to use ceramic or POSCAP capacitors. The V_{OUT} ripple (ΔV_{OUT}) can be estimated using Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (11)$$

When using ceramic capacitors, the impedance dominates the capacitance at f_{SW}. The capacitance causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated using Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Since ΔV_{OUT} caused by the ESR is small, an external ramp is required to stabilize the system. The external ramp can be generated via R4 and C4.

When using POSCAP capacitors, the ESR dominates the impedance at f_{SW}. The ramp voltage generated from the ESR dominates ΔV_{OUT}. ΔV_{OUT} can be estimated using Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

The maximum C_{OUT} (C_{OUT_MAX}) should be considered in the design application. The MP8639 has a soft-start time (t_{SS}) of about 1.6ms. If C_{OUT} is too high, V_{OUT} cannot reach the intended value based on the feedback resistor divider during t_{SS} and fails to regulate. C_{OUT_MAX} can be approximately limited using Equation (14):

$$C_{OUT\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (14)$$

Where I_{LIM_AVG} is the average start-up current during SS.

Selecting the Inductor

An inductor is required to supply constant current to the output load while being driven by the switched V_{IN}. A larger-value inductor results in a smaller ripple current and lower ΔV_{OUT}; however, it also has a larger physical footprint, higher series resistance, and lower saturation current.

A good rule for determining the inductance (L) is to design the inductor's peak-to-peak inductor ripple current (ΔI_L) to be between 30% and 50% of the maximum output current (I_{OUT_MAX}). The peak inductor current (I_{L_PEAK}) should also remain below the maximum switching current limit. L can be calculated using Equation (15):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

To prevent the inductor from saturating under the maximum I_{L_PEAK}, the saturation current (I_{SAT}) must exceed 7.5A.

Table 1 shows design examples for when ceramic capacitors are used.

Table 1: Design Example

V_{OUT} (V)	C_{OUT} (F)	L (µH)	C4 (pF)	R4(kΩ)	R1 (kΩ)	R2 (kΩ)	R9(Ω)
0.6	22µ x 3	0.68	NS	NS	0	NS	NS
1	22µ x 3	0.68	220	NS	40.2	60.4	499
1.8	22µ x 3	1 to 1.5	220	NS	40.2	20	499
2.5	22µ x 4	1 to 1.5	220	887	84.5	24.3	499
3.3	22µ x 4	1.5	220	499	80.6	15.4	499

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended for improved thermal performance. For the best results, refer to Figure 11 and follow the guidelines below:

1. Place the high-current paths (AGND, VIN, and SW) as close to the device as possible using short, direct, and wide traces.
2. Place C_{IN} as close to VIN and AGND as possible.
3. Place the decoupling capacitor as close to VCC and GND as possible.
4. Keep SW short and away from the feedback network.
5. Keep the bootstrap (BST) path as short as possible using a >50mil trace.
6. To improve thermal performance, connect the VIN and GND pads using a large copper plane.
7. To improve thermal dissipation, add multiple vias with a 10mil drill and 18mil copper width close to the VIN and AGND pads.

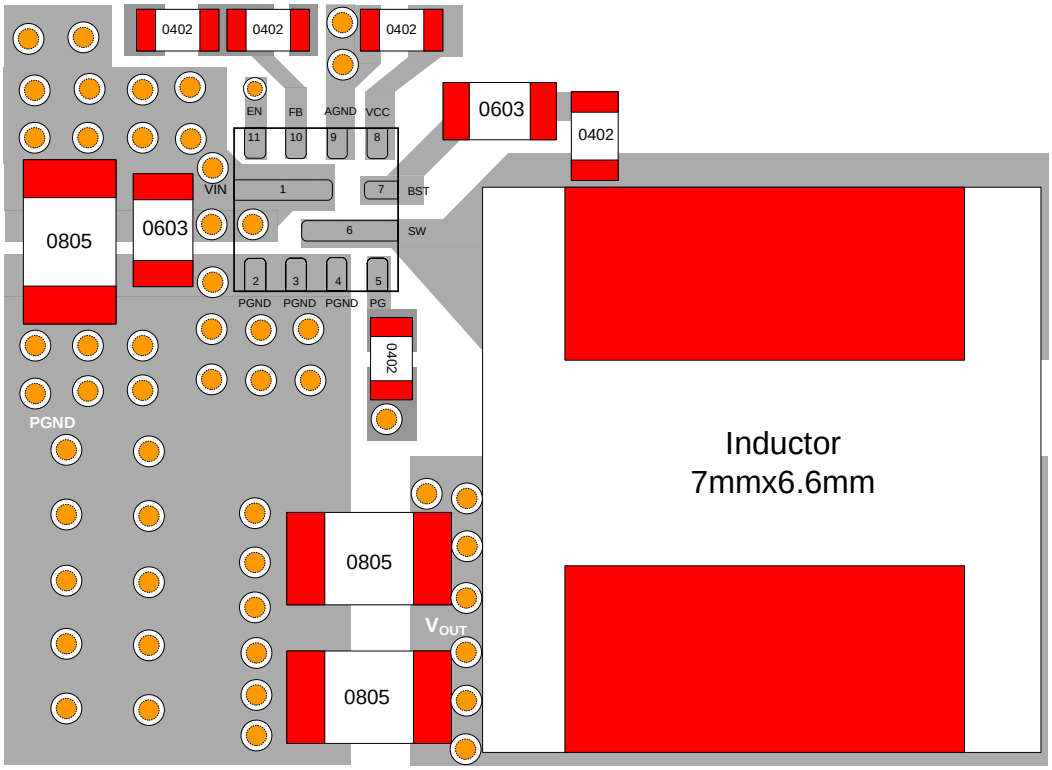


Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

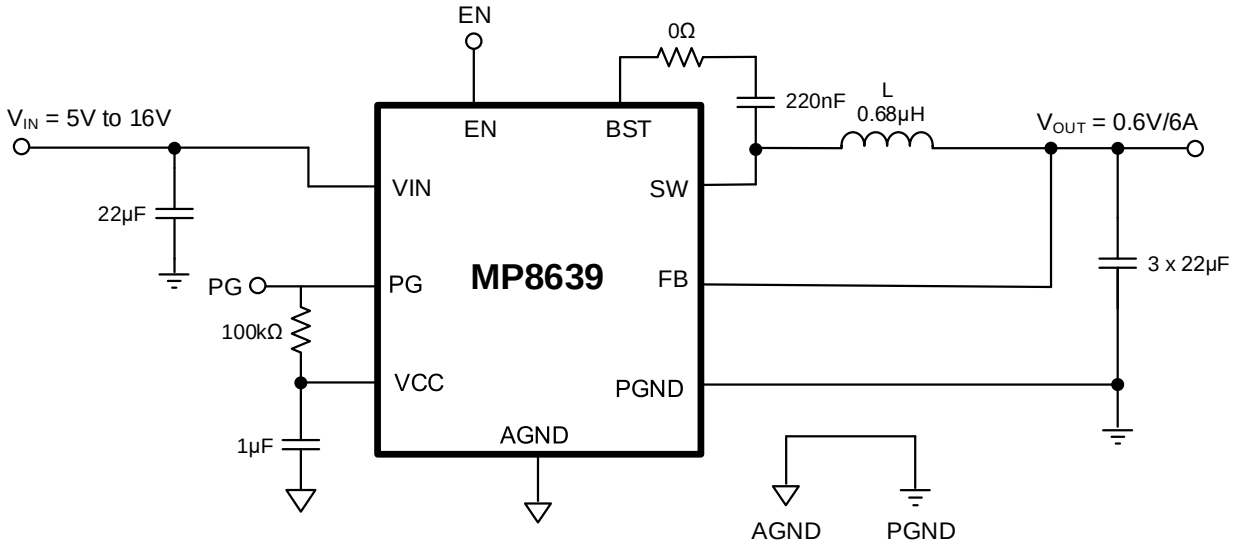


Figure 12: Typical Application Circuit with Low-ESR Ceramic C_{OUT} (V_{IN} = 5V to 16V, V_{OUT} = 0.6V, I_{OUT} = 6A)

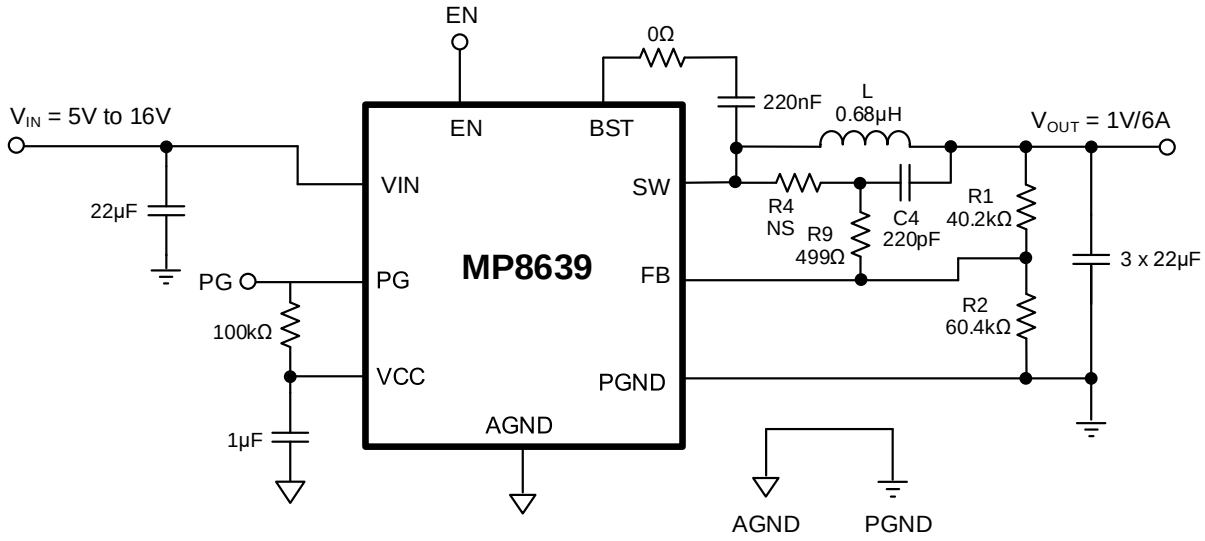


Figure 13: Typical Application Circuit with Low-ESR Ceramic C_{OUT} (V_{IN} = 5V to 16V, V_{OUT} = 1V, I_{OUT} = 6A)

TYPICAL APPLICATION CIRCUITS *(continued)*

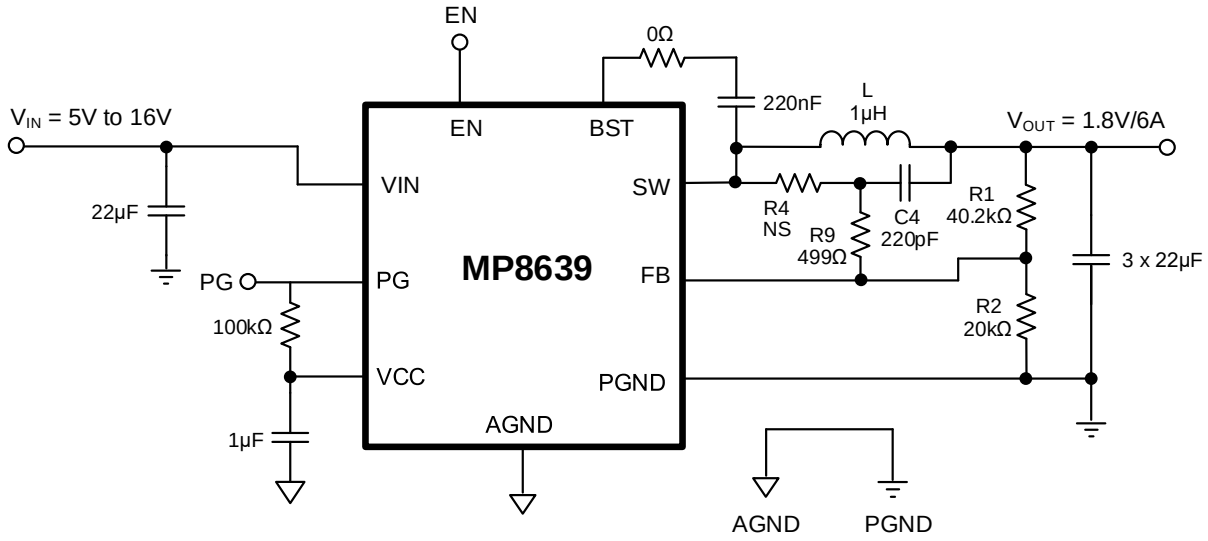


Figure 14: Typical Application Circuit with Low-ESR Ceramic C_{OUT} (V_{IN} = 5V to 16V, V_{OUT} = 1.8V, I_{OUT} = 6A)

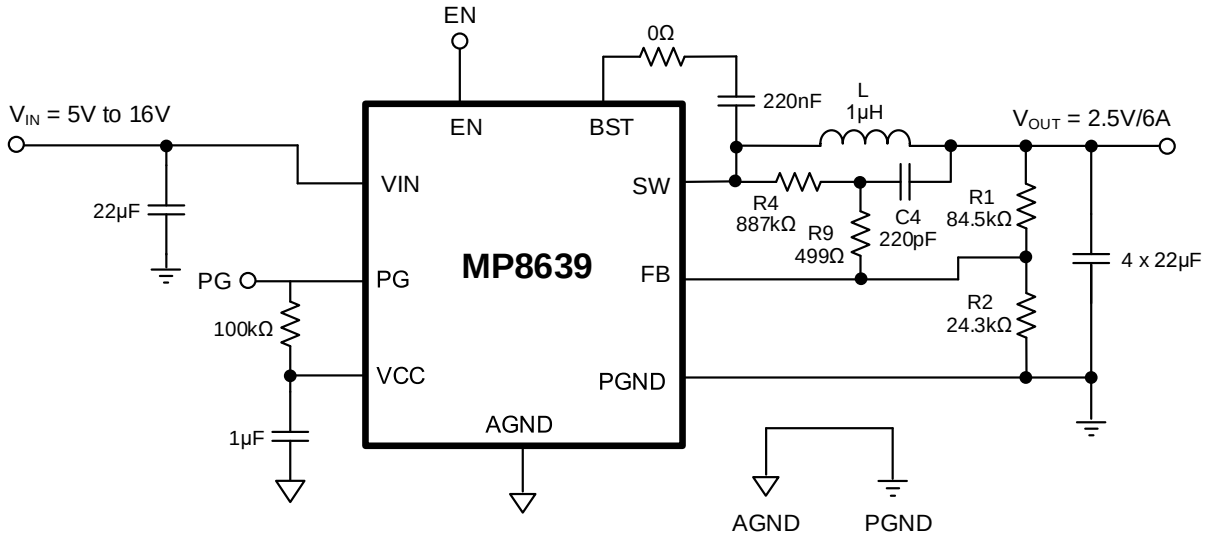


Figure 15: Typical Application Circuit with Low-ESR Ceramic C_{OUT} (V_{IN} = 5V to 16V, V_{OUT} = 2.5V, I_{OUT} = 6A)

TYPICAL APPLICATION CIRCUITS *(continued)*

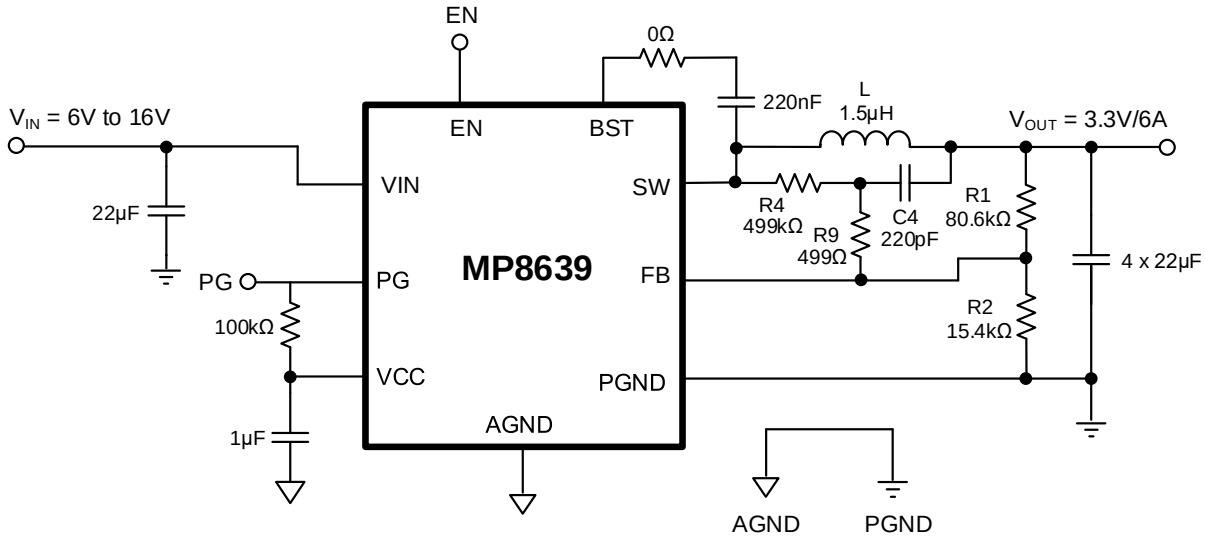
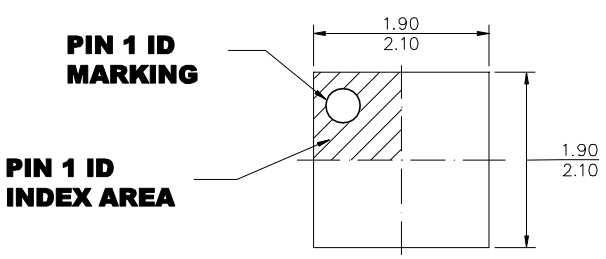


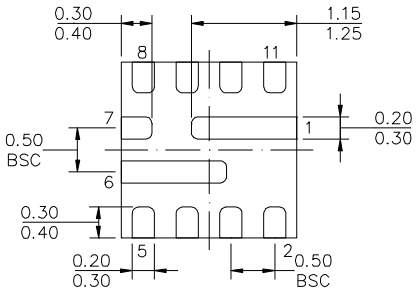
Figure 16: Typical Application Circuit with Low-ESR Ceramic C_{OUT} (V_{IN} = 6V to 16V, V_{OUT} = 3.3V, I_{OUT} = 6A)

PACKAGE INFORMATION

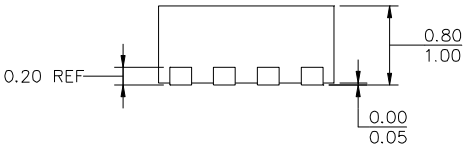
QFN-11 (2mmx2mm)



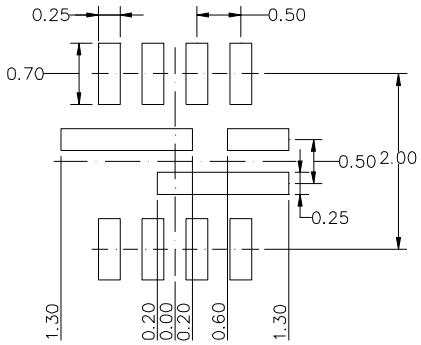
TOP VIEW



BOTTOM VIEW



SIDE VIEW

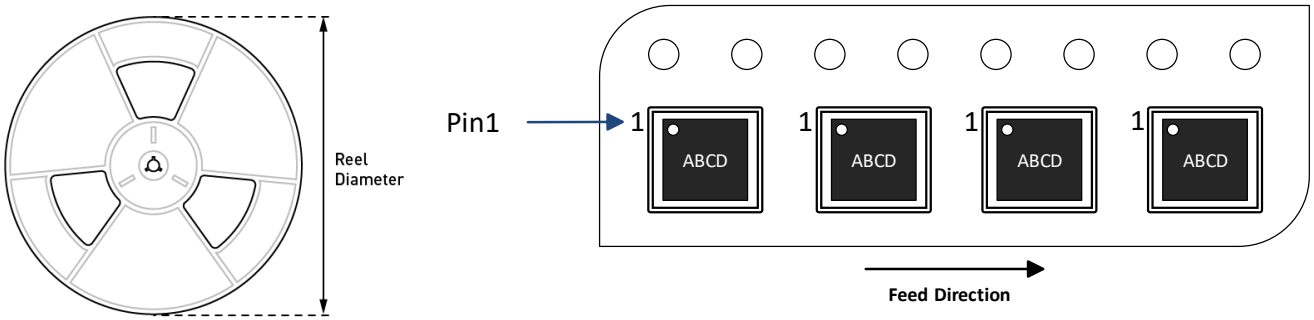


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1 AND PIN6 HAVE THE SAME LENGTH AND WIDTH
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VCCD.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8639GG-Z	QFN-11 (2mmx2mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/22/2022	Initial Release	-