MP6982

Fast Turn-Off, Intelligent Rectifier with No Auxiliary Winding Requirement

DESCRIPTION

The MP6982 is a fast turn-off, intelligent rectifier for GaN HEMT applications. When combined with an external GaN HEMT, the MP6982 can replace a Schottky diode for higher efficiency. The device regulates the external synchronous rectification (SR) GaN HEMT's forward voltage drop ($V_{FORWARD}$) to about 40mV and turns off before the drain-to-source voltage (V_{DS}) reverses.

The MP6982 can generate its own supply voltage without the need for auxiliary winding, which makes it suitable for charger applications with a low output voltage (V_{OUT}), or for high-side (HS) SR configurations. The configurable ringing detection circuitry prevents the MP6982 from falsely turning on during discontinuous conduction mode (DCM) and quasi-resonant (QR) operations.

The MP6982 is available in a space-saving TSOT23-6 package.

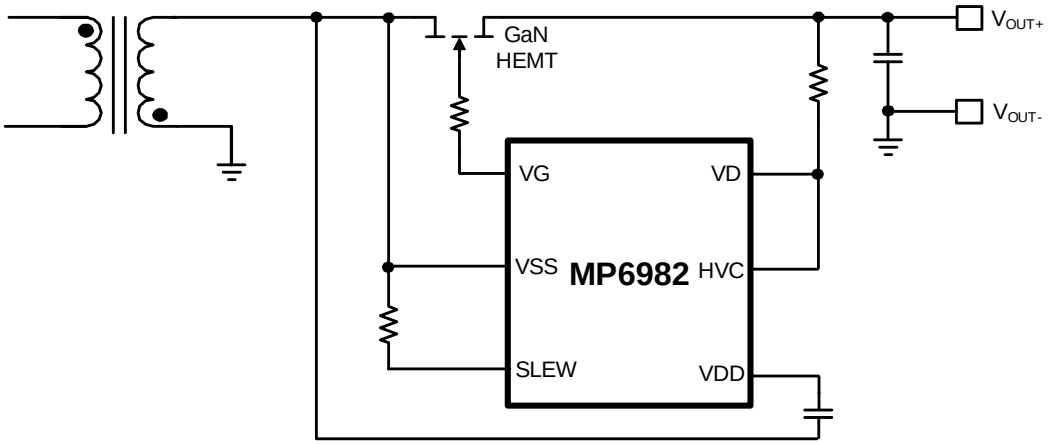
FEATURES

- Supports Discontinuous Conduction Mode (DCM), Continuous Conduction Mode (CCM), Quasi-Resonant (QR) Operation, and Active-Clamp Flyback (ACF) Operation
- Up to 600kHz Switching Frequency (f_{SW}) for GaN HEMT Applications
- Wide Output Voltage Range Down to 0V, Operational Even during an Output Short
- No Auxiliary Winding Requirement for High-Side (HS) or Low-Side (LS) Rectification
- Ringing Detection Prevents False Turn-On during DCM and QR Operation
- Compatible with Energy Star Standards
- 30ns Typical Fast Turn-Off and Fast Turn-On Delay
- 150µA Typical Quiescent Current (I_Q)
- Supports HS and LS Rectification
- Available in a TSOT23-6 Package

APPLICATIONS

- USB Power Delivery (PD) Fast Chargers
- Adapters
- Flyback Power Supplies with Very Low and/or Variable Output Voltages

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6982GJ	TSOT23-6	*See Below*	1

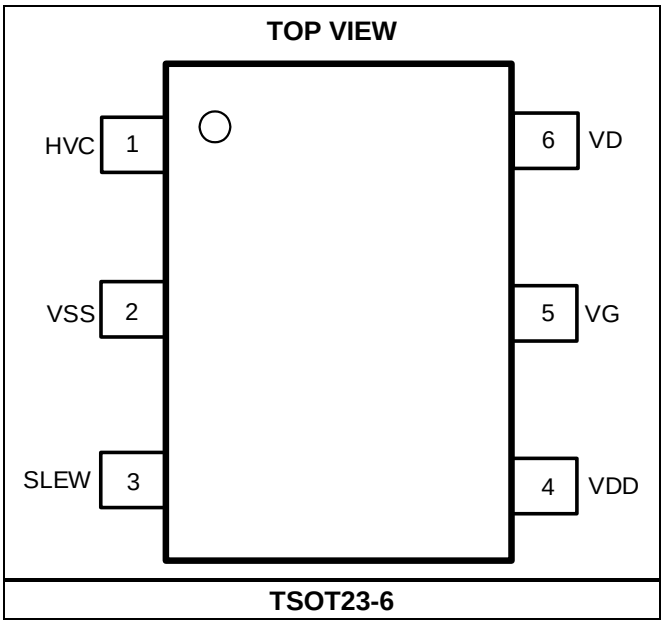
* For Tape & Reel, add suffix -Z (e.g. MP6982GJ-Z).

TOP MARKING

|BULY

BUL: Product code of MP6982GJ
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	HVC	**HV linear regulator input.**
2	VSS	**Ground.** The VSS pin is used as a GaN HEMT's source sense reference for the VD pin.
3	SLEW	**Signal slew rate detection configuration.** The SLEW pin prevents the SR controller from falsely turning on by ringing below the turn-on threshold at the VD pin during discontinuous conduction mode (DCM) and quasi-resonant (QR) operation. Any signal slower than the pre-set slew rate cannot turn on VG.
4	VDD	**Linear regulator output.** The VDD pin supplies power to the device.
5	VG	**Gate driver output.**
6	VD	**GaN HEMT's drain voltage sense.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD, VG to VSS .....-0.3V to +14V
VD, HVC to VSS .....-1V to +180V
SLEW to VSS .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) 0.56W
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C
Storage temperature ..... -55°C to +150°C

Recommended Operating Conditions (3)

VDD to VSS .....4.5V to 13V
VD, HVC to VSS .....-1V to +150V
Maximum junction temperature (T_J).....125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 .....220 .....110 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 5.4V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Management						
VDD voltage (V_{DD}) under-voltage lockout (UVLO) rising threshold	$V_{DD\_UVLO\_RISING}$		4	4.2	4.4	V
V_{DD} UVLO hysteresis			0.1	0.2	0.3	V
VDD maximum charging current	I_{VDD}	V_{DD} = 5V, V_{HVC} = 12V	30	50	75	mA
		V_{DD} = 4V, V_D = 30V	20	40	62	mA
VDD regulation voltage		V_D = 12V, V_{HVC} = 12V	5	5.4	5.7	V
		V_{HVC} = 3V, V_D = 12V	4.6	5	5.4	V
Operating current	I_{CC}	V_{DD} = 5.4V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz		1.8	2.2	mA
		V_{DD} = 5V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz		1.72	2.1	mA
Quiescent current	I_Q	V_{DD} = 5V		150	180	µA
Shutdown current	I_{SD}	V_{DD} = $V_{DD\_UVLO\_RISING}$ - 0.1V			100	µA
Control Circuitry						
Forward regulation voltage (V_{SS} to V_D)	V_{FWD}		23	40	55	mV
Turn-on threshold (V_{DS})	V_{DRV_ON}		-115	-86	-57	mV
Turn-off threshold (V_{SS} to V_D)	V_{DRV_OFF}		-6	+3	+12	mV
Turn-on delay	t_{DELAY_ON}	C_{LOAD} = 2.2nF		30	50	ns
Turn-off delay	t_{DELAY_OFF}	C_{LOAD} = 2.2nF		25	45	ns
Turn-off propagation delay (5) (6)				15		ns
Turn-on blanking time	t_{BLANK_ON}	C_{LOAD} =2.2nF	105	180	250	ns
Turn-off blanking threshold (V_{DS})	V_{BLANK_OFF}		2	2.5	3	V
Turn-off threshold during the minimum on time (V_{DS})			1.3	1.8	2.1	V
Turn-on slew rate detection timer	t_{SLEW}	R_{SLEW} = 400kΩ		40		ns
Gate Driver (VG)						
Gate driver low voltage	V_{G_LOW}	I_{LOAD} = 10mA		0.01	0.02	V
Gate driver high voltage	V_{G_HIGH}	I_{LOAD} = 0mA	4.9			V
Maximum source current (5) (6)				0.5		A
Maximum sink current (5) (6)				3		A
Pull-down resistance		I_{LOAD} = 10mA		1	2	Ω

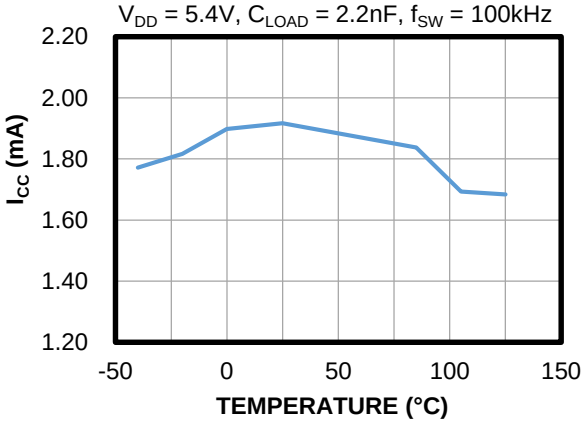
Note:

5) Guaranteed by characterization.
6) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

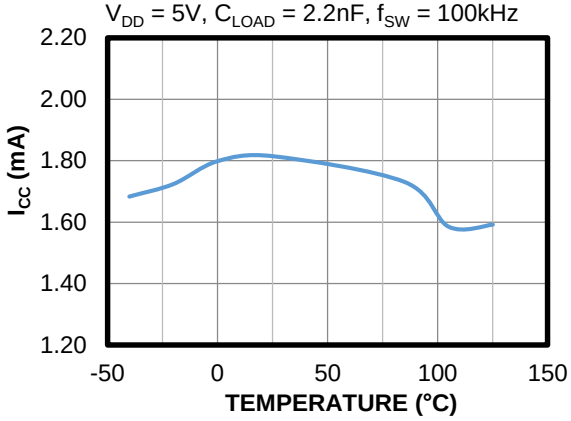
Operating Current vs. Temperature

V_{DD} = 5.4V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz



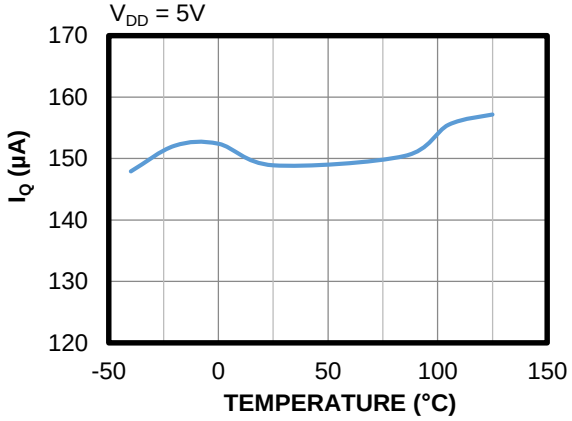
Operating Current vs. Temperature

V_{DD} = 5V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz



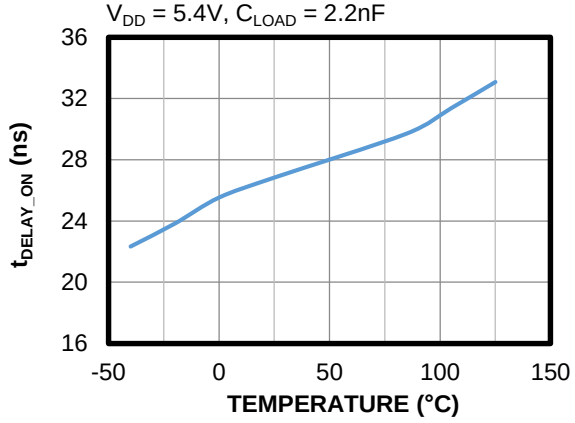
Quiescent Current vs. Temperature

V_{DD} = 5V



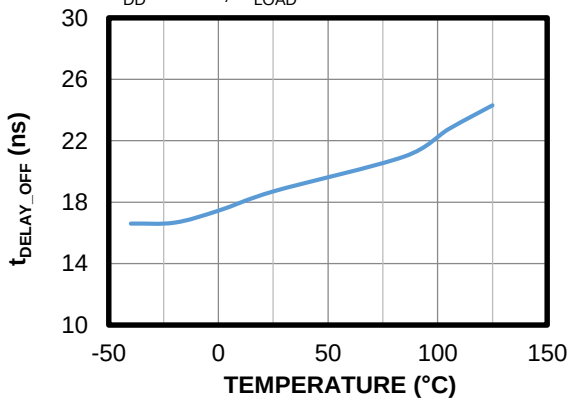
Turn-On Delay vs. Temperature

V_{DD} = 5.4V, C_{LOAD} = 2.2nF

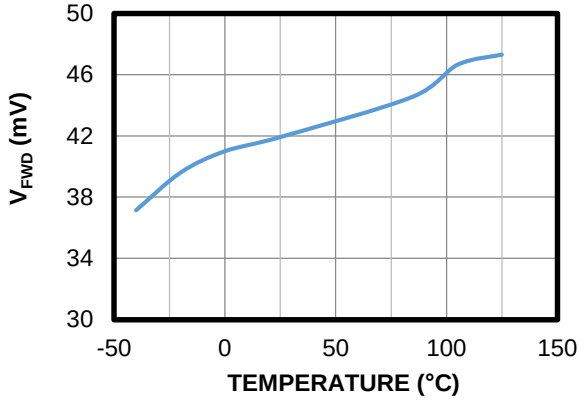


Turn-Off Delay vs. Temperature

V_{DD} = 5.4V, C_{LOAD} = 2.2nF



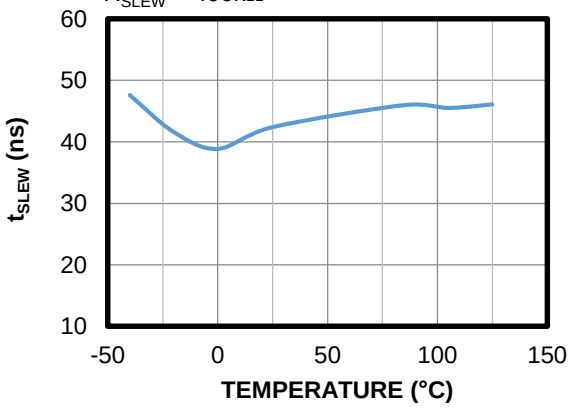
V_{SS} - V_D Forward Regulation Voltage vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

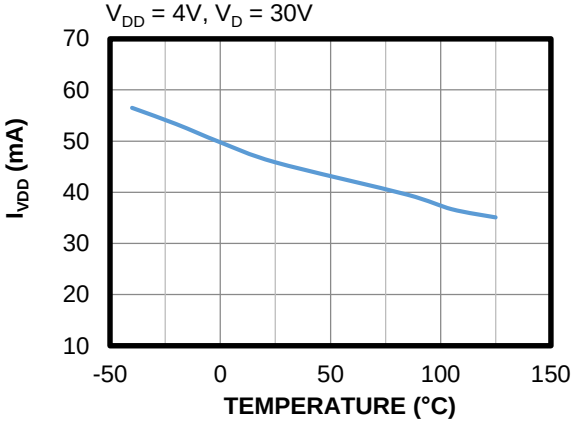
Turn-On Slew Rate Detection Timer vs. Temperature

R_{SLEW} = 400kΩ



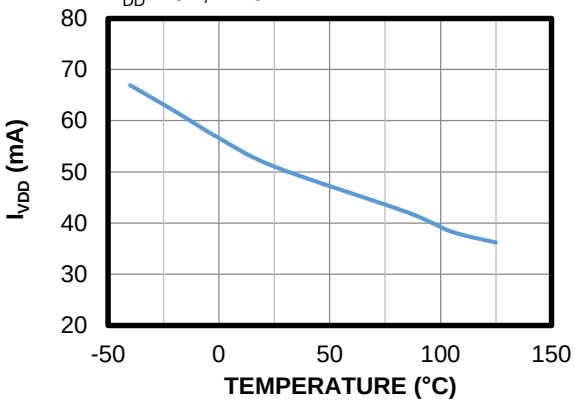
VDD Maximum Charging Current vs. Temperature

V_{DD} = 4V, V_D = 30V



VDD Maximum Charging Current vs. Temperature

V_{DD} = 5V, HVC = 12V

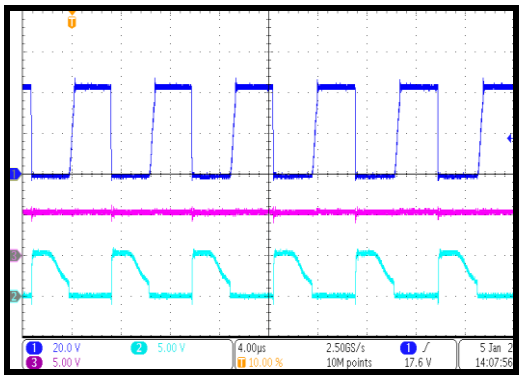


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

65W QR Flyback Application Operation

V_{IN} = 110V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A,
HVC is connected to VD

CH1: V_{DS} 20V/div.
CH3: V_{DD} 5V/div.
CH2: V_{GS} 5V/div.

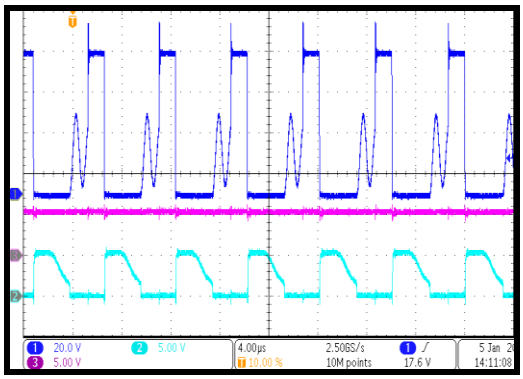


10µs/div.

65W QR Flyback Application Operation

V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A,
HVC connected to VD

CH1: V_{DS} 20V/div.
CH3: V_{DD} 5V/div.
CH2: V_{GS} 5V/div.

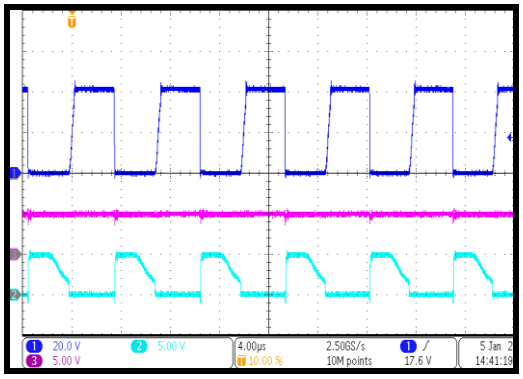


10µs/div.

65W QR Flyback Application Operation

V_{IN} = 110V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A,
HVC connected to VSS

CH1: V_{DS} 20V/div.
CH3: V_{DD} 5V/div.
CH2: V_{GS} 5V/div.

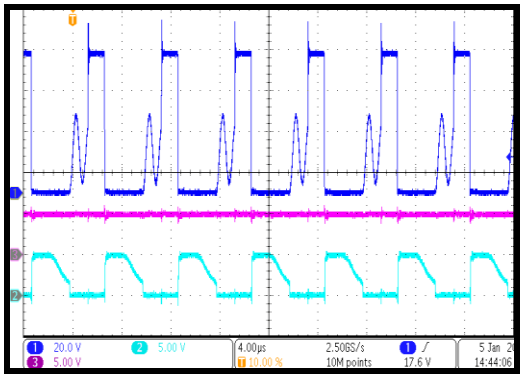


10µs/div.

65W QR Flyback Application Operation

V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A,
HVC connected to VSS

CH1: V_{DS} 20V/div.
CH3: V_{DD} 5V/div.
CH2: V_{GS} 5V/div.



10µs/div.

FUNCTIONAL BLOCK DIAGRAM

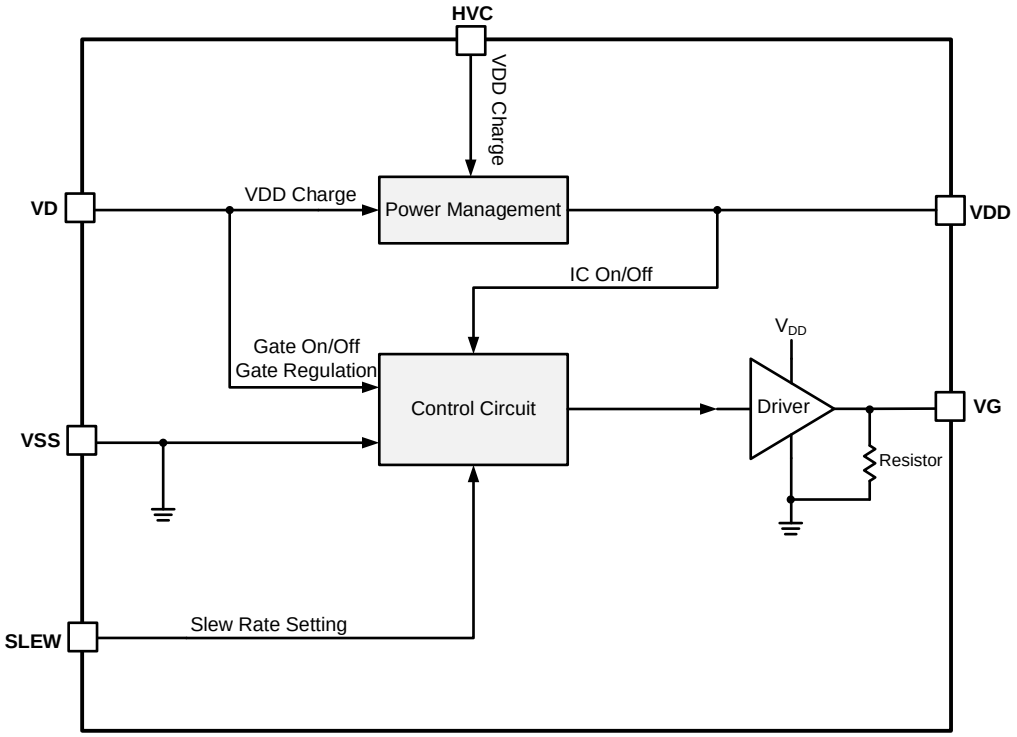


Figure 1: Functional Block Diagram

OPERATION

The MP6982 supports discontinuous conduction mode (DCM), continuous conduction mode (CCM), and quasi-resonant (QR) operation in flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the synchronous rectification (SR) GaN HEMT's current drops to 0A.

VDD Generation

The VDD pin supplies power to the MP6982, and can be charged by both HVC and VD.

If the HVC voltage (V_{HVC}) is below 4.7V, then a 40mA current source from VD charges the VDD voltage (V_{DD}) and regulates it at 5V. If V_{HVC} is between 4.7V and 6.1V, then a 50mA current source from HVC charges V_{DD} and regulates it at (V_{HVC} - 0.7V). If V_{HVC} exceeds 6.1V, then a 50mA current source from HVC charges V_{DD} via and clamps it at 5.4V.

Start-Up and Under-Voltage Lockout (UVLO)

When V_{DD} exceeds the V_{DD} under-voltage lockout (UVLO) rising threshold, the MP6982 exits UVLO and is enabled. Once V_{DD} drops below the V_{DD} UVLO falling threshold, the MP6982 enters sleep mode, and the gate driver voltage (V_{GS}) remains low.

Turn-On Phase

When the drain-to-source voltage (V_{DS}) drops to about 2V, a turn-on timer begins. This turn-on timer can be configured via an external SLEW resistor (R_{SLEW}). If V_{DS} reaches the turn-on threshold (V_{DRV_ON}) from 2V within the slew rate detection time (t_{SLEW}), then the GaN HEMT turns on after a turn-on delay (t_{DELAY_ON}).

If V_{DS} reaches V_{DRV_ON} after the timer ends, then V_{GS} remains off. This turn-on timer prevents the MP6982 from falsely turning on due to ringing from DCM and QR operation.

t_{SLEW} can be calculated with Equation (1):

$$t_{SLEW} = R_{SLEW} \times \frac{40ns}{400k\Omega} \quad (1)$$

Turn-On Blanking

The control circuitry contains a blanking function. When the GaN HEMT turns on, the control circuitry ensures that the on state lasts for a specific time period. The turn-on blanking time (t_{BLANK_ON}) prevents an accidental turn-off due to ringing. However, if V_{DS} reaches the turn-off threshold during the minimum on time (typically 2V), V_{GS} is pulled low immediately.

Conduction Phase

Once V_{DS} exceeds the forward regulation voltage ($-V_{FWD}$) according to the decrease of the switching current, the MP6982 lowers V_{GS} to increase the synchronous GaN HEMT's on resistance. With this control scheme, V_{DS} is adjusted to be approximately equal to $-V_{FWD}$, even when the current through the GaN HEMT is fairly low. This function is especially vital for CCM as it keeps V_{GS} low when the synchronous GaN HEMT turns off, thereby boosting the turn-off speed.

Turn-Off Phase

If V_{DS} rises high enough to trigger the turn-off threshold ($-V_{DRV\_OFF}$), V_{GS} is pulled to 0V after a very short turn-off delay (t_{DELAY_OFF}) (see Figure 2).

Turn-Off Blanking

After V_{GS} is pulled to 0V by V_{DS} reaching $-V_{DRV\_OFF}$, a turn-off blanking time is applied. During this blanking time, the gate driver signal latches off. The turn-off blanking is removed when V_{DS} exceeds the turn-off blanking threshold (V_{BLANK_OFF}) (see Figure 2).

Figure 2 shows the turn-on and turn-off timing diagram.

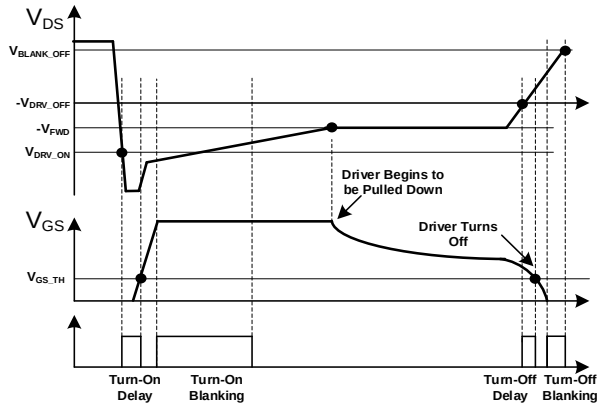


Figure 2: Turn-On/Turn-Off Timing Diagram

APPLICATION INFORMATION

Slew Rate Detection

During DCM, the demagnetizing ringing may bring V_{DS} below 0V. If V_{DS} reaches V_{DRV_ON} during the ringing period, an SR controller without slew rate detection may turn on the GaN HEMT by mistake. This not only increases power loss, but may also lead to shoot-through if the primary-side GaN HEMT turns on within the minimum on time.

Figure 3 shows a false turn-on without slew rate detection.

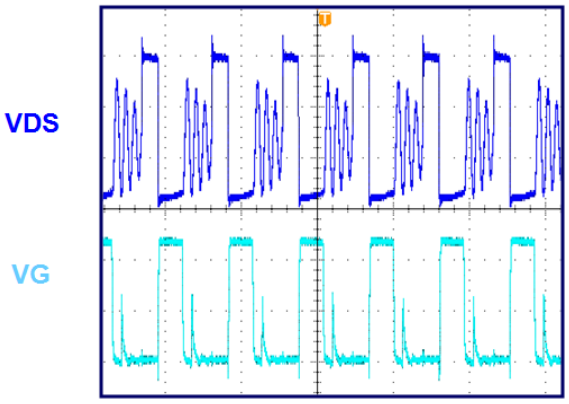


Figure 3: False Turn-On without Slew Rate Detection

The ringing slew rate is always significantly lower than it is when the primary GaN HEMT is completely turned off. A false turn-on can be prevented using slew rate detection (see Figure 4).

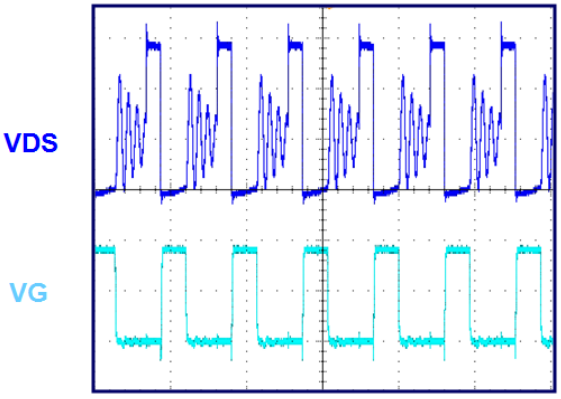


Figure 4: Preventing a False Turn-On with Slew Rate Detection

When the slew rate is below the threshold set by R_{SLEW}, the IC does not turn on the gate even when V_{DS} reaches V_{DRV_ON} (see the Turn-On Phase section on page 9).

Selecting the External Resistor on VD and HVC

Over-voltage (OV) conditions can damage the device; therefore, the application design must guarantee safe operation, especially on the high-voltage pin.

One common OV condition occurs when the SR GaN HEMT turns on. In this scenario, the VD pin's voltage drop may exceed the negative rating.

It is recommended to place an external resistor between VD and the GaN HEMT drain. The resistance is typically recommended to be ≥300Ω. This value varies on a case-by-case basis. Note that a higher-value resistor may compromise the VDD supply and slow down the slew rate for V_{DS} detection.

It is not typically recommended to use a >1kΩ resistance. Choose an appropriate resistance based on the VDD supply and slew rate conditions.

In applications where HVC may experience a negative voltage bias (e.g. in high-side [HS] applications without auxiliary winding), the same resistance as VD should be placed on HVC externally. If a block diode is used, the reverse recovery time should be below 250ns.

Typical System Implementations

Figure 5 shows the typical system IC implementation for low-side (LS) rectification.

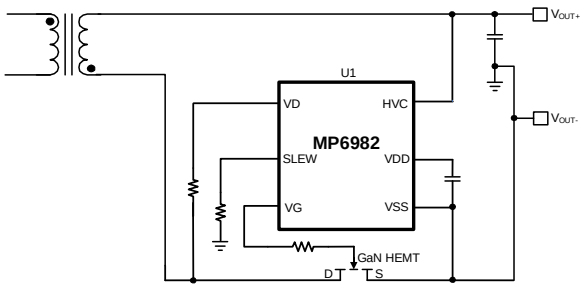


Figure 5: Low-Side Rectification

The MP6982 can support most LS rectification applications with V_{OUT} down to 0V.

If used for HS rectification, there are three ways to achieve a system without an auxiliary winding requirement (see Figure 6, Figure 7, and figure 8 on page 11).

Figure 6 shows a typical system IC implementation for HS rectification, where HVC is connected to VD. V_{DD} is generated regulated at 5.4V.

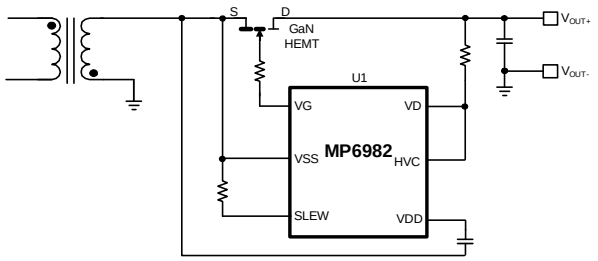


Figure 6: High-Side Rectification (V_{DD} Is Regulated at 5.4V)

Figure 7 shows a typical system IC implementation for HS rectification, where HVC is connected to the secondary ground via an external diode. V_{DD} is generated from HVC and regulated at 5.4V.

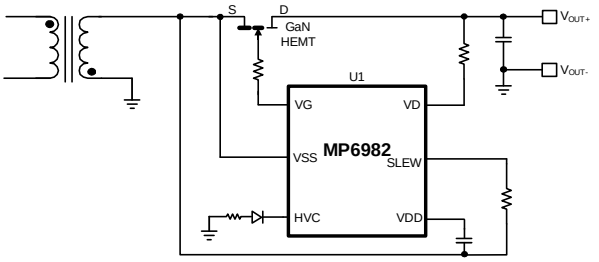


Figure 7: High-Side Rectification (V_{DD} Is Regulated at 5.4V)

The maximum V_{HVC} (V_{HVC_MAX}) can be calculated with Equation (2):

$$V_{HVC\_MAX} = V_{IN} \times \frac{N_s}{N_p} \quad (2)$$

Figure 8 shows a typical system IC implementation for HS rectification, where HVC is shorted to VSS. V_{DD} is generated by V_{DS} and regulated at 5V.

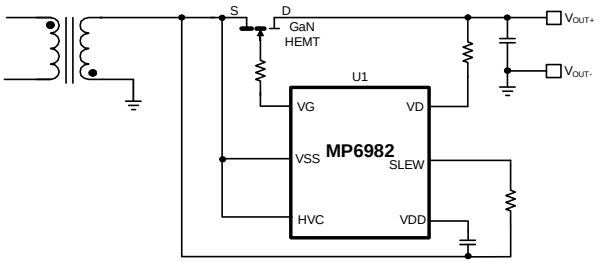


Figure 8: High-Side Rectification (V_{DD} Is Regulated at 5V)

Selecting the Synchronous Rectification (SR) GaN HEMT

Choosing the SR GaN HEMT is a trade-off between the on resistance ($R_{DS(ON)}$) and the cost. For high efficiency, it is recommended to choose a GaN HEMT with a lower $R_{DS(ON)}$. However, a GaN HEMT with a lower on resistance typically has a higher cost.

V_{DS} is adjusted to be approximately $-V_{FWD}$ during the driving period while the switching current is fairly small. Since the gate driver is pulled low when V_{DS} (equal to $-I_{SD}$ x $R_{DS(ON)}$) exceeds -40mV, a GaN HEMT with too low an $R_{DS(ON)}$ is not recommended. The GaN HEMT's $R_{DS(ON)}$ does not contribute to conduction loss. The conduction loss (P_{CON}) can be calculated with Equation (3)

$$P_{CON} = -V_{DS} \times I_{SD} \approx I_{SD} \times 40mV \quad (3)$$

To achieve fairly high use of the GaN HEMT, it should be turned on completely for at least 50% of the SR conduction period. V_{DS} can be calculated with Equation (4):

$$V_{DS} = -I_C \times R_{DS(ON)} = -I_{OUT} / D \times R_{DS(ON)} \leq -V_{FWD} \quad (4)$$

Where V_{DS} is the GaN HEMT's drain-to-source voltage, D is the secondary-side duty cycle, I_{OUT} is the output current, and V_{FWD} is the forward regulation voltage (about 40mV).

Figure 9 shows a typical SR flyback application. At 50% duty cycle, the GaN HEMT's $R_{DS(ON)}$ should exceed (20 / I_{OUT}) (in mΩ). For a 5A application, the $R_{DS(ON)}$ should be ≥4mΩ.

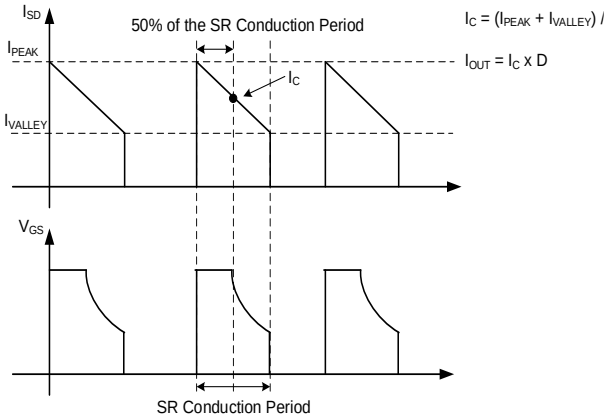


Figure 9: Synchronous Rectification Flyback Application

Layout Example

Figure 10 shows a layout example for an HS application of a flyback power supply, which is a single layer with a through-hole transformer and a SR GaN HEMT in an FCLGA package. The SR GaN HEMT's RC snubber network is comprised of R_{SN} and C_{SN}. The sensing loop (VD and VSS to the SR GaN HEMT) is optimized and kept separate from the power loop. The VDD decoupling capacitor (C2) is placed beside VDD.

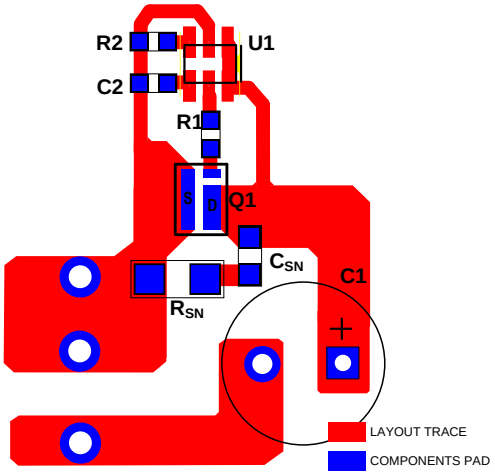


Figure 10: Layout Example in a Flyback High-Side Application

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 10 and Figure 11, and follow the guidelines below:

Sensing for VD/VSS

1. Place the sensing connection (VD/VSS) as close to the GaN HEMT's drain and source as possible. Keep the sensing loop as small as possible.
2. Place the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other (see Figure 10).

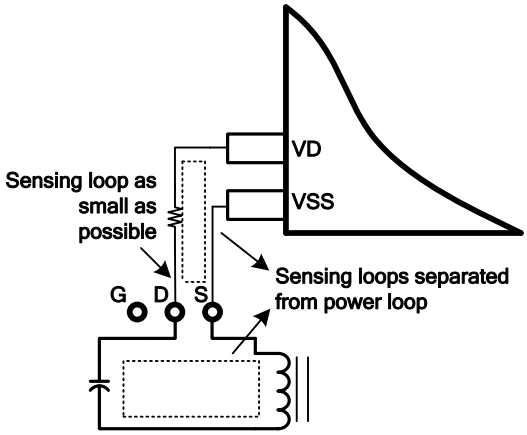


Figure 10: Voltage Sensing for VD/VSS

3. Connect a ceramic decoupling capacitor between VDD and PGND, placed close to the IC for adequate filtering.
4. Keep the gate driver loop as small as possible to reduce parasitic inductance.
5. Keep the driver signal far away from the VD sensing trace.

TYPICAL APPLICATION CIRCUIT

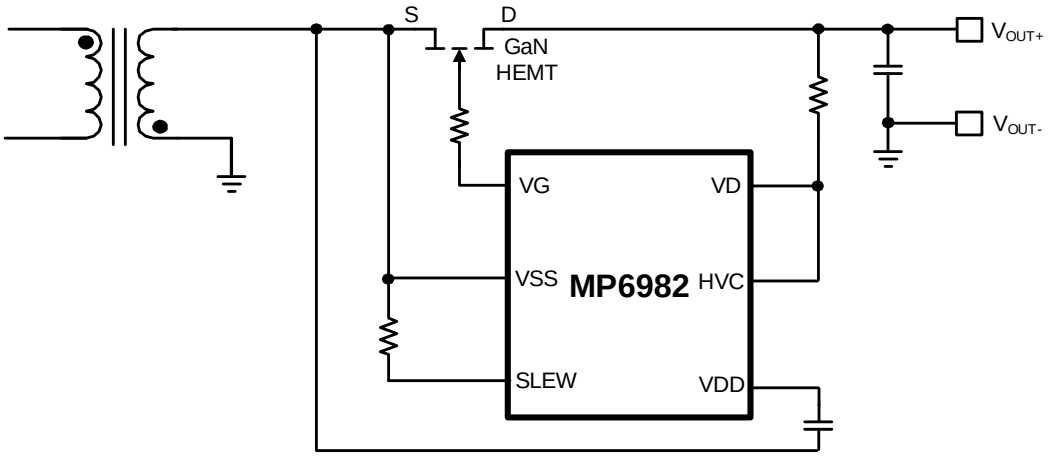
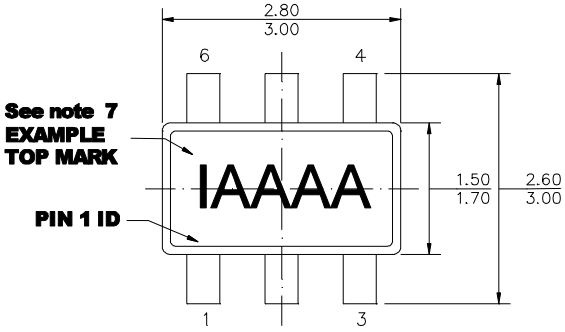


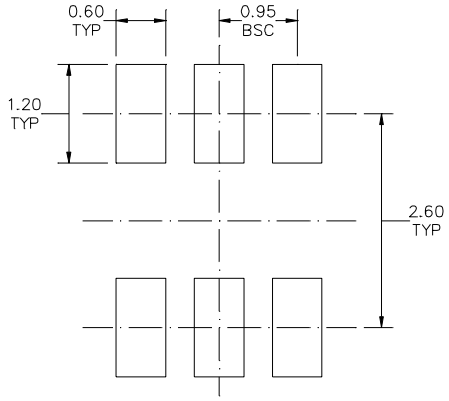
Figure 11: Typical Application Circuit

PACKAGE INFORMATION

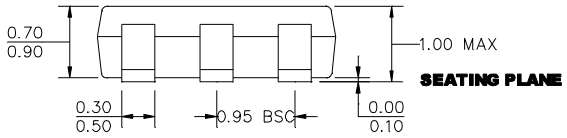
TSOT23-6



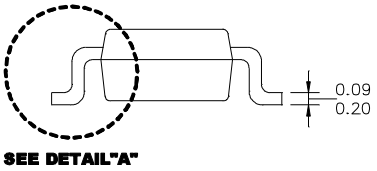
TOP VIEW



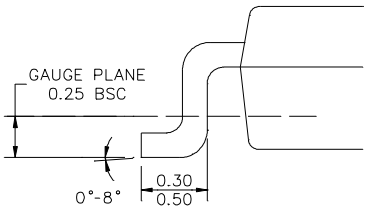
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

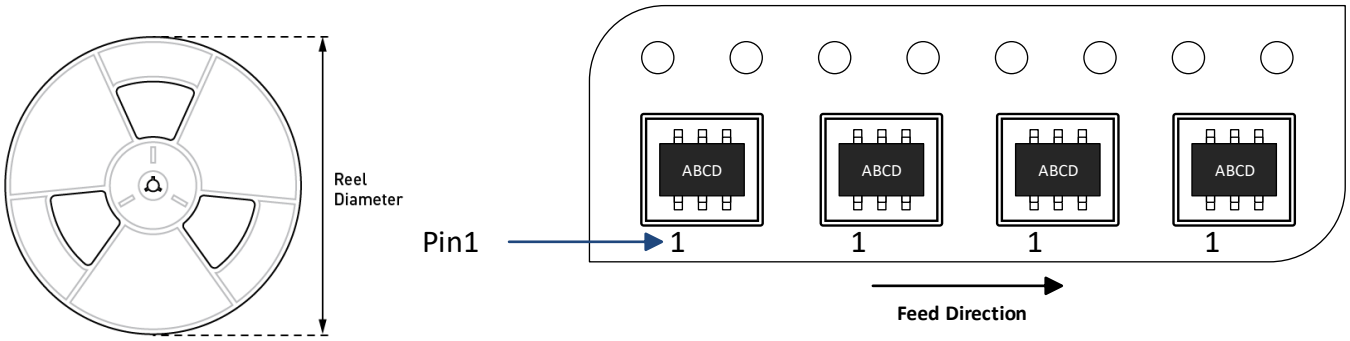


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK).

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6982GJ-Z	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/25/2023	Initial Release	-