MP6908L

Fast Turn-Off Intelligent Rectifier with No Auxiliary Winding Requirement

DESCRIPTION

The MP6908L is a low-drop diode emulator IC. When combined with an external switch, the MP6908L can replace Schottky diodes in high-efficiency flyback converters. The MP6908L regulates the forward drop of an external synchronous rectifier (SR) MOSFET to about 40mV, then switches off once the voltage becomes negative.

The MP6908L can generate its own supply voltage for battery charging applications that can have low output voltage or short-circuit output conditions, as well as high-side SR configuration. Configurable ringing detection circuitry prevents the MP6908L from false turn-off after V_{DS} oscillates in discontinuous conduction mode (DCM), or during quasi-resonant operation.

The MP6908L is available in a space-saving TSOT23-6 package.

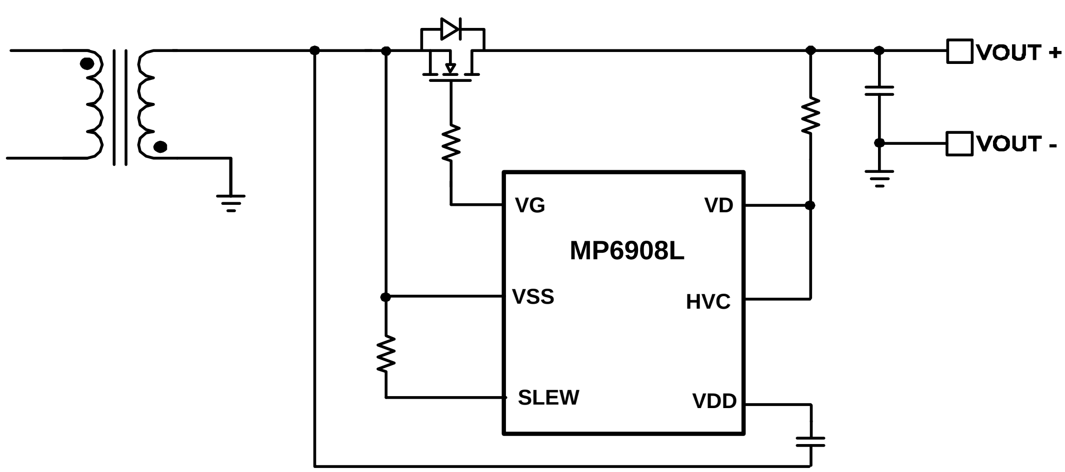
FEATURES

- Wide Output Voltage Range Down to 0V, No Short-Circuit Current Flows through the Body Diode
- Auxiliary Winding for High-Side or Low-Side Rectification is Not Required
- Ringing Detection Prevents False Turn-On in DCM and Quasi-Resonant Operations
- Works with Standard and Logic-Level SR MOSFETs
- Compatible with Energy Star
- 30ns Fast Turn-Off and Turn-On Delay
- 100µA Quiescent Current
- Supports DCM, CCM, and Quasi-Resonant Operation
- Supports Both High-Side and Low-Side Rectification
- Available in a TSOT23-6 Package

APPLICATIONS

- USB PD Quick Chargers
- Adapters
- Flyback Power Supplies with Very Low and/or Variable Output Voltages

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6908LGJ	TSOT23-6	*See Below*	1

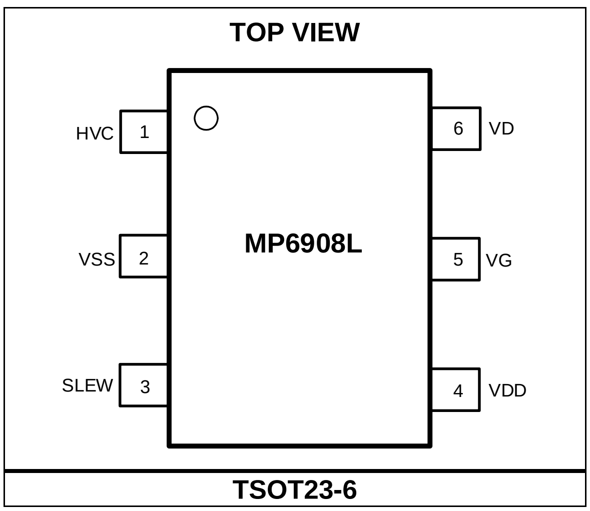
* For Tape & Reel, add suffix –Z (e.g. MP6908LGJ–Z).

TOP MARKING

|BPAY

BPA: Product code of MP6908LGJ
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	HVC	**High-voltage linear regulator input.**
2	VSS	**Ground.** VSS is also used as a MOSFET source sense reference for VD.
3	SLEW	**Configuration for turn-on signal slew rate detection.** The SLEW pin prevents the synchronous rectifier (SR) controller from a false turn-on. A false turn-on can be triggered by ringing below the turn-on threshold at the VD pin in discontinuous conduction mode (DCM) or quasi-resonant mode. Any signal slower than the preset slew rate cannot turn on VG.
4	VDD	**Linear regulator output.** VDD supplies power to the MP6908L.
5	VG	**Gate drive output.**
6	VD	**MOSFET voltage-sense drain.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD, VG to VSS...........................-0.3V to +14V
VD, HVC to VSS............................-1V to +180V
SLEW to VSS ....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
……………………………………………….0.56W
Junction temperature ....150°C
Lead temperature (solder) ....260°C
Storage temperature .... -55°C to +150°C

ESD Ratings

Human body model (HBM):
VD pin ....-2000V/+350V
Other pins .... ±2000V
Charged device model (CDM)…-1000V/+1250V

Recommended Operation Conditions (3)

VDD to VSS.....................................4.5V to 13V
VD, HVC to VSS............................-1V to +150V
Maximum junction temperature (T_J)..........125°C

Thermal Resistance (4) *θJA* *θJC*

TSOT23-6............................220 .....110 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = 5V, T_J = -40°C to +125°C, unless otherwise noted.

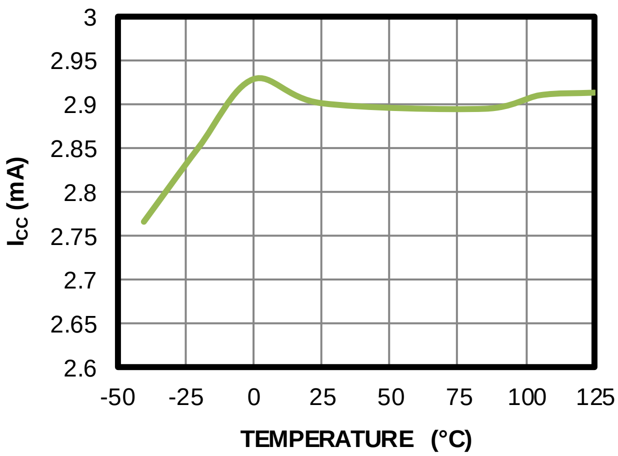
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Management Section						
VDD UVLO rising			4.0	4.2	4.4	V
VDD UVLO hysteresis			0.1	0.2	0.3	V
VDD maximum charging current	I_{VDD}	VDD = 7V, HVC = 40V		70		mA
		VDD = 4V, VD = 30V		40		mA
VDD regulation voltage		VD = 12V, HVC = 12V	8.5	9	9.5	V
		HVC = 3V, VD = 12V	4.6	5	5.4	V
Operating current	I_{CC}	VDD = 9V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz		2.9	3.5	mA
		VDD = 5V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz		1.72	2.1	mA
Quiescent current	$I_{Q(VDD)}$			100	130	µA
Shutdown current	$I_{SD(VDD)}$	VDD = UVLO threshold - 0.1V			100	µA
Control Circuitry Section						
Forward regulation voltage (VSS/VD)	V_{FWD}		25	40	55	mV
Turn-on threshold (V_{DS})			-115	-86	-57	mV
Turn-off threshold (VSS/VD)			-6	3	+12	mV
Turn-on delay	t_{D-ON}	C_{LOAD} = 2.2nF		30	50	ns
Turn-off delay	t_{D-OFF}	C_{LOAD} = 2.2nF		25	45	ns
Turn-off propagation delay (5)				15		ns
Turn-on blanking time	t_{B-ON}	C_{LOAD} = 2.2nF	1.1	1.6	2.1	µs
Turn-off blanking threshold (V_{DS})	V_{B-OFF}		2		3	V
Turn-off threshold during minimum on time (V_{DS})			1.3	1.8	2.1	V
Turn-on slew rate detection timer	t_{SLEW}	R_{SLEW} = 400kΩ	65	90	115	ns
Gate Driver Section						
VG (low)	V_{G-L}	I_{LOAD} = 10mA		0.01	0.02	V
VG (high)	V_{G-H}	I_{LOAD} = 0mA		VDD		V
Maximum source current (5)				0.5		A
Maximum sink current (5)				3		A
Pull-down impedance		Same as VG (low)		1	2	Ω

Note:

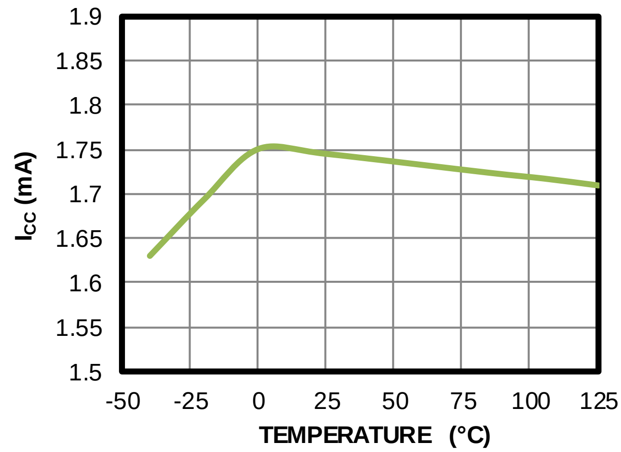
5) Guaranteed by characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

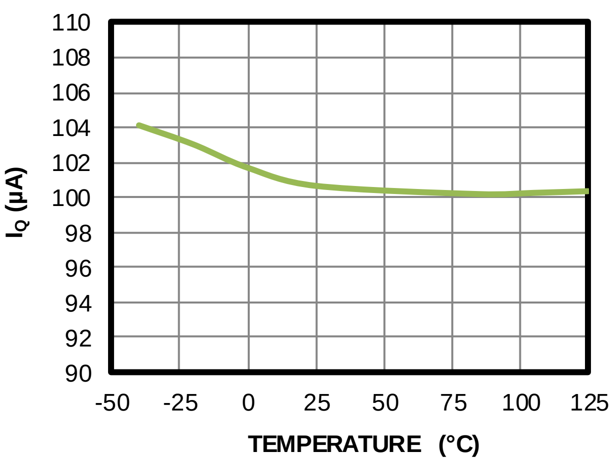
Operating Current vs. Temperature
VDD = 9V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz



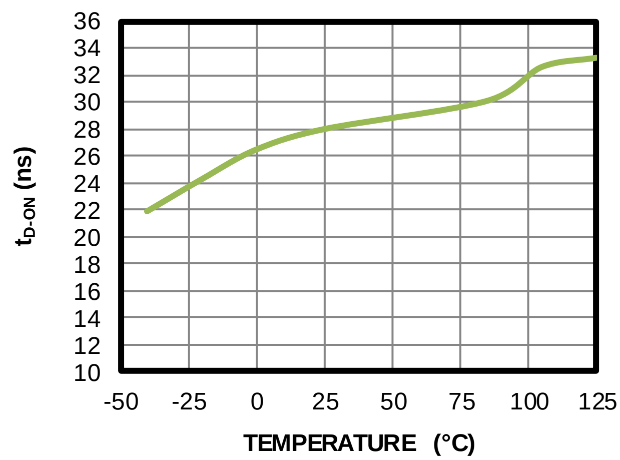
Operating Current vs. Temperature
VDD = 5V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz



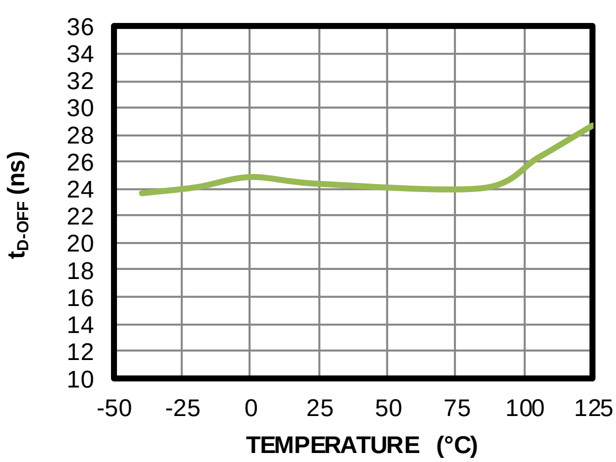
Quiescent Current vs. Temperature
VDD = 5V



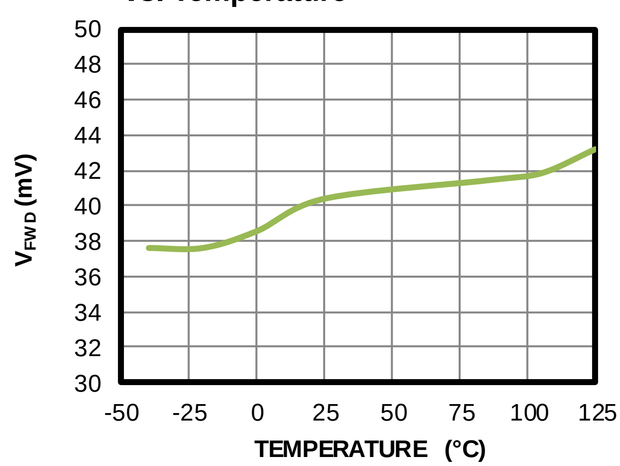
Turn-On Delay vs. Temperature
VDD = 9V, C_{LOAD} = 2.2nF



Turn-Off Delay vs. Temperature
VDD = 9V, C_{LOAD} = 2.2nF



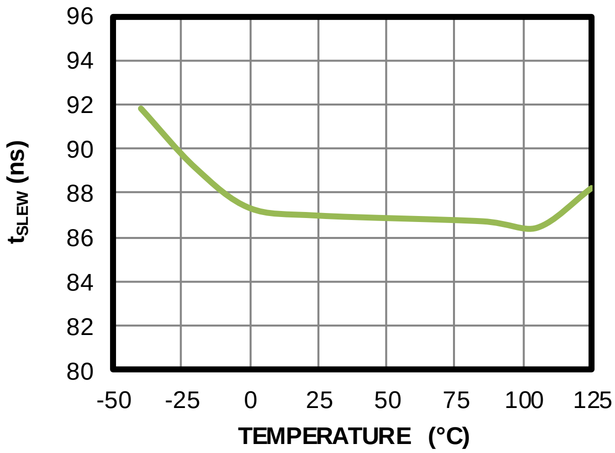
Forward Regulation Voltage (VSS - VD) vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

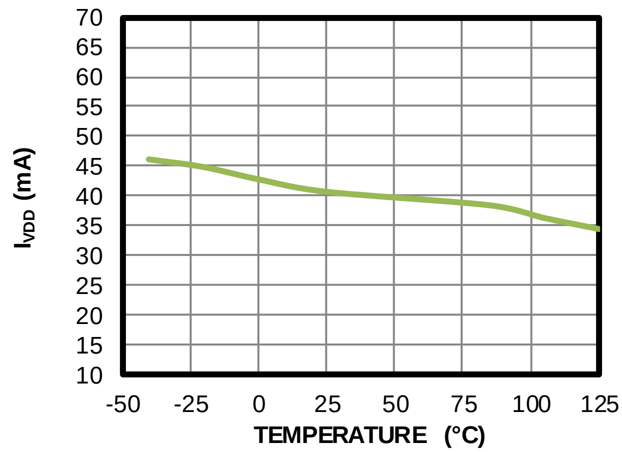
Turn-On Slew Rate Detection Timer vs. Temperature

R_{SLEW} = 400kΩ



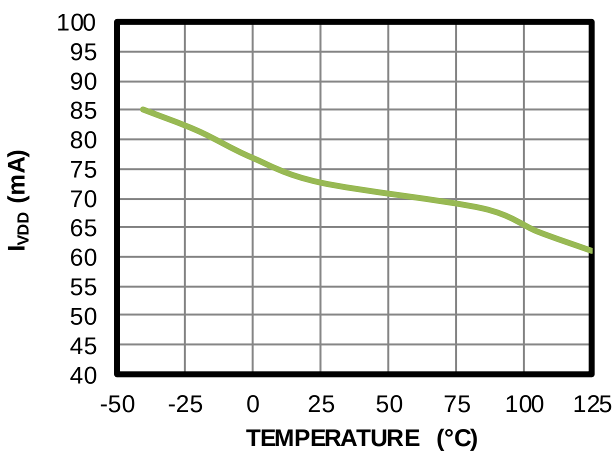
VDD Maximum Charging Current vs. Temperature

VDD = 4V, VD = 30V



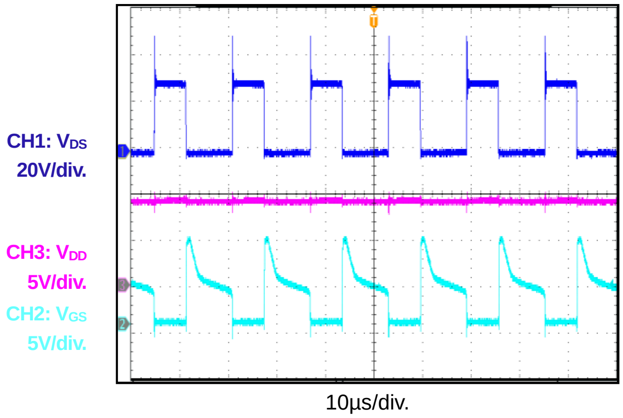
VDD Maximum Charging Current vs. Temperature

VDD = 7V, HVC = 40V

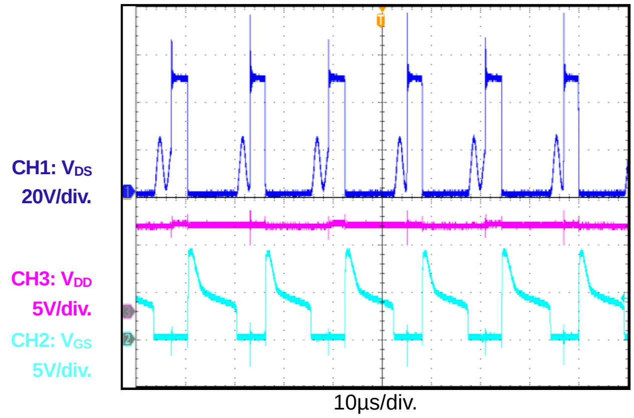


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

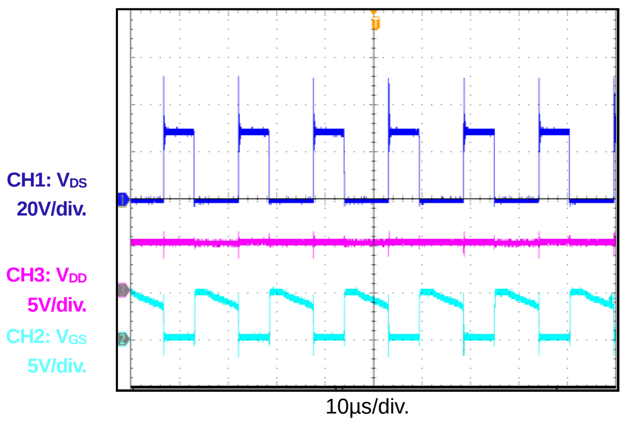
Operation in 36W Flyback Application
V_{IN} = 110V_{AC}, V_{OUT} = 12V, I_{OUT} = 3A, HVC connected to VD



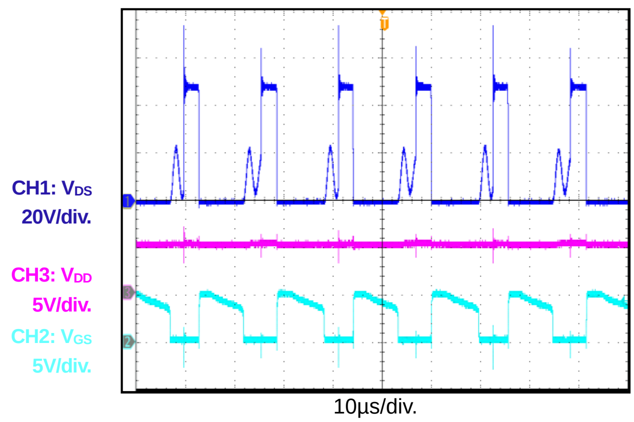
Operation in 36W Flyback Application
V_{IN} = 220V_{AC}, V_{OUT} = 12V, I_{OUT} = 3A, HVC connected to VD



Operation in 36W Flyback Application
V_{IN} = 110V_{AC}, V_{OUT} = 12V, I_{OUT} = 3A HVC connected to VSS



Operation in 36W Flyback Application
V_{IN} = 220V_{AC}, V_{OUT} = 12V, I_{OUT} = 3A HVC connected to VSS



FUNCTIONAL BLOCK DIAGRAM

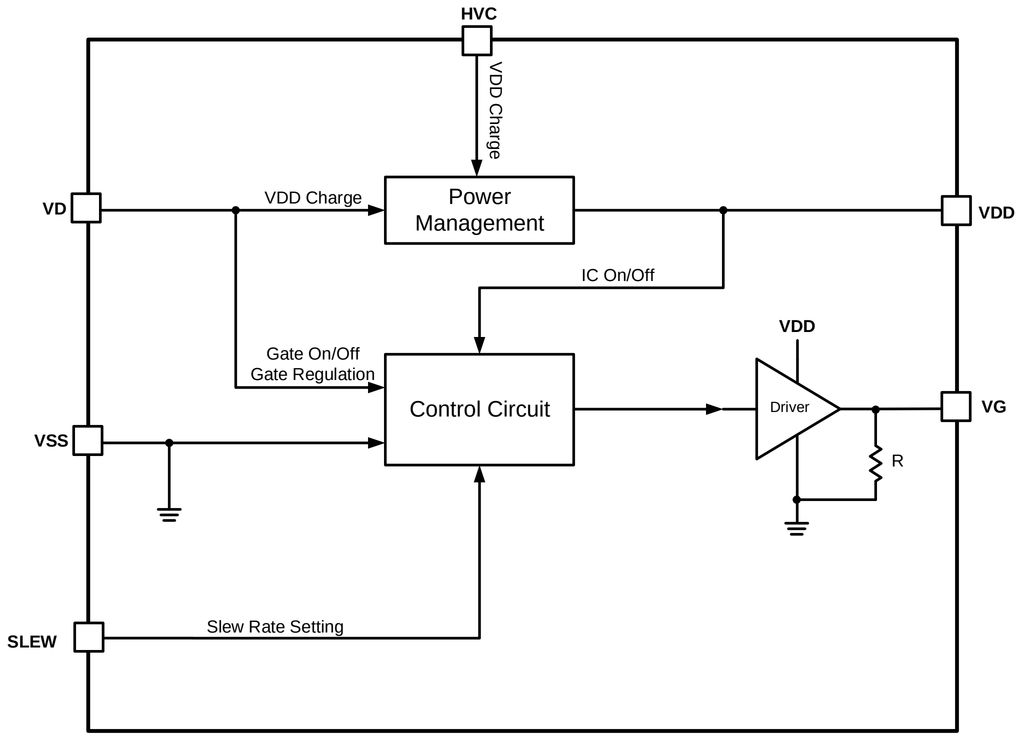


Figure 1: Functional Block Diagram

OPERATION

The MP6908L supports discontinuous conduction mode (DCM), continuous conduction mode (CCM), and quasi-resonant mode in flyback converters. The control circuitry controls the gate in forward mode, and turns the gate off when the synchronous rectifier (SR) MOSFET current drops to 0A.

VDD Generation

The capacitor at the VDD pin supplies power to the IC. It can be charged up by either HVC or VD.

When the HVC voltage (V_{HVC}) is below 4.7V, VD charges the external VDD capacitor via a 40mA current source, and regulates VDD to 5V.

When 4.7V < V_{HVC} < 9.7V, VD stops charging VDD. The HVC pin charges VDD via a 70mA current source, and regulates VDD at V_{HVC} - 0.7V. When V_{HVC} > 9.7V, HVC charges VDD via a 70mA current source, and clamps VDD at 9V.

The VDD voltage may be below the under-voltage lockout (UVLO) threshold if VDD is charged through HVC while V_{HVC} rises to 4.7V. This means that the output voltage cannot be below 5V when HVC is connected to the output in a low-side SR configuration (see the Typical System Implementations section on page 11 for more details).

Start-Up and Under-Voltage Lockout (UVLO)

When VDD exceeds 4.2V, the MP6908L passes the under-voltage lockout (UVLO) threshold and the device is enabled. If VDD drops below 4V, the MP6908L enters sleep mode, and V_{GS} remains low.

Turn-On Phase

When V_{DS} drops to about 2V, a turn-on timer begins counting. This turn-on timer can be configured by an external resistor connected to the SLEW pin. If V_{DS} reaches the -86mV turn-on threshold from its original 2V within the time (t_{SLEW}) set by the timer, the MOSFET turns on after a turn-on delay (t_{D-ON}, typically 30ns) (see Figure 2). If V_{DS} reaches -86mV after the timer ends, the gate voltage (V_G) remains off. This turn-on timer prevents the MP6908L from false turn-on due to ringing from DCM or quasi-resonant operations.

t_{SLEW} can be calculated with Equation (1):

$$t_{SLEW} = R_{SLEW} \times \frac{90ns}{400k\Omega} \quad (1)$$

Figure 2 shows the turn-on/turn-off diagram.

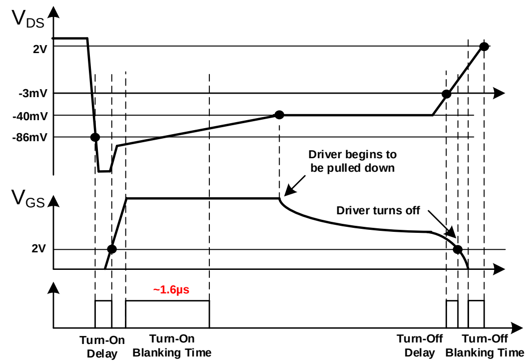


Figure 2: Turn-On/Turn-Off Timing Diagram

Turn-On Blanking Time

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on state lasts for a specific period of time. The turn-on blanking time (t_{B-ON}, typically 1.6μs) prevents the device from accidentally turning off due to ringing. However, if V_{DS} rises to between 2V and 3V within the turn-on blanking time, V_{GS} is pulled low immediately.

Conduction Phase

When V_{DS} exceeds the forward voltage drop (V_{FWD}, typically -40mV) according to the decreasing switching current, the MP6908L lowers the gate voltage level to raise the synchronous MOSFET's on resistance.

With this control scheme, V_{DS} is adjusted to be about -40mV even when the current through the MOSFET is fairly low. This function keeps the driver voltage at a very low level when the synchronous MOSFET is turned off, which boosts the turn-off speed and is especially important in CCM.

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold (typically -3mV), the gate voltage is pulled to 0V after a very short turn-off delay (t_{D-OFF}, typically 25ns) (see Figure 2).

Turn-Off Blanking Time

Once the gate driver voltage (V_{GS}) is pulled to 0V when V_{DS} reaches the turn-off threshold (typically -3mV), a turn-off blanking time is initiated. During this time, the gate driver signal latches off. The turn-off blanking time completes when V_{DS} exceeds 2V (see Figure 2).

APPLICATION INFORMATION

Slew Rate Detection Function

In DCM, the demagnetizing ringing may force V_{DS} to drop below 0V. If V_{DS} reaches the turn-on threshold during voltage ringing in DCM, an SR controller that does not have the slew rate detection function may turn on the MOSFET by mistake. Figure 3 shows the waveform of this false turn-on. This not only increases power loss, but may also lead to shoot-through if the primary-side FET is turned on within the minimum on time.

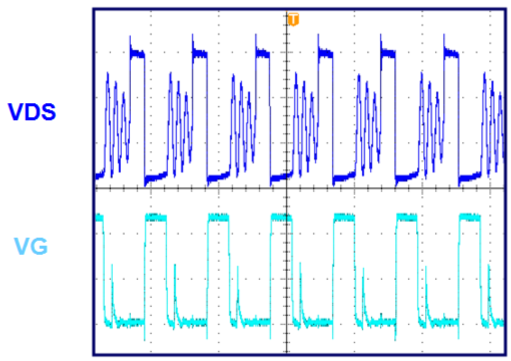


Figure 3: False Turn-On (No Slew Rate Detection)

Note that the ringing slew rate is always much lower when the primary MOSFET is turned off. A false turn-on can be prevented by implementing slew rate detection (see Figure 4). When the slew rate is below the threshold set by R_{SLEW}, the IC does not turn on the gate, even when V_{DS} reaches the turn-on threshold.

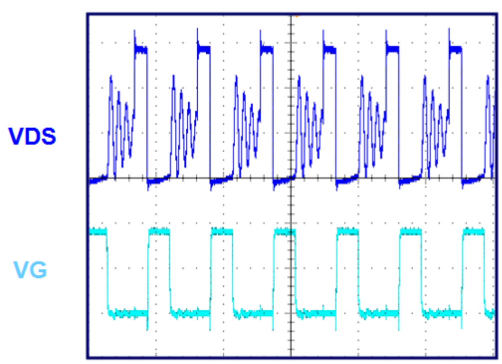


Figure 4: Preventing a False Turn-On with Slew Rate Detection

Selecting an External Resistor on VD and HVC

Over-voltage conditions can damage the device, so the application should be designed to guarantee safe operation, especially on the high-voltage pin.

One common over-voltage condition is triggered when the SR MOSFET's body diode turns on, as the forward voltage drop may exceed the negative rating on the VD pin. In this scenario, it is recommended to place an external resistor between VD and the MOSFET drain. Generally, the recommended resistance is 300Ω or greater.

However, this resistor cannot be too large, because a higher-value resistor can compromise the VDD supply and slow down the slew rate on V_{DS} detection. It is not recommended to use a resistor greater than 1kΩ. The resistor value should be determined based on the conditions of the VDD supply and slew rate.

In applications where HVC may also suffer from a negative voltage bias (e.g. in a high-side set-up without auxiliary winding), an external resistor between 300Ω and 1kΩ should be connected to HVC.

Typical System Implementations

Figure 5 shows the typical system implementation when the IC's power supply is derived from the output voltage (V_{OUT}). This function is available in low-side rectification.

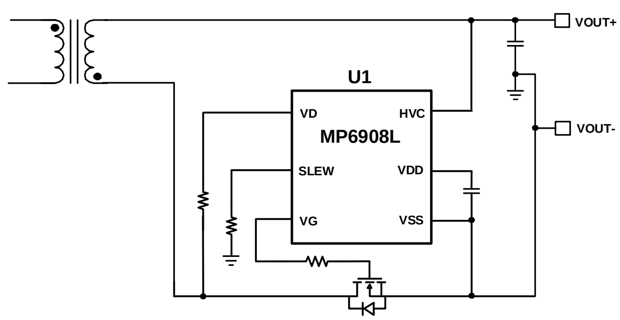


Figure 5: Low-Side Rectification

If the MP6908L is used for high-side rectification, a self-supplying system can be achieved through three methods, described below:

<u>Method 1</u>: Figure 6 shows how to implement high-side rectification when HVC is connected to VD. In this scenario, VDD is generated from HVC, then regulated at 9V.

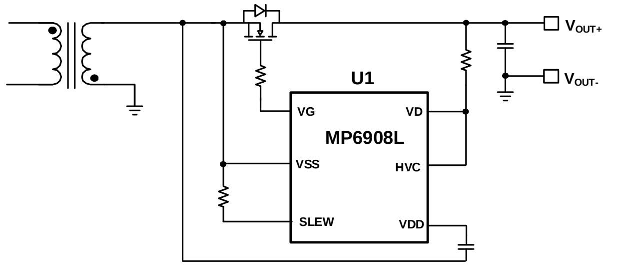


Figure 6: High-Side Rectification when HVC is Connected to VD (VDD Regulated at 9V)

Method 2: Figure 7 shows when HVC connected to the secondary ground through an external diode. In this scenario, VDD is generated from HVC, and regulated at 9V.

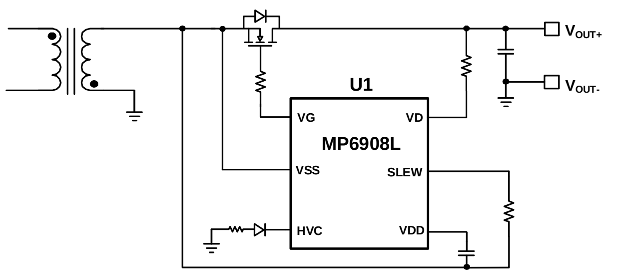


Figure 7: High-Side Rectification when HVC is Connected to a Secondary Ground (VDD Regulated at 9V)

The maximum voltage at HVC can be calculated with Equation (2):

$$V_{HVC(MAX)} = V_{IN} \times \frac{N_S}{N_P} \quad (2)$$

Method 3: Similar to method 2, HVC works when V_{HVC} is below 4.7V, since HVC is shorted to VSS (see Figure 7). In this scenario, VDD is generated by V_{DS}, and regulated at 5V.

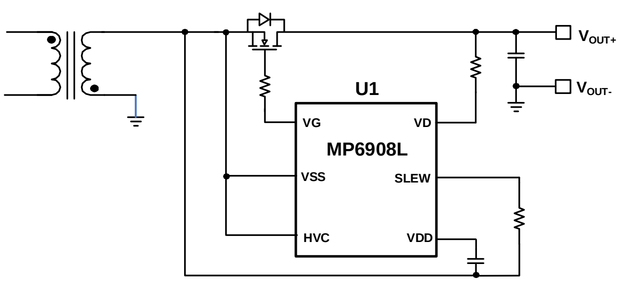


Figure 7: High-Side Rectification (VDD Regulated at 5V)

Selecting the SR MOSFET

Power MOSFET selection is a tradeoff between the on resistance ($R_{DS(ON)}$) and charge gate (Q_G). To achieve higher efficiency, it is recommended to choose a MOSFET with a smaller $R_{DS(ON)}$. Typically, Q_G is greater with a smaller $R_{DS(ON)}$, which lowers the turn-on/turn-off speed and leads to greater power and driver loss. Because V_{DS} is adjusted to be about -40mV during the driving period (when the switching current is fairly small), a MOSFET with a low $R_{DS(ON)}$ is not recommended because the gate driver is pulled low when $V_{DS} = -I_{SD} \times R_{DS(ON)}$ exceeds -40mV. The MOSFET's $R_{DS(ON)}$ does not contribute to the conduction loss. The conduction loss is determined by $P_{CON} = -V_{DS} \times I_{SD}$, which is about $I_{SD} \times 40mV$.

To obtain the best efficiency from the MOSFET's $R_{DS(ON)}$, the MOSFET should be fully turned on for at least 50% of the SR conduction period. Calculate V_{DS} with Equation (3):

$$V_{DS} = -I_C \times R_{DS(ON)} = -I_{OUT} / D \times R_{DS(ON)} \leq -V_{FWD} \quad (3)$$

Where V_{DS} is drain-source voltage of the MOSFET, D is the duty cycle of the secondary side, I_{OUT} is output current, and V_{FWD} is the forward voltage threshold (about 40mV).

Figure 8 shows the typical waveform of a flyback application. Assume this application has a 50% duty cycle. The MOSFET's $R_{DS(ON)}$ should not be below 20 / I_{OUT} (mΩ). For example, for a 5A application, $R_{DS(ON)}$ should not be below 4mΩ.

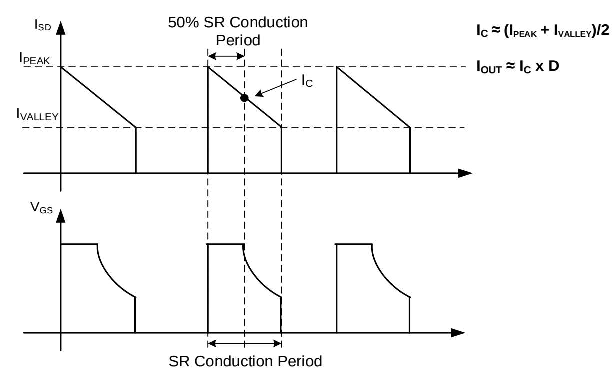


Figure 8: Typical Waveforms with Synchronous Rectification in a Flyback Application

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 9, Figure 10, and Figure 11, and follow the guidelines below:

Sensing for VD/VSS

1. Place the sensing connection (VD/VSS) as close as possible to the MOSFET (drain/source).
2. Keep the sensing loop as small as possible.
3. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other (see Figure 9).

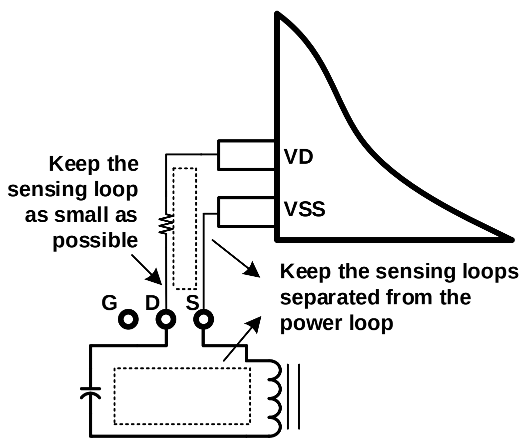


Figure 9: Voltage Sensing for VD/VSS

4. Place a decoupling ceramic capacitor between VDD to PGND, and ensure that it is close to the IC for adequate filtering.

Gate Driver Loop

1. Keep the gate driver loop as small as possible to minimize parasitic inductance.
2. Route the driver signal far away from the VD sensing trace on the PCB.

Layout Examples

Figure 10 shows a layout example of a 1-layer PCB with a through-hole transformer and an SR MOSFET in a TO220 package. R_{SN} and C_{SN} are the RC snubber network for the SR MOSFET. The sensing loop (VD and VSS to the SR MOSFET) is minimized and kept separate from the power loop. The VDD decoupling capacitor (C2) is placed beside VDD.

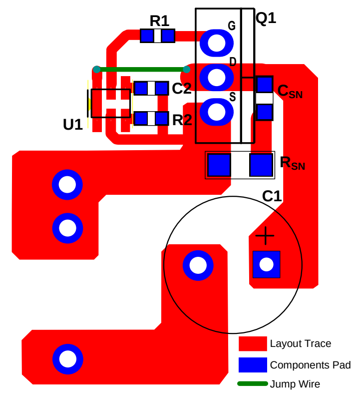


Figure 10: Layout Example with an SR MOSFET in a TO220 Package

Figure 11 shows a layout example of a 1-layer PCB with an SR MOSFET in a PowerPAK/SO8 package, which also has a minimized sensing loop and power loop. This prevents the loops from interfering with each other.

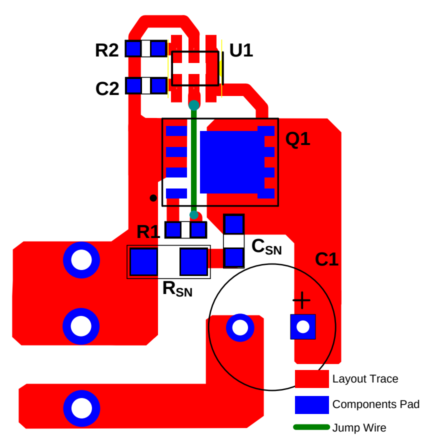
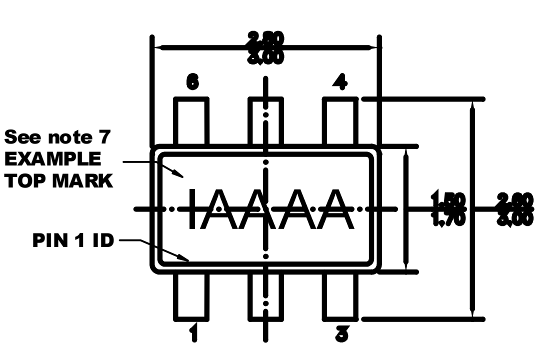


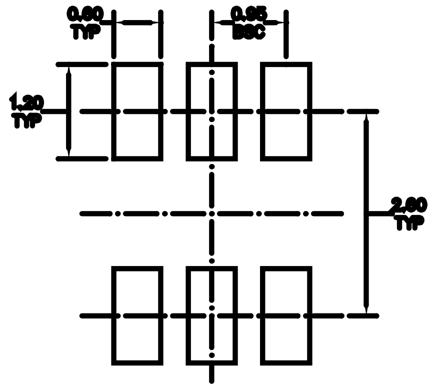
Figure 11: Layout Example with an SR MOSFET in a PowerPAK/SO8 Package

PACKAGE INFORMATION

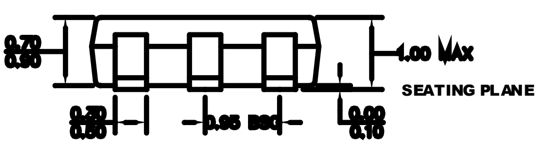
TSOT23-6



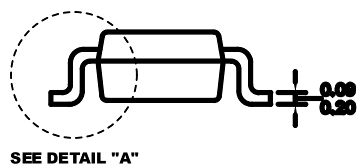
TOP VIEW



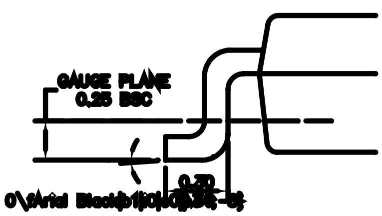
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

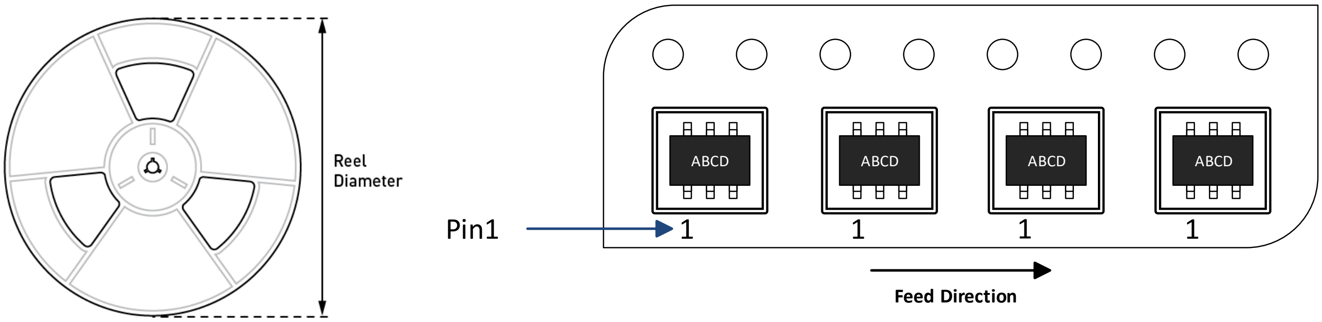


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT (SEE EXAMPLE TOP MARK).

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6908LGJ–Z	TSOT23-6	3000	N/A	7in	8mm	4mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	10/28/2020	Initial Release	-