MP6631B

35V, 3A Peak Phase Current, Three-Phase BLDC Motor Driver

DESCRIPTION

The MP6631B is a three-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs. The device supports a single external Hall-effect sensor or triple external Hall-effect sensors, with up to 3A of peak phase current and a 3.6V to 35V input voltage (V_{IN}) range. The device features a short soft start (SS) configuration for small size motors.

The MP6631B controls the motor speed through the pulse-width modulation (PWM) signal or the DC signal on the PWM/DC pin. It provides closed-loop and open-loop speed control and a built-in configurable speed curve function. It also features a sinusoidal drive for maximum torque, as well as low speed ripple and noise across the full speed range.

The MP6631B features rotational speed detection. The rotational speed detector is an open-drain output via the FG/RD pin. It outputs a high or low voltage relative to the Hall comparator's output. The motor direction is controlled via the DIR pin.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown.

The MP6631B is available in a QFN-26 (3mmx4mm) package.

FEATURES

- 3.6V to 35V Operating Input Voltage (V_{IN}) Range
- Up to 3A of Peak Phase Current
- Integrated 160mΩ High-Side MOSFETs (HS-FETs) and Low-Side MOSFETs (LS-FETs)
- Sinusoidal Drive
- Supports 0V to 1.2V DC Input or 1kHz to 100kHz Pulse-Width Modulation (PWM) Input
- Supports Triple-Hall or Single-Hall Element Differential Input
- Closed-/Open-Loop Speed Control
- Direction/Brake Input
- Power-Save Mode (PSM)
- 0.5s/4.5s Lock Protection
- Over-Current Protection (OCP)
- Single-Pulse or Triple-Pulse FG Output per Electrical Cycle
- Rotational Speed Indication via the FG/RD Pin
- Soft Start (SS) for Low Noise and Current Overshoot
- Available in a QFN-26 (3mmx4mm) Package

APPLICATIONS

- Fans
- General Three-Phase Brushless DC (BLDC) Motors
- Pumps

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TYPICAL APPLICATION

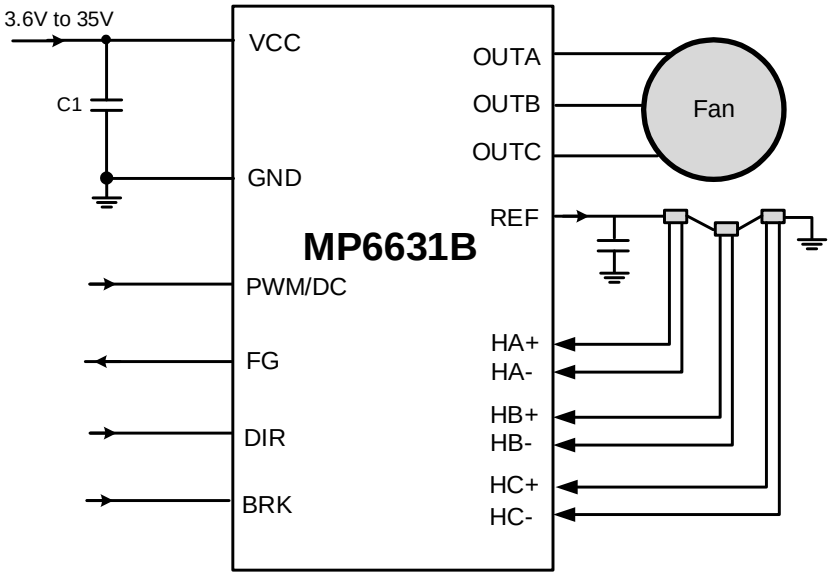

Figure 1: Triple Hall-Effect Sensor Application

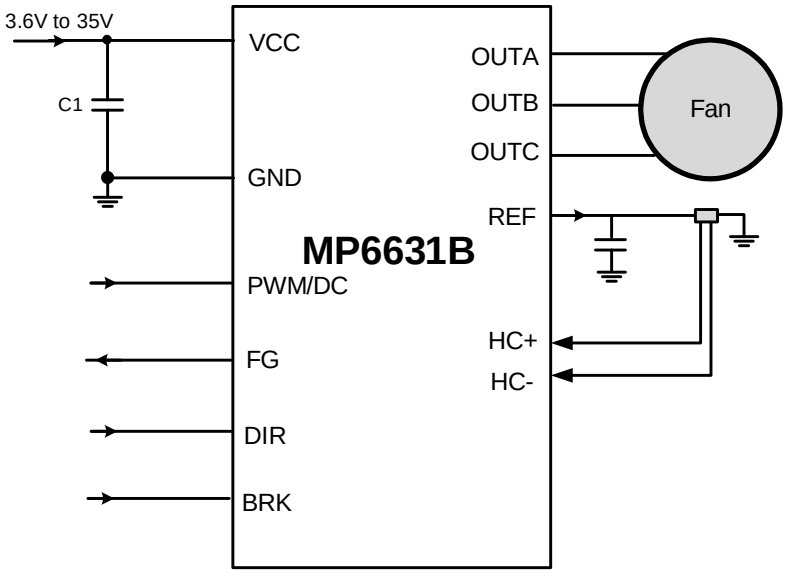

Figure 2: Single Hall-Effect Sensor Application

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Level
MP6631BGL-xxxx**	QFN-26 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6631BGL-xxxx-Z).

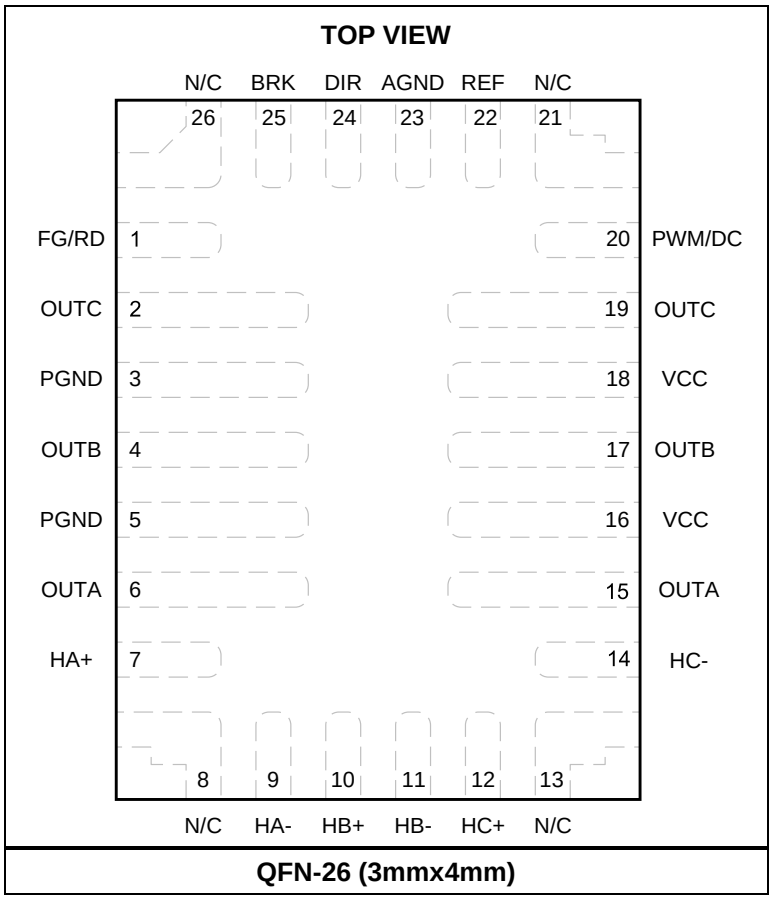
** “xxxx” is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for non-default function options. The default code is “0000”.

TOP MARKING

MPYW
6631
BLLL

MP: MPS prefix
Y: Year code
W: Week code
6631B: Part number
LLL: Lot number

PACKAGE REFERENCE



QFN-26 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	FG/RD	**Speed or rotor lock indication.** The FG/DR pin is an open-drain output that is pulled up externally. FG/RD can be used for speed indication (FG) or rotor lock indication (RD).
2, 19	OUTC	**Phase C terminal.**
3, 5	PGND	**Power ground.**
4, 17	OUTB	**Phase B terminal.**
6, 15	OUTA	**Phase A terminal.**
7	HA+	**Phase A positive Hall input terminal.**
9	HA-	**Phase A negative Hall input terminal.**
10	HB+	**Phase B positive Hall input terminal.**
11	HB-	**Phase B negative Hall input terminal.**
12	HC+	**Phase C positive Hall input terminal.**
14	HC-	**Phase C negative Hall input terminal.**
16, 18	VCC	**Input supply voltage.** The VCC pin must be bypassed locally.
20	PWM/DC	**Rotational speed control input pin.** Pull the PWM/DC pin high internally using a 500kΩ resistor. When DC_PWM = 0, apply a 1kHz to 100kHz pulse-width modulation (PWM) signal to the pin for speed control. When DC_PWM = 1, apply a 0V to 1.2V DC voltage to the pin for speed control.
22	REF	**5V LDO output.** The REF pin must be bypassed locally.
23	AGND	**Analog ground.**
24	DIR	**Direction control pin.** Pull this pin low for forward rotation (A → B → C); pull it high for reverse rotation (A → C → B). Pull DIR low internally using a resistor.
25	BRK	**Brake pin.** Pull the BRK pin high to brake the motor. Pull BRK low internally using a resistor.
8, 13, 21, 26	NC	

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{CC}) ..... -0.3V to +38V
OUTA, OUTB, OUTC.....-0.3V to V_{CC} + 0.3V
All other pins..... -0.3V to +5.8V
Lead temperature ..... 260°C
Continuous power dissipation (T_A = 25°C) (2)
.....2.6W
Junction temperature (T_J) ..... 150°C
Storage temperature..... -60°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 2kV

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) ..... 3.6V to 35V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-26 (3mmx4mm) ..... 48 ..... 11 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted. (5)

Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC input supply under-voltage lockout (UVLO) rising threshold	V_{CC_UVLO}		3	3.3	3.5	V
VCC UVLO hysteresis				360		mV
Operating supply current	I_{CC}			6.7		mA
Standby current	$I_{STANDBY}$			130		μA
DIR input high voltage	V_{DIR_H}		1.5			V
DIR input low voltage	V_{DIR_L}				0.4	V
BRK input high voltage	V_{BRK_H}		1.5			V
BRK input low voltage	V_{BRK_L}				0.4	V
Pulse-width modulation (PWM) input high voltage	V_{PWM_H}	DC_PWM = 0	1.5			V
PWM input low voltage	V_{PWM_L}	DC_PWM = 0			0.4	V
PWM pull-up resistance	R_{PWM}	DC_PWM = 0		500		kΩ
DC input high voltage	V_{DC_H}	DC_PWM = 1	1.08	1.2	1.32	V
DC input low voltage	V_{DC_L}	DC_PWM = 1		0		V
REF output voltage	V_{REF}			5.24		V
REF load regulation	I_{REF_LO}	I_{REF} = 30mA		5.2		V
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 100mA		85		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 100mA		75		mΩ
Cycle-by-cycle current limit	I_{OCP}	OCP_SEL = 11, T_J = 25°C	2.7	3		A
Switching frequency	f_{SW}	T_J = 25°C	24.5	25	25.8	kHz
FG output low-level voltage	V_{FG_L}	$I_{FG/RD}$ = 3mA		0.2	0.4	V
Rotor-lock detection time	t_{RD}			0.5		sec
Zero-current detection (ZCD) threshold	I_{ZCD}			5		mA
Hall input low voltage, common mode	V_{HCM_LO}			1		V
Hall input high voltage, common mode	V_{HCM_HI}			4.5		V
Hall input minimum differential voltage	V_{HDM_MIN}	T_J = 25°C	60			mV_{PK-PK}
Thermal shutdown threshold (5)				160		°C
Thermal shutdown hysteresis (5)				25		°C

Note:

5) Guaranteed by design.

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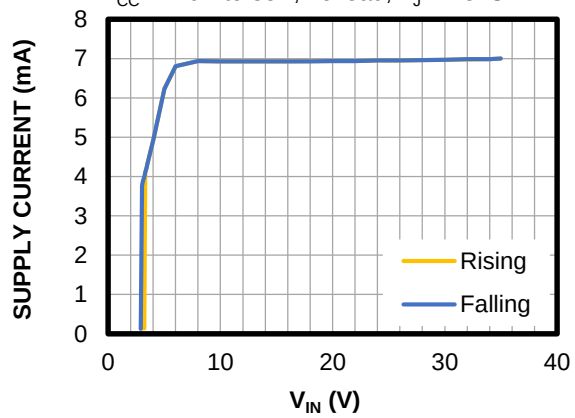
TYPICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

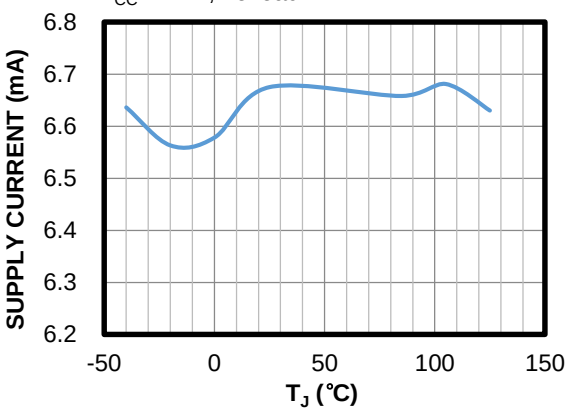
Supply Current vs. Input Voltage

V_{CC} = 2.9V to 35V, no load, T_J = 25°C

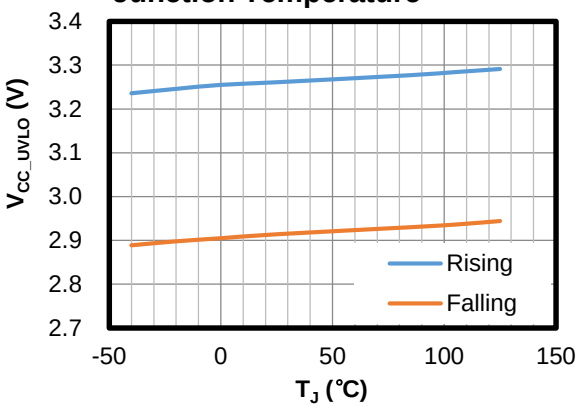


Supply Current vs. Junction Temperature

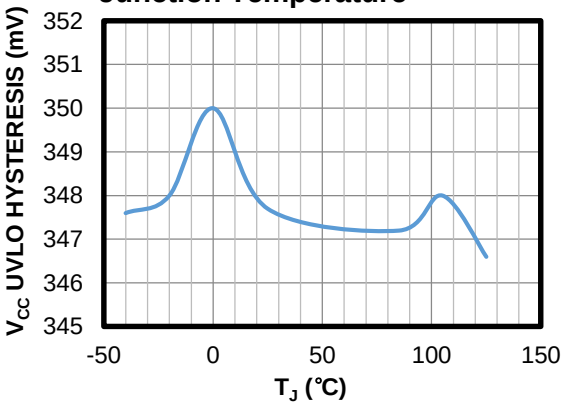
V_{CC} = 12V, no load



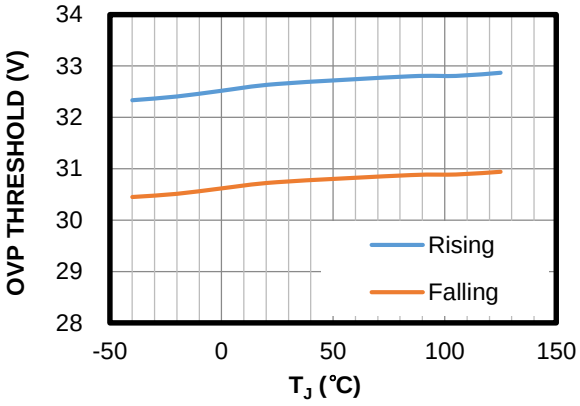
VCC UVLO Threshold vs. Junction Temperature



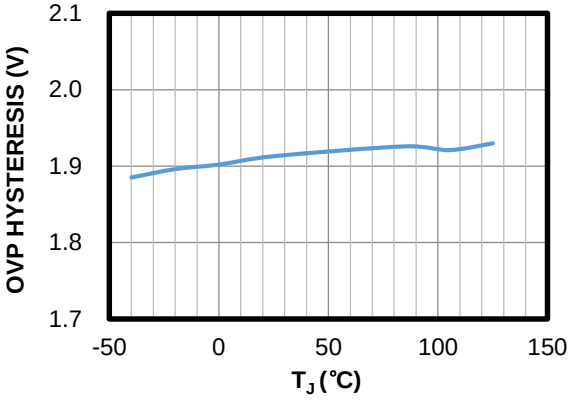
VCC UVLO Hysteresis vs. Junction Temperature



OVP Threshold vs. Junction Temperature



OVP Hysteresis vs. Junction Temperature



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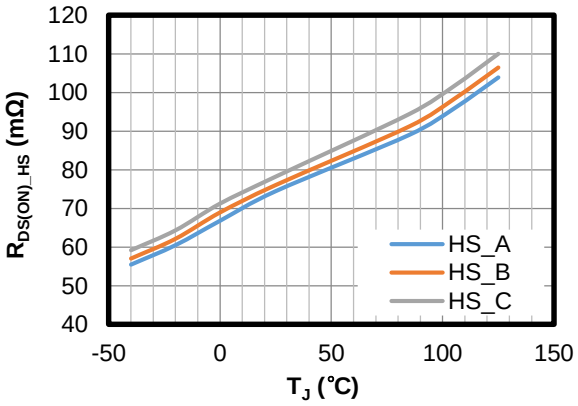
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

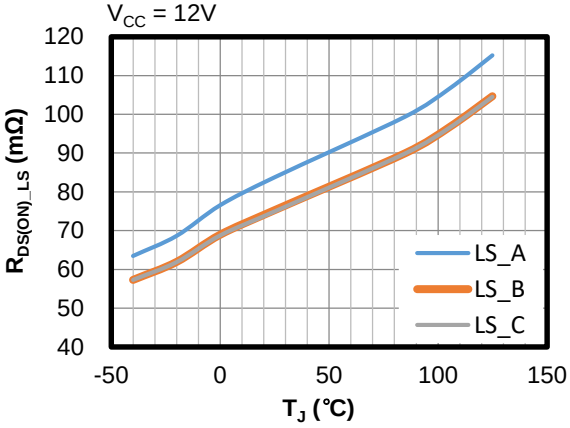
HS-FET On Resistance vs. Junction Temperature

V_{CC} = 12V



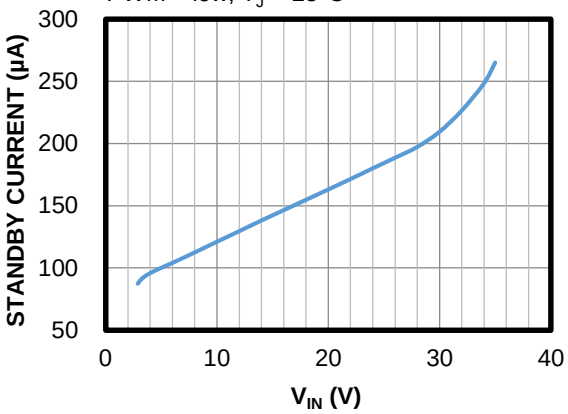
LS-FET On Resistance vs. Junction Temperature

V_{CC} = 12V



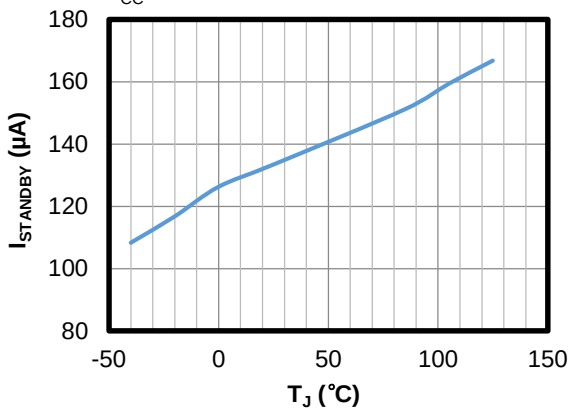
Standby Current vs. Input Voltage

PWM = low, T_J = 25°C



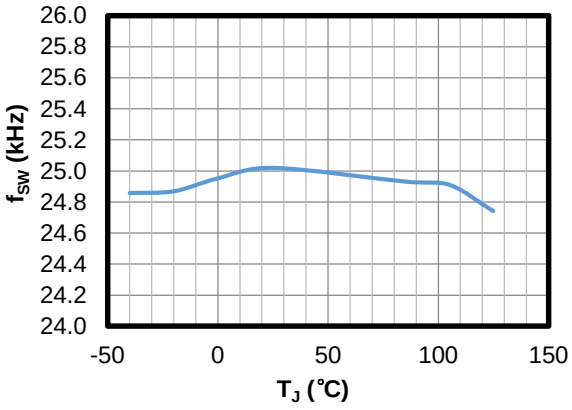
Standby Current vs. Junction Temperature

V_{CC} = 12V



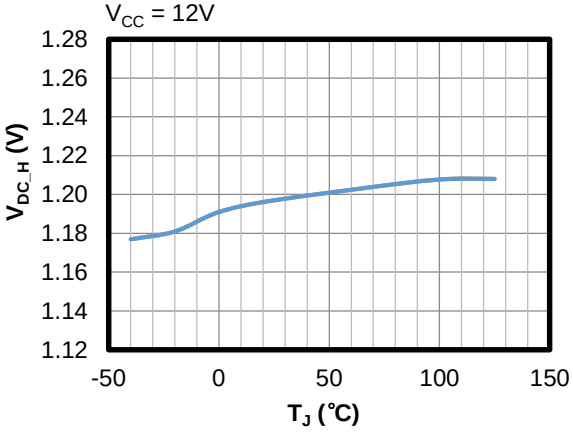
Switching Frequency vs. Junction Temperature

V_{CC} = 12V



DC Input High Threshold vs. Junction Temperature

V_{CC} = 12V



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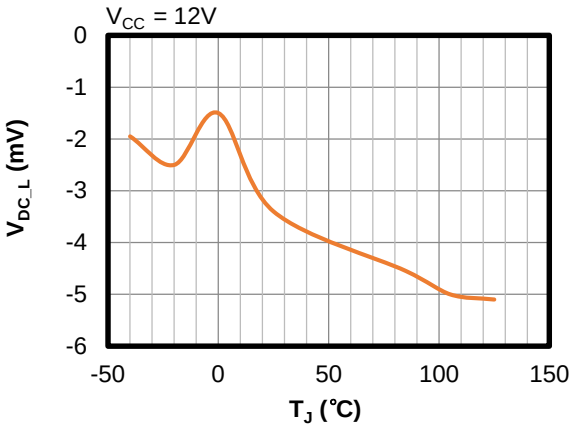
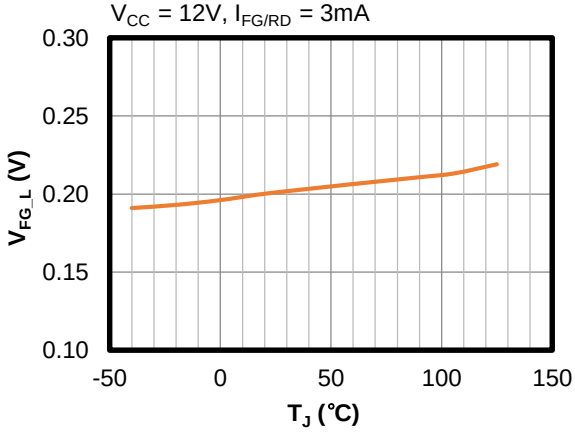
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

DC Input Low Threshold vs. Junction Temperature



FB Output Low-Level Voltage vs. Junction Temperature



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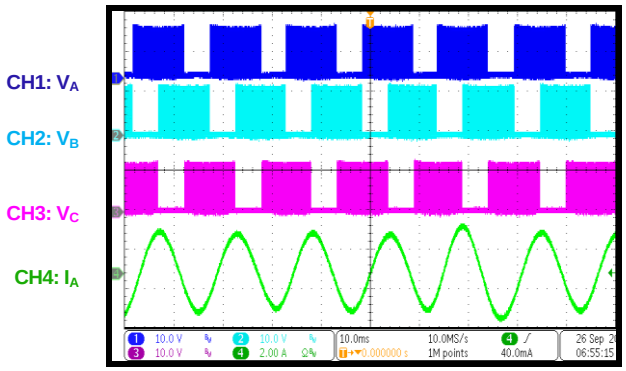
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors, unless otherwise noted.

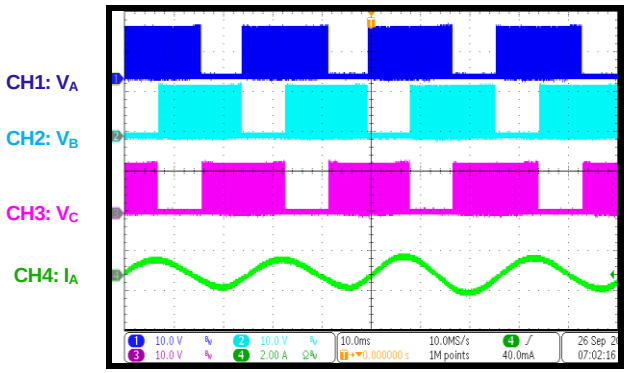
Steady State

PWM duty = 100%, DIR = low, counterclockwise



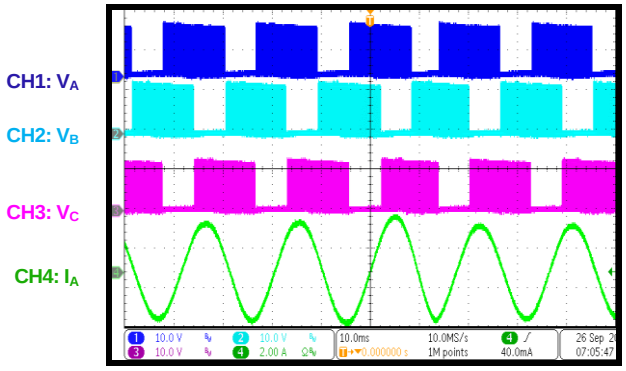
Steady State

PWM duty = 50%, DIR = low, counterclockwise



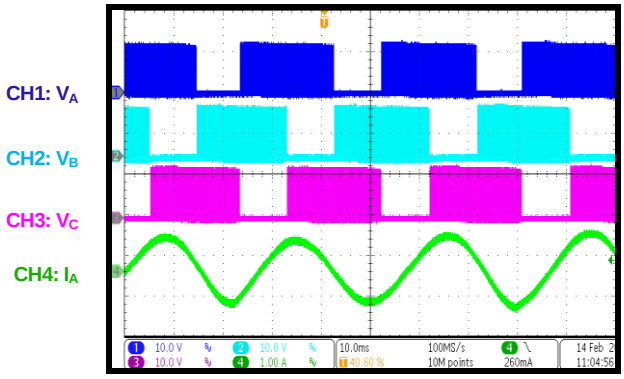
Steady State

PWM duty = 100%, DIR = high, clockwise



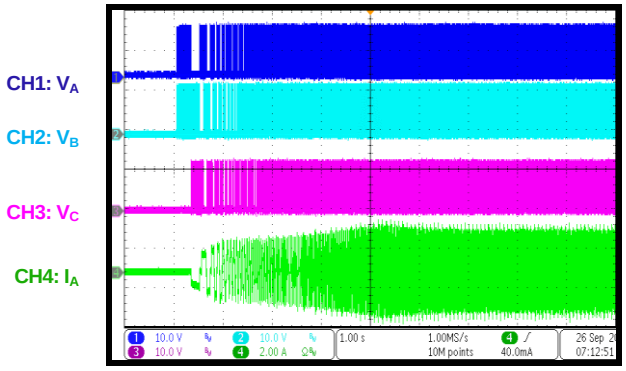
Steady State

PWM duty = 50%, DIR = high, clockwise



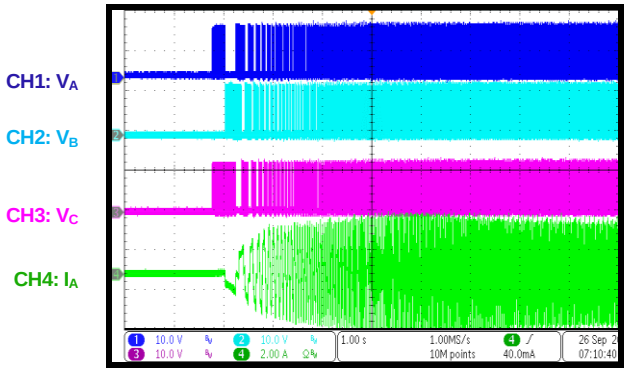
PWM On

PWM duty = 0% to 100%, triple Hall-effect sensor, DIR = low, counterclockwise



PWM On

PWM duty = 0% to 100%, triple Hall-effect sensor, DIR = high, clockwise



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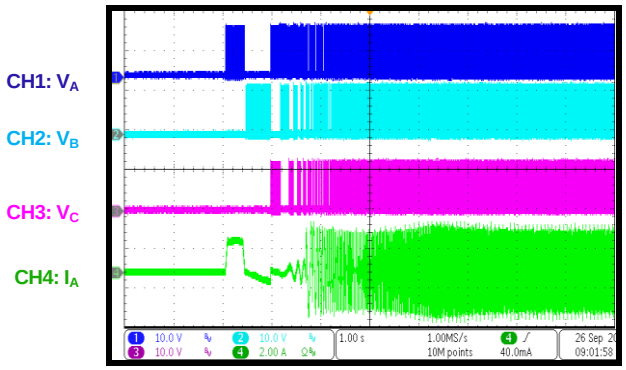
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors, unless otherwise noted.

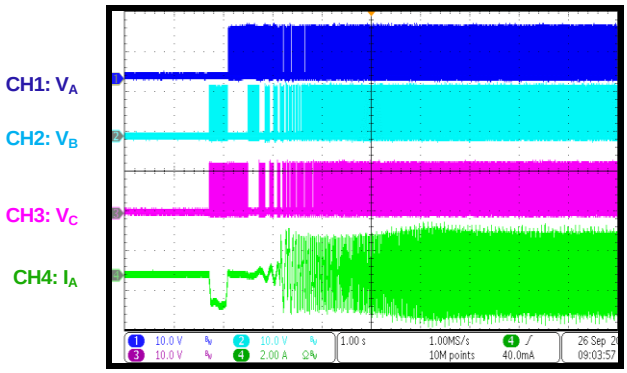
PWM On

PWM duty = 0% to 100%, single Hall sensor, DIR = low, counterclockwise



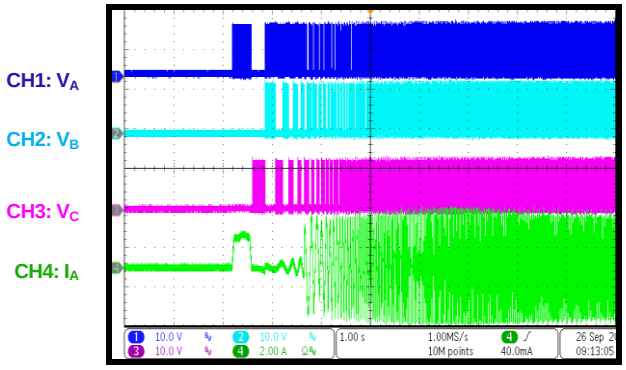
PWM On

PWM duty = 0% to 100%, single Hall sensor, DIR = low, counterclockwise



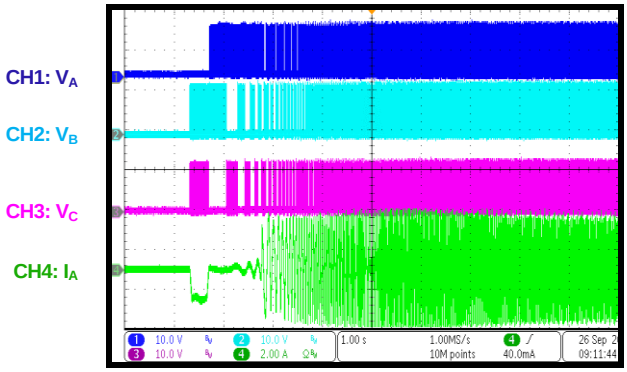
PWM On

PWM duty = 0% to 100%, single Hall sensor, DIR = high, clockwise



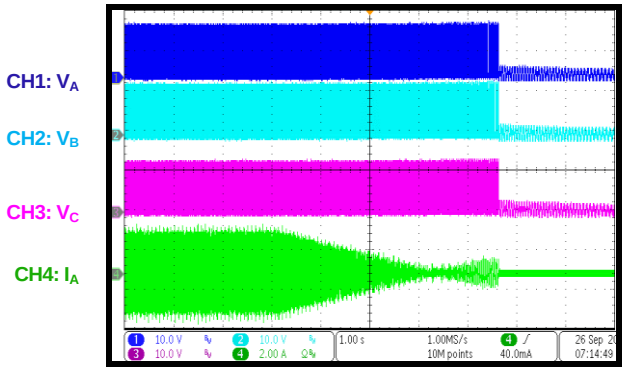
PWM On

PWM duty = 0% to 100%, single Hall sensor, DIR = high, clockwise



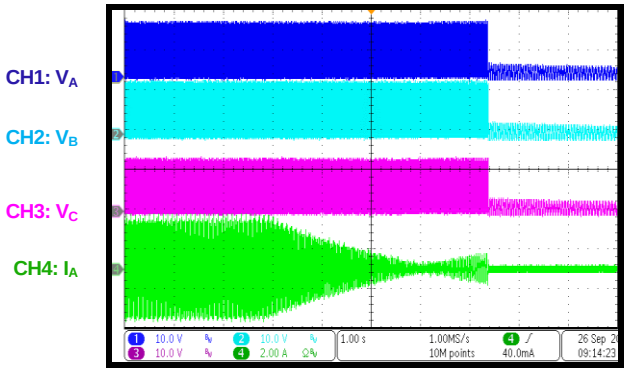
PWM Off

PWM duty = 100% to 0%, DIR = low, counterclockwise



PWM Off

PWM duty = 100% to 0%, DIR = high, clockwise



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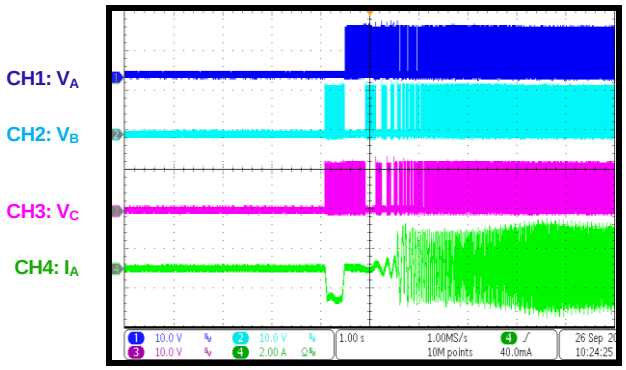
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors, unless otherwise noted.

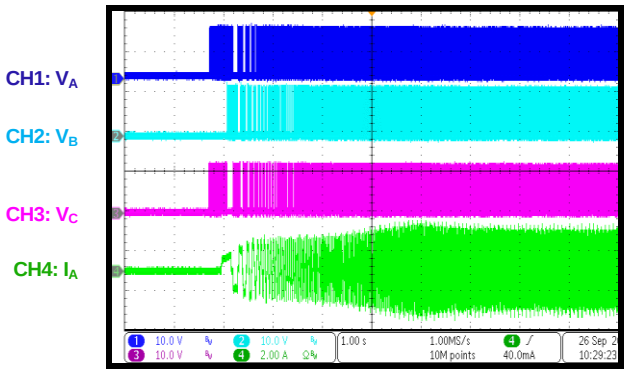
Start-Up through VCC

V_{CC} = 0V to 12V, PWM duty = 100%, single Hall sensor, DIR = low, counterclockwise



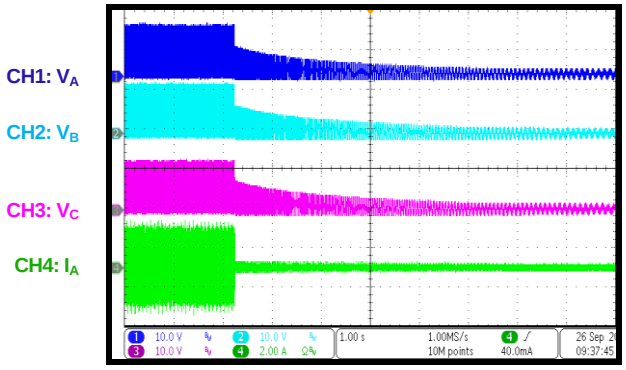
Start-Up through VCC

V_{CC} = 0V to 12V, PWM duty = 100%, triple Hall sensor, DIR = low, counterclockwise



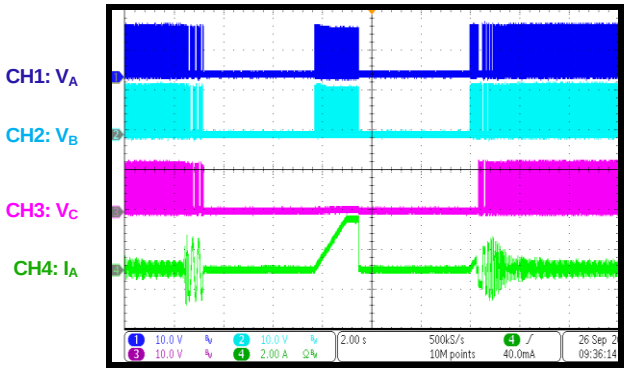
Shutdown through VCC

V_{CC} = 0V to 12V, PWM duty = 100%, DIR = low, counterclockwise



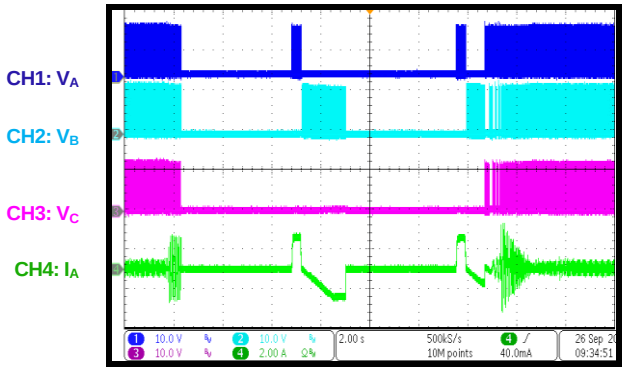
Rotor Lock and Retry

PWM duty = 25%, triple Hall sensor, lock rotor then release



Rotor Lock and Retry

PWM duty = 25%, single Hall sensor, lock rotor then release



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FUNCTIONAL BLOCK DIAGRAM

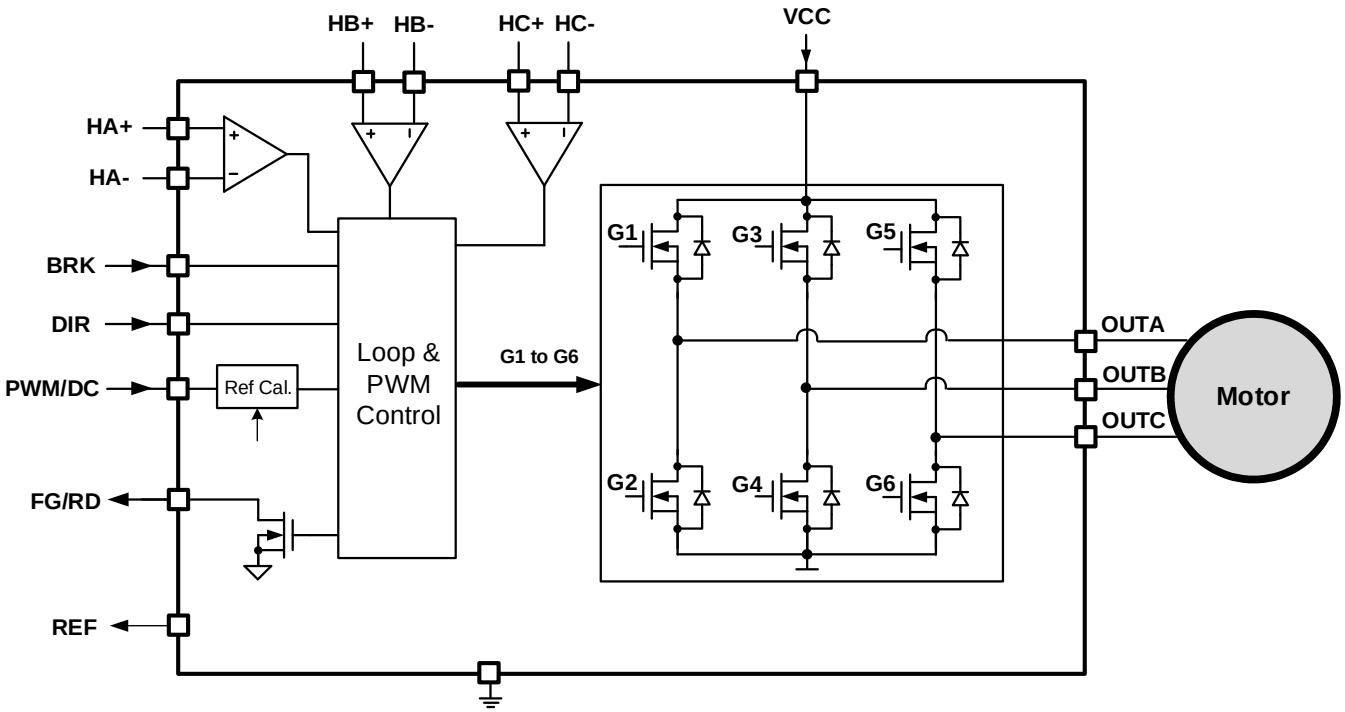

Figure 3: Functional Block Diagram

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OPERATION

The MP6631B is a three-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs. The MP6631B controls the motor speed via the pulse-width modulation (PWM) signal or the DC voltage (V_{DC}) on the PWM/DC pin, with closed-loop and open-loop speed control, as well as a built-in, configurable speed curve function.

The MP6631B also features a rotational speed detector. The rotational speed detector is an open-drain output via the FG/RD pin. It outputs a high or low voltage relative to the external Hall signal. The motor direction is controlled via the DIR pin, and the BRK pin is used to brake the motor.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MP6631B features a sinusoidal drive. Figure 4 shows the MP6631B's output drive, where HA, HB, and HC are the outputs of Hall A, Hall B, and Hall C, respectively, and OUTA, OUTB, and OUTC are the output of the OUTA, OUTB, and OUTC pins, respectively.

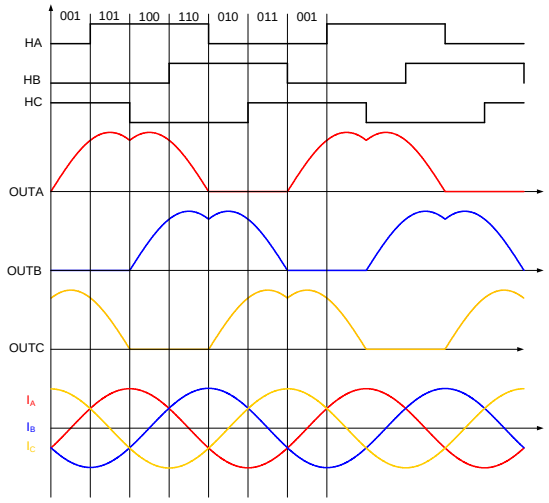

Figure 4: MP6631B Hall Output and Output Drive

Speed Control

The PWM/DC pin controls the motor speed in an open or closed loop via the PWM signal or V_{DC}. PWM/DC accepts a wide 1kHz to 100kHz input frequency range, or a 0V to 1.2V voltage.

If DC_PWM = 1, the motor speed is controlled via V_{DC} on the PWM/DC pin.

If DC_PWM = 0, the motor speed is controlled via the input PWM signal duty cycle.

Starting Duty Cycle and Minimum Speed

The starting duty cycle is configured by the DIN_MIN bits. When PWM input duty cycle is below the duty cycle set by DIN_MIN, the fan speed supports two modes:

1. When SPD_ZERO is set to 0, the speed maintains the minimum speed.
2. When SPD_ZERO is set to 1, the speed is at 0.

Speed Curve Configuration

The SPD_MAX registers configure the speed when the input duty cycle is at 100%. Otherwise, the MP6631B provides a five-point curve configuration function where the output speed can be configured when the input duty cycle is 37.5%, 50%, 62.5%, 75%, or 87.5%. Linear interpolation occurs between the adjacent duty cycles.

The DIN_MIN register sets the minimum input duty cycle, and SPD_MIN sets the minimum output duty cycle and minimum speed.

Figure 5 shows the curve configuration when SPD_ZERO = 1.

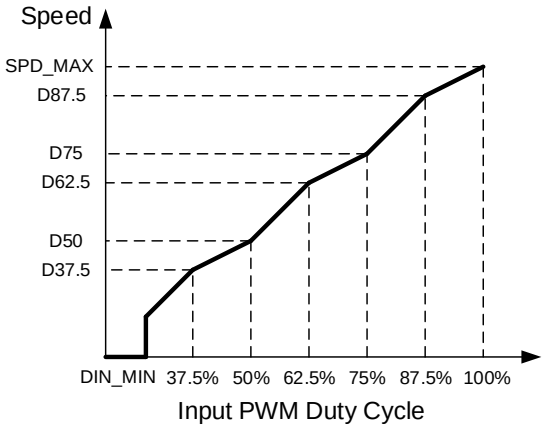

Figure 5: Curve Configuration when SPD_ZERO = 1

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Figure 6 shows the curve configuration when SPD_ZERO = 0.

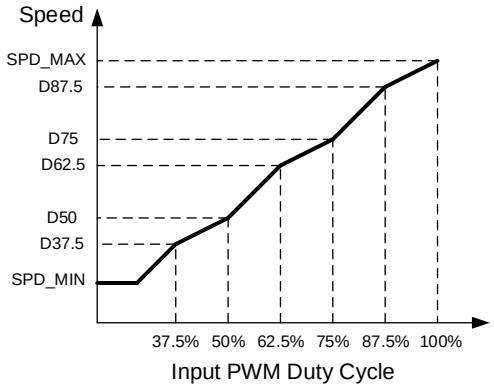

Figure 6: Curve Configuration when SPD_ZERO = 0

Speed Closed-Loop and Open-Loop Control

In closed-loop mode (OPEN_L = 0, CLOSE_H = 1), the MP6631B internally detects the Hall signal speed and feedback to the control loop, which adjusts the output PWM duty cycle in a closed loop. By doing this, the motor speed follows the reference exactly.

In open-loop mode (OPEN_L = 1), the OUT1 and OUT2 output duty cycles depend directly on the PWM signal or V_{DC}.

In mixed mode (OPEN_L = 0, CLOSE_H = 0), the MP6631B operates in closed-loop mode when the PWM input duty cycle is below 87.5%, and operates in open-loop mode when the input duty cycle exceeds 87.5%.

Soft-Start Time

To reduce the input inrush current during start-up, the MP6631B provides the reference speed's configurable soft-start time (t_{SS}) by setting register TDYN, bits[1:0]. t_{SS} can be configured to be between 0.3s and 5.2s.

The 0.3s t_{SS} option is provided for small inertia applications such as a small-sized motor.

Closed-Loop Integrator Gain

In closed-loop mode, the closed-loop integrator gain depends on registers KI[7:0] and KP[7:0].

Higher KI and KP values lead to quick loop response. KI and KP should be adjusted according to the dynamic response and steady state operation.

Single- or Triple-Hall Input Mode

The MP6631B supports either a single or triple Hall-effect sensor. If a single Hall-effect sensor is employed, the Hall selection bit must set the single Hall sensor, and Hall C is used as the control.

Direction Control

The motor direction is controlled via the DIR pin. When DIR is pulled low, the MP6631B operates in forward rotation in the following sequence: A → B → C → A…

When DIR is pulled high, the MP6631B operates in reverse rotation in the following sequence: A → C → B → A…

Alignment

At the beginning of start-up in single Hall sensor applications, the MP6631B aligns the rotor in certain positions depending on the Hall outputs. After the alignment time set by the TOPS register elapses, the MP6631B enters pre-startup. This function is only enabled in single Hall sensor applications.

Pre-Startup Timer

During pre-startup, the MP6631B gradually increases the output duty cycle with the timer, set by TPRE[1:0]. This provides sufficient torque for robust start-up and avoids current overshoot during start-up.

- TPRE = 0: Timer period is 2.5ms
- TPRE = 1: Timer period is 5ms
- TPRE = 2: Timer period is 10ms
- TPRE = 3: Timer period is 20ms

A longer timer period leads to lower soft pre-startup current, but increases the pre-startup time.

Cycle-by-Cycle Over-Current Protection (OCP)

Under normal switching, if the current flowing through the MOSFET exceeds the threshold set by register OCP, bits[1:0] after a set blanking time, the high-side MOSFETs (HS-FETs) turn off and the low-side MOSFETs (LS-FETs) turn on immediately. The MP6631B resumes normal switching during the next switching cycle.

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Maximum Peak Current Limit

If the load current is not limited by OCP and the current exceeds the maximum peak current limit threshold (typically 6A), all MOSFETs turn off and the MP6631B tries to restart after a lock-retry time.

Speed Detection

The FG signal on the FG/RD pin outputs an internal Hall change signal for speed indication. Different FG signal frequencies are provided. The frequencies are selected by setting the FGRD bit to 00, 01, or 10. The FG/RD pin is an open-drain output, and must be pulled up externally via a resistor.

Locked-Rotor Protection

If the motor rotor is locked and the Hall signal edge is not detected within the 0.5s detection time, then the MP6631B turns on all LS-FETs and auto-restarts after the recovery time (typically 4.5s). By setting the FGRD bit to 11, the FG/RD pin's signal is set to rotor-lock indication. During a locked-rotor fault, FG/RD remains low.

Over-Voltage Protection (OVP)

If the voltage on the VCC pin (V_{CC}) exceeds the over-voltage (OV) threshold (typically 34V), the MP6631B turns off the HS-FETs and turns on the LS-FETs. Once V_{CC} drops below 32V, the device resumes normal operation.

Thermal Shutdown

The MP6631B features thermal monitoring. If the MP6631B's die temperature exceeds 160°C, the output duty cycle decreases to reduce power consumption until the die temperature drops below 135°C.

Under-Voltage Lockout (UVLO)

If V_{CC} falls below the UVLO threshold, all the device circuitries are disabled and the internal logic resets. Once V_{CC} exceeds the UVLO threshold, the device restarts and resumes normal operation.

Test Mode and Factory Mode

To configure the internal registers, the MP6631B supports test mode. In test mode, all internal registers can be read/written. After the design is finalized, the register values can be configured to the non-volatile memory (NVM), which can be configured twice. Ask an FAE or sales for the MPS Fan Driver GUI software for easy parameter changes and memory configuration.

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REGISTER DESCRIPTION

Register Map

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	SPD_MAX[7:0]							
01h (OTP/REG)	SPD_MAX[15:8]							
02h (OTP/REG)	SPD_MIN							
03h (OTP/REG)	HI_FREQ	RESERVED	DIN_MIN					
04h (OTP/REG)	OVP_EN	WAIT_TM		RESERVED	MAX_EN	CLOSE_H	OPEN_L	RESERVED
05h (OTP/REG)	RESERVED	TDYN		TPRE		SPD_ZERO	SINGLE	RESERVED
06h (OTP/REG)	HAL_POL	RESERVED	DC_PWM	FGRD		ILIM		TPOS
07h (OTP/REG)	LOCK	SW_SEL	THETA_COMP					
08h (OTP/REG)	KI							
09h (OTP/REG)	KP							
0Ah (OTP/REG)	RESERVED		WAIT_SEL	RESERVED		OCP_EN	OCP_BH	OVP_BH
0Bh (OTP/REG)	D37.5							
0Ch (OTP/REG)	D50							
0Dh (OTP/REG)	D62.5							
0Eh (OTP/REG)	D75							
0Fh (OTP/REG)	D87.5							
10h (REG)	RESERVED		OTP_PAGE		RESERVED			DEBUG

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MAX_SPEED_1 (00h)

The MAX_SPEED_1 command sets the maximum speed in closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MAX[7:0]	0xFF	Sets the maximum speed when the input duty cycle is 100%. 8-bit least significant bit (LSB). Electrical speed = 7.5rpm / LSB.

MAX_SPEED_2 (01h)

The MAX_SPEED_2 command sets the maximum speed in closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MAX[15:8]	0x08	Sets the maximum speed when the input duty cycle is 100%. 8-bit most significant bit (MSB). Combined with SPD_MAX[7:0] to set the maximum speed (electrical speed).

MIN_SPEED (02h)

The MIN_SPEED command sets the minimum speed in closed-loop speed control or the minimum output duty cycle in open-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MIN	0x20	Sets the minimum speed or minimum output duty cycle. In closed-loop mode, this bit sets the minimum speed (electrical speed), depending on the HI_FREQ bit, where: If HI_FREQ = 0, then 60rpm / LSB If HI_FREQ = 1, then 480rpm / LSB In open-loop mode, this bit sets the minimum output duty cycle, where the minimum output duty cycle = SPD_MIN[7:0] / 255 and the default is 12.5%.

CFR_1 (03h)

The CFR_1 command refers to the control function register and sets the switching frequency (f_{SW}), brake mode, and starting duty cycle.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	HI_FREQ	0	Selects the high frequency. 0: High frequency is not selected (default) 1: High frequency is selected If HI_FREQ = 1, the SW bit must be set to 1.
6	N/A	RESERVED	0	Reserved.
5:0	OTP/REG	DIN_MIN	0x10	Sets the starting duty cycle, where the starting duty cycle = DIN_MIN / 128 and the default is 12.5%.

CFR_2 (04h)

The CFR_2 command enables over-voltage protection (OVP), and sets the wait status, maximum speed below starting duty cycle, and open-loop/closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	OVP_EN	0	Enables OVP. 0: Disable OVP (default) 1: Enable OVP

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6:5	OTP/REG	WAIT_TM[1:0]	00	Selects the waiting time or speed threshold at start-up. Combined with WAIT_SEL, these bits can select the fixed time that the IC waits before output switching, or the motor speed threshold at which the IC starts driving the motor. The waiting time or speed threshold can be selected as follows: If WAIT_SEL = 1, wait for a fixed time. The time setting is WAIT_TM = 00: 1.2s, 01: 1.8s, 10: 3s, 11: 4.2s. If WAIT_SEL = 0, wait for the motor speed to drop to a certain speed, where WAIT_TM = 00: 1000rpm (electrical speed), 01: 600rpm, 10: 150rpm, 11: 60rpm. This function is active for triple Hall sensor applications.
4	N/A	RESERVED	0	Reserved.
3	OTP/REG	MAX_EN	0	Enables the maximum speed when the PWM input duty cycle < DIN_MIN. 0: Disabled (default) 1: Maximum output speed or maximum output duty cycle when the PWM input duty cycle < DIN_MIN MAX_EN is only active when SPD_ZERO = 0.
2	OTP/REG	CLOSE_H	0	Enables closed-loop speed control when the PWM input duty cycle > 87.5%. 0: Open-loop speed control when the PWM input duty cycle > 87.5% (default) 1: Closed-loop speed control when the PWM input duty cycle > 87.5%
1	OTP/REG	OPEN_L	1	Enables open-loop speed control. 1: Open-loop speed control (default) 0: Closed-loop speed control when the PWM input duty cycle < 87.5%
0	N/A	RESERVED	0	Reserved.

START_HALL (05h)

The START_HALL command sets some details for start-up and the Hall-effect sensor.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	0	Reserved.
6:5	OTP/REG	TDYN	00	Sets the soft dynamic time. The output duty cycle reference time ranges from 0% to 100%. 00: 1.3s (default) 01: 2.6s 10: 5.2s 11: 0.3s
4:3	OTP/REG	TPRE	10	Pre-startup time bits. The output duty cycle's time duration increases by 1 step until the pre-startup process ends. 00: 2.5ms 01: 5ms 10: 10ms (default) 11: 20ms
2	OTP/REG	SPD_ZERO	1	Enables zero speed. 0: Maintain the minimum speed when the PWM input duty cycle < DIN_MIN 1: Stop when the PWM input duty cycle < DIN_MIN

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1	OTP/REG	SINGLE	1	Selects the number of Hall sensors. 0: Triple Hall sensor application 1: Single Hall sensor application (default)
0	N/A	RESERVED	0	Reserved.

CFR_3 (06h)

The CFR_3 command sets the Hall polarity selection, pulse-width modulation (PWM) input and FG/RD output, current limit threshold, and alignment time.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	HAL_POL	0	Selects the Hall input signal polarity. 0: Original (default) 1: Inverse
6	N/A	RESERVED	1	Reserved.
5	OTP/REG	DC_PWM	0	Selects the DC input or pulse-width modulation (PWM) input for the PWM/DC pin. 0: PWM input (default) 1: DC input
4:3	OTP/REG	FGRD	00	Selects the FG/RD pin output. 00: 1x (default) 01: 1/2x 10: 1/4x for single Hall sensor applications, 3x for triple Hall sensor applications 11: RD
2:1	OTP/REG	ILIM	11	Sets the current limit threshold. 00: 0.7A 01: 1.5A 10: 2.2A 11: 3A (default)
0	OTP/REG	TPOS	0	Sets the alignment time. 0: 320ms (default) 1: 650ms

PWM_SW_COMP (07h)

The PWM_SW_COMP command enables lock protection, and sets f_{SW} and the compensation angle.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	LOCK	0	Enables lock protection. 0: enable lock protection (default) 1: disable lock protection
6	OTP/REG	SW_SEL	0	Selects the switching frequency (f_{SW}). 0: 25kHz (default) 1: 50kHz

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5:0	OTP/REG	THETA_COMP	0x00	Sets the leading/lag compensation angle. 0x00: Auto compensation. The non-zero value sets the fixed compensation. The MSB is the signed bit. MSB = 0: leading Compensation angle = THETA_COMP[5:0] x 15 / 8° + 0.94° MSB = 1 lag Compensation angle = 119.06° - THETA_COMP[5:0] x 15 / 8°

KI (08h)

The KI command configures the integral parameter for closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	KI	0x01	Configures the integral parameter for closed-loop speed control.

KP (09h)

The KP command configures the gain parameter during closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	KP	0x01	Configures the gain during closed-loop speed control.

CFR_4 (0Ah)

The CFR_4 command sets the wait function for start-up, over-current protection (OCP), and the over-voltage protection (OVP) response.

Bits	Access	Bit Name	Default	Description
7:6	N/A	RESERVED	00	Reserved.
5	OTP/REG	WAIT_SEL	0	Selects the wait function for start-up. 0: The IC does not drive until the speed drops below the threshold speed during start-up (default) 1: The IC does not drive for a fixed time during start-up
4:3	N/A	RESERVED	00	Reserved.
2	OTP/REG	OCP	0	Enables over-current protection (OCP). 0: Enabled 1: Disabled
1	OTP/REG	OCP_BH	0	Selects the OCP response. 0: Turn on the LS-FETs and resume switching during the next switching cycle (default) 1: Decrease the output duty cycle
0	OTP/REG	OVP_BH	0	Selects the over-voltage protection (OVP) response. 0: Turn on the LS-FETs when OVP is triggered 1: Turn off all the MOSFETs

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SPEED_CURVE_1 (0Bh)

The SPEED_CURVE_1 command configures the speed when the input PWM duty cycle is 37.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D37.5	0x60	Sets the speed or output duty cycle when the input PWM duty cycle = 37.5%. For open-loop control, set the output duty cycle when the input PWM duty cycle = 37.5%. Output duty cycle = D37.5[7:0] / 256. For closed-loop control, set the reference speed when the input PWM duty cycle = 37.5%. Speed = D37.5[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_2 (0Ch)

The SPEED_CURVE_2 command configures the speed when the input PWM duty cycle is 50%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D50	0x80	Sets the speed or output duty cycle when the input PWM duty cycle = 50%. For open-loop control, set the output duty cycle when the input PWM duty cycle = 50%. Output duty cycle = D50[7:0] / 256. For closed-loop control, set the reference speed when the input PWM duty cycle = 50%. Speed = D50[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_3 (0Dh)

The SPEED_CURVE_3 command configures the speed when the input PWM duty cycle is 62.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D62.5	0xA0	Sets the speed or output duty cycle when the input PWM duty cycle = 62.5%. For open-loop control, set the output duty cycle when the input PWM duty cycle = 62.5%. Output duty cycle = D62.5[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty cycle = 62.5%. Speed = D62.5[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_4 (0Eh)

The SPEED_CURVE_4 command configures the speed when the input PWM duty cycle is 75%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D75	0xC0	Sets the speed or output duty cycle when the input PWM duty cycle = 75%. For open-loop control, set the output duty cycle when the input PWM duty cycle = 75%. Output duty cycle = D75[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty cycle = 75%. Speed = D75[7:0] / 256 x SPD_MAX[15:0].

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SPEED_CURVE_5 (0Fh)

The SPEED_CURVE_5 command configures the speed when the input PWM duty cycle is 87.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D87.5	0xE0	Sets the speed or output duty cycle when the input PWM duty cycle = 87.5%. For open-loop control, set the output duty cycle when the input PWM duty cycle = 87.5%. Output duty cycle = D87.5[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty cycle = 87.5%. Speed = D87.5[7:0] / 256 x SPD_MAX[15:8].

OTP_DEBUG (10h)

The OTP_DEBUG command sets the one-time programmable (OTP) indicator and configures debugging mode.

Bits	Access	Bit Name	Default	Description
7:6	N/A	RESERVED	00	Reserved.
5:4	REG	OTP_PAGE	0	OTP memory page indicator. 00: No OTP configured 01: OTP page 1 is configured 10: OTP page 2 is configured
3:1	N/A	RESERVED	000	Reserved.
0	REG	DEBUG	0	Debugging bit. Write 1 to exit debugging mode.

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APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible. Sufficient capacitance must be applied to maintain a stable input voltage (V_{IN}) and reduce input switching voltage noise and ripple. C_{IN}'s impedance must be low at the switching frequency (f_{SW}). Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics.

The capacitance depends on the DC voltage applied on the capacitor. A ceramic capacitor can lose more than 50% of its capacitance when the voltage is close to the voltage rating. Leave a sufficient voltage rating margin when selecting C_{IN}.

To absorb chargeback energy, an additional electrolytic capacitor is recommended.

Input Clamping TVS Diode

High voltage spikes are created when the energy stored in the motor charges back to C_{IN}. To avoid these spikes, it is recommended to use a voltage-clamping transient voltage suppressor (TVS) diode. The maximum clamping voltage should be below the MP6631B's maximum operating V_{IN}.

Hall Placement and Connection

Hall sensors are required to operate the MP6631B, which supports Hall elements with differential inputs. When Hall elements are used, the Hall sensors can be connected in series or in parallel. The Hall input signal polarity can be inversed via register HAL_POL, bit[7].

Figure 7 shows the Hall sensors connected in series.

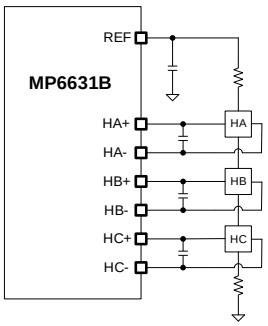

Figure 7: Series Hall Elements Connection

Figure 8 shows the Hall sensors connected in parallel.

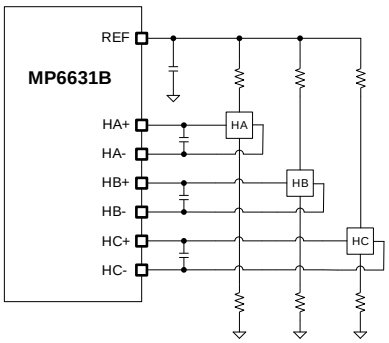

Figure 8: Parallel Hall Elements Connection

The MP6631B's Hall-sensor IC outputs logic polarity with an open-drain output, and requires an external pull-up resistor (R_{PULL_UP}).

Figure 9 shows the Hall-sensor IC connection.

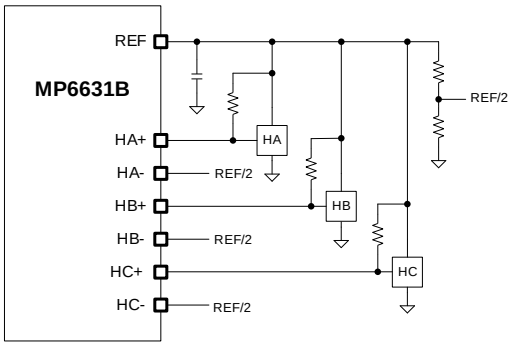

Figure 9: Hall Sensor Connection

Hall Sensor Placement Example

The MP6631B supports either a single or triple Hall-effect sensor. As an example, consider the Hall sensor placement for a 4-pole, 6-slot motor. There are two conditions to evaluate:

1. When the current flows into the stator phase winding, the north magnetic field is generated, and can be checked via the right-hand theorem of the magnetic field.
2. If the Hall sensor output is high when the north pole is close to the Hall sensor's branded side.

If the north magnetic field is generated and the Hall sensor output is high, both conditions are satisfied, and the Hall sensor placement is as follows (see Figure 10 on page 24):

- Hall A is aligned with phase B's central line.

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- Hall B is aligned with phase C's central line.
- Hall C is aligned with phase A's central line.

In single Hall sensor applications, Hall C is the active Hall sensor.

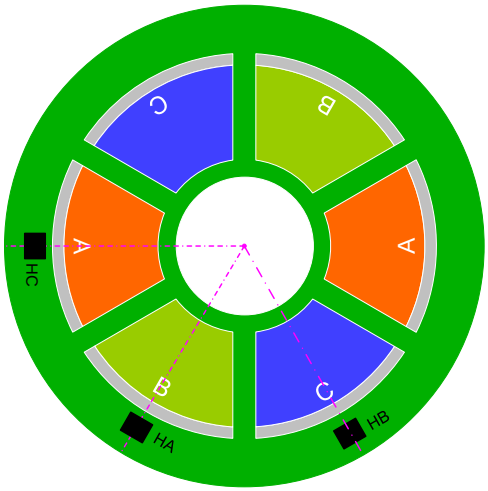

Figure 10: Hall Sensor Placement Option 1

If one of these conditions is not satisfied, the Hall sensor placement can be shifted 180° into an electrical angle, resulting in the following Hall sensor placement (see Figure 11):

- Hall A is aligned with the central line of phase A and phase C.
- Hall B is aligned with the central line of phase A and phase B.
- Hall C is aligned with the central line of Phase B and Phase C.

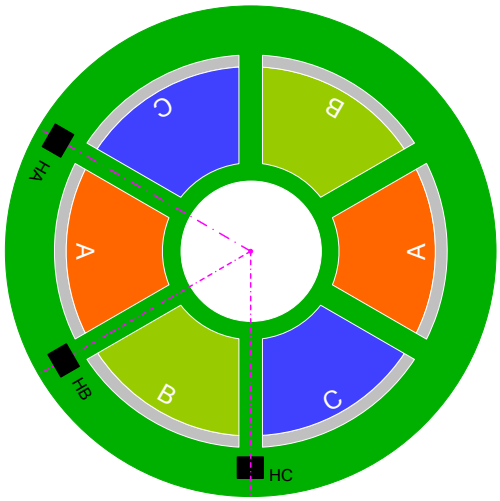

Figure 11: Hall Sensor Placement Option 2

The MP6631B supports inverse polarity of Hall input signal with register bit HAL_POL.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 12 and Figure 13, and follow the guidelines below:

1. After selecting C_{IN}, place a 100nF/X7R bypass capacitor as close to the VCC and GND pins as possible.

Figure 12 shows the recommended PCB layout when the MP6631B is placed on the top layer and the bypass capacitor is placed on the bottom layer.

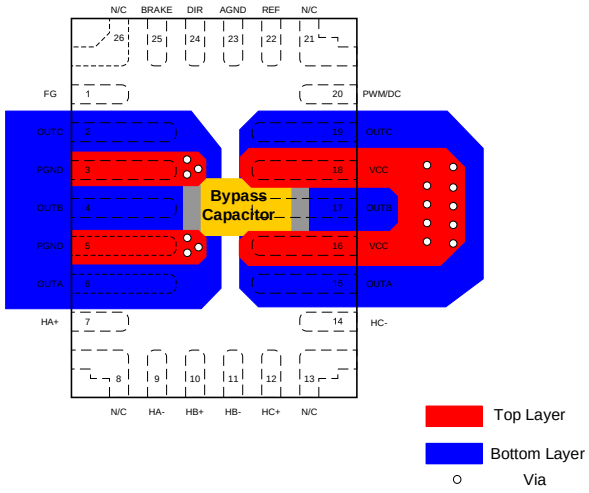

Figure 12: Recommended PCB Layout (Top View)

Figure 13 shows the side view of the MP6631B's recommended PCB layout.

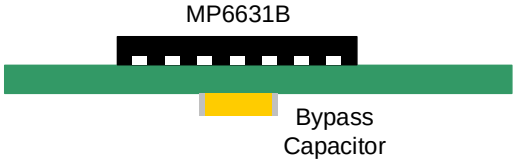

Figure 13: Recommended PCB Layout (Side View)

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TYPICAL APPLICATION CIRCUIT

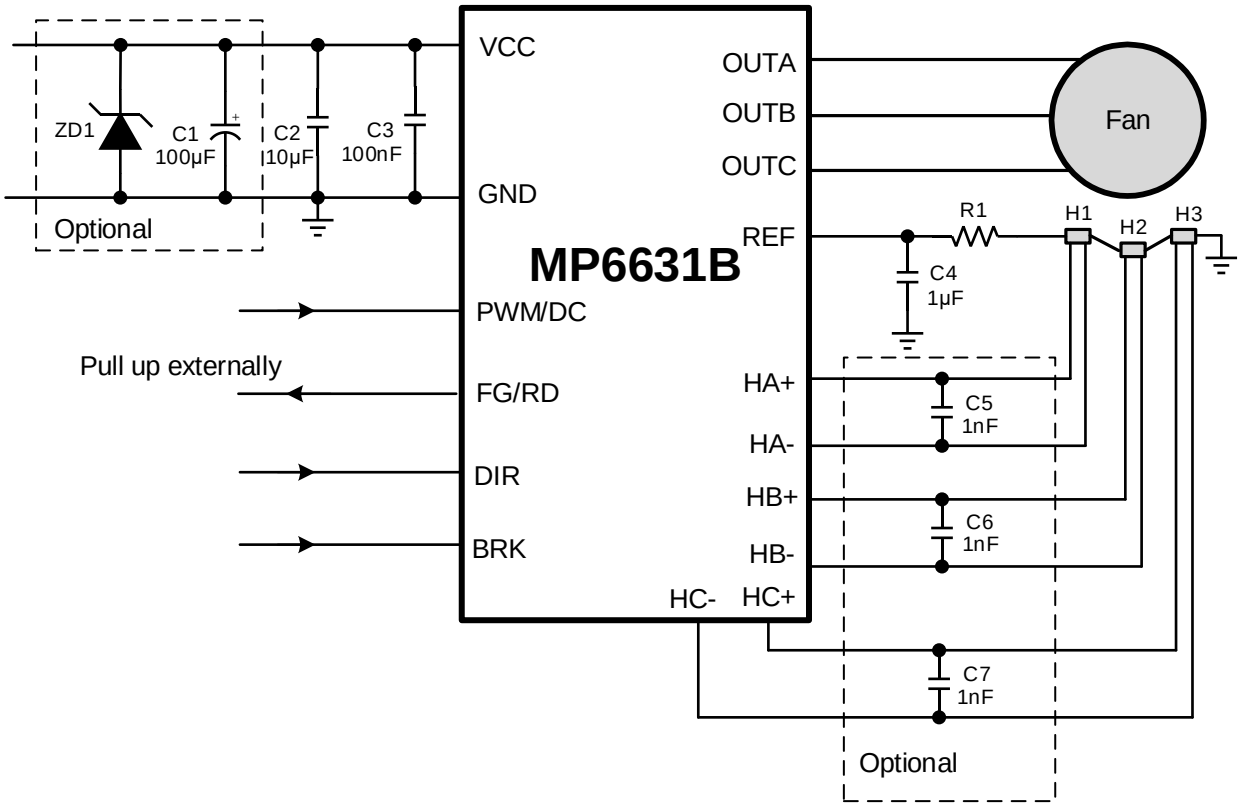

Figure 14: Triple Hall-Effect Sensor Application

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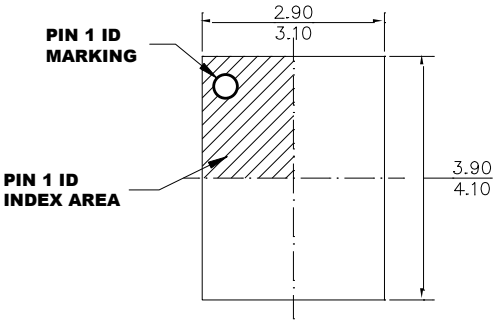
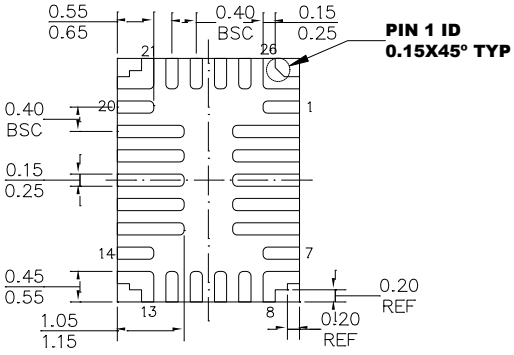
PACKAGE INFORMATION

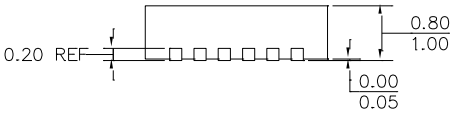
QFN-26 (3mmx4mm)



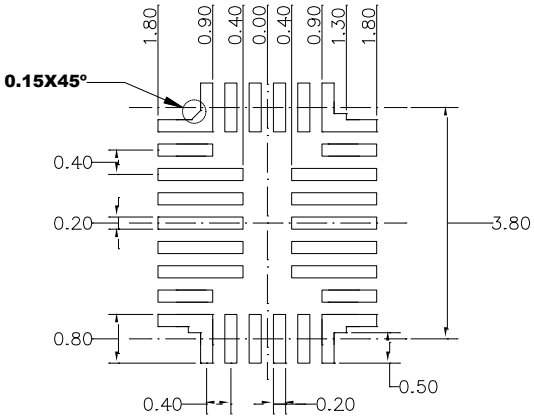
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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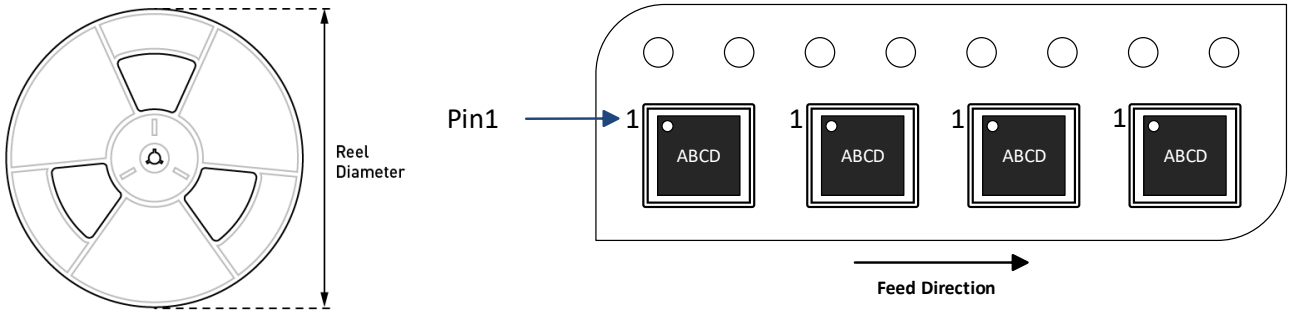
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6631BGL-xxxx-Z	QFN-26 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/2/2024	Initial Release	-

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