MP4255

36V, 3A, Dual-Channel Buck Converters with Digital Interface for Power Delivery

DESCRIPTION

The MP4255 integrates two dual-channel, monolithic step-down converters with an digital interface. Each channel can deliver up to 3A of output current (I_{OUT}) across a wide 4V to 36V input voltage (V_{IN}) range, with excellent load and line regulation.

The device is designed for USB charger applications with dual ports. Both channels can work with an external USB power delivery (PD) controller.

The digital interface and one-time programmable (OTP) memory provide flexibly configurable parameters.

Full protection features include over-current protection (OCP), output over-voltage protection (OVP), and thermal shutdown.

The MP4255 requires a minimal number of readily available, standard external components, and is available in a QFN-21 (4mmx5mm) package.

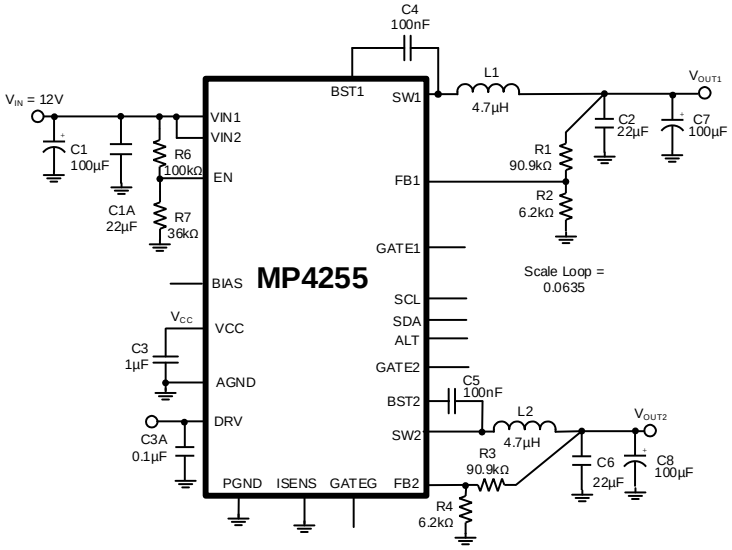
FEATURES

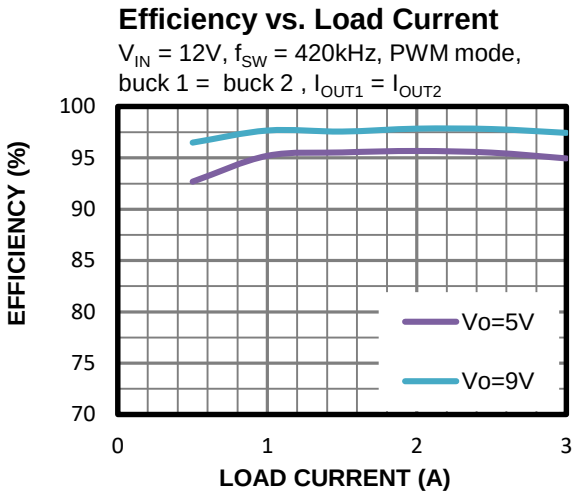
- Dual 3A or Shared 6A Buck Converter
- Supports USB PD 3.1
- Wide 4V to 36V Operating Input Voltage (V_{IN}) Range
- 1V to 36V Output Voltage (V_{OUT}) Range
- 0.1V to 1.63V Reference Voltage (V_{REF}) Range with 0.8mV Steps
- Selectable Switching Frequency (f_{SW}) (250kHz, 420kHz, 1.1MHz, or 2.1MHz)
- Frequency Spread Spectrum (FSS)
- Low-Dropout (LDO) Mode
- Line Drop Compensation
- Accurate, Adjustable Output Current Limit (I_{OUT_LIMIT}) with 50mA/Step via the Digital Interface
- 22mΩ/26mΩ Internal, Low $R_{DS(ON)}$ Power MOSFETs
- Digital Interface and One-Time Programmable (OTP) Memory with Digital Interface Compatible Parameters:
  - Pulse-Frequency Modulation/Pulse-Width Modulation (PFM/PWM) Mode, I_{LIMIT}, V_{OUT}, FSS, Phase Delay, and Line Drop Compensation
- Bus Voltage (V_{BUS}) Isolation N-Channel MOSFET Gate Driver
- Load-Shedding Alert
- EN Shutdown Active Discharge
- Available in a QFN-21 (4mmx5mm) Package
- Available in a Wettable Flank Package

APPLICATIONS

- USB Power Delivery (PD)
- USB Dedicated Charging Ports (DCP)
- DC/DC Power Supplies

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number**	Package	Top Marking	MSL Rating
MP4255GVE-xxxx*	QFN21 (4mmx5mm)	*See Below*	1
MP4255GVE-0000*			
MP4255GVE-0001*			
MP4255GVE-0002*			
EVKT-MP4255	Evaluation Kit	N/A	N/A

* For Tape & Reel, add suffix -Z (e.g. MP4255GVE-xxxx-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code. MP4255GVE-0000 is the default configuration, which can be written once by the user. Other configuration codes are already programmed by the MPS factory, and cannot be reprogrammed by the user.

TOP MARKING

MPSYWW

MP4255

LLLLLL

E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4255: Part number
LLLLLL: Lot number
E: Wettable flank package

EVALUATION KIT EVKT-MP4255

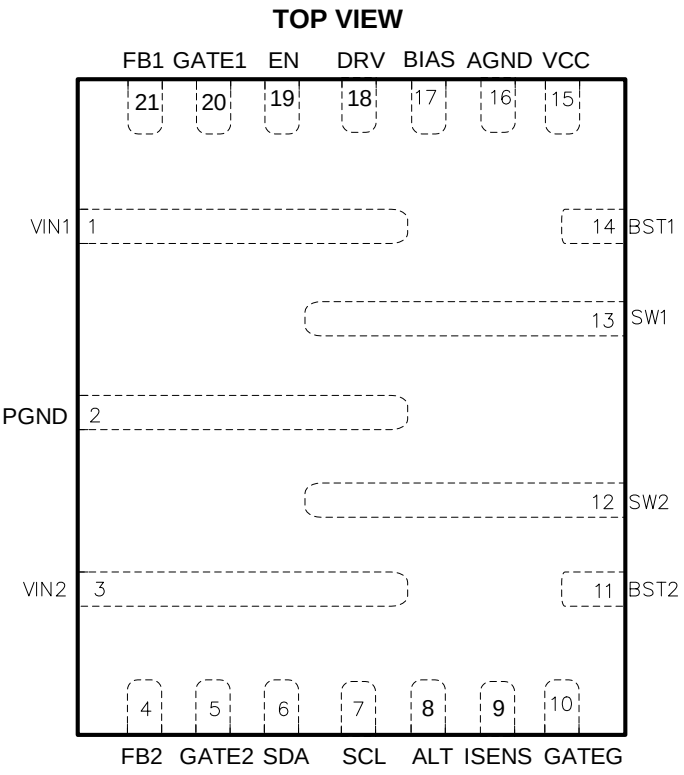
EVKT-MP4255 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV4255-VE-00A	MP4255 evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes USB to digital communication interface, one USB cable, and one ribbon cable	1
3	MP4255GVE-0000	MP4255 IC with default configuration (can be used for OTP configuration)	2

Order directly from MonolithicPower.com or our distributors.

Figure 1: EVKT-MP4255 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-21 (4mmx5mm) with Wettable Flanks

PIN FUNCTIONS

Pin #	Name	Description
1	VIN1	**Channel 1 input voltage**. The MP4255 operates from a 4V to 36V input voltage (V_{IN}). The input capacitor (C1) reduces voltage spikes at the input. Place C1 as close to the IC as possible. The VIN1 pin is the drain of the channel 1 internal power device. VIN1 also supplies power to the entire device. Connect VIN1 and VIN2 together.
2	PGND	**Power ground.** The PGND pin is the reference ground of channel 1. PGND requires extra consideration during PCB layout. Connect the PGND and AGND pins using copper traces and multiple vias.
3	VIN2	**Channel 2 input voltage**. The MP4255 operates from a 4V to 36V V_{IN}. The input capacitor (C2) reduces voltage spikes at the input. Place C2 as close to the IC as possible. The VIN2 pin is the drain of the channel 2 internal power device. Connect VIN1 and VIN2 together.
4	FB2	**Buck 2 feedback**.
5	GATE2	**Gate driver.** The GATE2 pin is the gate driver that turns the bus voltage (V_{BUS}) isolation N-channel MOSFET on.
6	SDA	**Digital interface data line.**
7	SCL	**Digital interface clock signal input.**
8	ALT	**Digital interface alert pin.** The ALT pin is an open-drain output that is pulled low.
9	ISENS	**Second current-limit sense.**
10	GATEG	**External MOSFET gate driver.**
11	BST2	**Bootstrap 2.** Connect a 0.1µF to 0.22µF between the SW2 and BST2 pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
12	SW2	**Switch 2 output.** Connect the SW2 pin to the pad using a wide PCB trace.
13	SW1	**Switch 1 output.** Connect the SW1 pin to the pad using a wide PCB trace.
14	BST1	**Bootstrap 1.** Connect a 0.1µF to 0.22µF between the SW1 and BST1 pins to form a floating supply across the HS-FET driver.
15	VCC	**Internal 5V LDO output**. Use a 1µF decoupling capacitor to decouple the VCC pin.
16	AGND	**Analog ground.** Connect the AGND and PGND pins using copper traces and multiple vias. Connect AGND to the ground node of the VCC capacitor (C_{VCC}).
17	BIAS	**Internal VCC LDO bias input**. Connect the BIAS pin to a 5V or 9V output voltage (V_{OUT}) to improve system efficiency. Add an RC low-pass filter between the output and BIAS.
18	DRV	**LDO output.** The LDO output has a 1mA load capability. V_{OUT} can be set via the digital interface. Use a 0.1µF decoupling capacitor to decouple the DRV pin.
19	EN	**Enable control.** Pull the EN pin high to turn the device on; pull EN low to turn it off. EN has an internal pull-down resistor (R_{EN}).
20	GATE1	**Gate driver**. The GATE1 pin is the gate driver that turns the V_{BUS} isolation N-channel MOSFET on.
21	FB1	**Buck 1 feedback.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} 40V
V_{SW}.....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SWx} + 5.5V
V_{BIAS}, V_{GATE}, V_{ISENS} .....-0.3V to +30V
V_{EN} .....-0.3V to +10V (2)
All Other Pins.....-0.3V to +5.5V
Continuous Power Dissipation (T_A = 25°C) (3) (6)
QFN-21 (4mmx5mm)..... 5.08W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V (4)
Charged-device model (CDM) 750V (5)

Recommended Operating Conditions (6)

Operating input voltage (V_{IN}) range ....4V to 36V
Operating output voltage (V_{OUT}) range.....
.....1V to V_{IN} x D_{MAX}
Output current (I_{OUT})..... 3A per channel or
…….....shared 6A for dual channels
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EV4255-VE-00A (7).....24.6….6.3…°C/W
QFN-21 (4mmx5mm) (8).....44……9…..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For more details, see the Enable (EN) Control section on page 17.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature can be calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per JEDEC specification JESD22-A114. JEDEC document JEP155 states that a 500V human-body model (HBM) allows for safe manufacturing with a standard ESD control process. HBM is with regard to ground.
5) Per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP157 states that a 250V charged-device model (CDM) allows for safe manufacturing with a standard ESD control process.
6) The device is not guaranteed to function outside of its operating conditions. The digital interface output voltage (V_{OUT}) command does not support >21V. If a >21V V_{OUT} is required, a higher V_{OUT} can be set by the feedback resistor (R_{FB}).
7) Measured on the EV4255-VE-00A, 4-layer PCB, 55mmx55mm.
8) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown current	I_{SD}	V_{EN} = 0V, T_J = 25°C		0.5	5	μA
		T_J = -40°C to +125°C		0.5	30	μA
Quiescent current	I_Q	No switching, both channels enabled		0.3		mA
EN rising threshold	V_{EN_RISING}		-5%	1.6	+5%	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-down resistance	R_{EN}	V_{EN} = 2V		2		MΩ
Thermal shutdown (9)	T_{SD}	OTP = 011b		170		°C
Thermal hysteresis (9)	T_{SD_HYS}			20		°C
VCC regulator voltage	V_{CC}	I_{CC} = 0mA to 50mA, T_J = -40°C to 125°C	4.5	5	5.25	V
Step-Down Converters (Channel 1 and Channel 2)						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$	Only monitoring VIN1	3.2	3.35	3.5	V
V_{IN} UVLO hysteresis	V_{UVLO_HYS}			300		mV
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			22		mΩ
Low-side MOSFET (LS-FET on resistance	$R_{DS(ON)\_LS}$			26		mΩ
Feedback (FB) voltage	V_{FB0}	V_{OUT} is set to 1.25V	0.092	0.1	0.108	V
	V_{FB1}	V_{OUT} is set to 5V (default)	-2%	0.400	+2%	V
	V_{FB2}	V_{OUT} is set to 9V	-1.5%	0.720	+1.5%	V
	V_{FB3}	V_{OUT} is set to 20V	-1.5%	1.600	+1.5%	V
Output over-voltage protection (OVP)	V_{OVP}		114	120	125	% of V_{OUT}
Output OVP recovery	$V_{OVP\_RECOVERY}$		104	109	114	% of V_{OUT}
HS-FET peak current limit	I_{HS_PEAK}			13		A
LS-FET valley current limit	I_{LS_VALLEY}	Falling edge		8		A
LS-FET sink current	I_{LS_SINK}			-3.6	-2	A
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +150°C			30	
Output current limit	I_{OUT_LIMIT}	Digital interface is set to 1, T_J = 0°C to 85°C, f_{SW} = 420kHz	-5%	3.6	+5%	A
Switching frequency	f_{SW1}	Digital interface is set to 1	-20%	250	+20%	kHz
	f_{SW2}	Digital interface is set to 2 (default)	-20%	420	+20%	kHz
	f_{SW3}	Digital interface is set to 3	-20%	1100	+20%	kHz
	f_{SW4}	Digital interface is set to 4	-20%	2100	+20%	kHz
Frequency dithering				±12		%
Maximum duty cycle (9)	D_{MAX1}	f_{SW} = 420kHz		95		%
	D_{MAX2}	LDO mode		99		%
Minimum off time (9)	t_{OFF_MIN}			100		ns
Minimum on time (9)	t_{ON_MIN}			80		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-start time	t_{SS}	V_{OUT} = 5V, output is between 10% and 90%, constant slew rate for other output voltages		0.8		ms
Second Current-Limit Sense						
ISENS rising threshold	I_{SENS_RISING}	Buck converters are disabled once I_{SENS_RISING} is triggered, GATE1 and GATE2 are off	130	160	190	mV
ISENS falling threshold	$I_{SENS\_FALLING}$		70	100	130	mV
ISENS deglitch time (9)	t_{ISENS}	Release edge		20		µs
ISENS pull-down current	I_{ISENS_PD1}	V_{ISENS} = 12V		17		mA
	I_{ISENS_PD2}	V_{ISENS} = 80mV		2.5		mA
GATEG pull-down resistance	R_{GATEG}			12	25	Ω
Gate Drivers (GATE1 and GATE2)						
GATE output voltage	$V_{GATE,}$	V_{IN} = 12V, V_{CC} = 5V	16	17	18	V
GATE source current	I_{GATE}		-30%	21.5	+30%	µA
DRV voltage	V_{DRV}		5.7	5.95	6.2	V
		1mA load	5.45	5.82	5.95	V
Digital Interface Specifications (High-Speed Mode) (9)						
ALT pull-down resistance	R_{ALT}			10	25	Ω
ALT leakage	I_{ALT_LKG}	Pull-up with 5V			1	µA
Input logic high voltage	V_{IN_HIGH}	Digital interface is pulled up to V_{DD}, V_{DD} = 1.8V to 5V	1.4			V
Input logic low voltage	V_{IN_LOW}				0.45	V
Output logic low voltage	V_{OUT_LOW}				0.4	V
SCL clock frequency	f_{SCL}			400		kHz
SCL high time	t_{HIGH}		60			Ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DATA}		10			ns
Data hold time	t_{HOLD_DATA}			60		ns
Set-up time for a repeated start condition	t_{SU_START}		160			ns
Hold time for a repeated start condition	t_{HOLD_START}		160			ns
Bus free time between a start and stop condition	t_{BUS_FREE}		160			ns
Set-up time for a stop condition	t_{SU_STOP}		160			ns
SCL and SDA rise time	t_{RISE}		10		300	ns
SCL and SDA fall time	t_{FALL}		10		300	ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pulse width of the suppressed spike	t_{SPIKE}		0		50	ns
Bus line capacitance	C_{BUS}	Per bus line			400	pF

Note:

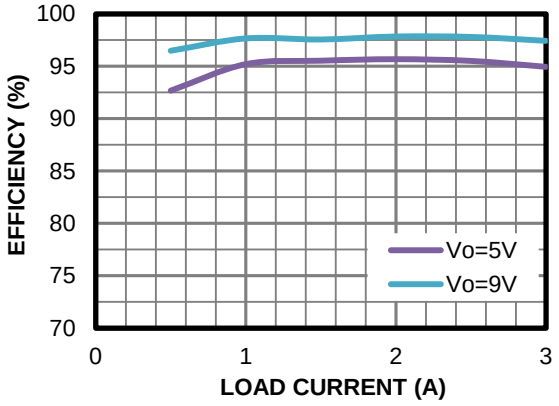
9) Guaranteed by characterization test.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

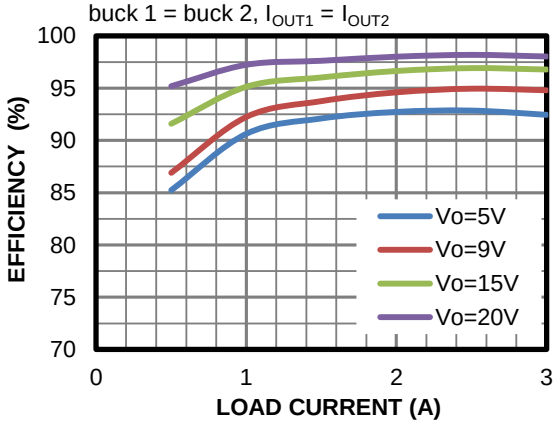
Efficiency vs. Load Current

V_{IN} = 12V, f_{SW} = 420kHz, forced PWM mode, buck 1 = buck 2 , I_{OUT1} = I_{OUT2}



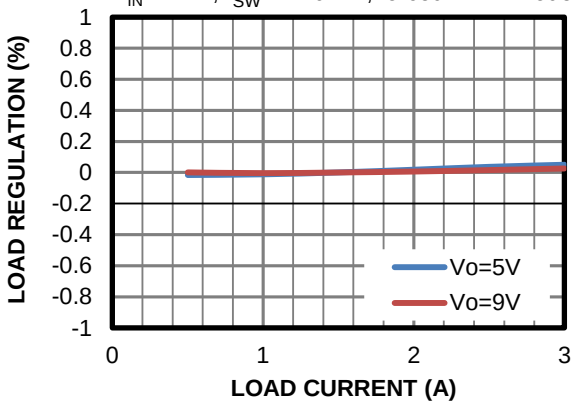
Efficiency vs. Load Current

V_{IN} = 24V, f_{SW} = 420kHz, forced PWM mode, buck 1 = buck 2, I_{OUT1} = I_{OUT2}



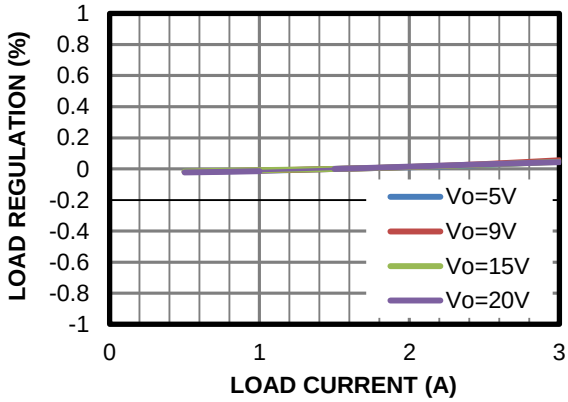
Load Regulation

V_{IN} = 12V, f_{SW} = 420kHz, forced PWM mode



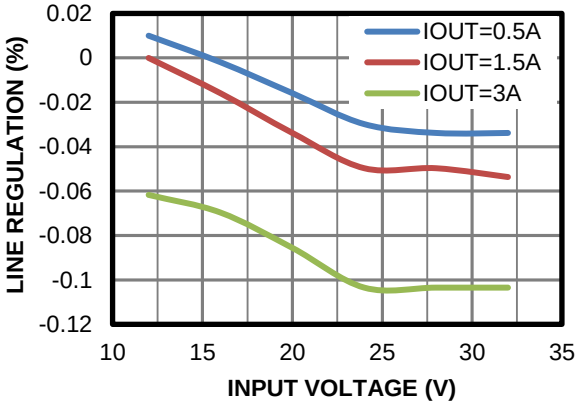
Load Regulation

V_{IN} = 24V, f_{SW} = 420kHz, forced PWM mode



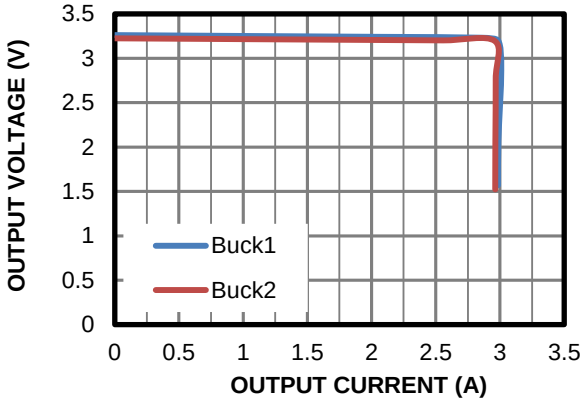
Line Regulation

V_{OUT} = 5V, f_{SW} = 420kHz, forced PWM mode



Output Voltage vs. Output Current

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, forced PWM mode

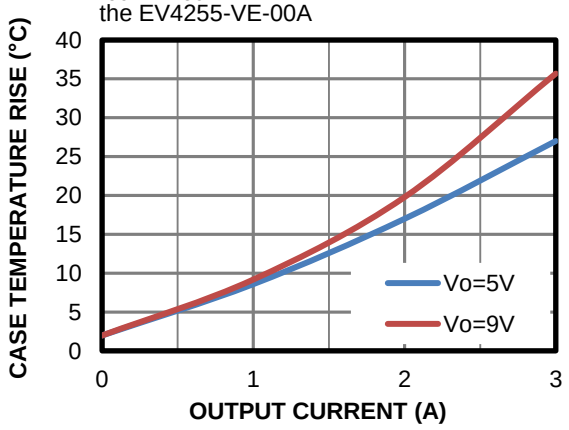


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

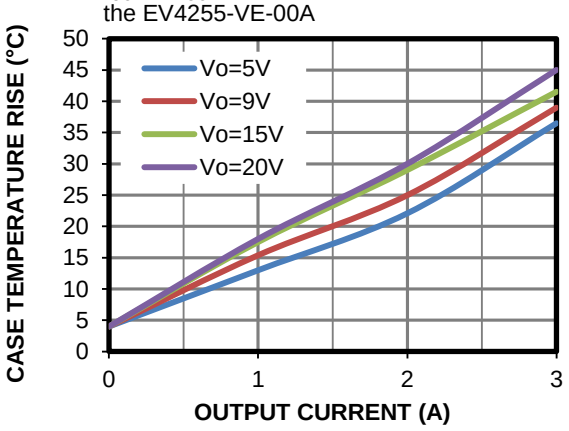
Case Temperature Rise

V_{IN} = 12V, forced PWM mode, f_{SW} = 420kHz, I_{OUT1} = I_{OUT2}, buck 1 = buck 2, measured on the EV4255-VE-00A



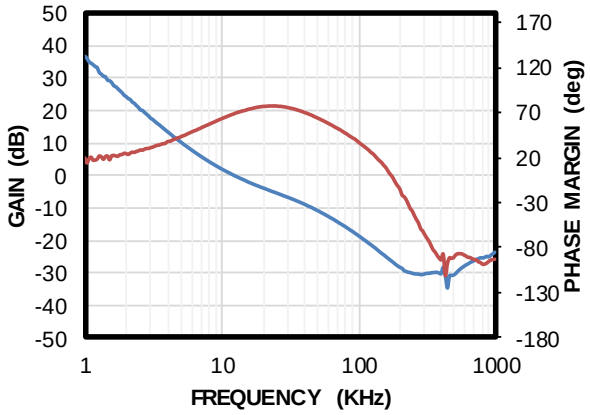
Case Temperature Rise

V_{IN} = 24V, forced PWM mode, f_{SW} = 420kHz, I_{OUT1} = I_{OUT2}, buck 1 = buck 2, measured on the EV4255-VE-00A



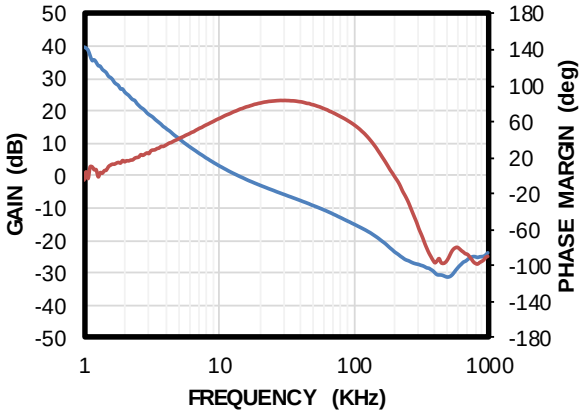
Bode Plot

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, C_{OUT} = 100µF (hybrid e-cap, ESR = 20mΩ) + 22µF (ceramic), BW = 12.6kHz, PM = 70.04°



Bode Plot

V_{IN} = 12V, V_{OUT} = 9V, I_{OUT} = 3A, C_{OUT} = 100µF (hybrid e-cap, ESR = 20mΩ) + 22µF (ceramic), BW = 14KHZ, PM = 72.82°

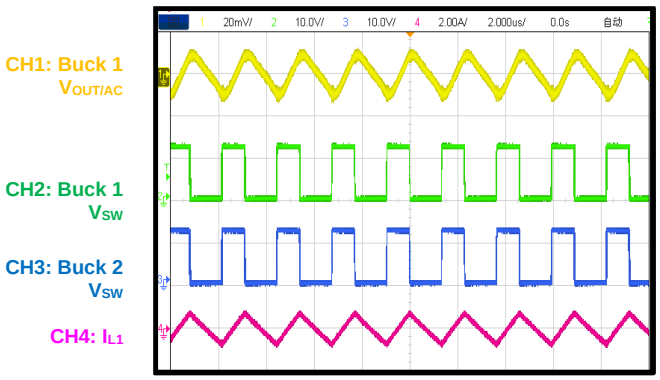


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

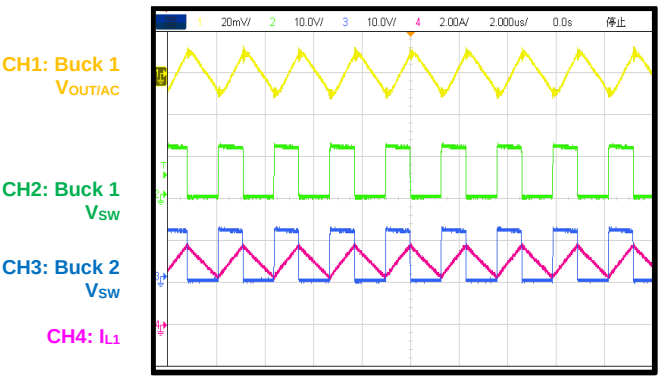
Output Ripple

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 0A, forced PWM mode



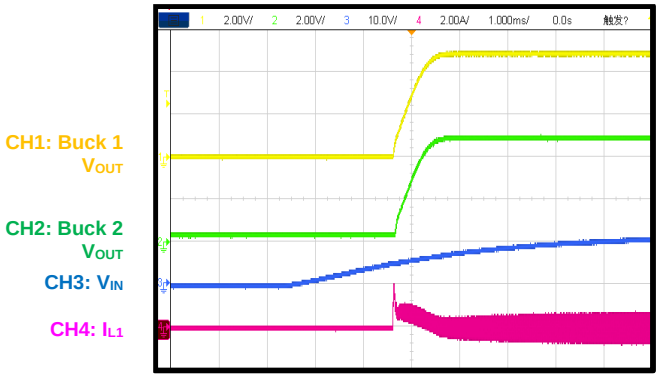
Output Ripple

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A , forced PWM mode



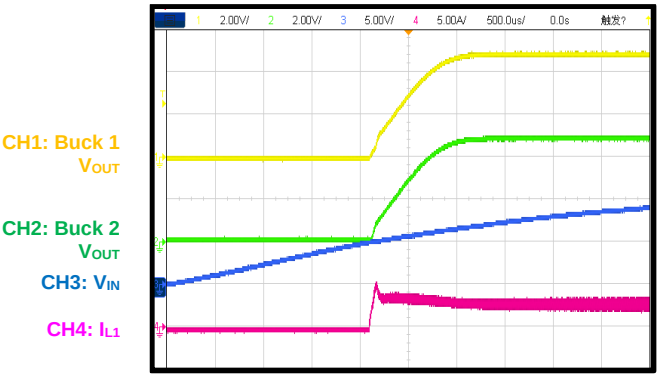
Start-Up

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 0A, forced PWM mode



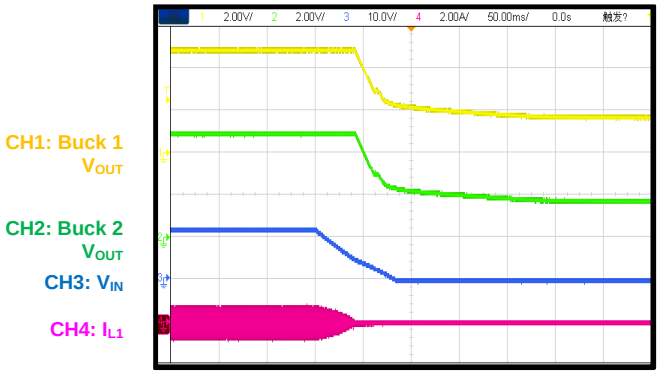
Start-Up

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A, forced PWM mode



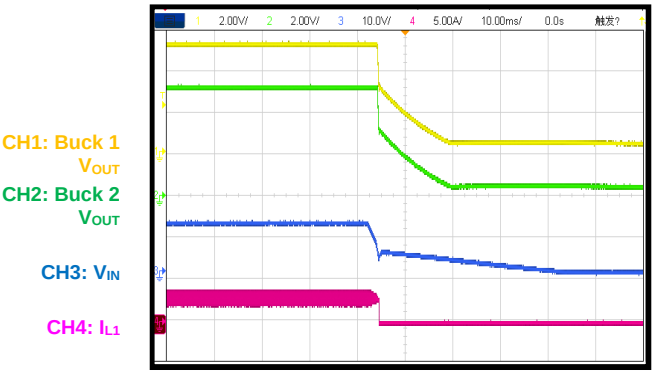
Shutdown

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 0A, forced PWM mode



Shutdown

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A, forced PWM mode

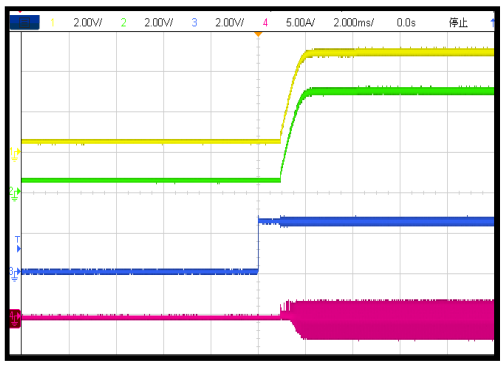


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

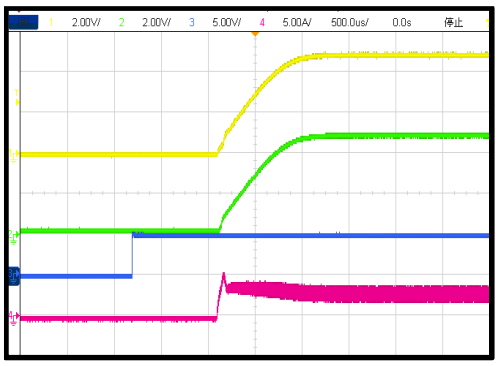
Start-Up through EN

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 0A, forced PWM mode



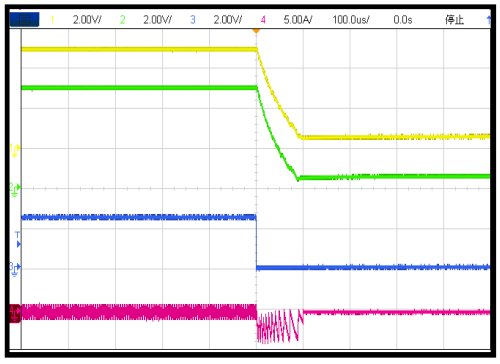
Start-Up through EN

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A, forced PWM mode



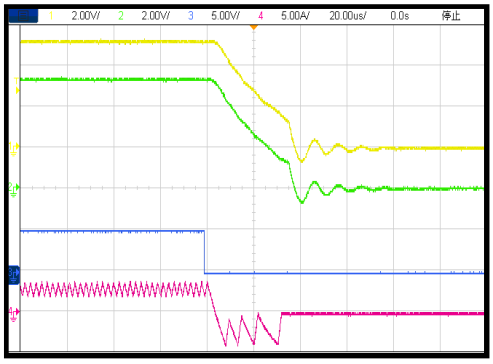
Shutdown through EN

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 0A, forced PWM mode



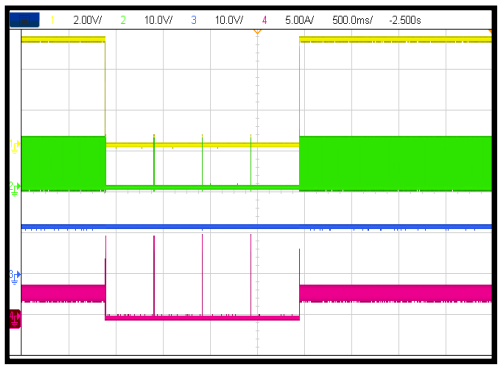
Shutdown through EN

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A, forced PWM mode



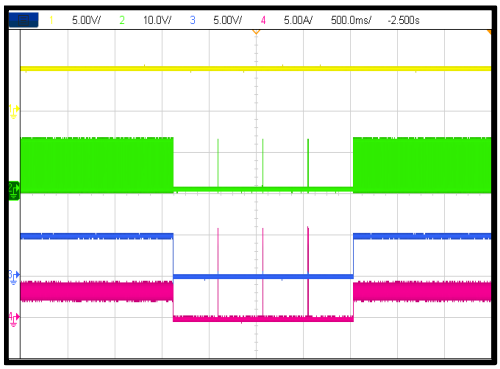
Buck 1 Output SCP Entry and Recovery

V_{IN} = 12V, buck 1 V_{OUT} = 5V, buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A



Buck 2 Output SCP Entry and Recovery

V_{IN} = 12V, buck 1 V_{OUT} = 5V, buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A

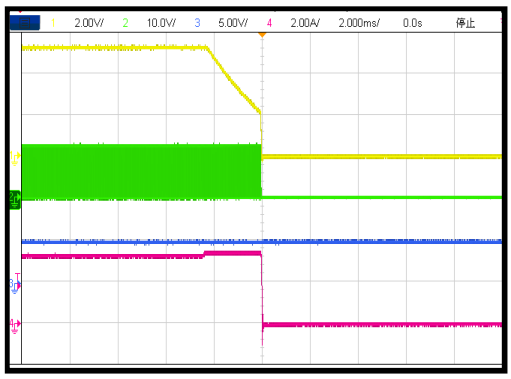


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

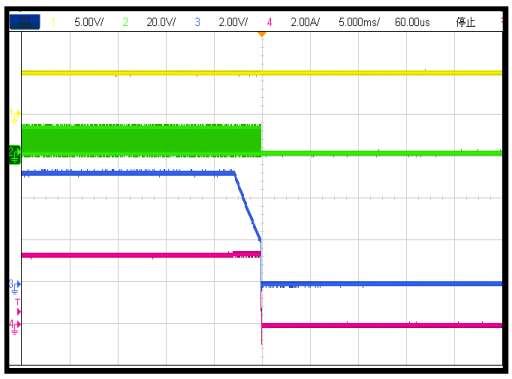
Buck 1 Output OCP Test

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT2} = 0A, I_{LIMIT} = 3.6A, I_{OUT1} ramps up slowly



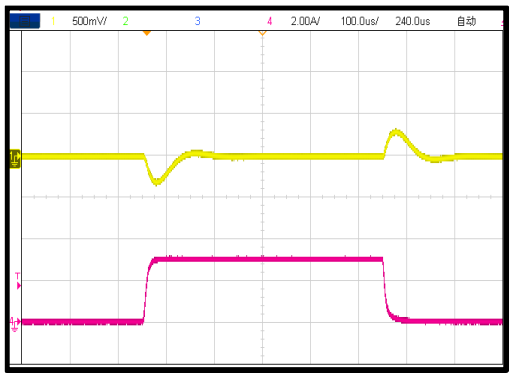
Buck 2 Output OCP Test

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = 0A, I_{LIMIT} = 3.6A, I_{OUT2} ramps up slowly



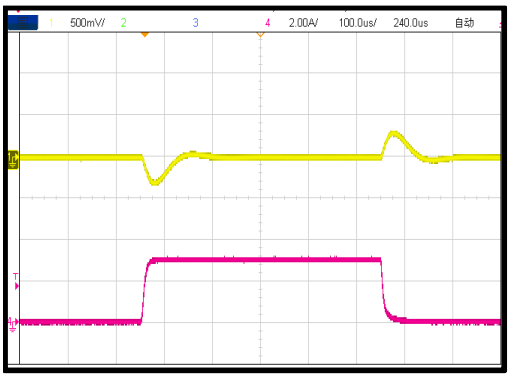
Load Transient (Buck 1 Output)

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = 0A to 3A, 2.5A/µs slew rate



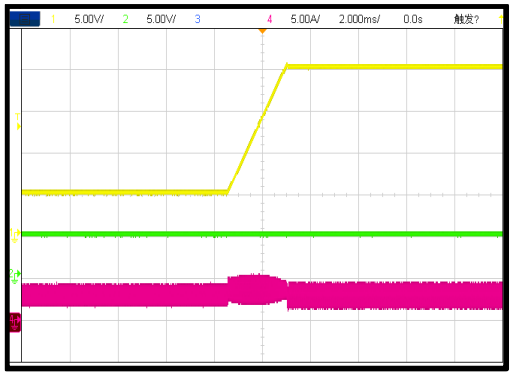
Load Transient (Buck 2 Output)

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT2} = 0A to 3A, 2.5A/µs slew rate



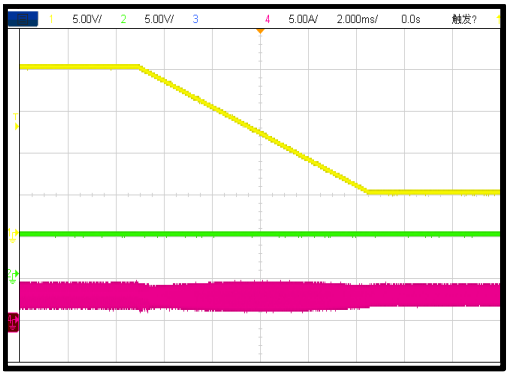
Buck 1 V_{OUT} Transition via the Digital Interface

V_{IN} = 24V, buck 2 V_{OUT} = 5V,
buck 1 V_{OUT} = 5V to 20V, I_{OUT1} = I_{OUT2} = 3A



Buck 1 V_{OUT} Transition via the Digital Interface

V_{IN} = 24V, buck 2 V_{OUT} = 5V,
buck 1 V_{OUT} = 20V to 5V, I_{OUT1} = I_{OUT2} = 3A

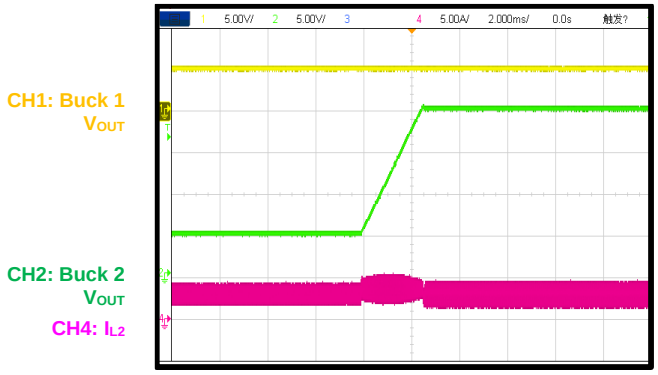


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

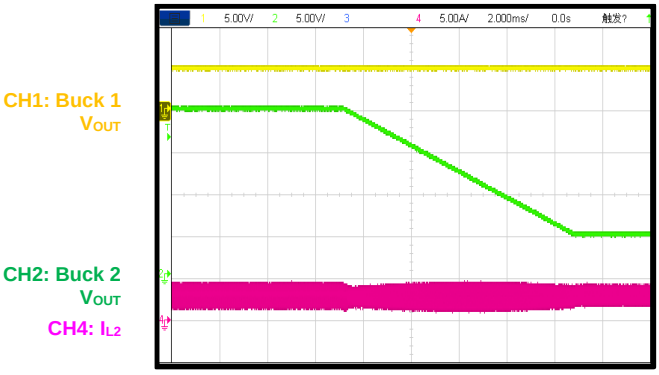
Buck 2 V_{OUT} Transition via the Digital Interface

V_{IN} = 24V, buck 1 V_{OUT} = 5V,
buck 2 V_{OUT} = 5V to 20V, I_{OUT1} = I_{OUT2} = 3A



Buck 2 V_{OUT} Transition via the Digital Interface

V_{IN} = 24V, buck 1 V_{OUT} = 5V,
buck 2 V_{OUT} = 20V to 5V, I_{OUT1} = I_{OUT2} = 3A



FUNCTIONAL BLOCK DIAGRAM

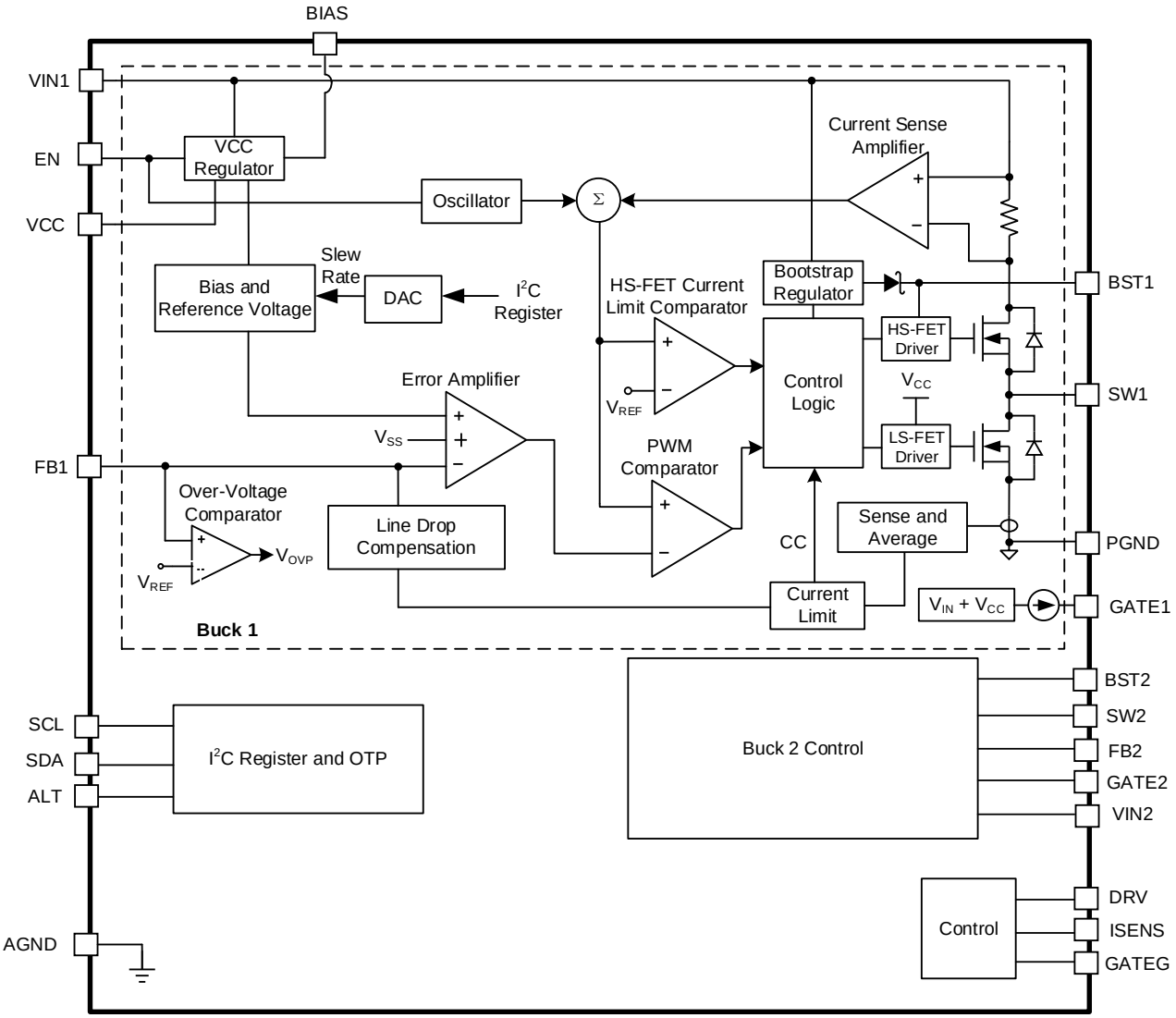


Figure 2: Functional Block Diagram

OPERATION

Buck Converters

The MP4255 integrates two dual-channel, monolithic, synchronous, rectified, step-down switch-mode converters with internal power MOSFETs. It offers a compact solution that can achieve a dual 3A or shared 6A of continuous output current (I_{OUT}) across a wide 4V to 36V input voltage (V_{IN}) range, with excellent load and line regulation.

Each step-down converter operates with fixed-frequency and peak current control mode to regulate the output voltage (V_{OUT}). There is an internal oscillator that generates two phase-shift reference clocks. Each reference clock initiates the pulse-width modulation (PWM) cycle of each channel, which turns on the integrated high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the comparator voltage (V_{COMP}). If the HS-FET turns off, it remains off until the next clock cycle begins.

Error Amplifier (EA) per Channel

The error amplifier (EA) compares the internal feedback voltage (V_{FB}) to the internal reference voltage (V_{REF}) and outputs V_{COMP}. V_{COMP} controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Bias and VCC Regulator

Most of the internal circuitry is powered by the internal VCC LDO regulator. The MP4255 has two internal regulators (LDO1 and LDO2) (see Figure 3).

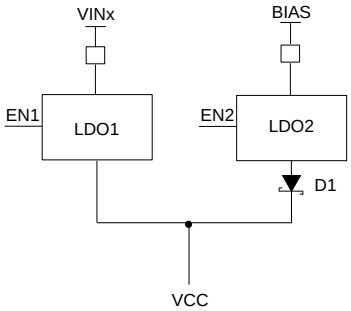


Figure 3: LDO Structure

LDO1 takes the VINx input and operates across the entire V_{IN} range. If V_{IN} exceeds 5V, the regulator output is in full regulation, and the VCC voltage (V_{CC}) is 5V. If V_{IN} drops below 5V, then the output degrades.

LDO2 is powered by the BIAS pin. Connect the BIAS pin to an external power supply (>4.8V). LDO2 turns on once the BIAS voltage (V_{BIAS}) exceeds 4.8V. If LDO2 is enabled, then LDO1 is disabled. For ≥5V output applications, connect BIAS to the output to improve efficiency. The diode (D1) between BIAS and the internal circuit is used for reverse current blocking. If the BIAS function is not used, connect the BIAS and ground pins.

Use an external 1µF ceramic decoupling capacitor to decouple VCC.

Enable (EN) Control

The MP4255 offers enable (EN) control via the EN pin, which has two different EN thresholds. If the EN voltage (V_{EN}) exceeds 0.7V, then VCC is enabled. If V_{EN} exceeds 1.6V, then the IC starts up and begins normal operation. EN is clamped internally via a 10V Zener diode (see Figure 4).

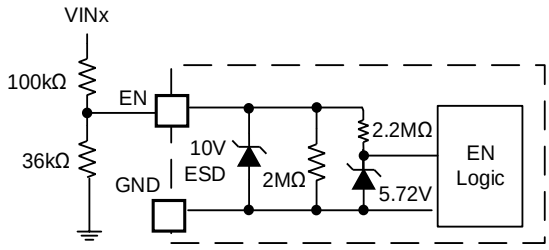


Figure 4: EN Circuit with a 10V Zener Diode

Connect the EN pin to the VINx and ground pins via two resistor dividers.

It is recommended to connect a 100kΩ resistor between the VINx and EN pins, and a 36kΩ resistor between the EN and ground pins. Do not place a >1nF capacitor on the EN pin.

The EN rising threshold is 1.6V, and the EN falling threshold is 1.4V. The V_{IN} rising threshold is 6.05V, and the V_{IN} falling threshold is 5.29V. This means that the EN circuit is enabled once V_{IN} exceeds 6.05V.

The V_{IN} start-up threshold (V_{IN_SU}) can be calculated with Equation (1):

$$V_{IN\_SU}(V) = V_{EN\_SU}(V) \times (1+\frac{R_{TOP}}{R_{BOT}}) = 6.05V \quad (1)$$

The V_{IN} shutdown threshold (V_{IN_SD}) can be calculated with Equation (2):

$$V_{IN\_SD}(V) = V_{EN\_SD}(V) \times (1+\frac{R_{TOP}}{R_{BOT}}) = 5.29V \quad (2)$$

If EN is connected directly to a voltage source without a pull-up resistor, limit the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

Under-Voltage Lockout (UVLO) Protection

Under-voltage lockout (UVLO) protection protects the IC from operating at an insufficient supply voltage by monitoring V_{IN} via the UVLO comparator. The UVLO rising threshold is 3.35V, and its falling threshold is 3.05V.

Internal Soft Start (SS)

Soft start (SS) prevents V_{OUT} from overshooting during start-up. Once the IC starts up, the internal circuitry generates an SS voltage (V_{SS}) that ramps up from 0V to 5V. If V_{SS} drops below V_{REF}, then the EA uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, then the EA uses V_{REF} as the reference.

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the low-side MOSFET (LS-FET) and the HS-FET until V_{SS} exceeds the V_{FB}.

Low-Dropout (LDO) Mode

The MP4255 has a low-dropout (LDO) function once V_{IN} reaches V_{OUT}. Once the minimum off time (t_{MIN_OFF}) is triggered, the on time (t_{ON}) is extended and the switching frequency (f_{SW}) decreases. If the maximum on time (t_{ON_MAX}) is triggered, then the MP4255 operates at maximum duty cycle (about 99.4%).

Constant-Current (CC) Mode Over-Current Protection (OCP)

The MP4255 senses the LS-FET current (I_{LS}) and uses this information to match the I_{OUT} amplitude. If I_{OUT} exceeds the set current limit (I_{LIMIT}), then the device enters constant-current (CC) limit mode. In this mode, the current amplitude is limited.

V_{OUT} decreases as the load resistance decreases until V_{FB} drops below the under-voltage (UV) threshold. If an over-current (OC) fault occurs, the MP4255 enters hiccup mode to periodically restart the part. Hiccup mode is especially useful if the output is dead shorted to ground, as it greatly reduces the average short-circuit current, reduces thermal issues, and protects the converter. The MP4255 exits hiccup mode once the OC fault is removed.

If V_{OUT} is set above 6.3V, then the hiccup UV threshold is 2.4V. If V_{OUT} is set below 5.5V, then the hiccup UV threshold is about 30% of V_{REF}.

Output Over-Voltage Protection (OVP)

The MP4255 provides output over-voltage protection (OVP). If V_{OUT} exceeds 120% of V_{REF}, then the HS-FET turns off. The LS-FET turns on to discharge V_{OUT} until I_{LS} reaches -3.6A, and then turns off. Once the next internal clock starts, the LS-FET turns on again and repeats this process. The MP4255 resumes normal operation once V_{FB} drops to 109% of V_{REF}.

Input Over-Voltage Protection (OVP)

The MP4255 provides input over-voltage protection (OVP). If both the output OVP and input OVP rising thresholds (39.5V) are triggered at the same time, the device shuts down. If V_{IN} drops below the input OVP falling threshold (37V), then the device starts up and resumes normal operation. The MP4255 continues operating while the input OVP warning threshold is triggered. The input OVP warning rising threshold is 37.5V, and the falling threshold is 35V.

Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor (C_{BST}) powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, and has a hysteresis of 150mV. The BST1 voltage (V_{BST1}) is regulated internally by V_{CC} via D2, M1, and C2 (see Figure 5).

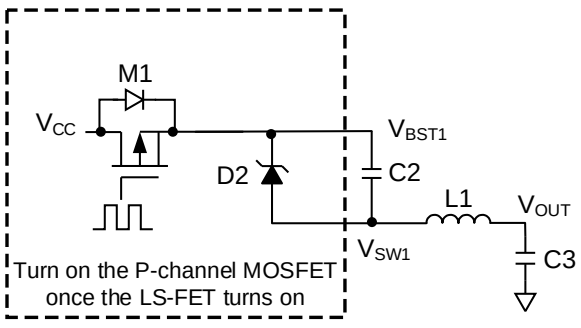


Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If digital interface operation is set up, and both VIN1 and EN exceed their respective rising thresholds, then the MP4255 starts up.

The reference block start up first to generate a stable V_{REF} and currents. Then the internal regulator starts up and provides a stable supply for the remaining circuitries.

Several events can shut down the chip: V_{EN} going low, V_{IN} going low, an digital interface operation off command, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rails are pulled down. The floating driver is not subject to this shutdown command.

EN Shutdown Discharge

Pull the EN pin low to have the buck converter enter output discharge mode. In output discharge mode, the internal soft-start capacitor (C_{SS}) starts to discharge. The part continues to operate in discharge mode until C_{SS} discharges to a low level.

In this mode, the LS-FET turns on and remains on until I_{LS} reaches the negative I_{LIMIT} (about -3.6A). The LS-FET turns on again once the next clock cycle begins.

Output Line Drop Compensation

The MP4255 is capable of compensating for a V_{OUT} drop (e.g. a high impedance caused by a long trace) to maintain a fairly constant load-side voltage. It uses the sensed load current through the LS-FET to sink a current (I_{COMP}) at the FB pin (see Figure 6).

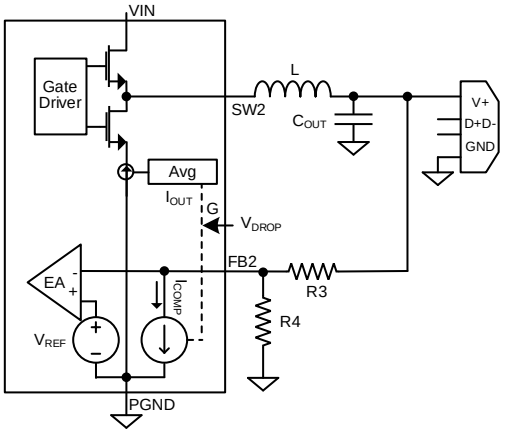


Figure 6: Line Drop Compensation

I_{COMP} can be calculated with Equation (3):

$$I_{COMP} = G \times I_{OUT} \quad (3)$$

Where G is the gain.

The gain is fixed internally, but can be configured via the digital interface.

V_{OUT} can be estimated with Equation (4):

$$v_{OUT} = \left(\frac{R3}{R4} + 1\right) \times v_{REF} + R3 \times G \times I_{OUT} \quad (4)$$

The line drop compensation amplitude (A_{LDC}) under certain I_{OUT} conditions can be calculated with Equation (5):

$$A_{LDC} = R3 \times G \times I_{OUT} \quad (5)$$

R3 can be used to adjust the line drop compensation amplitude.

GATEG Pin Logic

The MP4255 integrates a GATEG pin. Table 1 shows the GATEG logic table.

Table 1: GATEG Logic Table

Condition	GATEG Status
$V_{IN} < V_{IN\_UVLO\_RISING}$	Open drain
$V_{EN} < V_{EN\_UVLO\_RISING}$	Open drain
OPERATTION is off	Open drain
I_{SENS_RISING} >160mV	0

The second I_{LIMIT} through the current sense resistor (R_{CS}) is about 160mV.

Bus Voltage Isolation N-Channel MOSFET Driver

The GATE1 and GATE2 pins source a weak 20μA pull-up current to turn on Q1 and Q2, which turns on the bus voltage (V_{BUS}). The maximum GATEx driving voltage (25V) is equal to V_{IN1} + V_{CC} via an internal charge pump. A 300kΩ resistor (R7) or Zener diode is required to clamp the maximum Q1 gate-to-source voltage (V_{GS}) (see Figure 7 on page 20). In this configuration, the reverse current is blocked during shutdown. If EN is turned off via the digital interface, or the device is shut down via the EN pin, V_{BUS} is discharged before GATE1 and GATE2 turn off.

When the second current limit is triggered, (ISENS > 160mV), GATE1 and GATE2 also turn off.

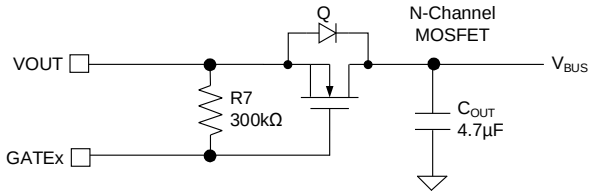


Figure 7: V_{BUS} Isolation Schematic for GATEx

System

Load Shedding vs. Temperature

The MP4255 monitors the die temperature and alerts the host if a thermal threshold is triggered.

The load shedding temperature threshold is configurable via the digital interface and one-time programmable (OTP) memory through the MFR_OT_WARN_LIMIT register.

Thermal Shutdown

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. The silicon die temperature is monitored internally. If the silicon die temperature exceeds the thermal shutdown threshold (about 160°C), then the device shuts down. Once the die temperature drops below 140°C, the part initiates an SS and resumes normal operation. The thermal shutdown threshold is configurable via the digital interface and OTP (set to 010b by default).

Digital Interface Timing

The digital interface is active once both V_{IN} and V_{EN} exceed their respective UVLO thresholds.

DIGITAL INTERFACE

Digital Serial Interface

The digital interface is an open-standard power management protocol that defines a means of communication with power conversion devices and other devices.

The digital interface is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage (V_{BUS}) externally while they are idle. While the lines are connected, a master device generates an SCL signal and device address, and arranges the communication sequence. This is based on the digital interface operation principles.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and end of the digital interface transfer. A start command (S) is defined as the SDA signal transitioning from high to low while SCL is high. A stop command (P) is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 8).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit.

Digital Interface Update Sequence

The MP4255 requires a start condition, a valid digital interface address, a register address byte, and a data byte for a single data update. The device acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid digital interface address selects the MP4255. The device performs an update on the falling edge of the LSB byte.

Digital Interface Message Format

Figure 9 on page 22 shows the digital interface message format. The white cells indicate that the bus host is actively driving the bus. The gray cells indicate that the MP4255 is driving the bus. Additional components are defined below:

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

“A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device.

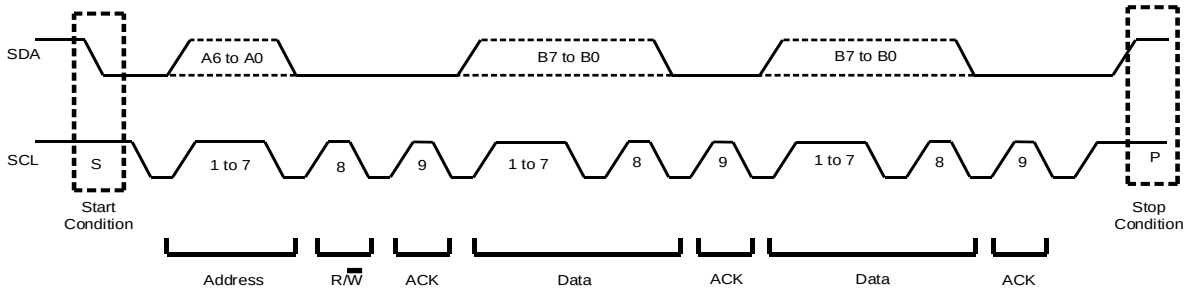


Figure 8: Data Transfer across the Digital Interface

a) Send Byte

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	P

b) Receive Byte

1	7	1	1	8	1	1
S	Slave Address	Rd	A	Command Code	A	P

c) Write Byte

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

d) Write Word

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

e) Read Byte

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	$\overline{A}$	P

f) Read Word

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	$\overline{A}$	P

Figure 9: Digital Interface Message Format

REGISTER DISCRIPTION

Digital Interface Register

Command Name	Command Code	Description	Type	Data Format	OTP	Default Value (11)
PAGE (1 page) (10)	0x00	See the PAGE section on page 25	R/W byte	Register	No	0
OPEARTION (2 pages)	0x01	On/off	R/W byte	Register	Yes	Off
CLEAR_FAULTS (1 page)	0x03		Send byte	Register	No	-
WRITE_PROTECT (1 page)	0x10		R/W byte	Register	No	-
STORE_USER_ALL (1 page)	0x15	Supports one-time programmable (OTP) memory once	Send byte	Register	No	-
RESTORE_USER_ALL (1 page)	0x16		Send byte	Register	No	-
VOUT_MODE (1 page)	0x20	V_{OUT} format and exponent (2^{-10})	R byte	Register	No	2^{-10} (0x16)
VOUT_COMMAND (2 pages)	0x21		R/W word	Linear L16	Yes	5V
VOUT_SCALE_LOOP (2 pages)	0x29		R/W word	Linear L11	Yes	0.08
STATUS_BYTE (2 pages)	0x78		R/W byte	Register	No	-
STATUS_WORD (2 pages)	0x79		R word	Register	No	-
STATUS_VOUT (2 pages)	0x7A		R byte	Register	No	-
STATUS_INPUT (1 page)	0x7C		R byte	Register	No	-
STATUS_TEMPERATURE (1 page)	0x7D		R byte	Register	No	-
STATUS_CML (1 page)	0x7E		R byte	Register	No	-
MFR_BUCK_CTRL1 (2 pages)	0xD0	PWM/PFM mode, output discharge, hiccup timer, output OVP, EN, and phase delay	R/W byte	Register	Yes	-
MFR_BUCK_CTRL2 (1 page)	0xD1		R/W byte	Register	Yes	-
MFR_CURRENT_LIMIT (2 pages)	0xD2	Sets I_{LIMIT} continuously	R/W byte	Register	Yes	3.6A
MFR_CTRL3 (1 page)	0xD3	Digital interface address, over-temperature protection threshold	R/W byte	Register	Yes	-
MFR_CTRL4 (1 page)	0xD4	Frequency, slew rate, over-temperature protection warning threshold	R/W byte	Register	Yes	-
MFR_CRC_ERROR_FLAG (1 page)	0xD5	Goes high if restore over-temperature protection data cyclic redundancy check (CRC) error occurs	R byte	Register	No	0
OTP_CONFIGURATION_CODE (1 page)	0xD6	Represents the device	R/W byte	Register	Yes	-
OTP_REVISION_NUMBER (1 page)	0xD7	1 byte (e.g. 0x01)	R/W byte	Register	Yes	-
MFR_STATUS_MASK (1 page)	0xD8	Masks the ALT# pin indication	R/W byte	Register	Yes	-

Notes:

10) "0xFF" means that both bucks are being controlled at the same time.
11) The default register values are for the default MP4255 configuration code (MP4255-0000).

DIGITAL INTERFACE REGISTERS

Data Format (Linear16 and Linear11)

Linear16 (L16) format is used for the V_{OUT} command (see Figure 10).

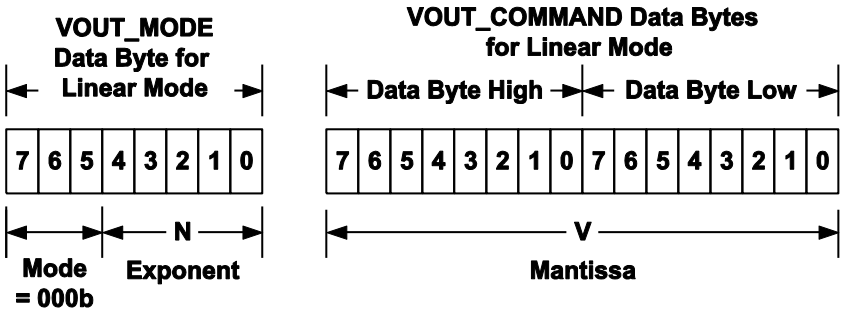


Figure 10: Linear16 Format

The MODE bits are set to 000b. The voltage can be calculated with Equation (6):

$$Voltage = V \times 2^{N} \quad (6)$$

Where Voltage is the parameter of interest (in volts), V is a 16-bit unsigned binary integer, and N is a 5-bit two's complement binary integer.

Linear11 (L11) format is used for other commands, such as the V_{OUT} scale loop, I_{OUT}, and temperature (see Figure 11).

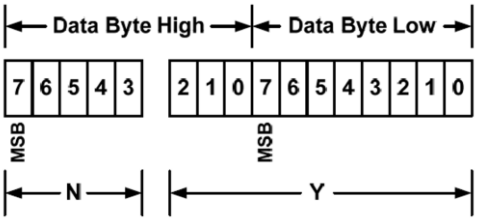


Figure 11: Linear11 Format

The relation between the 11-bit two's complement integer (Y), the 5-bit two's complement integer (N), and the real-world value (X) can be estimated with Equation (7):

$$X = Y \times 2^{N} \quad (7)$$

Devices that use the linear format should be able to accept and process any value of N.

PAGE

The PAGE register provides the ability to configure, control, and monitor the device via one address. Note that there are multiple outputs on the device. Set PAGE to 0xFF to control both channels simultaneously.

Bit	Description
7:1	Reserved
0	Selects the buck converter and output being controlled. 0: Buck 1 and output 1 are selected (default) 1: Buck 2 and output 2 are selected
7:0	Selects the buck converter and output being controlled. 0xFF: Both channels are controlled simultaneously

In regard to PAGE 0 mode and PAGE 1 mode, the registers that have one page can be read and written under PAGE 1 mode. For example, the CLEAR_FAULT register has one page, but it can be accessed and changed while PAGE is set to either 0 or 1.

If PAGE is set to 0xFF, then all of the buck 1 and buck 2 registers (including the MFR registers) are written to the same value once the digital interface master sends a write command.

OPERATION

The OPERATION register configures the operational state of the converter. Set OPERATION to 0x80 to enable the output. Set OPERATION to 0x00 or 0x40 to disable the output.

Bit	Description
7	Enables the converter's output. Note that the EN pin has a higher control priority than this bit. 0: Disabled (default) 1: Enabled
6:0	Reserved

CLEAR_FAULTS

The CLEAR_FAULTS register clears any fault bits that have been set. This command clears all bits in all of the status registers simultaneously. If the ALT signal is asserted, then this command also releases the device's ALT signal output.

If the fault is still present once the bit is cleared, then the fault bit is immediately reset, and the host is notified. This is a write-only command. There is no data byte for this command.

WRITE_PROTECT

The WRITE_PROTECT register controls writing to the digital interface device. This command provides protection against accidental changes. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Data Byte Value	Description
1000 0000	Disables all writes except for the WRITE_PROTECT command
0100 0000	Disable all writes except for the WRITE_PROTECT, OPERATION, and PAGE commands
0010 0000	Disable all writes except for the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands
0000 0000	Enable all writes to all commands (default)

STORE_USER_ALL

The STORE_USER_ALL register instructs the digital interface device to copy the entire contents of the operating memory to the matching locations in the OTP (non-volatile user store memory). Any items in operating memory that do not have matching locations in the user store are ignored.

The STORE_USER_ALL command can be used while the device is operating; however, the device rejects the digital interface write operation until OTP configuration is complete. During this process, the digital interface read command is still supported. While storing the user memory to the OTP, the device does a cyclic redundancy check (CRC) calculation, and stores the CRC result in a 1-byte OTP cell.

The output turns off during this operation. It starts up again after the OTP configuration is complete.

This command has no data bytes. This is a write-only command. Only the default MP4255 configuration (MP4255-0000) allows a one-time STORE_USER_ALL operation. Other configuration codes (MP4255-0000) are already OTP-configured in the factory, so they do not support user configurations.

RESTORE_USER_ALL

The RESTORE_USER_ALL register instructs the digital interface device to copy the entire contents of the OTP to the corresponding locations in the digital interface register. The values in the operating memory are overwritten by the value retrieved from the user store. Any items in user store that do not have corresponding locations in the digital interface register are ignored.

The RESTORE_USER_ALL command can be used while the device is operating; however, the device rejects the digital interface write operation until the OTP restoration process is complete. The digital interface read command is still supported during this process. While restoring the OTP data to the user memory, the device does a CRC calculation and compares the calculated result to the stored CRC result in the OTP cell. The OTP value is restored to the digital interface register once the values match one other.

The output turns off during this operation. It starts up again after the OTP configuration is complete.

This command has no data bytes. This is a write-only command.

VOUT_MODE

Command	VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	MODE			N				
Default Value	0	0	0	1	0	1	1	0

The MP4255 only supports linear mode. The mode bits are set to 000b by default. N is set to a fixed value of -10.

VOUT_COMMAND

The VOUT_COMMAND register sets V_{OUT}. It follows the L16 data format.

Command	VOUT_COMMAND															
Format	L16															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Data byte high								Data byte low							
Default Value (5V)	5120 decimal															

V_{OUT} can be calculated with Equation (8):

$$V_{OUT} = V \times 2^{-10} \quad (8)$$

Where V is a 16-bit unsigned binary integer of VOUT_COMMAN bits[15:0].

The actual V_{OUT} resolution or minimum step is 0.8mV/K. Where K is the value set by VOUT_SCALE_LOOP. For example, if the feedback resistor (R_{FB}) ratio (V_{OUT} / V_{FB}) equals 12.5, then K is 0.08. The real VOUT_COMMAND resolution is 10mV (see Figure 12).

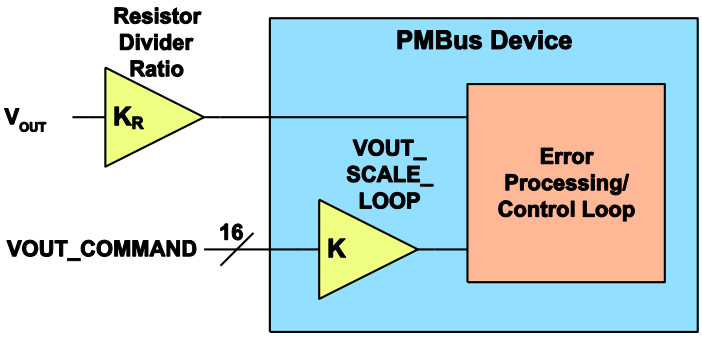


Figure 12: Resistor Divider Ratio

The internal V_{REF} is equal to V_{OUT} x K, and ranges between 0.1V and 1.63V, with a 0.8mV step.

VOUT_SCALE_LOOP

V_{OUT} is typically sensed via a resistor divider (R1 + R2) (see Figure 13).

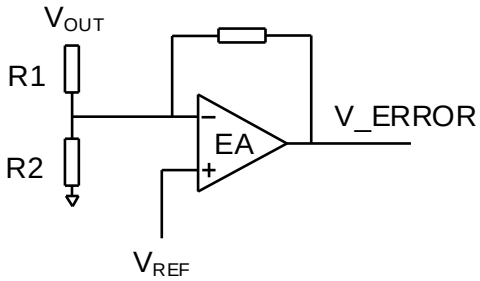


Figure 13: Output Voltage Sense

The resistor divider reduces V_{OUT} or scales down V_{OUT} so that the value supplied to the control circuit is equal to V_{REF}. The VOUT_SCALE_LOOP register has 2 data bytes encoded in linear format. It functions similar to the VOUT_COMMAND data format. The VOUT_SCALE_LOOP value is unitless.

Command	VOUT_SCALE_LOOP															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N					Data byte high			Data byte low							
Default Value (0.08)	-10 decimal, 10110 binary					82 decimal, 00001010010 binary										

VOUT_SCALE_LOOP is determined by V_{FB} / V_{OUT} or R2 / (R1 + R2). VOUT_SCALE_LOOP calculated with Equation (9):

$$VOUT\_SCALE\_LOOP = X \times 2^{-10} \quad (9)$$

Where X is an 11-bit, unsigned binary integer of VOUT_SCALE_LOOP bits[10:0] (0.08 by default).

In real applications, the user should always set the VOUT_SCALE_LOOP value equal to the external R2 / (R1 + R2) value.

To select VOUT_SCALE_LOOP, follow the steps below:

1. Confirm the maximum V_{OUT}. The MP4255's maximum V_{REF} is 1.638V. Once the maximum V_{OUT} is confirmed, there is a minimum feedback ratio value: (R1 + R2) / $R2_{MIN}$ = VOUT_MAX / 1.638.
2. Confirm the minimum V_{OUT} change resolution. The MP4255's minimum V_{REF} resolution is 0.8mV. The V_{OUT} change resolution is equal to 0.8mV x (R1 + R2) / R2. This means that the maximum feedback ratio (R1 + R2) / $R2_{MAX}$ = $V_{OUTMIN\_DVS\_STEP}$ / 0.8.
3. Choose a proper R2 / (R1 + R2) value that meets the requirements of step 1 and step 2.
4. Set the VOUT_SCALE_LOOP value according to step 3.

For example, in USB PD applications, a 3.3V to 21V output with a 20mV resolution is required for 60W PPS APDO. To obtain the required values, follow the steps below:

1. (R1 + R2) / $R2_{MIN}$ = 21V / 1.638V = 12.82
2. (R1 + R2) / $R2_{MAX}$ = 20mV / 0.8mV = 25
3. Choose (R1 + R2) / R2 = 15.7. Note that this value can be set to any value between 12.82 and 25.
4. VOUT_SCALE_LOOP = 0.0635 according to step 3. In real USB PD applications, set R1 to 93.1kΩ and R2 to 6.2kΩ for a higher V_{OUT} to meet MFI certification requirements.

STATUS_BYTE

The STATUS_BYTE register returns 1 byte of information with a summary of the most critical faults.

Bit	Name	Description
7	BUSY	A fault has been detected because the device is busy and unable to respond.
6	OFF	The OFF bit is asserted if the unit is not providing power to the output, regardless of the reason (e.g. the device is not turned on). This bit is a non-latch protection. It updates its status automatically without a CLEAR_FAULTS command.
5	VOUT_OV_FAULT	An output over-voltage (OV) fault has occurred.
4	IOUT_OC_FAULT	An output over-current (OC) fault has occurred. If the device reaches the CC limit, or if it enters hiccup mode, this bit is set.
3	VIN_UV_FAULT	An input under-voltage (UV) fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred (e.g. an over-temperature [OT] fault or a CRC error has occurred).
0	NONE_OF_THE_ABOVE	A fault or warning not listed in bits[7:1] has occurred.

STATUS_WORD

The STATUS_WORD register returns 2 bytes of information with a summary of the MP4255's fault conditions. Based on the information in these bytes, the host can receive more information by reading the corresponding status registers.

The low byte of STATUS_WORD is the same register as STATUS_BYTE.

Byte	Bit	Name	Description
Low	7:0	-	See the STATUS_BYTE register on page 28.
High	7	VOUT	A output fault or warning has occurred.
	6	IOUT/POUT	An I_{OUT} condition has occurred. If the device reaches the I_{LIMIT} or enters hiccup mode, this bit is set.
	5	INPUT	A V_{IN} fault or warning has occurred.
	4	OC_EXIT	This bit indicates whether I_{OUT} drops below I_{LIMIT}. If the IC exits CC mode before entering hiccup mode, this bit is set high. Hiccup mode recovery does not set this bit. Send a CLEAR_FAULTS command to reset this bit.
	3	PG_STATUS#	If the PG signal is present, this bit is ineffective. This bit is a non-latch protection. It updates its status automatically without a CLEAR_FAULTS command. If V_{OUT} drops below 80% of the set-up value, this bit is set to indicate that V_{OUT} is not good. If V_{OUT} exceeds 90% of the set-up value, this bit is cleared and V_{OUT} is power good. The PG signal rising edge is about 80%, and the falling edge is about 90%.
	2	RESERVED	Reserved.
	1	OTHER	A bit in the STATUS_OTHER register is set.
	0	UNKNOWN	A fault type not listed in bits[15:1] of the STATUS_WORD register has been detected.

Most bits remain set; however, there are two exceptions: the OFF bit and the PG_STATUS# bit. These bits always reflect the current state of the device and the PG signal (if present).

STATUS_VOUT

The STATUS_VOUT register returns 1 byte of data to indicate whether a fault or warning has occurred.

Bit	Name	Description
7	VOUT_OV_FAULT	Output OV fault indicator.
6	VOUT_OV_WARNING	Output OV warning indicator.
5	VOUT_UV_WARNING	Output UV warning indicator.
4	VOUT_UV_FAULT	Output UV fault indicator.
3:0	RESERVED	Reserved.

STATUS_INPUT

The STATUS_INPUT register returns 1 byte of data to indicate whether a fault or warning has occurred. This command is only one page.

Bit	Name	Description
7	VIN_OV_FAULT	Input OV fault indicator.
6	VIN_OV_WARNING	Input OV warning indicator.
5	VIN_UV_WARNING	Input UV warning indicator.
4	VIN_UV_FAULT	Input UV fault indicator.
3	RESERVED	Reserved.
2	RESERVED	Reserved.
1	RESERVED	Reserved.
0	RESERVED	Reserved.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE register returns 1 byte of data to indicate whether a fault or warning has occurred. This command is only one page.

Bits	Bit Name	Description
7	OT_FAULT	OT fault indicator. This bit's over-temperature threshold is set by MFR_OT_FAULT_LIMIT.
6	OT_WARNING	Over-temperature (OT) warning indicator. See Register Map section on page 33 for more details.
5	UT_WARNING	Under-temperature (UT) warning indicator. The UT warning threshold is -20°C, with a 10°C hysteresis.
4	UT_FAULT	UT fault indicator. The UT fault threshold is -40°C, with a 10°C hysteresis.
3	OT_WARNING_EXIT	The OT_WARNING falling edge sets this bit high. There is a 20°C hysteresis.
2:0	RESERVED	Reserved.

OTP-REGISTER VALUE SELECTED TABLE BY DEFAULT (MP4255-0001)

Table 2: OTP Default Values (MP4255-0001)

OTP Item	Description	Default Value
GATE1_2_EN	Enable/disable function	1 (enabled)
SLAVE_ADDRESS	Sets the digital interface slave address A5:A1 bit	61h
FREQ	Sets the switching frequency (f_{SW})	01 (420kHz)
SLEW_RATE	Sets the adjustable V_{REF} slew rate	10 (0.4mv/μs V_{REF} rising slew rate and 0.1mv/μs V_{REF} falling slew rate)
DITHER_ENABLE	Enables the frequency spread spectrum (FSS)	Disabled
DRV_VOLTAGE	DRV pin voltage (LDO output)	6V
PHASE_DELAY	Selects the buck's switching clock phase delay (from buck 1 to buck 2)	00 (0° phase delay)
OTP_THRESHOLD	Thermal shutdown threshold	170°C
OT_WARNING_ THRESHOLD	Thermal warning threshold	150°C
OTP configuration code	OTP configuration code (defined by MPS)	0x01

Table 3: OTP Default Values (MP4255-0001)

OTP Item	Description	CH1 Default Value	CH2 Default Value
OPERATION	Buck converter and output on/off control	On	On
Output voltage	Output voltage	5V	5V
V_{OUT} scale loop	1 / (V_{OUT} FB Ratio)	0.0635	0.0635
OUTPUT_OVP_EN	Enables output OVP	Enabled	Enabled
Hiccup timer	OCP off timer	500ms	500ms
OUTPUT_DISCHARGE_EN	Enables EN output discharge	Enabled	Enabled
PFM/PWM_MODE	Selects auto-PFM/PWM mode or forced PWM mode	Forced PWM mode	Forced PWM mode
Output current limit	Output current limit	5.2A	5.2A
Line drop compensation gain	Line drop compensation gain	0μA/A	0μA/A
VOUT_MSK	Masks the ALT pin indication for V_{OUT}	Masked	Masked
IOUT/POUT_MASK	Masks the ALT pin indication for I_{OUT} and P_{OUT}	Not masked	Not masked
INPUT_MSK	Masks the ALT pin indication for V_{IN}	Masked	Masked
TEMP_MSK	Masks the ALT pin indication for the IC temperature	Not masked	Not masked
PG_STATUS#_MSK	Masks the ALT pin indication for the PG status	Masked	Masked
PG_ALT_EDGE_MSK	Masks the ALT pin indication for the PG rising/falling edges	Masked	Masked
Other mask	Masks the ALT pin indication for other signals	Masked	Masked

OTP DEFAULT DESCRIPTIONS AND VALUES (MP4255-0002)

Table 4: OTP Default Values (MP4255-0002)

OTP Item	Description	Default Value
GATE1_2_EN	Enable/disable function	1 (enabled)
SLAVE_ADDRESS	Sets the digital interface slave address A5:A1 bit	61h
FREQ	Sets the switching frequency (f_{SW})	01 (420kHz)
SLEW_RATE	Sets the adjustable V_{REF} slew rate	10 (0.4mv/µs V_{REF} rising slew rate and 0.1mv/µs V_{REF} falling slew rate)
DITHER_ENABLE	Enables the frequency spread spectrum (FSS)	Disabled
DRV_VOLTAGE	DRV pin voltage (LDO output)	6V
PHASE_DELAY	Selects the buck's switching clock phase delay (from buck 1 to buck 2)	00 (0° phase delay)
OTP_THRESHOLD	Thermal shutdown threshold	170°C
OT_WARNING_ THRESHOLD	Thermal warning threshold	150°C
OTP configuration code	OTP configuration code (defined by MPS)	0x02

Table 5: OTP Default Values (MP4255-0002)

OTP Item	Description	CH1 Default Value	CH2 Default Value
OPERATION	Buck converter and output on/off control	Off	Off
Output voltage	Output voltage	5V	5V
V_{OUT} scale loop	1 / (V_{OUT} FB Ratio)	0.0635	0.0635
OUTPUT_OVP_EN	Enables output OVP	Enabled	Enabled
Hiccup timer	OCP off timer	500ms	500ms
OUTPUT_DISCHARGE_EN	Enables EN output discharge	Enabled	Enabled
PFM/PWM_MODE	Selects auto-PFM/PWM mode or forced PWM mode	Forced PWM mode	Forced PWM mode
Output current limit	Output current limit	5.2A	5.2A
Line drop compensation gain	Line drop compensation gain	0µA/A	0µA/A
VOUT_MSK	Masks the ALT pin indication for V_{OUT}	Masked	Masked
IOUT/POUT_MASK	Masks the ALT pin indication for I_{OUT} and P_{OUT}	Not masked	Not masked
INPUT_MSK	Masks the ALT pin indication for V_{IN}	Masked	Masked
TEMP_MSK	Masks the ALT pin indication for the IC temperature	Not masked	Not masked
PG_STATUS#_MSK	Masks the ALT pin indication for the PG status	Masked	Masked
PG_ALT_EDGE_MSK	Masks the ALT pin indication for the PG rising/falling edges	Masked	Masked
Other mask	Masks the ALT pin indication for other signals	Masked	Masked

DIGITAL INTERFACE REGISTER MAP

Register Map

Name	Reg	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MFR_BUCK_CTRL1	0xD0	R/W	DROPOUT_EN	LINE_DROP_COMPENSATION_GAIN			OUTPUT_OVP_EN	HICCUP_TIMER	OUTPUT_DISCHARGE_EN	PFM/PWM_MODE
MFR_BUCK_CTRL2	0xD1	R/W	GATE1_2_EN	-	PHASE_DELAY		-	DRV_VOLTAGE		DITHER_ENABLE
MFR_CURRENT_LIMIT	0xD2	R/W	CONSTANT_CURRENT_LIMIT (1A to 6.4A/50mA Step)							
MFR_CTRL3	0xD3	R/W	SLAVE_ADDRESS (A5:A1)					OTP_THRESHOLD		
MFR_CTRL4	0xD4	R/W	FREQ (250kHz, 420kHz, 1.1MHz, or 2.1MHz)		SLEW_RATE		-	OT_WARNING_THRESHOLD		
MFR_CRC_ERROR_FLAG	0xD5	R	-							CRC_ERROR
OTP_CONFIGURATION_CODE	0xD6	R/W	Determined by MPS							
OTP_REVISION_NUMBER	0xD7	R/W	Determined by MPS							
MFR_STATUS_MASK	0xD8	R/W	Masks the ALT pin indication if a fault or event occurs.							

Digital Interface Slave Address (A7:A1)

The default digital interface slave address is 61h.

Binary	Hex
1100 001 (default)	61h
Adjustable via the digital interface for A5:A1	Set by MFR_CTRL3_D, bits[7:3]

Register 0xD0 (MFR_BUCK_CTRL1)

Reset Value: Set by the OTP
Type: Read and write
Pages: 2 pages

Bits	Name	Description
D[7]	DROPOUT_EN	0: LDO mode disabled 1: LDO mode enabled once V_{IN} reached V_{OUT} (default)
D[6:4]	LINE_DROP_ COMPENSATION_ GAIN	000: 0μA/A 001: 0.5μA/A 010: 1μA/A (default for buck 1 and buck 2) 011: 2μA/A 100: 4μA/A 101: 8μA/A
D[3]	OUTPUT_OVP_EN	Enables output over-voltage protection (OVP). 0: Output OVP is disabled 1: Output OVP is enabled (default)
D[2]	HICCUP_TIMER	Sets the buck over-current protection (OCP) hiccup timer. 0: 500ms (default) 1: 2s
D[1]	OUTPUT_ DISCHARGE_EN	Enables the output discharge function. It is an active discharge. The LS-FET turns on to discharge the output until it reaches the negative I_{LIMIT}. Then the LS-FET turns off. It turns on again once a new clock cycle starts. This discharge function is operational until the soft-start signal drops to 0. 0: Disabled 1: Enabled (default)
D[0]	PFM/PWM_MODE	Selects the buck to operate in either auto-PFM/PWM mode or forced PWM mode. 0: Auto-PFM/PWM mode 1: Forced PWM mode (default)

Register 0xD1 (MFR_BUCK_CTRL2)

Reset Value: Set by the OTP
Type: Read and write
Pages: Only 1 page

Bits	Name	Description
D[7]	GATE1_2_EN	0: The GATE1 and GATE2 outputs are disabled for a lower I_Q 1: The GATE1 and GATE2 outputs are enabled (default)
D[5:4]	PHASE_DELAY	Selects the buck's switching clock phase delay (from buck 1 to buck 2). 00: 0° phase delay 01: 90° phase delay 10: 180° phase delay (default) 11: 270° phase delay
D[2:1]	DRV_VOLTAGE	Sets the DRV voltage (V_{DRV}). 00: 5.5V 01: 6V (default) 10: 6.2V 11: 6.5V
D[0]	DITHER_ENABLE	0: FSS is disabled (default) 1: FSS is enabled

Register 0xD2 (MFR_ CURRENT_LIMIT)

Reset Value: Set by the OTP
Type: Read and write
Page: 2 pages

The MFR_CURRENT_LIMIT register sets the buck output current limit (I_{OUT_LIMT}).

Name	IOUT_LIM							
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value (3.6A)	72 integer							

The real-world output over-current (OC) (I_{OUT_OC}) can be calculated with Equation (10):

$$I_{OUT\_OC}\ (A) = I_{OUT\_LIMIT} \times 0.05 \quad (10)$$

Where I_{OUT_LIMIT} is an 8-bit unsigned binary integer of IOUT_LIM, bitsD[7:0].

The I_{OUT_OC} minimum step is 50mA. The I_{OUT_OC} minimum I_{LIMIT} is 1A, and its maximum I_{LIMIT} is 6.4A. The device is not guaranteed to operate outside of this setting range.

Register 0xD3 (MFR_CTRL3)

Reset Value: Set by the OTP
Type: Read and write
Page: Only 1 page

The MFR_CTRL3 register sets the thermal shutdown threshold.

Bits	Name	Description
D[7:3]	SLAVE_ADDRESS	Sets the digital interface slave address A5:A1 bit. 1100 001: 61h (default)
D[2:0]	OTP_THRESHOLD	Sets the over-temperature (OT) threshold. 000: 140°C 001: 150°C 010: 160°C (default) 011: 170°C 100 to 111: Reserved

Register 0xD4 (MFR_CTRL4)

Reset Value: Set by the OTP
Type: Read and write
Page: Only 1 page

The MFR_CTRL4 register sets the thermal warning trigger threshold.

Bits	Name	Description
D[7:6]	FREQ	Sets the buck f_{SW}. 00: 250kHz 01: 420kHz (default) 10: 1.1MHz 11: 2.1MHz
D[5:4]	SLEW_RATE	Sets the adjustable V_{REF} slew rate. The default is 10 (VOUT_SLEW_RATE = VREF_SLEW_RATE x Feedback Ratio). 00: 0.08mv/µs V_{REF} rising slew rate; 0.02mv/µs V_{REF} falling slew rate 01: 0.16mv/µs V_{REF} rising slew rate; 0.04mv/µs V_{REF} falling slew rate 10: 0.4mv/µs V_{REF} rising slew rate; 0.1mv/µs V_{REF} falling slew rate (default) 11: 0.8mv/µs V_{REF} rising slew rate; 0.2mv/µs V_{REF} falling slew rate
D[2:0]	OT_WARNING_ THRESHOLD	Sets the over-temperature (OT) warning threshold. There is a 20°C hysteresis for recovery. The default value is 100. 000: 80°C 001: 90°C 010:100°C 011: 110°C 100: 120°C (default) 101: 130°C 110: 140°C 111: 150°C

Register 0xD5 (MFR_CRC_ERROR_FLAG)

Reset Value: Set by the OTP
Type: Read only
Page: Only 1 page

Bit	Bit Name	Description
D[0]	CRC_ERROR_FLAG	If a CRC error occurs while restoring the OTP memory to the digital interface, this bit is set to 1. If a CRC error occurs, the OTP data is discarded, and the system uses the default digital interface or OTP register value.

Register 0xD8 (MFR_STATUS_MASK)

Reset Value: Set by the OTP
Type: Read and write
Page: 2 pages

The MFR_STATUS_MASK register can only mask the ALT pin behavior; the STATUS register still indicates each event.

Bit	Bit Name	Description
7	VOUT_MSK	0: Not masked (default) 1: Masked
6	IOUT/POUT_MSK	IOUT_OC_FAULT, IOUT/POUT, and OC_EXIT mask bit. 0: Not masked (default) 1: Masked
5	INPUT_MSK	0: Not masked 1: Masked (default)
4	TEMP_MSK	Temperature-related mask bit. 0: Not masked (default) 1: Masked
3	PG_STATUS#_MSK	High-level PG mask bit. 0: Not masked (default) 1: Masked
2	PG_ALT_EDGE_MSK	0: Not masked (the ALT pin indicates both the PG_STATUS# rising and falling edges) (default) 1: Masked (he ALT pin only indicates the PG_STATUS# falling edge, which means V_{OUT} has gone from a suboptimal to good transition)
1	BUSY_FAULT_MASK	0: Not masked (default) 1: Masked
0	CML_FAULT_MASK	0: Not masked (default) 1: Masked

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% greater than the maximum load current (I_{LOAD_MAX}). Select an inductor with a small DC resistance for high efficiency. The inductance (L_1) can be calculated with Equation (11):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (11)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current (ΔI_L) to be approximately 30% of I_{LOAD_MAX}. The maximum inductor peak current (I_{L_MAX}) can be estimated with Equation (12):

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (12)$$

If V_{IN} is 24V and V_{OUT} is 20V, L_1 should be 8µH. For automotive input application and PD applications, choose ΔI_L to be approximately 30% to 50% of I_{LOAD_MAX}. Table 6 shows the recommended inductor values for common switching frequencies (where D_{MAX} at ΔI_L is 30% to 50% of I_{OUT_MAX}).

Table 6: Recommended Inductor Values for Common f_{SW}

f_{SW}	V_{IN} (V)	Buck 1 and Buck 2 (V)	I_{OUT} (A)	L (µH)
250kHz	12	5	3	8.2
420kHz	12	5	3	4.7
1.1MHz	12	5	3	2.2
2.1MHz	12	5	3	1
250kHz	24	20	3	10
420kHz	24	20	3	8.2
1.1MHz	24	20	3	2.2
2.1MHz	24	20	3	1

It is recommended to use a fully shielded inductor to reduce EMI.

Selecting the Buck Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients. For CLA applications, a 100µF electrolytic capacitor and two 10µF ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the C1 (I_{C1}) can be calculated with Equation (13):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (13)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be estimated with Equation (14):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (14)$$

For simplification, choose an input capacitor with a RMS current rating greater than half of I_{LOAD_MAX}. C1 can be electrolytic, tantalum, or ceramic.

When using electrolytic capacitors, place two additional high-quality ceramic capacitors as close to VIN as possible. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (15):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (15)$$

Selecting the Buck Output Capacitor (C2)

The device requires an output capacitor (C2) to maintain the DC V_{OUT}. Calculate the output voltage ripple with Equation (16):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (16)$$

Where L_1 the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (17):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (17)$$

The MP4255's loop compensation is optimized for ceramic output capacitors.

Four 22µF ceramic output capacitors are recommended for good loop stability and transient response. The bandwidth is about 1/10 of the switching frequency (f_{SW}), with a >45° phase margin.

For polymer capacitor designs, the ESR zero frequency should exceed the internal, high-frequency compensation pole. The recommended ESR can be calculated with Equation (18):

$$ESR = 1 / (2 \times \pi \times C_{OUT} \times f_{SW}) \quad (18)$$

Table 7 shows the recommended input and output capacitor values at V_{IN} = 12V.

Table 7: Recommended Input and Output Capacitor Values (V_{IN} = 12V) (12)

Input Capacitor (4 x 22µF + 2 x 0.1µF)	Output Capacitor (4 x 22µF + 0.1µF)
Ceramic, 22µF, 25V	Ceramic, 22µF, 25V
Ceramic, 100nF, 25V	Ceramic, 100nF, 10V

Table 8 shows the recommended input and output capacitor values at V_{IN} = 12V.

Table 8: Recommended Input and Output Capacitor Values (V_{IN} = 24V) (13)

Input Capacitor (100µF + 4 x 10µF + 2 x 0.1µF)	Output Capacitor (100µF + 22µF + 4.7µF)
Electrolytic, 100µF, 35V	Electrolytic, 100µF, 25V, <50mΩ ESR
Ceramic, 10µF, 35V	Ceramic, 22µF, 25V
Ceramic 100nF, 50V	Ceramic, 4.7µF, 25V

Notes:

12) f_{SW} = 420kHz, V_{IN} = 12V, buck 1 and buck 2 = 5V/9V, and I_{OUT} = 3A.

13) f_{SW} = 420kHz, V_{IN} = 24V; buck 1 and buck 2 = 5V, 9V, 15V, or 20V; and I_{OUT} = 3A.

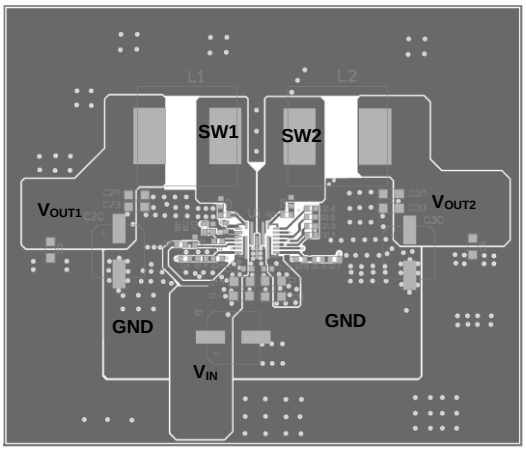
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 14 and follow the guidelines below:

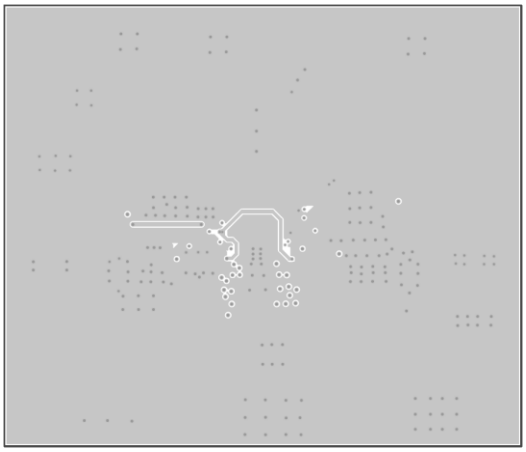
1. Use short, direct, and wide traces to connect VOUTx.
2. Connect the output filter on GND.
3. If required, place multiple vias on GND.
4. Use a large copper plane for the PGND connection.
5. Place multiple vias on PGND to improve thermal dissipation.
6. Connect AGND and PGND.
7. Place the ceramic input decoupling capacitors as close to VIN1, VIN2, and PGND as possible to reduce EMI.
8. Place a 0.1µF ceramic capacitors close to each VIN pin (VIN1 and VIN2).
9. Place the input filter on the bottom layer to reduce EMI.
10. Place the VCC decoupling capacitor as close to VCC as possible.

Note:

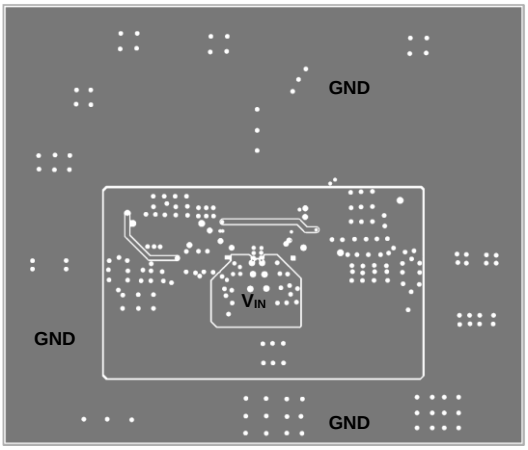
14) The recommended PCB layout is based on Figure 15 on page 41.



Top Layer



Mid-Layer



Bottom Layer

Figure 14: Recommended PCB Layout (14)

TYPICAL APPLICATION CIRCUIT

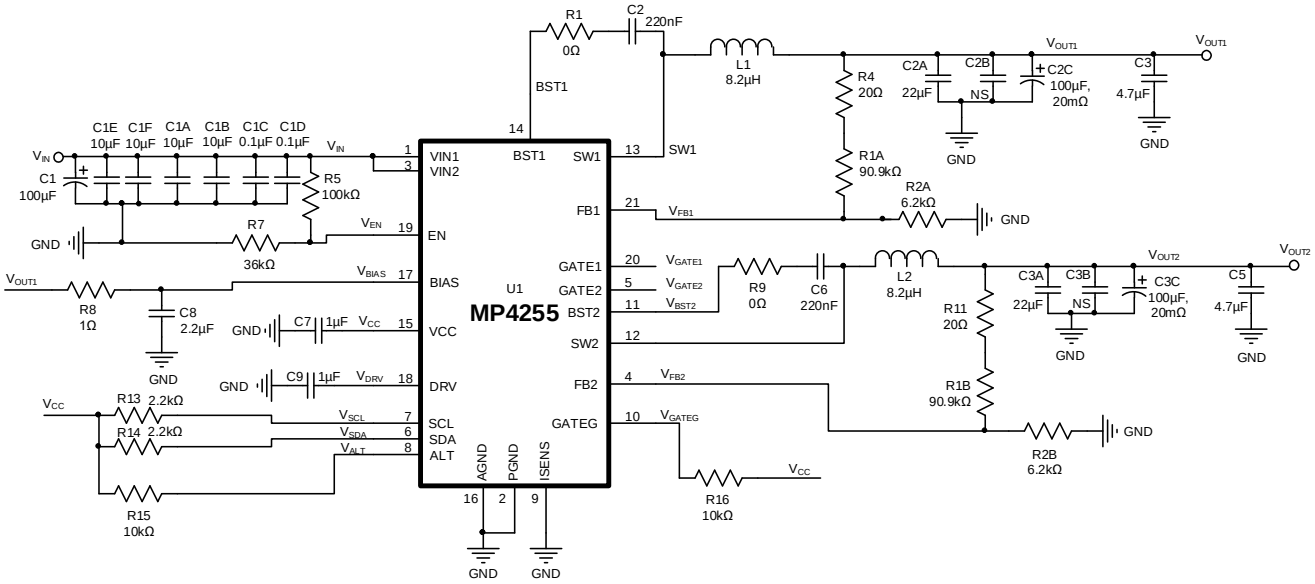
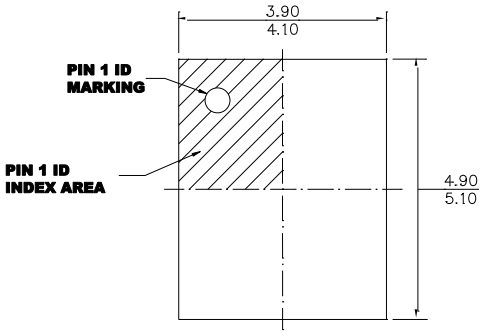


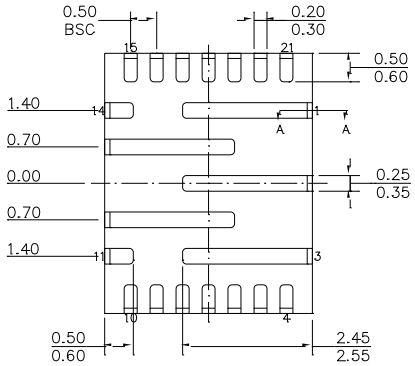
Figure 15: Typical Application Circuit (V_{IN} = 24V, V_{OUT1} = V_{OUT2} = 3.3V to 21V, Default Configuration)

PACKAGE INFORMATION

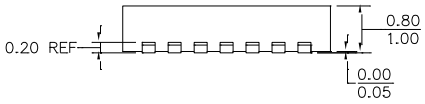
QFN-21 (4mmx5mm) with Wettable Flanks



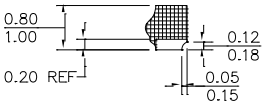
TOP VIEW



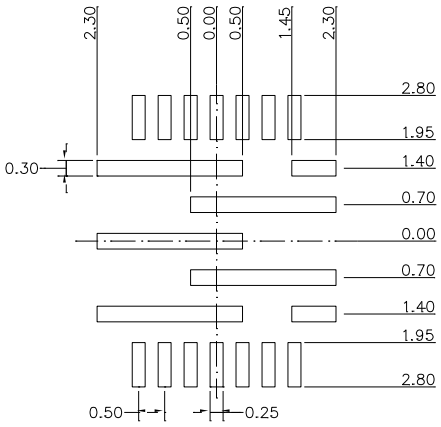
BOTTOM VIEW



SIDE VIEW



SECTION A-A

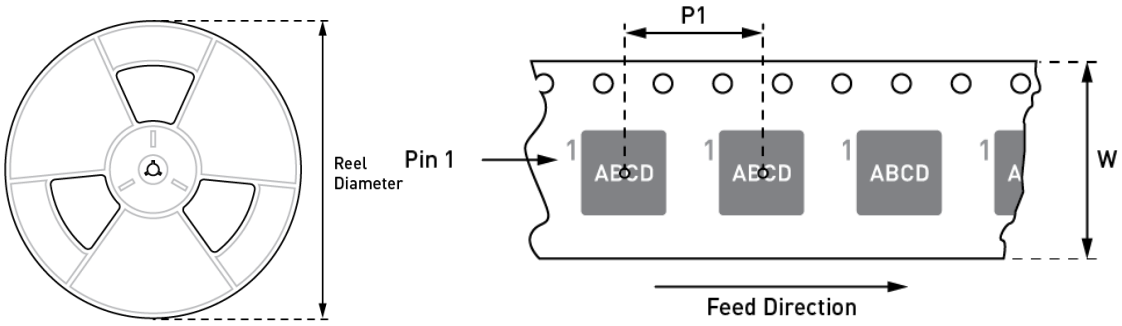


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1~3 AND PIN12~13 HAVE THE SAME LENGTH AND WIDTH.
2)ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4255GVE-xxxx-Z	QFN-21 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/31/2023	Initial Release	-