MP3439

5.2V, 3A, Dual-Phase Boost Converter with Output Disconnect and I²C Interface

DESCRIPTION

The MP3439 is a high-efficiency, synchronous, dual-phase boost converter with an output disconnect function.

The MP3439 adopts constant-on-time (COT) control topology to provide fast transient response. The integrated P-channel synchronous MOSFETs improve efficiency and disconnect the output from the input during shutdown. Dual-phase switching with high frequency provides a small-size power solution for up to 3A of load current (I_{LOAD}) from a 1-cell lithium battery.

The MP3439 provides a 400kHz I²C interface that can configure the output voltage (V_{OUT}), current limit, and light-load operation. It also supports frequency spread spectrum (FSS) to improve EMI performance.

The MP3439 is available in a small-size WLCSP-20 (1.75mmx2.10mm) package.

FEATURES

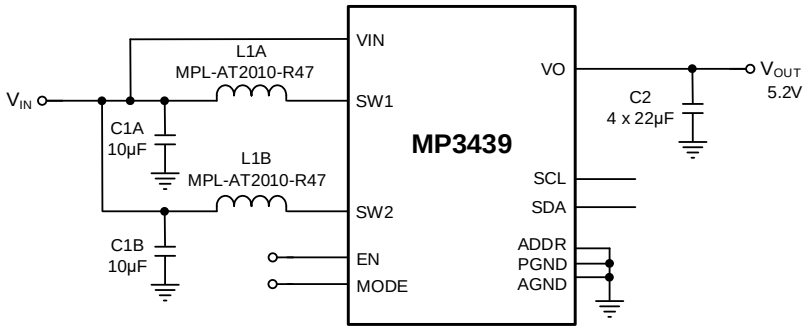
- 2.7V to 5V Input Voltage (V_{IN}) Range
- 5V to 5.5V I²C-Configurable Output Voltage (V_{OUT}) with 25mV Resolution.
- 2.5A and 3.5A Selectable Switching Valley Current Limit via the I²C
- 23µA Quiescent Current (I_Q)
- 1MHz and 2MHz Selectable Switching Frequency (f_{SW})
- Dual-Phase Boost Switching with 180° Shift
- 24mΩ and 29mΩ Internal FETs for Each Phase
- Constant-On-Time (COT) Control for Fast Transient Response
- Pulse-Skip Mode (PSM), Ultrasonic Mode (USM), and Forced Continuous Conduction Mode (FCCM) via the I²C or MODE Pin Setting
- Frequency Spread Spectrum (FSS) for Improved EMI
- Over-Current Protection (OCP), Short-Circuit Protection (SCP), Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP)
- True V_{OUT} Disconnect Function
- Available in a WLCSP-20 (1.75mmx2.10mm) Package

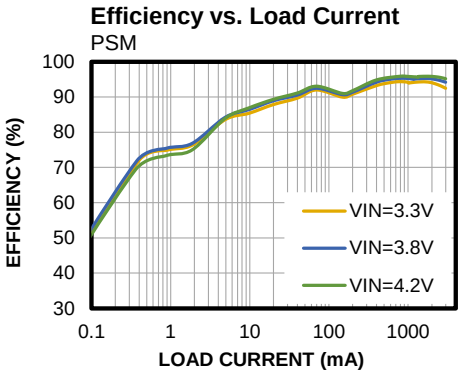
MPL Optimized Performance with MPS Inductor MPL-AT Series

APPLICATIONS

- Battery-Powered Products
- Power Banks and Battery Backup Units
- USB Power Supplies
- Consumer Electronic Accessories

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3439GC-xxxx**	WLCSP-20 (1.75mmx2.10mm)	*See Below*	1
MP3439GC-0000			

*For Tape & Reel, add suffix -Z (e.g. MP3439GC-xxxx-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the one-time programmable (OTP) memory. The default code is “0000”. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code. MP3439GC-0000 is the default version.

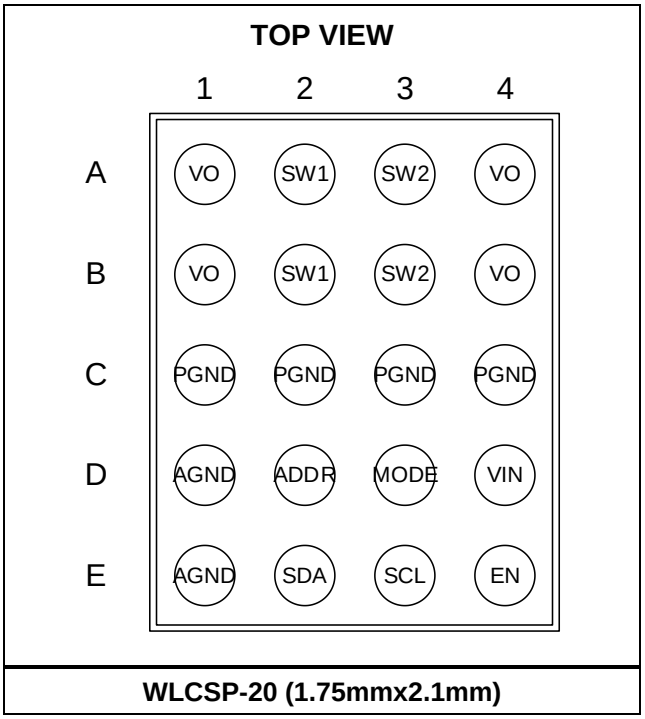
TOP MARKING

$\overline{\text{LEY}}$

LLL

LE: Product code of MP3439
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



WLCSP-20 (1.75mmx2.1mm)

PIN FUNCTIONS

Pin #	Name	Description
A1, A4, B1, B4	VO	**Boost power output.** Place the output capacitor (C_{OUT}) close to the VO and PGND pins. The VO pins are not connected together in the IC; these pins must be connected together on the PCB.
A2, B2	SW1	**Switch node for phase 1.** Connect the phase 1 power inductor to the SW1 pin.
A3, B3	SW2	**Switch node for phase 2.** Connect the phase 2 power inductor to the SW2 pin.
C1, C2, C3, C4	PGND	**Power ground.** The PGND pins are not connected together in the IC; these pins must be connected together on the PCB.
D1, E1	AGND	**Analog ground for the internal signal.**
D2	ADDR	**Address setting for the I^2C.** The ADDR pin is detected during start-up, and the pin status is latched to the IC. After start-up, changes to ADDR does not affect the MP3439's I^2C address.
D3	MODE	**Light-load operation selection.** Pull the MODE pin low to set light-load switching in pulse-skip mode (PSM). Pull MODE to about 0.5V to set light-load switching in ultrasonic mode (USM). Pull MODE high to set light-load switching in forced continuous conduction mode (FCCM). Pull down MODE internally to AGND via a resistor. MODE can also be masked using the internal MODE_PIN_ENABLE bit. For more details, see the Light-Load Operation section on page 17.
D4	VIN	**Power supply input.**
E2	SDA	**I^2C serial data.**
E3	SCL	**I^2C serial clock.**
E4	EN	**Chip enable control.** Pull the EN pin high to enable the MP3439; pull EN low to disable the MP3439. Pull down EN internally to AGND via a resistor.

ABSOLUTE MAXIMUM RATINGS (1)

SW1, SW2 .....-0.3V to +6.5V (8V for <5ns)
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
WLCSP-20 (1.75mmx2.10mm)..... 3.67W (4)
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Operating temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged-device model (CDM) 1000V

Recommended Operating Conditions (3)

Operating input voltage (V_{IN}) range ...2.7V to 5V
Output voltage (V_{OUT}).....5V to 5.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

WLCSP-20 (1.75mmx2.10mm)		
EVL3439-C-00A (4)	34	6 °C/W
JESD51-7 (5)	62	14.4 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EVL3439-C-00A, a 2-layer PCB (63mmx63mm).
5) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.8V, V_{OUT} = 5.2V, T_J = -40°C to +125°C [6], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Shutdown current	I_{SD}	V_{EN} = 0V, measured on the VIN pin, $T_J \le 85°C$		0.1	1	µA
Quiescent current	I_Q	V_{EN} = V_{IN} = 3.8V, V_{OUT} = 5.3V, no switching, no load, measured on the VO pin, $T_J \le 85°C$		23	35	µA
		V_{EN} = V_{IN} = 3.8V, V_{OUT} = 5.3V, no switching, no load, measured on VIN, $T_J \le 85°C$		7	9	µA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_R}$			2.4	2.6	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_F}$		2	2.15		V
Enable (EN) Control						
EN logic high threshold	V_{EN_H}				1	V
EN logic low threshold	V_{EN_L}		0.4			V
EN pin leakage current	I_{EN}	V_{EN} = 1.2V		1.2		µA
EN turn-on delay [7]	t_{EN}	EN on to linear charge mode		240		µs
Power Switching						
Switching frequency	f_{SW}	FREQ bit = 1	1.8	2	2.2	MHz
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			29		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			24		mΩ
LS-FET leakage		V_{EN} = 0V, V_{SW1} or V_{SW2} = 5.5V, float VO, $T_J \le 85°C$		0.1	1	µA
HS-FET leakage		V_{EN} = 0V, V_{SW1} or V_{SW2} = 0V, VO = 5.5V, $T_J \le 85°C$		0.1	1	µA
LS-FET minimum on time [7]	t_{ON_MIN}			40		ns
Switching Frequency Spread Spectrum						
f_{SW} spread spectrum upper range		FSS_AMP bit = 0 FREQ bit = 1		2.12		MHz
f_{SW} spread spectrum lower range		FSS_AMP bit = 0 FREQ bit = 1		1.88		MHz
Spread spectrum modulation frequency [7]		FSS_FSW bit = 1		10		kHz
Current Limit						
HS-FET switching valley current limit	I_{LIMIT_VALLY}	CURRENT_LIMIT bit = 1, for both phases	3	3.5	4	A
HS-FET zero-current detection (ZCD) threshold	I_{ZCD}	Pulse-skip mode (PSM)	0	150	300	mA
		Forced continuous conduction mode (FCCM)		-1.6		A

ELECTRICAL CHARACTERISTICS (*continued*)

V_{IN} = V_{EN} = 3.8V, V_{OUT} = 5.2V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pre-charge current limit		For each phase of the P-channel MOSFET, V_{IN} = 3.8V, V_{OUT} = 0V	0.35	0.5		A
		For each phase of the P-channel MOSFET, V_{IN} = 3.8V, V_{OUT} = 2.5V	0.7	1		A
Short-circuit protection (SCP) latch-off blank time (7)		Maximum linear charge mode time		8		ms
Output Voltage						
Output voltage	V_{OUT}	VOUT bits = 0b10000, T_J = 25°C	5.12	5.2	5.28	V
		VOUT bits = 0b10000, T_J = -40°C to +125°C	5.1	5.2	5.3	V
Output over-voltage protection (OVP)	V_{OVP_R}		5.6	5.8	6	V
Output OVP hysteresis	V_{OVP_HYS}			50		mV
V_{OUT} slew rate during boost soft-start (7)				6		V/ms
Soft-start time (7)		From EN high to V_{OUT} regulation, V_{IN} = 3.8V, V_{OUT} = 5.2V, C_{OUT} = 88µF, I_{OUT} = 0A		0.8	1	ms
Mode Selection						
PSM setting voltage					0.24	V
Ultrasonic mode (USM) setting voltage (8)			0.4	0.5	0.6	V
FCCM setting voltage			0.96			V
USM frequency				30		kHz
MODE pin leakage current		V_{MODE} = 1.2V		1		µA
Thermal Protection						
Thermal shutdown (7)	T_{STD}			150		°C
Thermal shutdown hysteresis (7)	T_{STD_HYS}			20		°C
I^2C Specification						
Slave address 1	V_{ADD_1}	Pull the ADDR pin low to AGND/PGND		61H		
Slave address 2	V_{ADD_2}	Float ADDR		62H		
Slave address 3	V_{ADD_3}	Pull ADDR high to V_{IN}		64H		
ADDR pin leakage current		Connect to 0V and 5V, during steady state	-0.1	0	0.1	µA
SCL/SDA input logic high	V_{IH}		0.84			V
SCL/SDA input logic low	V_{IL}				0.36	V
SDA output voltage logic low	V_{OUT_L}	Sink 3mA			0.24	V
SCL clock frequency	f_{SCL}			400		kHz
SCL high time (7)	t_{HIGH}		0.6			µs

ELECTRICAL CHARACTERISTICS (*continued*)

V_{IN} = V_{EN} = 3.8V, V_{OUT} = 5.2V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCL low time (7)	t_{LOW}		1.3			µs
Data set-up time (7)	t_{SU_DAT}		100			ns
Data hold time (7)	t_{HD_DAT}		0		0.9	µs
Set-up time for (repeated) start condition (7)	$t_{SU.STA}$		0.6			µs
Hold time for (repeated) start condition (7)	$t_{HD.STA}$		0.6			µs
Bus free time between a start and stop condition (7)	t_{BUF}		1.3			µs
Set-up time for stop condition (7)	t_{SU_STO}		0.6			µs
Rising time of SCL and SDA (7)	t_R		20 + 0.1 x C_B		300	ns
Falling time of SCL and SDA (7)	t_F		20 + 0.1 x C_B		300	ns
Pulse width of suppressed spike (7)	t_{SP}		0		50	ns
Capacitance for each bus line (7)	C_B				400	pF

Notes:

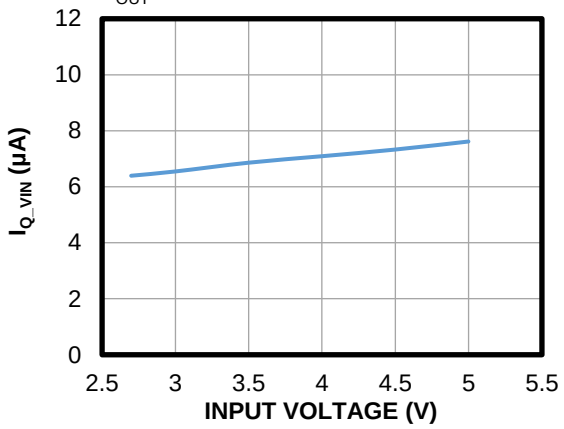
6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by sample characterization. Not tested in production.
8) For USM, add an external voltage on the MODE pin within this range.

TYPICAL CHARACTERISTICS

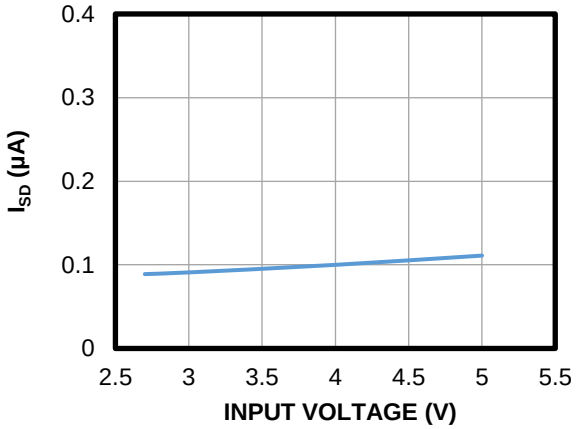
V_{IN} = 3.8V, V_O = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

VIN Quiescent Current vs. Input Voltage

V_{OUT} = 5.3V

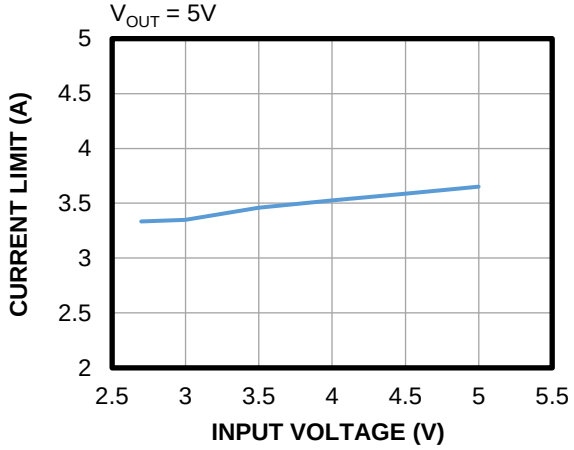


Shutdown Current vs. Input Voltage



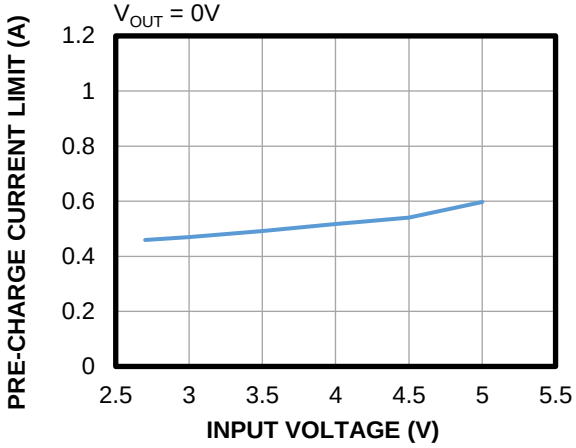
SW1/SW2 Current Limit vs. Input Voltage

V_{OUT} = 5V

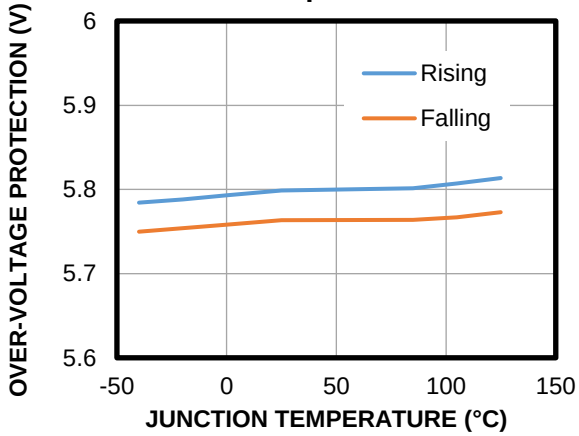


SW1/SW2 Pre-Charge Current Limit vs. Input Voltage

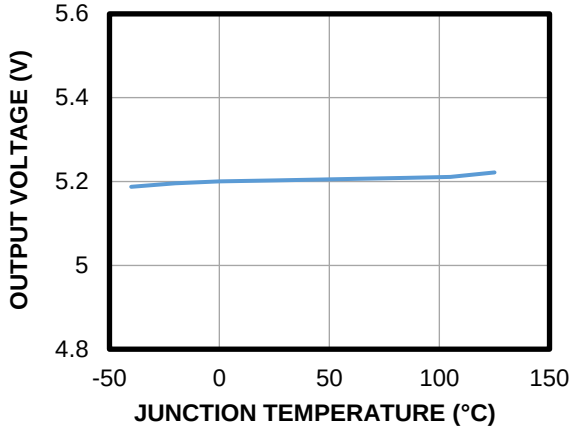
V_{OUT} = 0V



Over-Voltage Protection vs. Junction Temperature



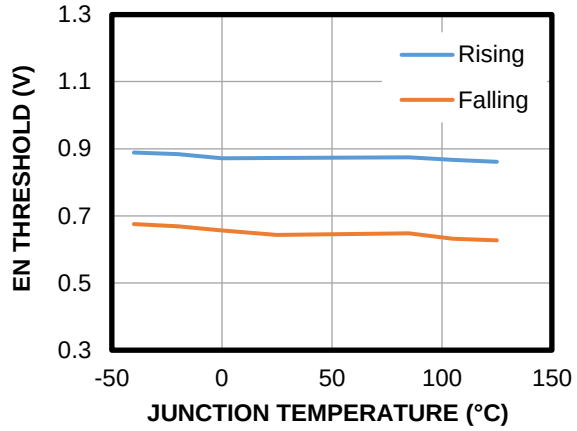
Output Voltage vs. Junction Temperature



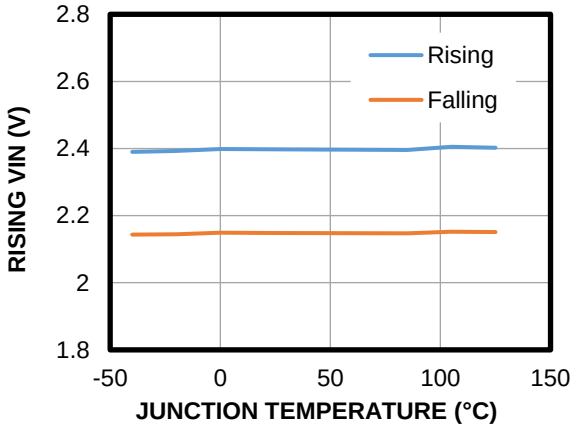
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.8V, V_O = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

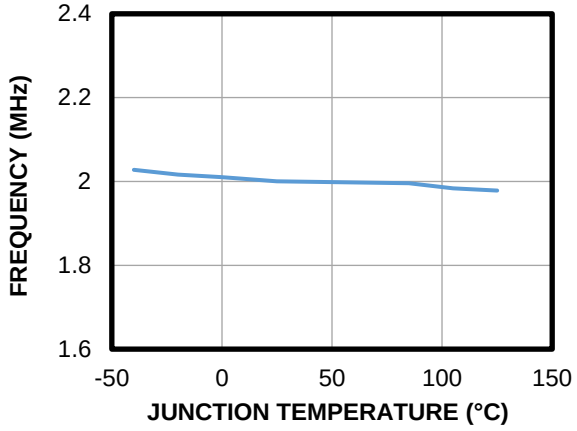
EN Threshold vs. Junction Temperature



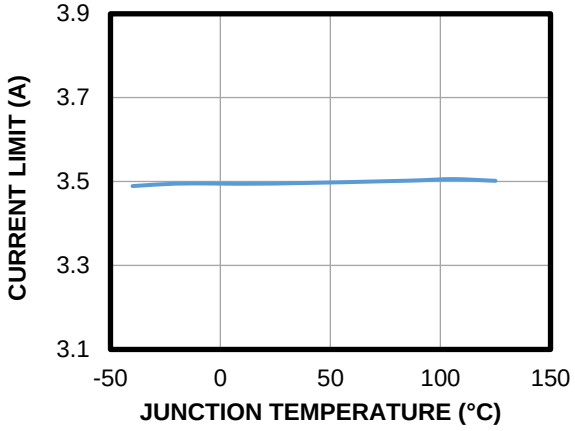
Rising VIN vs. Junction Temperature



Frequency vs. Junction Temperature

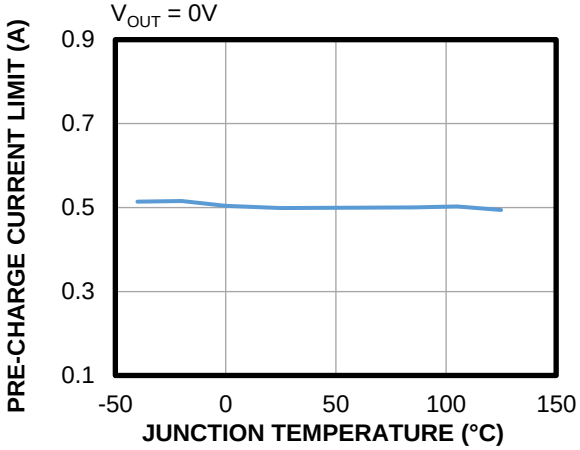


SW1/SW2 Current Limit vs. Junction Temperature



SW1/SW2 Pre-Charge Current Limit vs. Junction Temperature

V_{OUT} = 0V

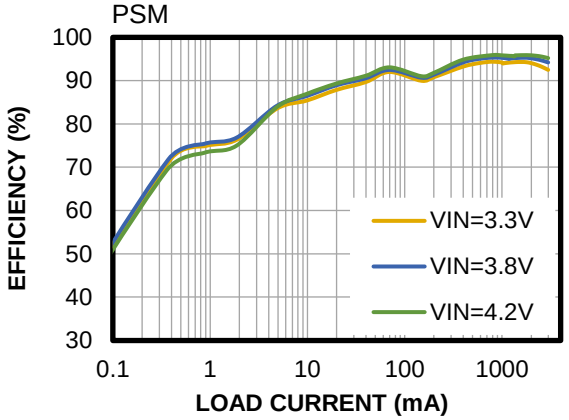


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 3.8V, V_O = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

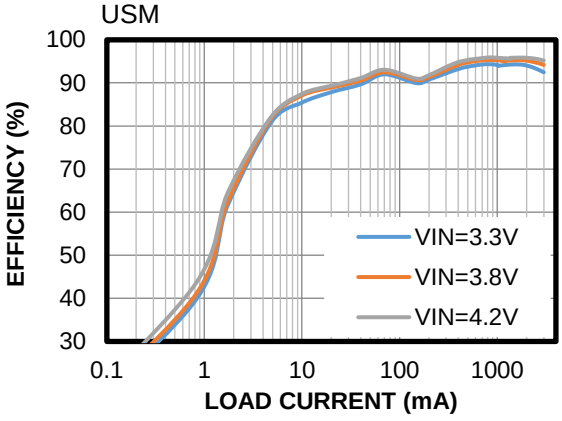
Efficiency vs. Load Current

PSM



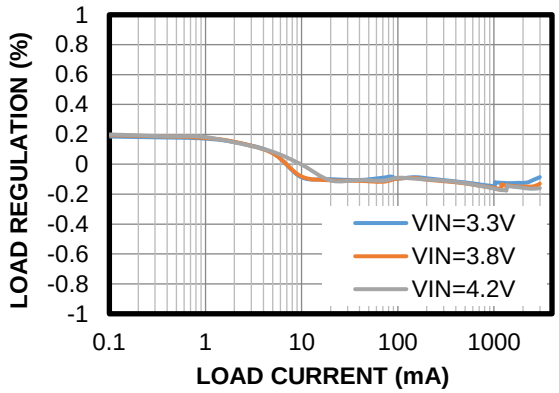
Efficiency vs. Load Current

USM



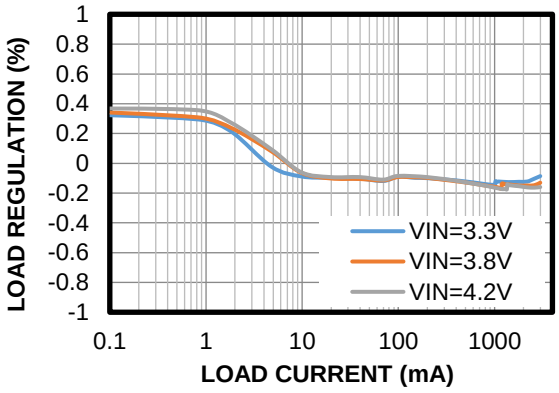
Load Regulation

PSM

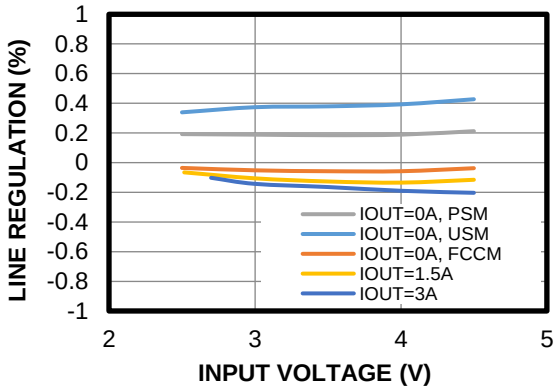


Load Regulation

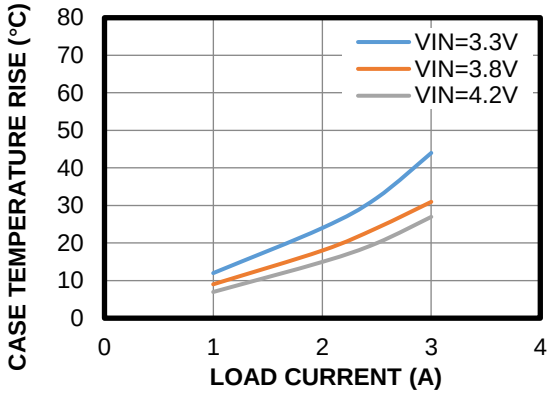
USM



Line Regulation



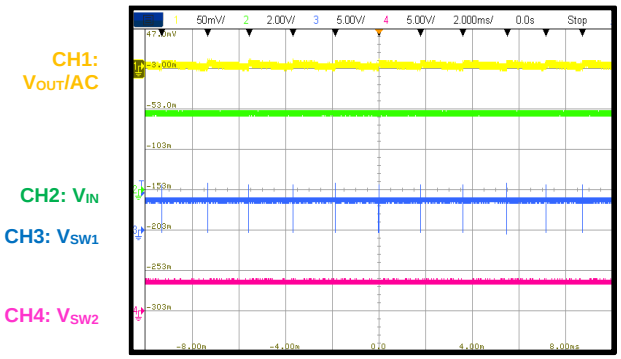
Case Temperature Rise



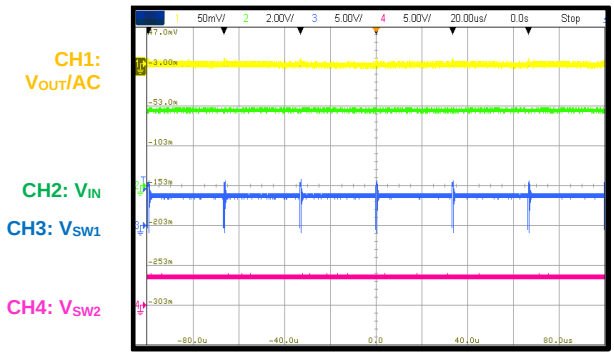
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 3.8V, V_O = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

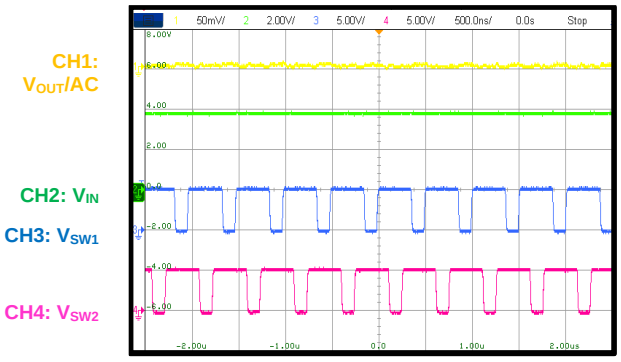
Steady State
PSM, I_{OUT} = 0A



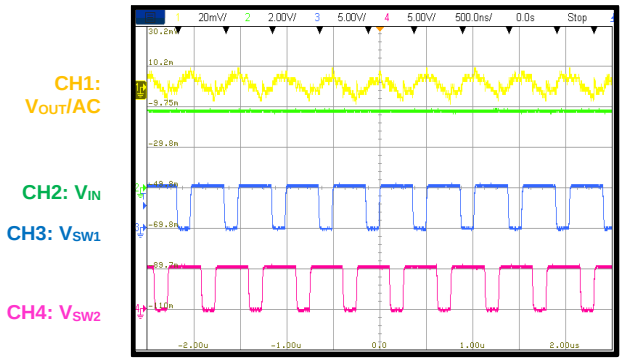
Steady State
USM, I_{OUT} = 0A



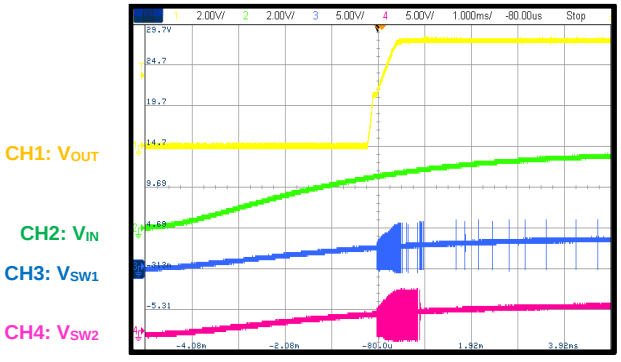
Steady State
FCCM, I_{OUT} = 0A



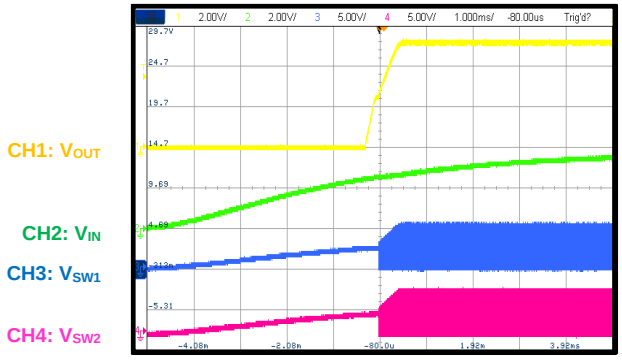
Steady State
I_{OUT} = 3A



Start-Up through VIN
I_{OUT} = 0A



Start-Up through VIN
R_{LOAD} = 2Ω

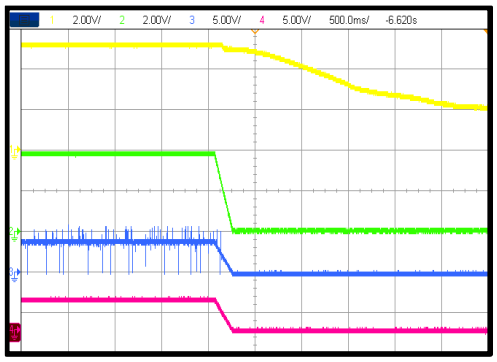


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 3.8V, V_O = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

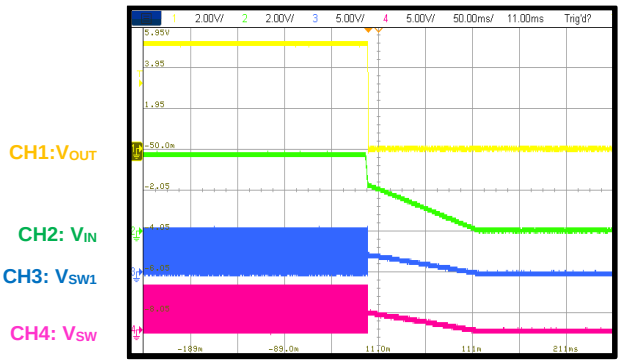
Shutdown through VIN

I_{OUT} = 0A



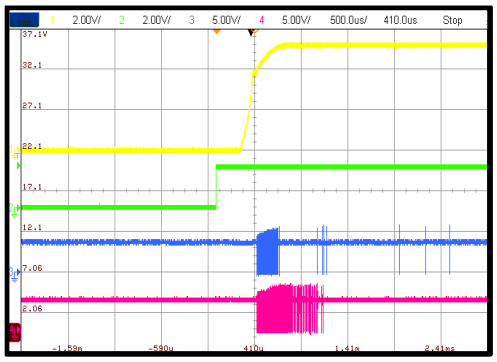
Shutdown through VIN

I_{OUT} = 3A



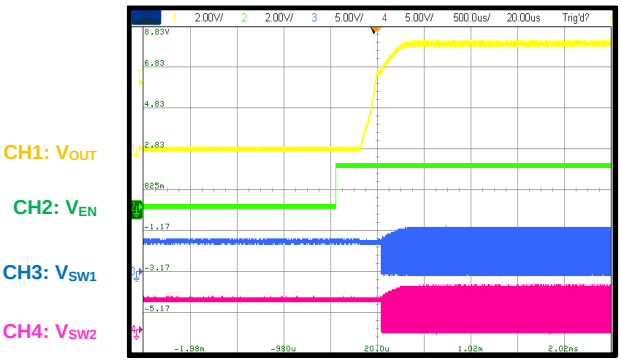
Start-Up through EN

I_{OUT} = 0A



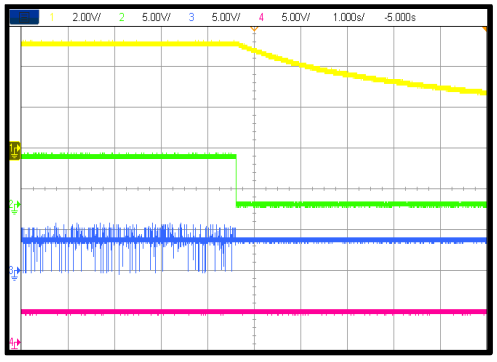
Start-Up through EN

R_{LOAD} = 2Ω



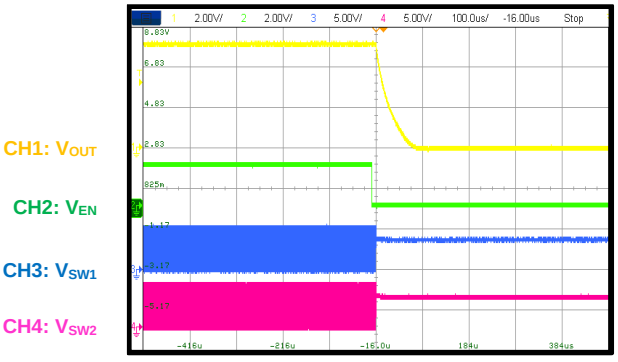
Shutdown through EN

I_{OUT} = 0A



Shutdown through EN

I_{OUT} = 3A

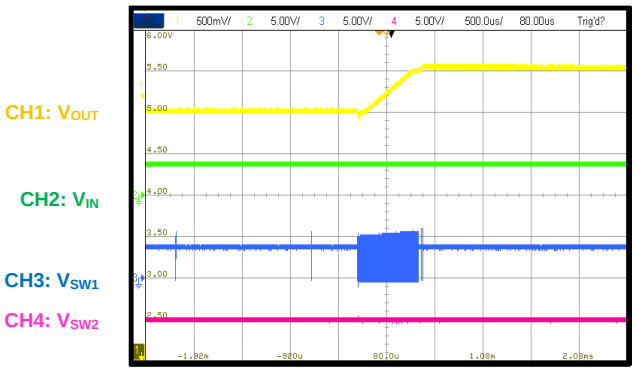


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 3.8V, V_O = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

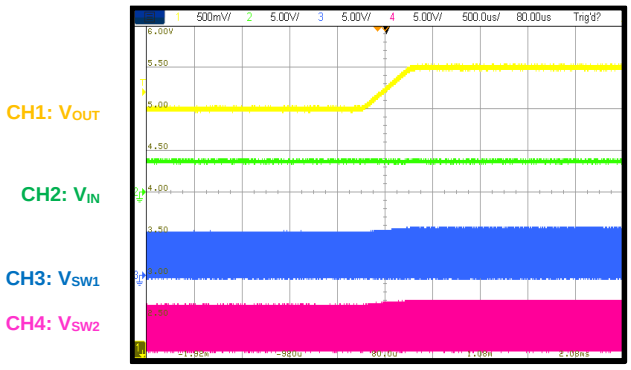
V_{OUT} Dynamic Voltage Change

I_{OUT} = 0A, V_{OUT} = 5V to 5.5V



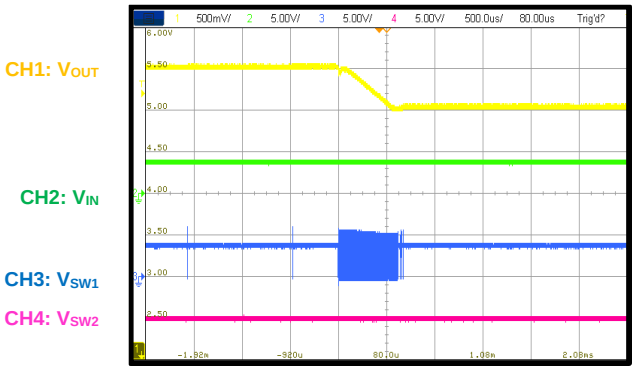
V_{OUT} Dynamic Voltage Change

I_{OUT} = 3A, V_{OUT} = 5V to 5.5V



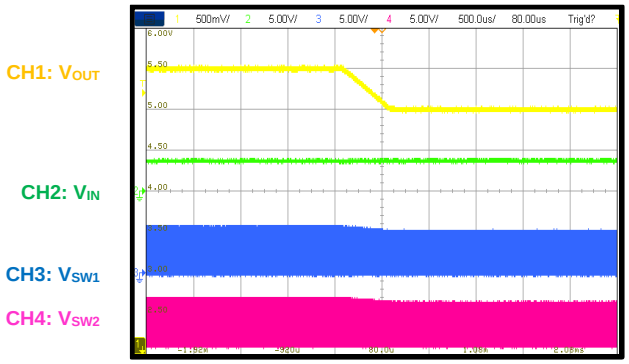
V_{OUT} Dynamic Voltage Change

I_{OUT} = 0A, V_{OUT} = 5.5V to 5V



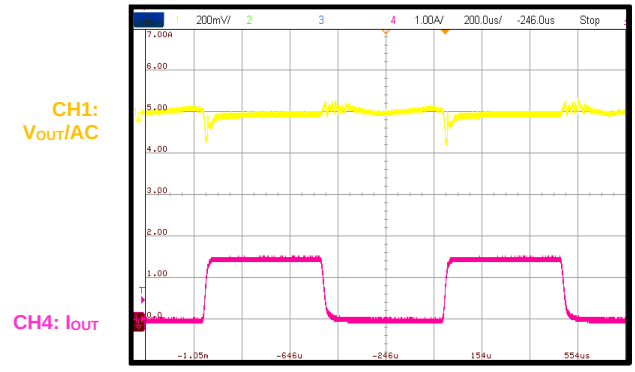
V_{OUT} Dynamic Voltage Change

I_{OUT} = 3A, V_{OUT} = 5.5V to 5V



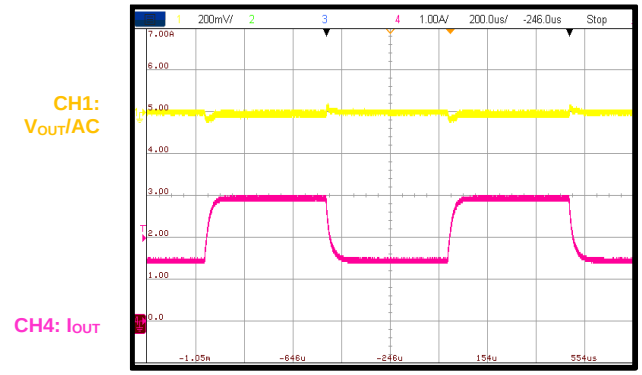
Load Transient

I_{OUT} = 0A to 1.5A, I_{RAMP} = 25mA/µs



Load Transient

I_{OUT} = 1.5A to 3A, I_{RAMP} = 25mA/µs

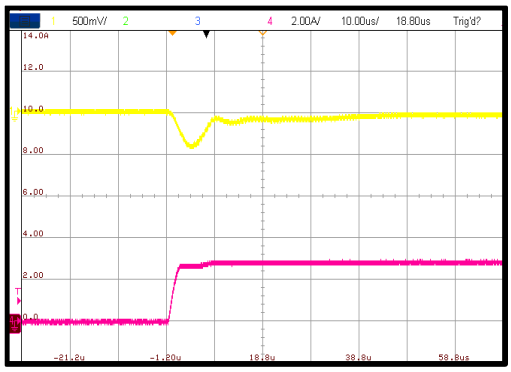


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 3.8V, V_O = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

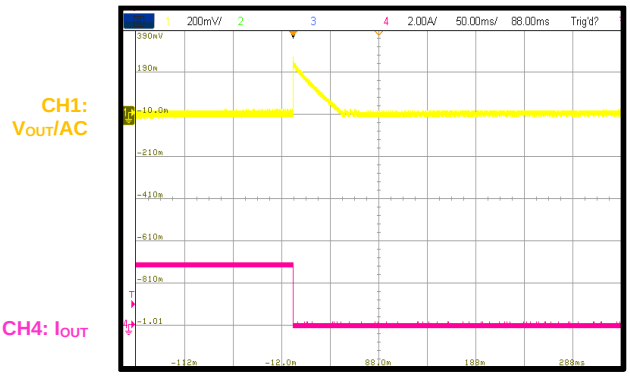
Load Transient

I_{OUT} = 10mA to 3A, I_{RAMP} = 1A/µs



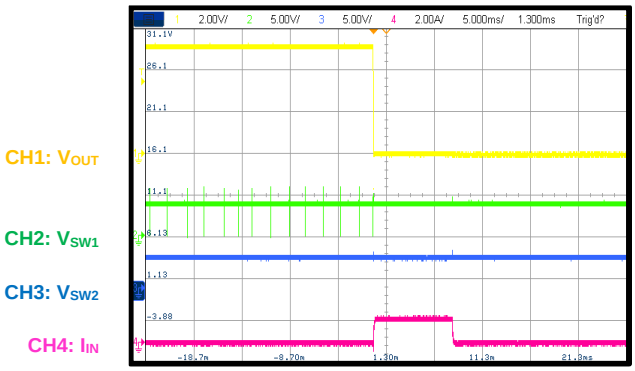
Load Transient

I_{OUT} = 3A to 0A, I_{RAMP} = 3A/100ns



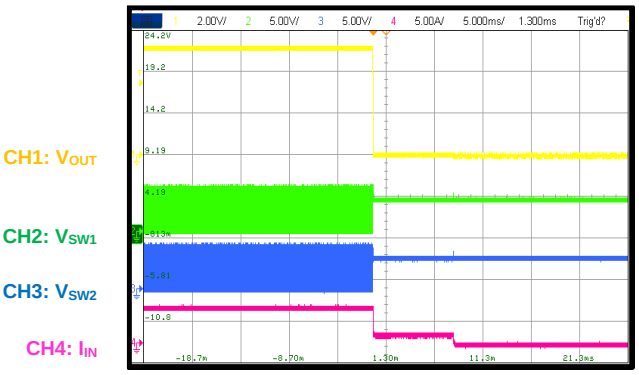
SCP Entry

I_{OUT} = 0A to short



SCP Entry

I_{OUT} = 3A to short



FUNCTIONAL BLOCK DIAGRAM

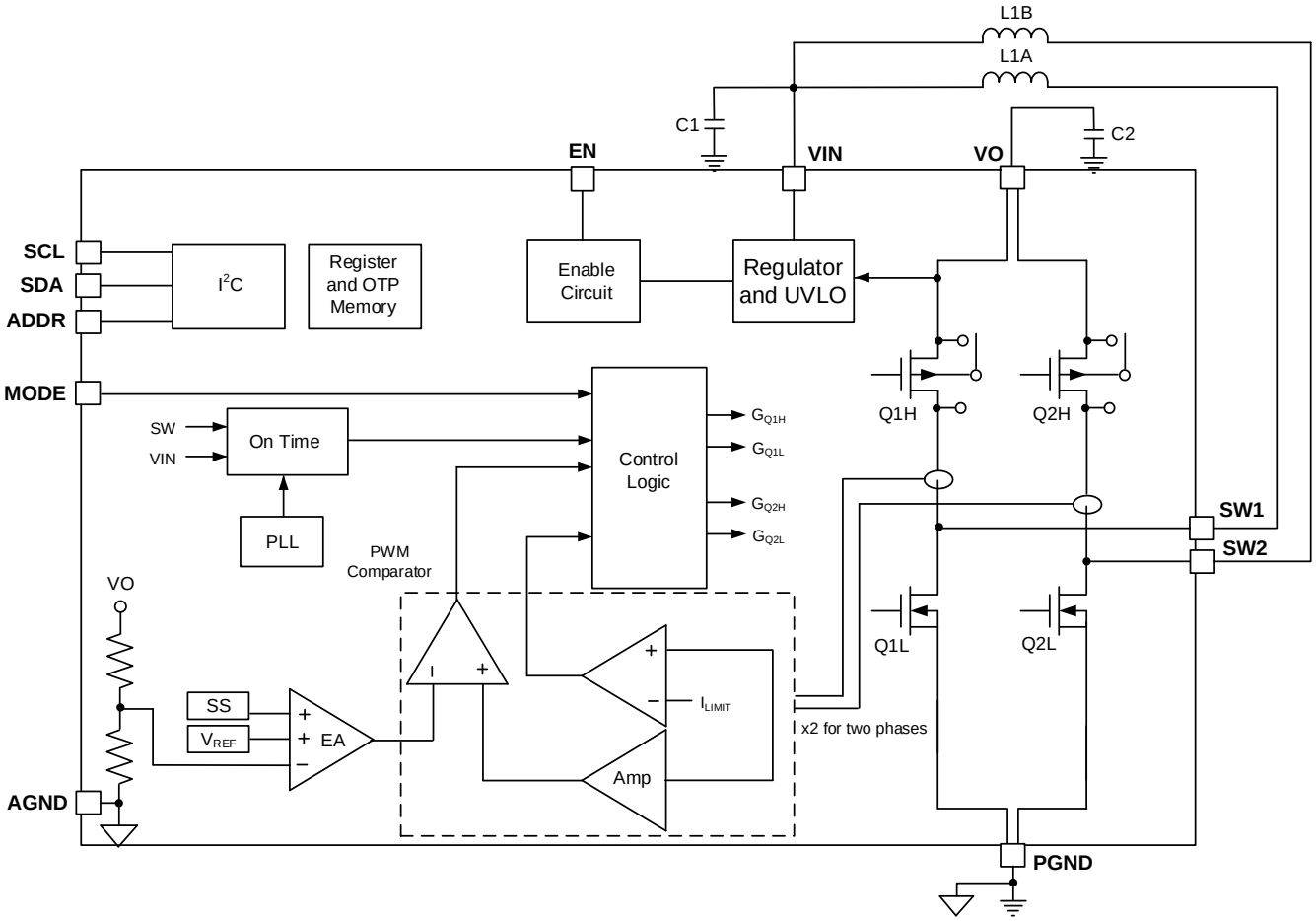


Figure 1: Functional Block Diagram

OPERATION

The MP3439 is a high-efficiency, synchronous, dual-phase boost converter with an output disconnect function. It adopts constant-on-time (COT) control topology with dual-phase switching mode, providing a small-size power solution for up to 3A of load current (I_{LOAD}) from a 1-cell lithium battery. Figure 1 on page 15 shows the functional block diagram.

Start-Up

When the MP3439 is enabled, both phases' high-side MOSFETs (HS-FETs) turn on to linearly charge the output capacitor (C_{OUT}) with a limited pre-charge current. Each phase of the P-channel MOSFET's pre-charge current is limited and proportional to the output voltage (V_{OUT}), which is about 0.5A when the VO pin voltage (V_O) is 0V and rises to 1A when V_O is charged to 2.5V. Figure 2 shows the one-phase current during start-up.

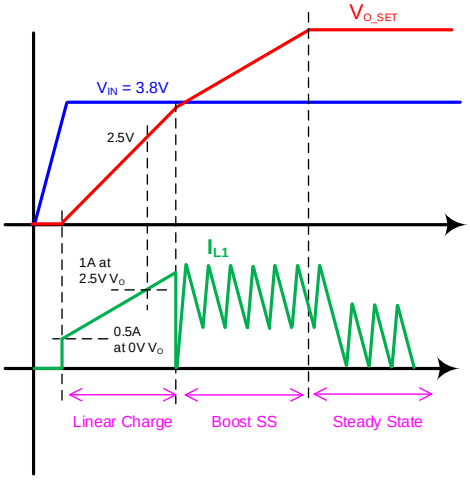


Figure 2: One-Phase Current in Start-Up Process

Once V_{OUT} is charged above V_{IN} - 0.2V, the MP3439 starts switching in boost mode, and V_O rises and is controlled by an internal soft-start (SS) signal. The SS period completes when the internal SS signal reaches the feedback reference voltage. Table 1 shows the mode selection during start-up.

Table 1: Mode Selection during Start-Up

VO Voltage	Mode
$V_O < V_{IN}$ - 0.2V	Linear charge mode
$V_O \geq V_{IN}$ - 0.2V	Boost switching mode

When V_O exceeds V_{IN}, the MP3439 powers the internal circuits from V_O instead of VIN.

Soft Start (SS)

The MP3439 provides SS by charging an internal capacitor with a current source. During the linear charge period, the SS signal continues to rise, following V_O. Once the linear charge elapses, the voltage on the SS capacitor (C_{SS}) is charged and ramps up V_O based on the internal fixed slew rate.

C_{SS} is discharged completely during a commanded shutdown, thermal shutdown, or short circuit at the output. SS also drops when V_O drops.

During soft start-up, the IC works in pulse-skip mode (PSM), regardless of whether the MODE pin (or MODE bits) is set to ultrasonic mode (USM) or forced continuous conduction mode (FCCM). This can guarantee smooth V_O ramping when V_O is biased to a set voltage during start-up. Under this condition, the IC disables the switching of both the HS-FETs and low-side MOSFETs (LS-FETs) until the voltage on the internal C_{SS} exceeds the internal FB voltage.

Boost Operation

The MP3439 uses COT control to regulate V_{OUT}. At the beginning of each cycle, the LS-FET turns on with a fixed on time, forcing the inductor current (I_L) to rise. After the on time, the LS-FET turns off and I_L flows to C_{OUT} through the HS-FET, causing I_L to decrease. If the I_L signal drops below the COMP voltage (V_{COMP}), which is an amplifier output comparing the V_O feedback voltage with the internal reference voltage, the HS-FET turns off and the LS-FET turns on again. The cycle repeats and V_O is charged high in each cycle.

Figure 3 on page 17 shows the steady state switching and I_L waveforms.

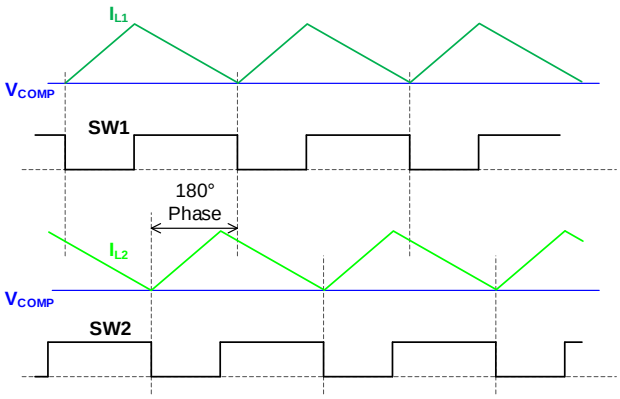


Figure 3: Boost Steady State Operation

The MP3439 supports dual-phase boost switching, where both phase share the V_{COMP} signal to balance the current in each phase.

Light-Load Operation

The MP3439 works at quasi-constant frequency with pulse-width modulation (PWM) control under heavy-load conditions. The device can be set to light-load operation using FCCM, PSM, or USM.

The MODE pin can set light-load operation when the MODE_PIN_ENABLE bit is set to 1. The internal MODE bits are used to set light-load operation if the MODE_PIN_ENABLE bit is 0. Light-load operation can be changed even when the IC is switching.

Forced Continuous Conduction Mode (FCCM)

The MP3439 works at fixed frequency with PWM mode under any load condition if the MODE pin is pulled high (or by setting the MODE bits to 0b10). When the load decreases, the average input current drops, and I_L may go negative from VO to VIN during the HS-FET's on period. This forces I_L to work in continuous mode with fixed frequency, producing a low V_O ripple.

Pulse-Skip Mode (PSM)

The MP3439 works in PSM under light-load conditions if the MODE pin is pulled low (or by setting the MODE bits to 0b00). In this mode, once I_L drops to 0A, the HS-FET turns off to prevent current flowing from VO to VIN. This forces I_L to work in discontinuous conduction mode (DCM).

If the internal V_{COMP} drops to the PSM threshold, the MP3439 works in sleep mode to decrease switching power loss and recover switching once V_{COMP} exceeds the PSM threshold. Under light-load conditions in DCM, the LS-FET's switching on time is reduced, which can guarantee lower current ripple, small V_O ripple, and avoid high audible noise.

PSM has significantly higher efficiency than FCCM at light loads, but the V_O ripple is higher in PSM compared to FCCM.

Ultrasonic Mode (USM)

To avoid audible noise below a 20kHz switching frequency (f_{SW}) in PSM, the MP3439 provides USM by setting the MODE pin to about 0.5V (or by setting the MODE bits to 0b01).

In USM, I_L works in DCM and the frequency stretches down when the load decreases to a moderate level. Switching does not stop when V_{COMP} drops to the PSM threshold. The MP3439 continues decreasing f_{SW} if the load decreases. Once the MP3439 does not detect the LS-FET's on state for 33µs, it forces the LS-FET on. This can limit the frequency to avoid audible frequency under light-load or no-load conditions.

USM may convert more energy to output than the required load due to the minimum 30kHz frequency, which results in V_O exceeding the default voltage. When V_O rises and V_{COMP} drops, the peak I_L may drop as well. If V_{COMP} drops below an internally clamped level, the HS-FET zero-current threshold (ZCD) threshold is gradually regulated to a negative level, allowing the energy in the inductor to flow back to VIN in each cycle. This can keep the output at the set voltage with a 30kHz frequency.

Dual-Phase Switching

The MP3439 uses dual-phase topology boost switching, where the two phases are equally spaced 180° apart. With dual-phase switching, the output ripple is low and the I_L rating is low.

Switching Frequency

The MP3439 supports 1MHz and 2MHz f_{SW} options with the set FREQ bit. By default, the MP3439 works at 2MHz for each phase switching.

The MP3439 supports a small, 40ns minimum on time (t_{ON_MIN}) for the LS-FET's on period, which can support a high VIN/VO ratio condition with

a 2MHz frequency. After triggering a 40ns t_{ON_MIN}, the MP3439 stretches down the frequency automatically, and V_{OUT} can be smoothly regulated.

Frequency Spread Spectrum (FSS)

To improve EMI performance, the MP3439 integrates a frequency spread spectrum (FSS) function. When this function is enabled by the FSS_EN bit, some of the f_{SW} variation is added to the fundamental f_{SW} set by the FSS_FSW bit based on the triangle spread spectrum shape. The modulation frequency is configured by the FSS_AMP bit.

FSS only works when I_L is in continuous conduction mode (CCM). If the load decreases and the MP3439 works in USM or PSM switching mode, then FSS is disabled automatically.

Output Disconnect

The MP3439 supports true output disconnect by eliminating the body diode conduction of the internal P-channel MOSFET rectifiers. This allows V_{OUT} to drop to 0V during shutdown or under short-circuit conditions.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP3439 senses the HS-FET current for the cycle-by-cycle current limit of both phases. The LS-FET remains off until the HS-FET current drops below the valley current limit threshold. The current limits of the two phases share the same valley current limit threshold, which can be selected at 2.5A or 3.5A via the I²C interface.

When an over-current or short-circuit condition occurs, I_L is limited in each cycle, and V_{OUT} drops. If V_{OUT} drops below V_{IN} - 0.2V, the MP3439 works in linear charge mode. In linear charge mode, the P-channel MOSFET current is limited in both phases, meaning the output can drop to 0V. The MP3439 triggers latch-off protection if linear charge mode works continuously for longer than 8ms.

If the linear charge period is shorter than 8ms, the MP3439 recovers to boost switching mode once V_{OUT} rises to V_{IN} - 0.2V again. If the MP3439 triggers latch-off protection after the 8ms linear charge period, the MP3439 only recovers after resetting the power supply, or resetting with the EN pin or ENPWR bit.

In linear charge mode, the internal SS signal is pulled low, and the MP3439 switches with SS control again during over-current protection (OCP) and short-circuit protection (SCP) recovery conditions.

Over-Voltage Protection (OVP)

If V_{OUT} exceeds the over-voltage protection (OVP) rising threshold, boost switching stops. This prevents over-voltage conditions from damaging the chip. When the output drops below the OVP falling threshold, the device resumes switching automatically.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. Once the die temperature exceeds 150°C, the IC shuts down and resumes normal operation after the die temperature drops (typically 20°C).

I²C INTERFACE

I²C Serial Interface

The I²C is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. When connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MP3439 features a 400kHz I²C interface. The I²C interface adds flexibility to the power supply solution. V_{OUT}, current limit, light-load operation, or other parameters can be instantaneously controlled by the I²C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate read/write (R/W) operation.

I²C Interface Address

The MP3439 can configure the I²C device address with different ADDR pin voltage settings, described below:

- Pull ADDR low to set the I²C address to 1100 001.
- Float ADDR to set the I²C address to 1100 010.
- Pull ADDR high to set the I²C address to 1100 100.

Table 2: I²C Address Setting via ADDR Pin

ADDR Voltage	ADDR Connection	I²C Address	
		Binary	Hex
<20% of V_{IN}	Connect to AGND/PGND	1100 001	61h
30% of V_{IN} to 70% of V_{IN}	Float pin	1100 010	62h
>80% of V_{IN}	Connect to VIN	1100 100	64h

Start and Stop Conditions

The start (S) and stop (P) conditions are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start condition is defined as the SDA signal transitioning from high to low while SCL is high. A stop condition is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 4).

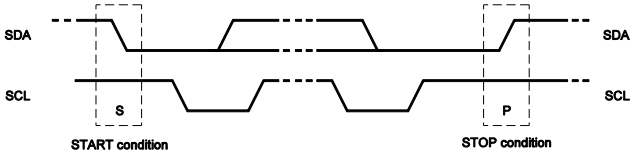


Figure 4: Start and Stop Conditions

The master then generates the SCL clocks and transmits the device address and the R/W direction bit on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP3439 requires a start condition, valid I²C address, register address byte, and data byte for a single data update. After receiving each byte, the MP3439 acknowledges by pulling the SDA line low during a single clock pulse's high period. A valid I²C address selects the MP3439. The MP3439 performs an update on the LSB byte's falling edge. Figure 5 on page 20 shows an example of writing to a single register. Figure 6 on page 20 shows an example of reading to a single register.

I²C Start-Up Timing

The I²C function is enabled once V_{IN} exceeds the under-voltage lockout (UVLO) threshold and EN is active.

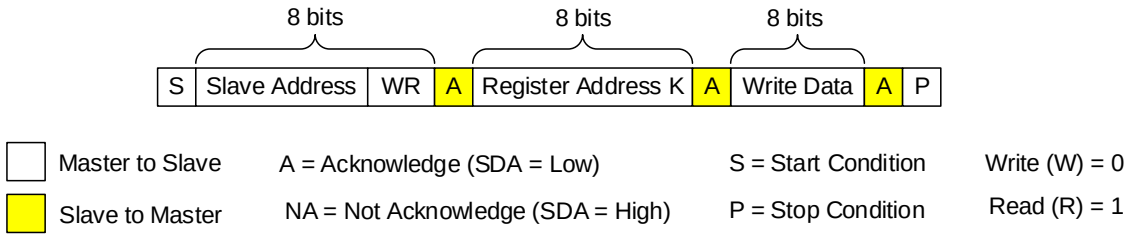


Figure 5: I²C Write Single Register Example

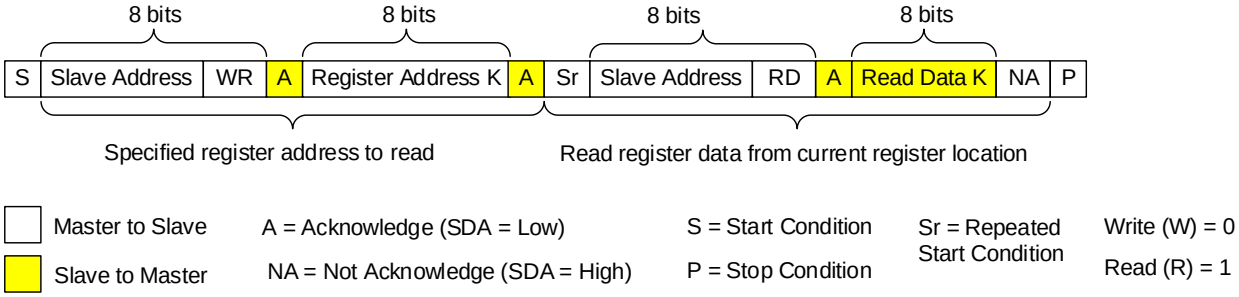


Figure 6: I²C Read Single Register Example

REGISTER MAP

Add	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	CTRL1	R/W	MODE		CURRENT_ LIMIT	VOUT				
01h	CTRL2	R/W	GO_BIT (9)	MODE_ PIN_ ENABLE	ENPWR	RESERVED (10)	FSS_ EN	FSS_AMP	FSS_FSW	FREQ

Notes:

9) GO_BIT cannot be configured by the one-time programmable (OTP) memory. All other bits are configurable via the OTP non-volatile memory (NVM).

10) Do not change the reserved register, otherwise the IC may work abnormally.

CTRL1 (00h)

Bits	Access	Bit Name	Default	Description
7:6	R/W	MODE	00	Sets the switching mode of pulse-skip mode (PSM), ultrasonic mode (USM), and forced continuous conduction mode (FCCM) at light loads. 00: PSM 01: USM 10: FCCM 11: Reserved The MODE bits only work after setting MODE_PIN_ENABLE to 0.
5	R/W	CURRENT_ LIMIT	1	Configures the switching valley current limit for both switching phases. The low-side MOSFET (LS-FET) does not turn on until the high-side MOSFET (HS-FET) current drops below the valley limit threshold. 0: 2.5A 1: 3.5A
4:0	R/W	VOUT	10000	Configures the VO voltage (V_O) between 5V and 5.5V. 25mV/LSB. The default output voltage (V_{OUT}) is 5.2V. V_{OUT} can be calculated with the following equation: $V_{OUT} = 5V + (V - 8) \times 25mV$ Where V is a 5-bit unsigned binary integer of VOUT, bits[4:0], and the MP3439's maximum V_{OUT} is clamped to 5.5V, even when V exceeds 28. See Table 2 for more details on configuring the VOUT bits. The MP3439 integrates a feedback resistor network between the VO pin and internal feedback reference voltage. The V_{OUT} change slew rate is fixed as 1mV/µs. See GO_BIT in the CTRL2 (01h) section on page 22 to implement the V_{OUT} change.

Table 2: VOUT Register and Voltage Settings

Register	V_{OUT}	Register	V_{OUT}	Register	V_{OUT}	Register	V_{OUT}
01000	5V	01001	5.025V	01010	5.05V	01011	5.075V
01100	5.1V	01101	5.125V	01110	5.15V	01111	5.175V
10000	5.2V	10001	5.225V	10010	5.25V	10011	5.275V
10100	5.3V	10101	5.325V	10110	5.35V	10111	5.475V
11000	5.4V	11001	5.425V	11010	5.45V	11011	5.475V
11100	5.5V	-	-	-	-	-	-

CTRL2 (01h)

Bit	Access	Bit Name	Default	Description
7	R/W	GO_BIT	0	Controls the MP3439 when the VO pin voltage (V_O) starts to change. Write the VOUT registers (00h) first, then write the GO_BIT to 1. V_O changes based on the new register setting. GO_BIT resets to 0 when the V_{OUT} change is done, meaning the internal reference voltage (V_{REF}) steps to the target V_{REF}. The host can read GO_BIT to determine whether V_O scaling is complete. If GO_BIT = 1 and the load is low, the MP3439 is forced into FCCM to help discharge the output capacitor (C_{OUT}). 0: V_O does not change 1: V_O changes based on the VOUT register setting. After V_O scaling finishes, this bit resets to 0 automatically The VOUT register is not writable when GO_BIT = 1.
6	R/W	MODE_PIN_ ENABLE	1	Enables the MODE pin function. 0: Disables the external MODE pin control using the internal MODE bits to control light-load operation 1: Enables the external MODE pin control, and does not use the internal MODE bits to control operation
5	R/W	ENPWR	1	Enables the MP3439's power switching. 1: Enables power switching 0: Disables power switching but the other internal control circuits work When the external EN pin is low, the converter is off, and the I^2C also shuts down. When the EN pin is high, the ENPWR bit takes over. The default ENPWR bit is set to 1. When the ENPWR bit is set to 0, the MP3439 stops switching, but the I^2C register does not reset.
4	R/W	RESERVED	1	Reserved. Do not change this bit in application.
3	R/W	FSS_EN	0	Enables the frequency spread spectrum (FSS) function. 0: Disables FSS 1: Enables FSS
2	R/W	FSS_AMP	0	Configures the FSS modulation amplitude. 0: ±6% of switching frequency (f_{SW}) 1: ±12% of f_{SW}
1	R/W	FSS_FSW	1	Configures the FSS modulation frequency. 0: 5kHz 1: 10kHz
0	R/W	FREQ	1	Configures f_{SW}. 0: 1MHz 1: 2MHz

APPLICATION INFORMATION

Setting the Output Voltage

The MP3439's V_{OUT} is configured by the VOUT register bits, which are between 5V and 5.5V, with a 25mV resolution. See the VOUT bit in the CTRL1 (00h) section on page 21 for more details about calculating V_{OUT}.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AT Series**

The MP3439 can utilize small surface-mount chip inductors due to its 2MHz f_{SW}. A 0.47µH inductor is suitable for most applications. Larger inductances allow for slightly greater output current (I_{OUT}) capability by reducing the inductor ripple current, which also increases component size. The inductance (L) for most designs can be calculated with Equation (1):

$$L = \frac{V_{IN}(V_O - V_{IN})}{f_{SW} \times V_O \times \Delta I_L} \quad (1)$$

Where ΔI_L is the acceptable inductor current ripple and is typically set as 30% to 50% of the average I_L.

The inductor should have a low DCR to reduce the resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 3 shows the MPS power inductor recommendations, where the part number can be selected based on the design requirements.

Table 3: Selecting the Power Inductor

Part Number	Inductance	Manufacturer
MPL-AT	0.47µH to 4.7µH	MPS
MPL-AT2010-R47	0.47µH	MPS

For more information, visit the Inductors page on the MPS website.

Selecting the Input Capacitor

The input capacitor (C_{IN}) requires a minimum capacitance of 10µF to ensure stability across the entire operating range. Low-ESR input capacitors reduce the input switching noise and peak current drawn from the battery. Ceramic capacitors are recommended for input decoupling and should be placed as close to the device as possible.

Selecting the Output Capacitor

C_{OUT} requires a minimum capacitance of 88µF at the configured V_{OUT} to ensure stability across the entire operating range. A higher capacitance may be required to lower the output ripple and transient ripple. Use low-ESR capacitors such as ceramic capacitors with X5R or X7R dielectrics.

Control Pin Setting

The MP3439 includes several control pins, including EN, ADDR, MODE, and SCL/SDA, which are described in more detail below.

EN

EN is the enable input pin that turns on and turns off all the internal circuits and switching. Connect the EN pin to VIN to automatically turn on the IC.

ADDR

ADDR is the MP3439's address setting pin. The different settings are described below:

- Pull ADDR low to set the I^2C address to 1100 001.
- Float ADDR to set the I^2C address to 1100 010.
- Pull ADDR high to set the I^2C address to 1100 100.

MODE

MODE is the MP3439's light-load operation selection pin, where the MODE_PIN_ENABLE bit is set to 1. The different settings are described below:

- Pull MODE low to set light-load switching in PSM.
- Pull MODE to about 0.5V to set light-load switching in USM
- Pull MODE high to set light-load switching in FCCM.

SCL/SDA

SCL and SDA are I^2C input pins that require an external pull-up resistor connected to VIN. Connect SCL or SDA to AGND if the I^2C is not used.

Design Example

Table 4 shows a design example following the application guidelines for the given specifications.

Table 4: Design Example

V_{IN}	V_{OUT}	I_{OUT}
2.7V to 4.5V	5.2V	3A

Figure 8 on page 26 shows the detailed application schematic. See the Typical Performance Characteristics section on page 10 for the typical performance and circuit waveforms. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines (11)

Efficient PCB layout of the high-frequency switching power supplies is critical for stable operation. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 7 and follow the guidelines below:

1. Place C_{OUT} as close to VO as possible, with minimal distance to PGND on both sides of the package.
2. Connect the two phases of the VO together via the vias and copper on the bottom side.
3. Keep the trace between the inductor and SW as wide and short as possible.
4. Connect the PGND trace using wide copper.
5. Place vias around PGND to lower the die temperature.
6. Keep the input loop (C1, L1, SW, and PGND) as small as possible.

Note:

11) The recommended PCB layout is based on the typical application circuit (see Figure 8 on page 26).

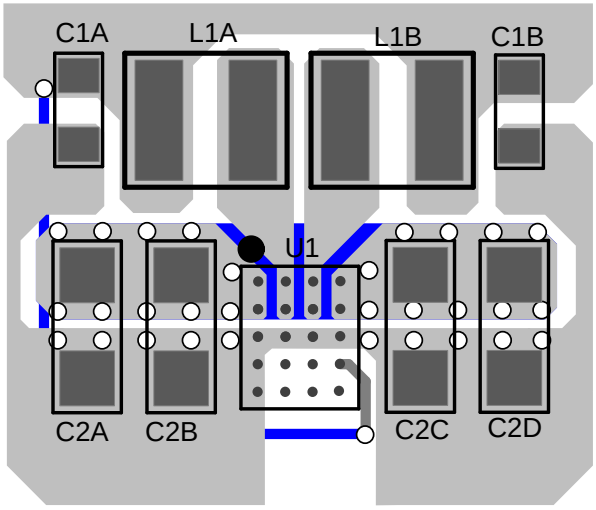


Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

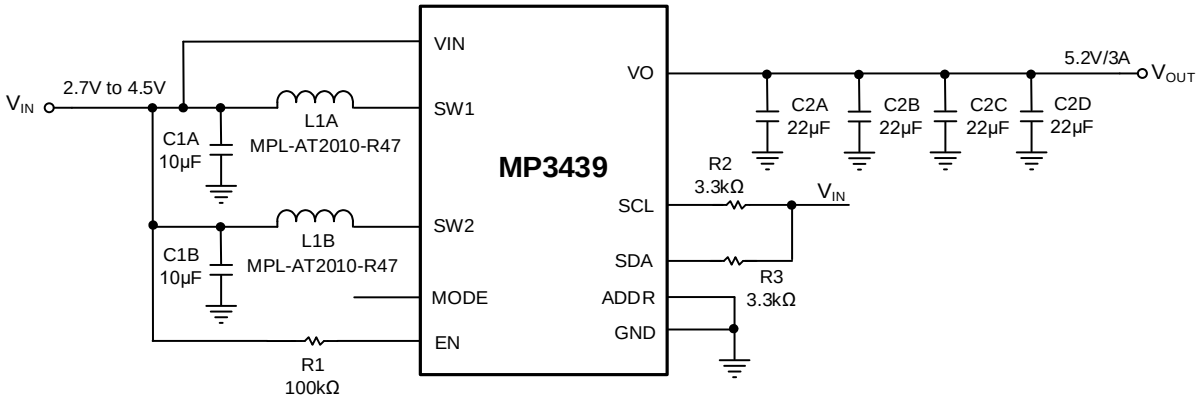


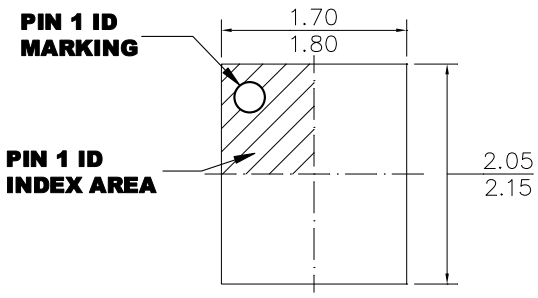
Figure 8: Typical Application Circuit (5.2V Output)

DEFAULT ONE-TIME PROGRAMMBLE (OTP) E-FUSE SELECTION (MP3439GC-0000-Z)

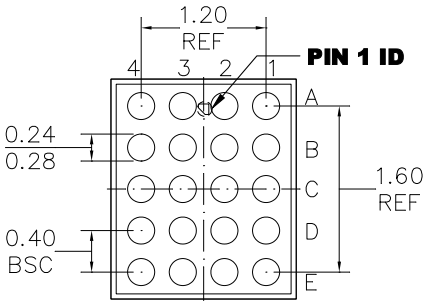
One-Time Programmable (OTP) Parameters	Selection
Mode	Pulse-skip mode (PSM)
Switching current limit	3.5A
Output voltage (V_{OUT})	5.2V
MODE pin	Enabled
Power switching	Enabled
Frequency spread spectrum (FSS) function	Disabled
FSS modulation amplitude	±6% of f_{SW}
FSS modulation frequency	10kHz
Switching frequency (f_{SW})	2MHz

PACKAGE INFORMATION

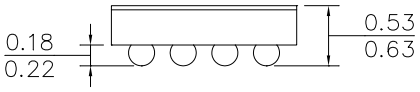
WLCSP-20 (1.75mmx2.10mm)



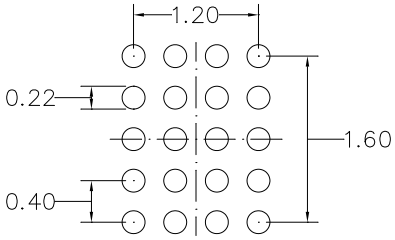
TOP VIEW



BOTTOM VIEW



SIDE VIEW

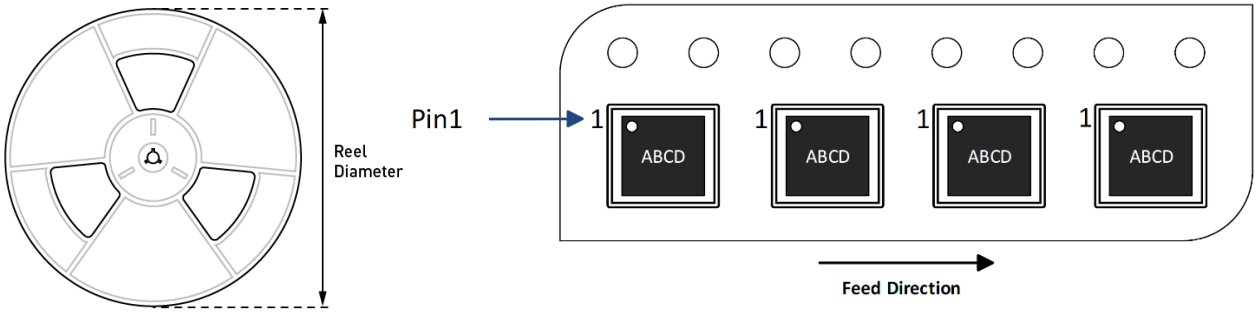


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3439GC-xxxx-Z	WLCSP-20 (1.75mmx 2.1mm)	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/31/2024	Initial Release	-