



MP2722

5A, Single-Cell, I²C-Controlled NVDC Buck Charger with Integrated USB Type-C DRP Detection

DESCRIPTION

The MP2722 is a highly integrated, 5A, switch-mode battery management device for single-cell Li-ion or Li-polymer battery. The narrow-voltage DC (NVDC) power management structure provides low impedance power path that optimizes charging efficiency, reduces battery charging time, and extends battery life during discharging.

The MP2722 is USB Type-C 1.3 compliant, and features dual-role power (DRP) mode with as sink preferred (try.SNK) and source preferred (try.SRC) support. The device's input source type identification algorithm supports USB battery charging specification 1.2 (BC1.2) and non-standard adapter detection.

The I²C interface offers complete operating control, including charging parameter configurations and status/interrupt monitoring.

The MP2722 supports a fully customizable JEITA profile with configurable temperature windows and actions.

The MP2722 is available in a QFN-22 (2.5mmx3.5mm) package.

FEATURES

- USB Type-C 1.3 Compliant
- Fully Integrated CC Controller with Dual-Role Power (DRP) Mode and Autonomous or Manual Mode
- Try.SNK and Try.SRC Mode Support
- Supports USB BC1.2 and Non-Standard Adapters
- 26V Sustainable Input Voltage (V_{IN})
- Configurable 80mA to 5A Charge Current (I_{CC}) via the I²C
- Configurable 100mA to 3.2A Input Current Limit (I_{IN_LIM}) via the I²C
- Minimum V_{IN} Loop for Maximum Adaptor Power Tracking
- Comprehensive Safety Features:
 - Fully Customizable JEITA Profile
 - Additional Negative Temperature Coefficient (NTC) Thermistor Input

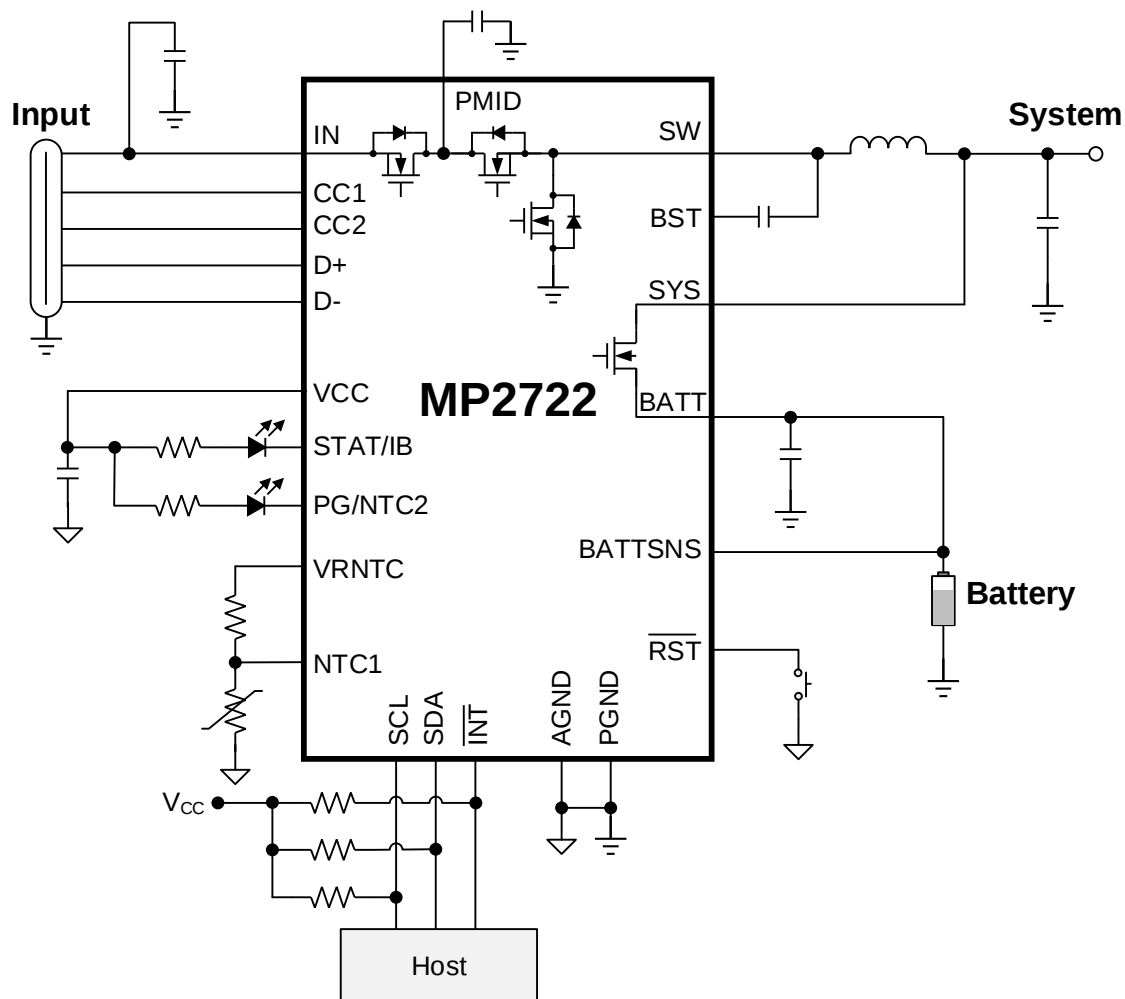
- Configurable Die Temperature Regulation from 60°C to 120°C
- Complete Charge and Pre-Charge Safety Timers
- Watchdog Safety Timer
- Lockable Registers for Charging Parameters
- Configurable 750kHz to 1.5MHz Switching Frequency (f_{SW})
- Integrated 15mΩ Low- $R_{DS(ON)}$ Battery MOSFET with Shipping and Reset Modes
- Ultra-Low 8.5μA Battery Discharge Current in Shipping Mode
- Down to 30mA Termination Current Settings for Wearable Applications
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Configurable Boost Converter for Source Mode and USB On-The-Go (OTG):
 - Configurable Output Current Limit Loop Up to 3A
 - Output Over-Current Protection (OCP)
 - Ability to Power into Large Capacitive Loads Up to 2mF
 - Configurable 5V to 5.35V Output Voltage
- Accuracy:
 - ±0.5% Battery Regulation Voltage (V_{BATT_REG})
 - ±5% I_{CC}
 - ±5% I_{IN_LIM}
 - Remote Battery Sensing for Fast Charge
 - ±2% Output Regulation in Boost Mode
- Available in a Small QFN-22 (2.5mmx3.5mm) Package

APPLICATIONS

- General ≤15W USB Type-C Applications
- Bluetooth Headphones
- Bluetooth Speakers
- Point-of-Sale (POS) Terminals
- Portable Cameras

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2722GRH-xxxx**	QFN-22 (2.5mmx3.5mm)	See Below	1
EVKT-MP2722	Evaluation Kit		

* For Tape & Reel, add suffix -Z (e.g. MP2722GRH-xxxx-Z).

** “xxxx” is the register setting option. The factory default code is “-0000”. This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an “-xxxx” value.

TOP MARKING

BVP
YWW
LLL

BVP: Product code of MP2722GRH-xxxx

Y: Year code

WW: Week code

LLL: Lot number

EVALUATION KIT EVKT-MP2722

EVKT-MP2722 Kit contents: (Items below can be ordered separately).

#	Part Number	Item	Quantity
1	EV2722-RH-00A	MP2722 evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I ² C communication interface device, one USB cable, and one ribbon cable	1
3	Online resources	Include the datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

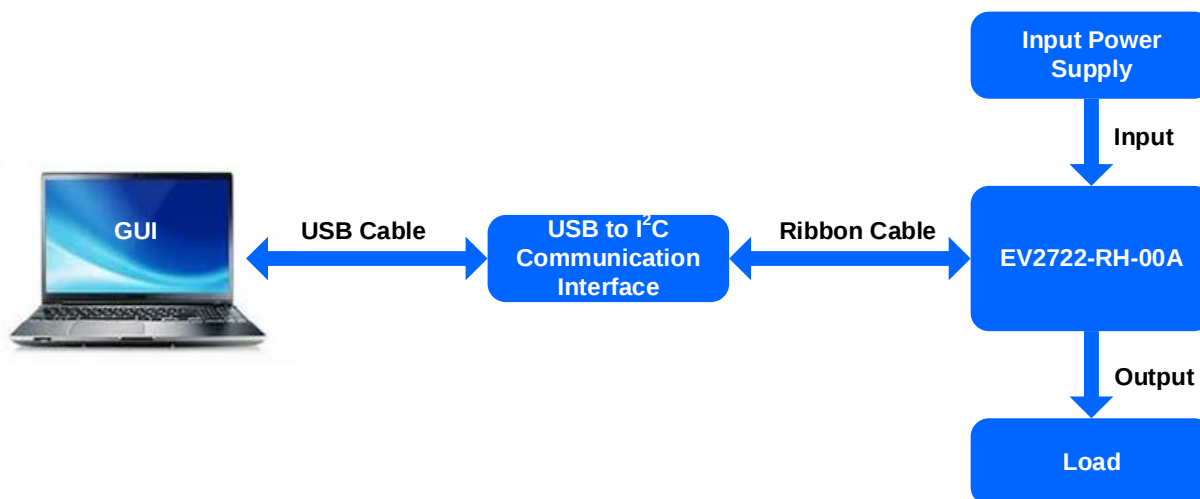
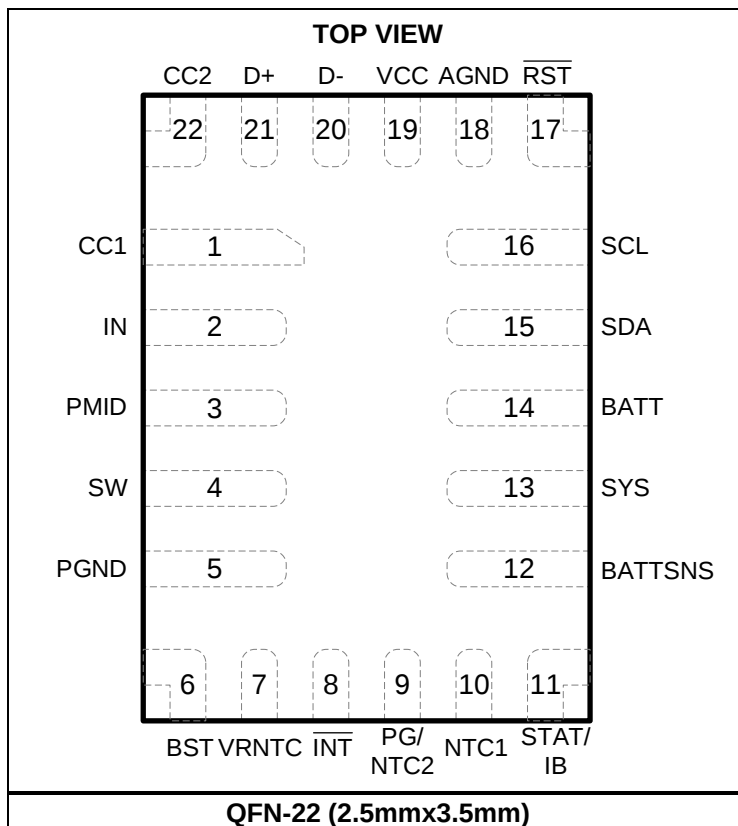


Figure 1: EVKT-MP2722 Evaluation Kit Set-Up

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Type ⁽¹⁾	Description
2	IN	P	Power input. Connect a 1μF ceramic capacitor from the IN pin to PGND.
3	PMID	P	Decoupling node for the power stage. Bypass the PMID pin with a minimum 10μF ceramic capacitor connected from PMID to PGND, and placed as close to the IC as possible with the shortest possible route.
4	SW	P	Switching node. Connect the SW pin to the inductor.
6	BST	P	Bootstrap power. Connect a 22nF capacitor between BST and SW pins to form a floating supply for the high-side MOSFET (HS-FET) driver.
13	SYS	P	System power output. Connect a minimum 20μF ceramic capacitor from the SYS pin to PGND.
14	BATT	P	Battery positive terminal. The internal narrow-voltage DC (NVDC) battery MOSFET is connected between the SYS and BATT pins. Place a minimum 20μF ceramic capacitor from BATT to PGND.
5	PGND	P	Power ground. Short the PGND pin to AGND on the PCB.
18	AGND	P	Analog ground. Short the AGND pin to PGND on the PCB.
19	VCC	P	Internal circuit power supply. Connect a 4.7μF ceramic capacitor from the VCC pin to AGND, placed as close to the IC as possible.
12	BATTSNS	AI	Battery voltage-sense pin for battery voltage regulation. Connect the BATTSNS pin as close as possible to the battery pack's positive terminal.
8	INT	DO	Open-drain interrupt output. This pin generates an active low 256μs pulse when the IC has a status or fault report. Pull this pin up to VCC or another logic rail with a 10kΩ resistor.
16	SCL	DI	I²C interface clock. Pull the SCL pin up to VCC or another logic rail with a 10kΩ resistor.
15	SDA	DIO	I²C interface data. Pull the SDA pin up to VCC or another logic rail with a 10kΩ resistor.
1	CC1	AIO	USB Type-C CC1 pin.
22	CC2	AIO	USB Type-C CC2 pin.
21	D+	AIO	Positive line of the USB data line pair. USB charger type detection is based on BC1.2. Non-standard adapter detection can also be implemented.
20	D-	AIO	Negative line of the USB data line pair. USB charger type detection is based on BC1.2. Non-standard adapter detection can also be implemented.
17	RST	DI	Battery MOSFET reset input. During shipping mode, pull this pin to logic low for a set time (t _{SHIPMODE}) to wake up the IC from shipping mode. When the input voltage (V _{IN}) is not present, setting this pin to logic low for a set time (t _{RST}) resets the SYS power by turning the battery MOSFET off for a set time (t _{SYS_RST}). Then the battery MOSFET is re-enabled. This pin is internally pulled up by a 200kΩ resistor. Float this pin if it is not used.
7	VRNTC	AO	Voltage output for powering up the NTC. The VRNTC pin is powered up to the same voltage as VCC when the buck or boost converter operates.
10	NTC1	AI	Temperature-sense input 1. Connect the NTC1 pin to a negative temperature coefficient (NTC) thermistor. Connect a resistor divider from VRNTC to NTC1 to AGND. NTC1 supports a JEITA profile.
9	PG/NTC2	DO/AI	Open-drain power good (PG) indicator. Pull the PG/NTC2 pin up with a 10kΩ resistor. This pin is active low when the VIN_GD bit = 1, and it can be configured to act as temperature-sense input 2.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type ⁽¹⁾	Description
11	STAT/IB	DO/AO	Charge status open drain output. Pull up this pin with a 10kΩ resistor. LOW indicates charging in progress. HIGH indicates not in charging or charging completes. Blinking with 1Hz indicates fault happens. Can be configured as battery current indication. IB pin sources a current which is proportional to the charge or discharge current of the battery. Connect a resistor from IB to AGND to get the battery current information.

Note:

- 1) AI = analog input, AO = analog output, AIO = analog input output, DI = digital input, DO = digital output, DIO = digital input output, P = power.

ABSOLUTE MAXIMUM RATINGS ⁽²⁾

IN to PGND	-0.3V to +26V
PMID to PGND	-0.3V to +26V
SW to PGND	-0.3V (-2V for 20ns) to +24V
PMID to IN	-0.3V to +12V
BATT, SYS to PGND	-0.3V to +6.5V
BST to SW	-0.3V to +5V
CC1, CC2 to AGND	-0.3V to +22V
All Other Pins to AGND	-0.3V to +5V
Continuous Power Dissipation (T _A = 25°C) ⁽³⁾	2W
Junction temperature	150°C
Lead temperature (solder)	260°C
Storage temperature	-65°C to +150°C

ESD Ratings

Human Body Model (HBM) ⁽⁴⁾	2000V
Charged Device Model (CDM) ⁽⁵⁾	250V

Recommended Operating Conditions ⁽⁷⁾

Supply voltage (V _{IN})	3.9V to 16V
Input current (I _{IN})	Up to 3.2A
System current (I _{SYS})	Up to 5A
Charge current (I _{CC})	Up to 5A
Discharge current (I _{DISCHG})	Up to 8A
Battery voltage (V _{BATT})	Up to 4.6V
Operating junction temp (T _J)	-40°C to +125°C

Thermal Resistance ⁽⁶⁾	θ_{JA}	θ_{JC}
QFN-22 (2.5mmx3.5mm)	50	12.... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Per ANSI/ESDA/JEDEC JS-001, all pins.
- Per ANSI/ESDA/JEDEC JS-002, all pins.
- Measured on JESD51-7, 4-layer PCB.
- The device is not guaranteed to function outside of its operating conditions.

ELECTRICAL CHARACTERISTICS

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent Current						
Battery discharge current in shipping mode	I _{BATT_SHIP}	V _{BATT} = 4V, V _{IN} = 0V, BATTFET disabled, T _A = -40°C to +85°C		8.5	12	μA
Battery discharge current in idle mode	I _{BATT_IDLE}	V _{BATT} = 4V, V _{IN} = 0V, BATTFET enabled, USB Type-C is disabled, T _A = -40°C to +85°C		44	64	μA
Battery discharge current in sink mode	I _{BATT_SINK}	V _{BATT} = 4V, V _{IN} = 0V, BATTFET enabled, T _A = -40°C to 85°C		46	65	μA
Battery discharge current in source mode	I _{BATT_SRC}	V _{BATT} = 4V, V _{IN} = 0V, BATTFET enabled, T _A = -40°C to +85°C		77	95	μA
Battery discharge current in dual-role power (DRP) mode	I _{BATT_DRP}	V _{BATT} = 4V, V _{IN} = 0V, BATTFET enabled, DRP toggle mode, T _A = -40°C to +85°C		60	79	μA
USB suspend mode current	I _{IN_SUSP}	V _{IN} = 5V, EN_BUCK = 0		0.8		mA
Power-On/Off						
Input operating range	V _{IN_OP}		3.9		16	V
Input under-voltage lockout (UVLO) threshold	V _{IN_UV}	V _{IN} falling, V _{BATT} = 0V	3.1	3.25	3.45	V
Input UVLO hysteresis	V _{IN_UV_HYS}	V _{IN} rising, V _{BATT} = 0V		250		mV
Input debounce time	t _{DEB}	V _{IN} debounce to set VIN_GD		15		ms
Hold-off timer	t _{HOLD}	VIN_GD = 1 to D+/D- detection starts		250		ms
Input vs. battery voltage headroom threshold	V _{HDRM}	V _{IN} - V _{BATT} , V _{BATT} = 4V, V _{IN} rising	135	240	340	mV
		V _{IN} - V _{BATT} , V _{BATT} = 4V, V _{IN} falling	10	80	175	mV
Input over-voltage protection (OVP) threshold	V _{IN_OV}	V _{IN} rising, VIN_OVP = 6.3V	6.1	6.3	6.55	V
		V _{IN} rising, VIN_OVP = 11V	10.5	11	11.55	V
		V _{IN} rising, VIN_OVP = 14V	13.5	14	14.55	V
Input OVP hysteresis	V _{IN_OV_HYS}	V _{IN} falling		250		mV
BATT UVLO threshold	V _{BATT_UV}	V _{IN} = 0V, V _{BATT} falling	2.4	2.5	2.6	V
BATT UVLO hysteresis	V _{BATT_UV_HYS}	V _{IN} = 0V, V _{BATT} rising		400		mV
POWER PATH						
System regulation voltage	V _{SYS_REG}	V _{BATT} < V _{SYS_MIN} , SYS_MIN = 100	3.7	3.82	3.94	V
Blocking FET on resistance	R _{ON_RBFET}	T _A = 25°C		15		mΩ
High-side MOSFET (HS-FET) on resistance	R _{ON_HS}	T _A = 25°C		25		mΩ
Low-side MOSFET (LS-FET) on resistance	R _{ON_LS}	T _A = 25°C		25		mΩ
Battery MOSFET on resistance	R _{ON_BFET}	T _A = 25°C		14		mΩ
Battery MOSFET forward voltage in supplement mode	V _{FWD}			30		mV

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Charge (T _A = 0°C to 70°C)						
Charge voltage configuration range	V _{BATT_RANGE}		3.6		4.6	V
Charge voltage step	V _{BATT_STEP}			25		mV
Battery charge voltage regulation	V _{BATT_REG}	VBATT = 4.2V	4.179	4.2	4.221	V
		VBATT = 4.35V	4.328	4.35	4.372	V
Charge current regulation range	I _{CC_RANGE}		0		5000	mA
Charge current step	I _{CC_STEP}			80		mA
Fast charge current	I _{CC}	ICC = 1040mA, V _{BATT} = 3.8V	0.98	1.04	1.15	A
		ICC = 2000mA, V _{BATT} = 3.8V	1.9	2	2.1	A
Pre-charge to fast charge threshold	V _{BATT_PRE}	V _{BATT} rising, V _{PRE} = 3V	2.9	3	3.1	V
Pre-charge to fast charge threshold hysteresis		V _{BATT} falling, V _{PRE} = 3V		250		mV
Pre-charge current	I _{PRE}	IPRE = 240mA, V _{BATT} = 2.5V	207.5	240	277.5	mA
Charge termination current threshold	I _{TERM}	ITERM = 120mA	90	120	150	mA
		ITERM = 30mA	18	30	42	mA
Trickle charge to pre-charge threshold	V _{BATT_TC}	V _{BATT} rising	1.9	2	2.1	V
Trickle charge to pre-charge threshold hysteresis		V _{BATT} falling		200		mV
Trickle charge current	I _{TC}	V _{BATT} = 1V, I _{TRICKLE} = 128mA	100	128	160	mA
Auto-recharge battery voltage threshold	V _{RECH}	V _{BATT} falling, V _{RECHG} = 100mV	45	90	135	mV
		V _{BATT} falling, V _{RECHG} = 200mV	135	190	245	mV
Input Regulation (T _A = 0°C to 70°C)						
Input minimum voltage regulation	V _{IN_LIM}	V _{IN_LIM} = 3.88V, V _{BATT} = 3.3V	3.758	3.88	4.002	V
		V _{IN_LIM} = 4.36V, V _{BATT} = 3.3V	4.236	4.36	4.484	V
Input minimum voltage regulation tracking battery	V _{IN_LIM_BATT}	V _{IN_LIM} = 3.88V, V _{BATT} = 4V	70	165	285	mV
Input current limit	I _{IN_LIM}	I _{IN_LIM} = 500mA	415	450	500	mA
		I _{IN_LIM} = 1.5A	1.34	1.41	1.5	A
		I _{IN_LIM} = 3A	2.7	2.84	3	A
Battery Over-Voltage Protection (OVP)						
Battery OVP threshold	V _{BATT_OVP}	V _{BATT} rising, percentage of V _{BATT_REG}	103	105	106.5	%
Battery OVP hysteresis				1.7		%
Thermal						
Junction temperature regulation ⁽⁸⁾	T _{J_REG}	T _{REG} = 80°C		80		°C
		T _{REG} = 120°C		120		°C
Thermal shutdown rising junction temperature ⁽⁸⁾	T _{J_SHDN}	Temperature rising		150		°C
Thermal shutdown hysteresis ⁽⁸⁾	T _{SHDN_HYS}			30		°C

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
JEITA NTC Monitor (T _A = 0°C to 70°C)						
NTC cold temperature rising threshold	V _{COLD}	As a percentage of V _{VRNTC} , V _{COLD} = 74.2% (0°C)	73.9	74.5	75.1	%
NTC cold temperature rising threshold hysteresis		As a percentage of V _{VRNTC}		1.4		%
NTC cool temperature rising threshold	V _{COOL}	As a percentage of V _{VRNTC} , V _{COOL} = 64.8% (10°C)	64.3	64.9	65.5	%
NTC cool temperature rising threshold hysteresis		As a percentage of V _{VRNTC}		1.4		%
NTC warm temperature falling threshold	V _{WARM}	As a percentage of V _{VRNTC} , V _{WARM} = 32.6% (45°C)	31.9	32.5	33.1	%
NTC warm temperature falling threshold hysteresis		As a percentage of V _{VRNTC}		1.4		%
NTC hot temperature falling threshold	V _{HOT}	As a percentage of V _{VRNTC} , V _{HOT} = 23% (60°C)	22.7	23.3	23.9	%
NTC hot temperature falling threshold hysteresis		As a percentage of V _{VRNTC}		1.4		%
BATTFET Over-Current Protection (OCP)						
BATTFET over-current (OC) threshold	I _{BATT_OCP}		7			A
PWM Converter						
Switching frequency	f _{SW}	SW_FREQ = 750kHz	630	750	895	kHz
		SW_FREQ = 1000kHz	900	1050	1280	kHz
		SW_FREQ = 1250kHz	1060	1250	1450	kHz
		SW_FREQ = 1500kHz	1260	1475	1680	kHz
Boost						
Boost regulation voltage	V _{PMID_REG}	V _{BOOST} = 5.15V, T _A = -40°C to +85°C	5.08	5.15	5.22	V
BATT_LOW comparator falling threshold	V _{BATT_LOW}	BATT_LOW = 3V	2.88	3	3.12	V
		BATT_LOW = 3.3V	3.2	3.33	3.46	V
BATT_LOW comparator hysteresis				200		mV
BATT_LOW comparator debounce time	t _{D_BATT_LOW}			10		ms
Boost output current limit	I _{BST_LIM}	OLIM = 500mA, T _A = 0°C to 70°C	500		615	mA
		OLIM = 1.5A, T _A = 0°C to 70°C	1500		1700	mA
Boost OVP threshold	V _{BST_OVP}	Boost mode, V _{IN} rising	5.5	5.8	6.1	V
VCC LDO						
VCC output voltage	V _{VCC}	V _{IN} = 5V, I _{VCC} = 5mA		3.65		V
IB Output (T _A = 0°C to 70°C)						
IB current output gain	I _{IB}	I _{IB} , charging, I _{BATT} = 100mA	1.1	2	2.8	μA
		I _{IB} , charging, I _{BATT} = 1A	18.2	20	22.1	μA
		I _{IB} , discharging, I _{BATT} = 100mA	1.1	2	2.8	μA
		I _{IB} , discharging, I _{BATT} = 1A	18.2	20	22.1	μA

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Impedance Test						
Input impedance test current	I _{VIN_SRC}	IVIN_SRC = 10μA	6	10	14	μA
		IVIN_SRC = 40μA	28	40	52	μA
		IVIN_SRC = 320μA	240	320	405	μA
Input impedance test voltage threshold	V _{VIN_TEST}	VIN_TEST = 0.5V	0.46	0.5	0.54	V
		VIN_TEST = 1.5V	1.4	1.5	1.6	V
Logic I/O for SCL, SDA, INT, RST, STAT						
Logic input low voltage	V _{IL}				0.4	V
Logic input high voltage	V _{IH}		1.3			V
Open-drain output low voltage	V _{OL}	I _{SINK} = 10mA			0.2	V
RST pull-up resistor	R _{PULL_UP}			200		kΩ
D+/D- Detection						
DCD D+ pull up current	I _{DP_SRC}		7	10	13	μA
DCD D- pull low resistance	R _{DM_DWN}		16	20	24	kΩ
D+/D- source voltage low	V _{SRC_L}		550	600	650	mV
D+/D- source voltage high	V _{SRC_H}		3.1	3.3	3.5	V
D+/D- sink current	I _{SNK}		50	100	150	μA
Data detect voltage	V _{DAT_REF}		300	350	400	mV
Non-standard 1.2V window	V _{1P2_TH}	Low threshold	0.95	1	1.05	V
		High threshold	1.33	1.4	1.47	V
Non-standard 2V window	V _{2P0_TH}	Low threshold	1.73	1.8	1.87	V
		High threshold	2.17	2.25	2.33	V
Non-standard 2.7V window	V _{2P7_TH}	Low threshold	2.3	2.4	2.5	V
		High threshold	2.9	3	3.1	V
USB Type-C CC Detection						
CC1 and CC2 pull-down resistance	R _{RD}		4.6	5.1	5.6	kΩ
CC1 and CC2 pull-up current source	I _{RP}	RP_CFG = 80μA	70	80	90	μA
		RP_CFG = 180μA	165	180	195	μA
		RP_CFG = 330μA	305	330	350	μA
Sink port vRd-Connect threshold	V _{RD_CNCT}		0.17	0.2	0.23	V
Sink port vRd-USB threshold	V _{RD_USB}		0.63	0.66	0.69	V
Sink port vRd-1.5 threshold	V _{RD_1P5}		1.22	1.26	1.3	V
Source port vRd-USB threshold	V _{SRC_RD_1}	RP_CFG = 80μA, low threshold	0.17	0.2	0.23	V
		RP_CFG = 80μA, high threshold	1.55	1.6	1.65	V
Source port vRd-1.5A threshold	V _{SRC_RD_2}	RP_CFG = 180μA, low threshold	0.37	0.4	0.43	V
		RP_CFG = 180μA, high threshold	1.55	1.6	1.65	V

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

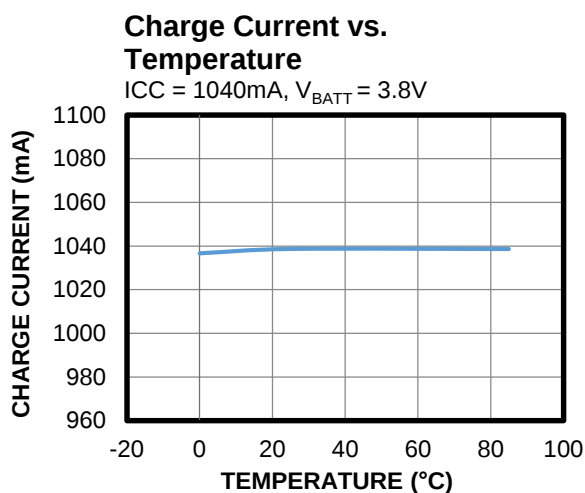
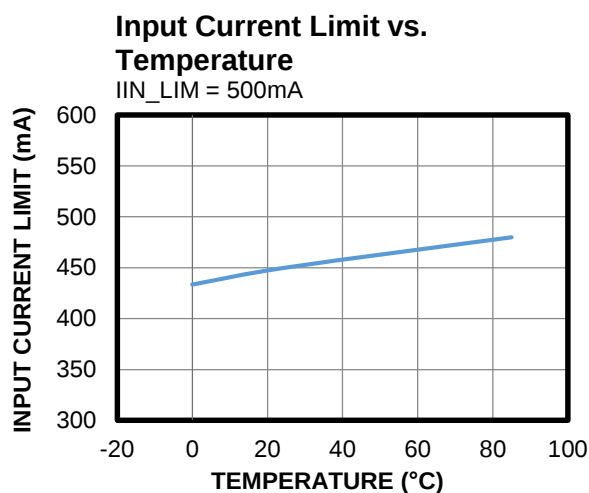
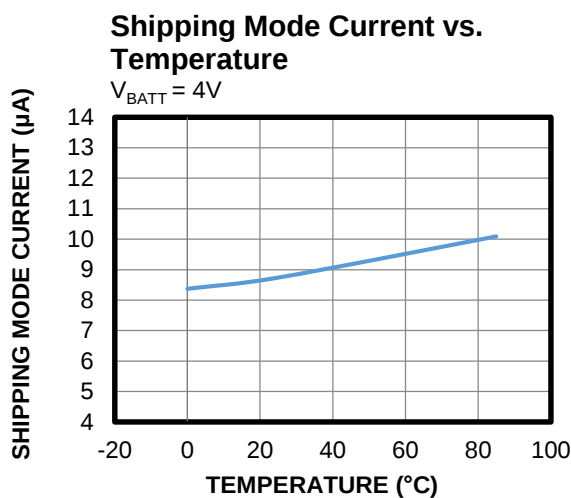
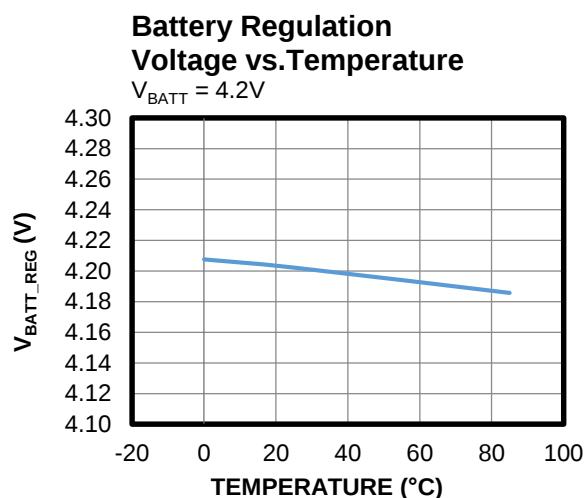
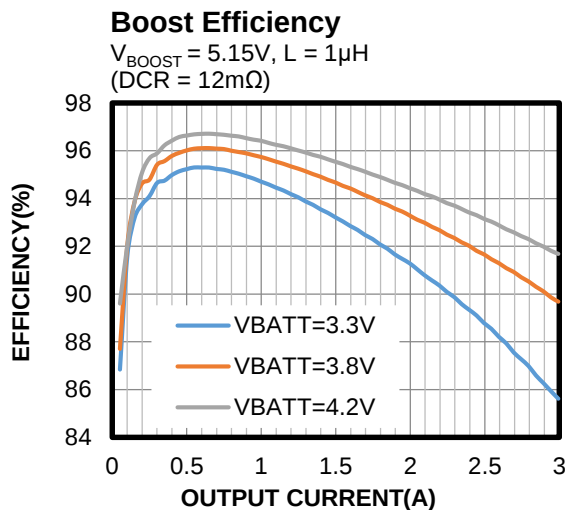
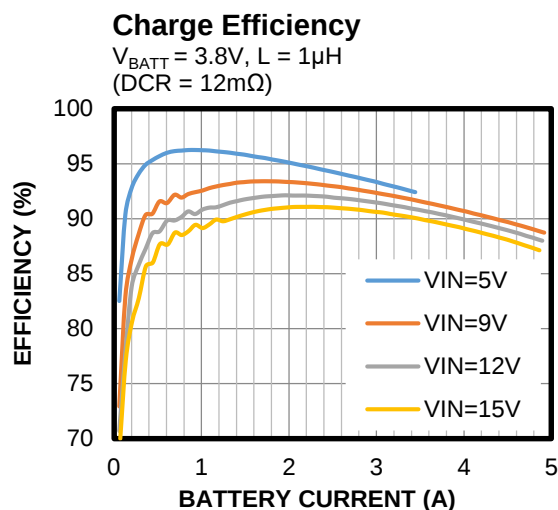
Parameters	Symbol	Condition	Min	Typ	Max	Units
Source port vRd-3A threshold	V _{SRC_RD_3}	RP_CFG = 330μA, low threshold	0.81	0.84	0.88	V
		RP_CFG = 330μA, high threshold	2.5	2.6	2.7	V
USB Type-C attachment debounce time	t _{CC_DEBOUNCE}		120	150	180	ms
CC pin debounce time for PD	t _{PD_DEBOUNCE}		12	15	18	ms
USB Type-C resistor (Rp) value change debounce time	t _{RP_CHANGE}		12	15	18	ms
DRP toggle period	t _{DRP}		70	80	90	ms
Duty cycle of advertised source port	d _{C SRC_DRP}		40	50	60	%
Try.SRC wait time	t _{DRP_TRY}		90	120	135	ms
Try.SRC debounce time	t _{TRYCCDEB}		12	15	18	ms
Try.SRC timeout	t _{TRYTIMEOUT}		900	1000	1100	ms
Timing						
Start-Up						
Legacy cable timer	t _{LEGACY}		65	75	85	ms
Battery Charger						
Charge termination deglitch time	t _{TERM_DGL}			250		ms
Charge timer	t _{CHG_TMR}	CHG_TIMER = 10hr	8	10	12	hr
Top-off timer	t _{TOP_OFF}	TOPOFF_TIMER = 30min	24	30	36	min
Battery auto-recharge deglitch time	t _{RECH_DGL}			100		ms
RST Timing						
RST low time to exit shipping mode	t _{SHIPMODE}		0.9	1.1	1.3	sec
RST low time to reset BATTFET	t _{RST}		8	10	12	sec
BATTFET reset time	t _{SYS_RST}		250	330	400	ms
Enter shipping mode delay	t _{SHIP_DLY}		10	12	15	sec
Watchdog and Clock						
Watchdog timer	t _{WDT}	WATCHDOG = 40s		40		sec
I ² C clock	f _{SCL}				400	kHz

Notes:

8) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$, $V_{BATT} = \text{full range}$, I²C-controlled, $I_{CC} = 2A$, $I_{IN_LIM} = 3A$, $V_{IN_MIN} = 4.36V$, $L = 1\mu H$ (DCR = 12mΩ), $T_A = 25^\circ C$, unless otherwise noted.

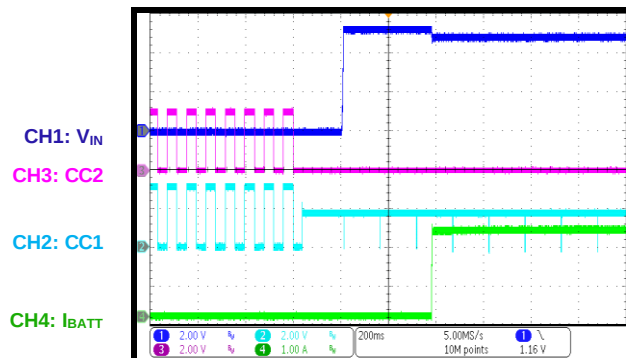


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 5V$, $V_{BATT} = \text{full range}$, I²C-controlled, $I_{CC} = 2A$, $I_{IN_LIM} = 3A$, $V_{IN_MIN} = 4.36V$, $L = 1\mu H$ (DCR = 12mΩ), $T_A = 25^\circ C$, unless otherwise noted.

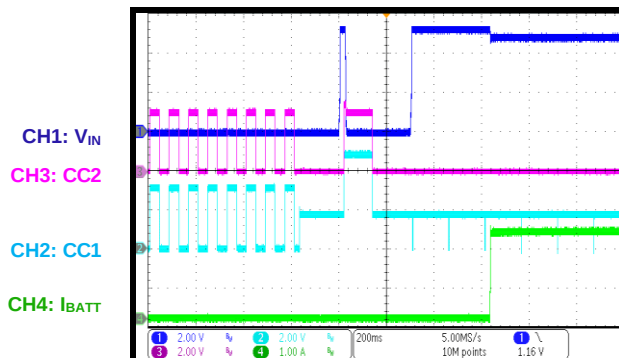
Adapter Plugged In

$I_{CC} = 2A$, $V_{BATT} = 3.3V$, $I_{SYS} = 0A$, DRP mode



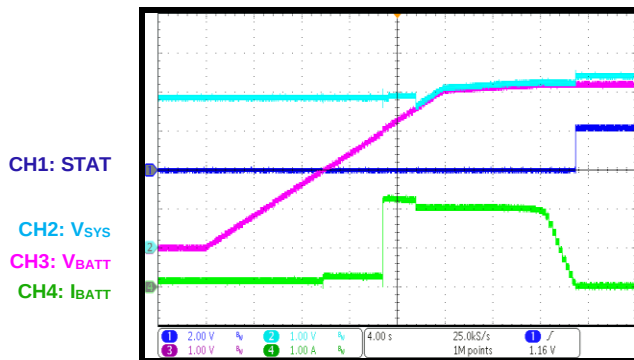
Adapter Plugged In

$I_{CC} = 2A$, $V_{BATT} = 3.3V$, $I_{SYS} = 0A$, DRP mode with Try.SRC



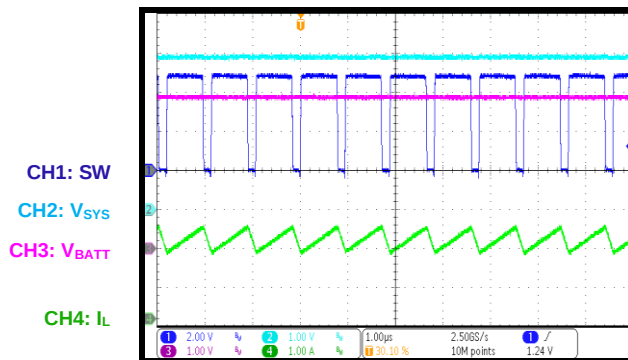
Battery Charge Profile

$V_{IN} = 5V$, $I_{CC} = 2A$, $I_{SYS} = 0A$



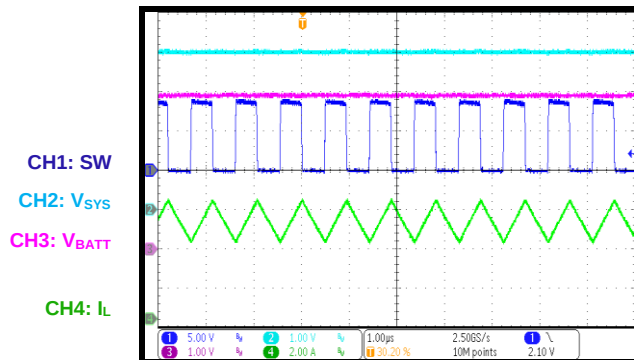
Charge Steady State

$V_{IN} = 5V$, $V_{BATT} = 3.8V$, $I_{CC} = 2A$, $I_{SYS} = 0A$



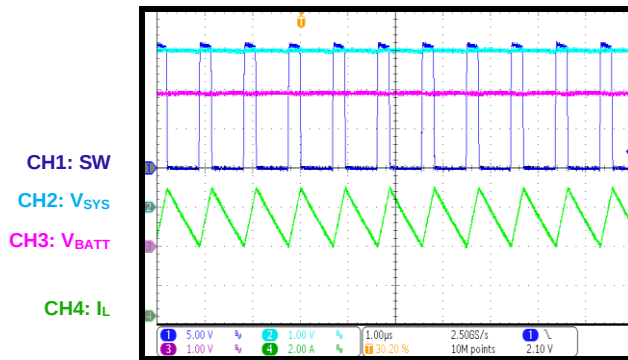
Charge Steady State

$V_{IN} = 9V$, $V_{BATT} = 3.8V$, $I_{CC} = 5A$, $I_{SYS} = 0A$



Charge Steady State

$V_{IN} = 16V$, $V_{BATT} = 3.8V$, $I_{CC} = 5A$, $I_{SYS} = 0A$

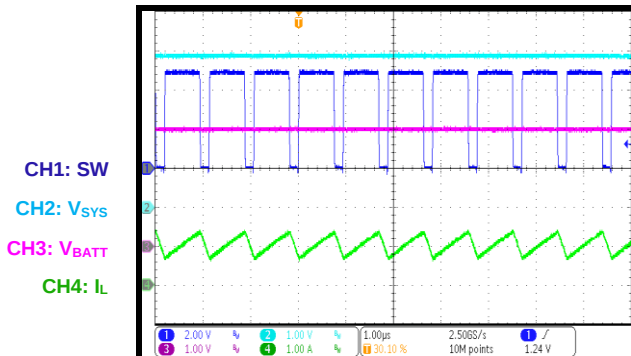


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 5V$, $V_{BATT} = \text{full range}$, I²C-controlled, $I_{CC} = 2A$, $I_{IN_LIM} = 3A$, $V_{IN_MIN} = 4.36V$, $L = 1\mu H$ (DCR = 12mΩ), $T_A = 25^\circ C$, unless otherwise noted.

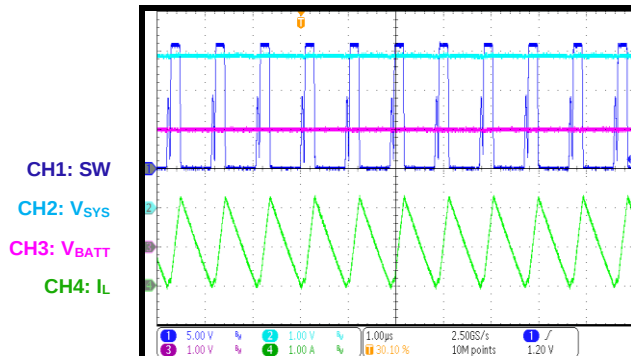
Charge Disable Steady State

$V_{IN} = 5V$, $V_{BATT} = 3V$, $I_{SYS} = 1A$



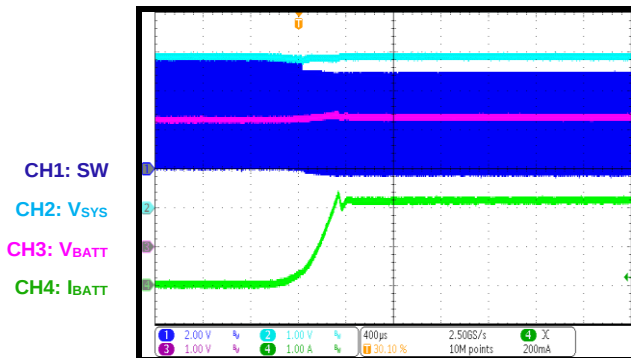
Charge Disable Steady State

$V_{IN}=16V$, $V_{BATT}=3V$, Charge disable, $I_{SYS}=1A$



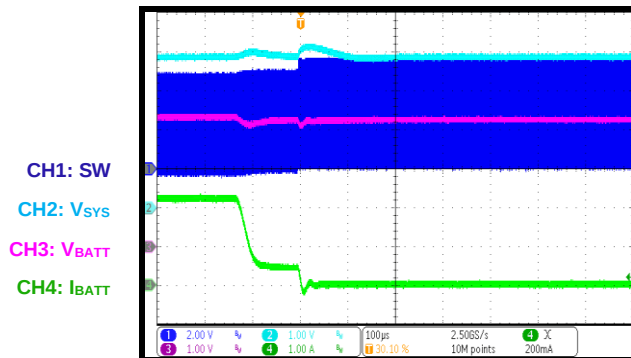
Charge Enabled

$V_{IN} = 5V$, $V_{BATT} = 3.3V$, $I_{CC} = 2A$, $I_{SYS} = 0A$



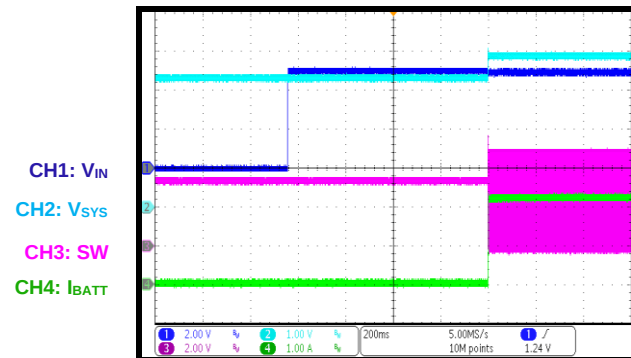
Charge Disabled

$V_{IN} = 5V$, $V_{BATT} = 3.3V$, $I_{CC} = 2A$, $I_{SYS} = 0A$



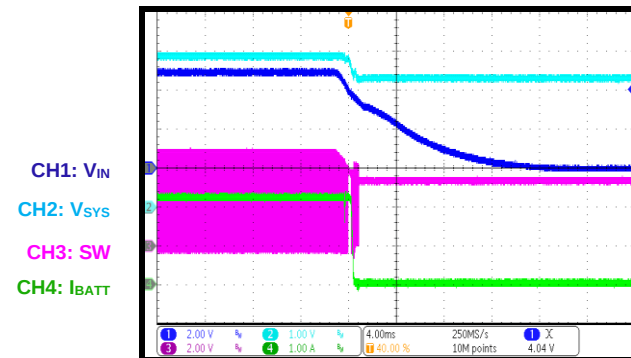
Start-Up

$V_{IN} = 5V$, $V_{BATT} = 3.3V$, $I_{CC} = 2A$, $I_{SYS} = 0A$



Shutdown

$V_{IN} = 5V$, $V_{BATT} = 3.3V$, $I_{CC} = 2A$, $I_{SYS} = 0A$



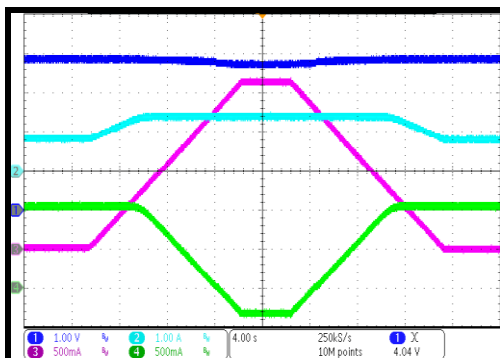
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 5V$, $V_{BATT} = \text{full range}$, I²C-controlled, $I_{CC} = 2A$, $I_{IN_LIM} = 3A$, $V_{IN_MIN} = 4.36V$, $L = 1\mu H$ (DCR = 12mΩ), $T_A = 25^\circ C$, unless otherwise noted.

Input Current Limit

$V_{IN} = 5V$, $I_{IN_LIM} = 1500mA$, $V_{BATT} = 3.8V$,
 $I_{CC} = 1040mA$

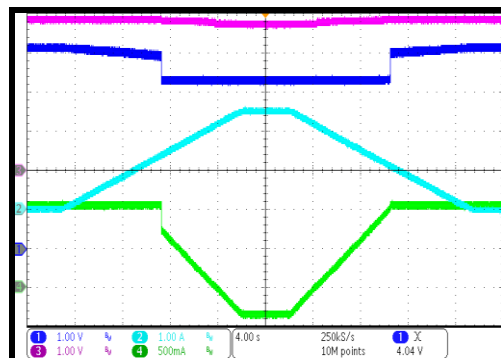
CH2: I_{IN}
CH1: V_{SYS}
CH3: I_{SYS}
CH4: I_{BATT}



Input Voltage Limit

$V_{IN} = 5V$ (2A), $I_{IN_LIM} = 3000mA$, $V_{BATT} = 3.8V$,
 $I_{CC} = 1040mA$

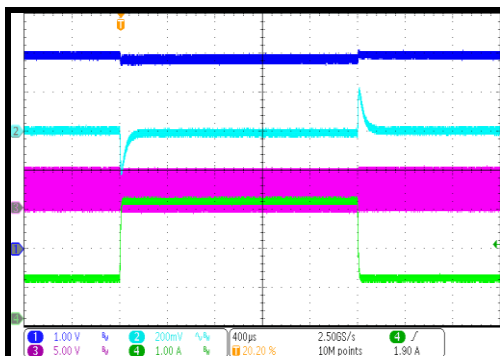
CH3: V_{SYS}
CH2: I_{SYS}
CH1: V_{IN}
CH4: I_{BATT}



SYS Load Transient

$V_{IN} = 5V$, $V_{BATT} = 3.3V$, charge disabled,
 $I_{SYS} = 1A$ to $3A$

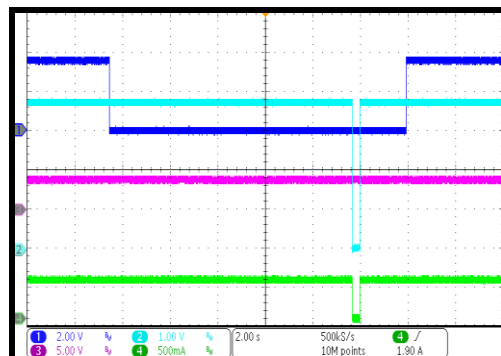
CH2: $V_{SYS/AC}$
CH3: SW
CH1: V_{IN}
CH4: I_{SYS}



BATTFET Reset

$V_{BATT} = 3.8V$, $I_{SYS} = 0.5A$

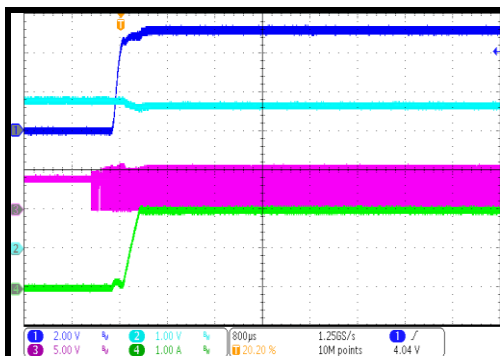
CH1: /RST
CH3: V_{BATT}
CH2: V_{SYS}
CH4: I_{SYS}



OTG Mode On

$V_{BATT} = 3.8V$, $V_{BOOST} = 5.15V$, $I_{OTG} = 2A$

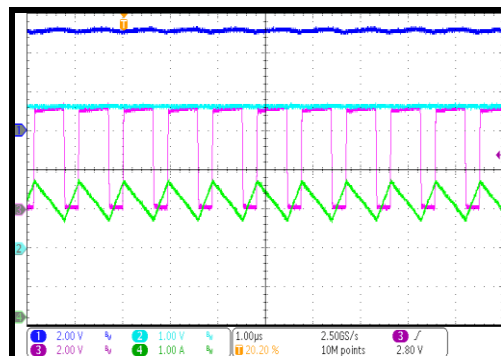
CH1: V_{IN}
CH3: SW
CH2: V_{BATT}
CH4: I_{OTG}



OTG Steady State Operation

$V_{BATT} = 3.8V$, $V_{BOOST} = 5.15V$, $I_{OTG} = 2A$

CH1: V_{IN}
CH3: SW
CH2: V_{BATT}
CH4: I_L



FUNCTIONAL BLOCK DIAGRAM

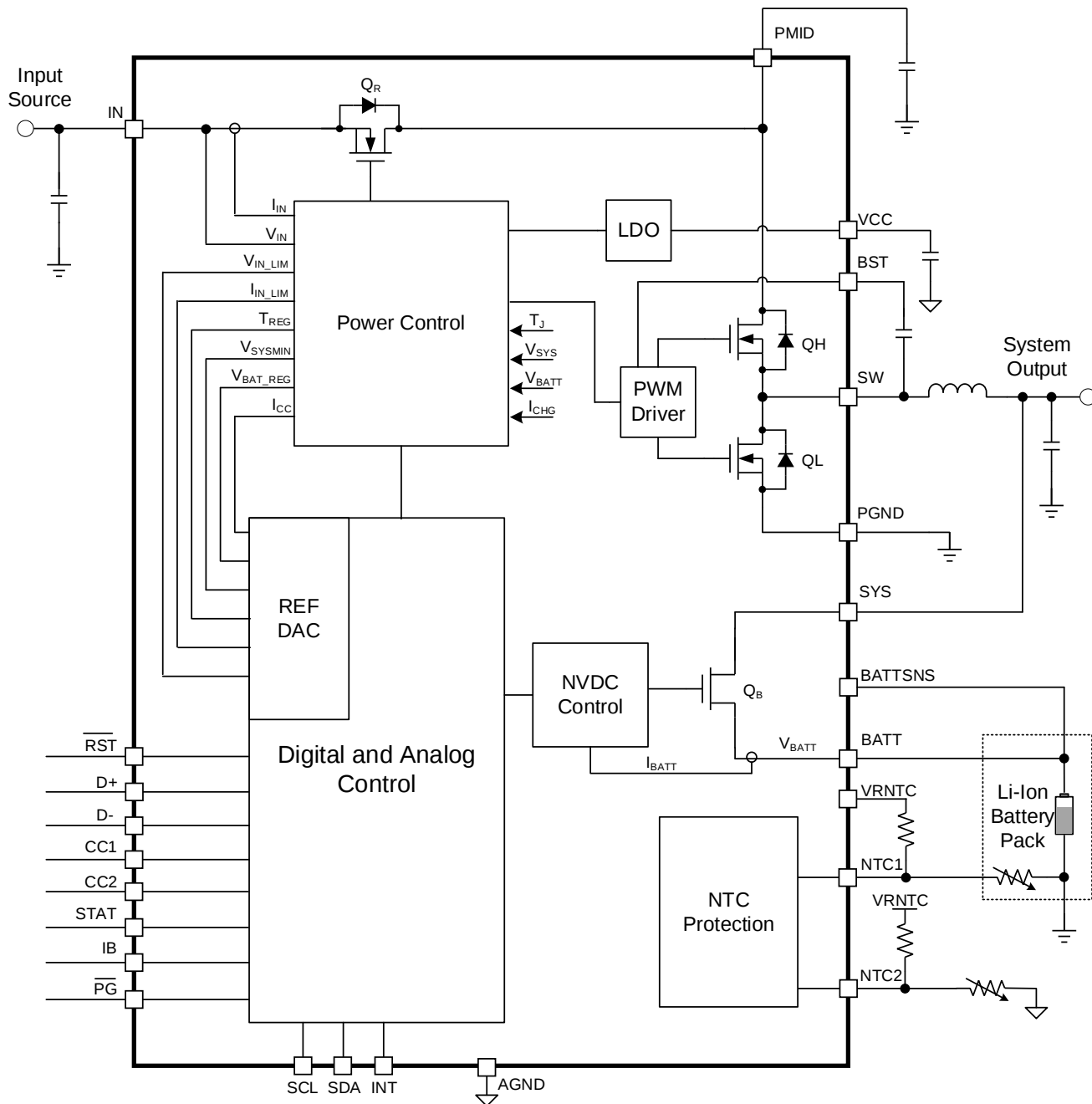


Figure 2: Functional Block Diagram

OPERATION

The MP2722 is a highly integrated, I²C-controlled, switch-mode battery charger IC with narrow-voltage DC (NVDC) power path management for the single-cell lithium-ion or lithium-polymer battery applications. The MP2722 integrates the reverse blocking MOSFET (RB-FET, Q_R), high-side switching MOSFET (HS-FET, Q_H), low-side switching MOSFET (LS-FET, Q_L), battery MOSFET (BATTFET, Q_B), and a USB Type-C 1.3 compliant, dual-role power (DRP), CC controller.

VCC Regulator

The VCC regulator is powered from the higher voltage between the BATT and PMID pins. The VCC pin requires an external 4.7μF bypass capacitor. The VCC pin provides power for the internal circuits and the gate drivers. When VCC pin voltage (V_{VCC}) exceeds the VCC under-voltage lockout (UVLO) threshold (V_{VCC_UV}), the I²C interface is ready for communication, and all of the registers are reset to their default values. The VCC pin can be used for external logic pull-up, but is not recommended for excess loads.

Battery Power-On

If an input source is not available, the battery is connected, and the battery voltage (V_{BATT}) exceeds the BATT UVLO threshold (V_{BATT_UV}), the BATTFET turns on and powers up the system. The low quiescent current and low voltage drop on BATTFET minimize battery consumption and maximize the battery runtime. The BATTFET's discharge current is monitored. If the system is overloaded or shorted to ground (I_{BATT} > I_{BATT_OCP}), the device turns off BATTFET immediately and sets the BATTFET_DIS bit to 1. The BATTFET can be re-enabled following the methods described in the Exiting Shipping Mode section on page 21.

Input Power-On

When an input source is plugged in, the IC detects the input source type and sets the input current limit (I_{IN_LIM}) before the buck converter starts. The start-up sequence from the input source is described in detail below:

1. The input voltage (V_{IN}) is detected.
2. The hold-off timer (about 250ms) runs.

3. Input source type detection starts.
4. I_{IN_LIM} is set.
5. If EN_BUCK = 1, the buck converter starts.
6. If EN_CHG = 1, charging starts.

Hold-Off Timer

When a valid input source is detected, the IC runs a hold-off timer (t_{HOLD}, typically about 250ms) before detecting the input source type. t_{HOLD} can be bypassed by setting HOLDOFF_TMR bit to 0.

Input Source Type Detection

The IC runs D+/D- detection when all of the following conditions are met:

- V_{IN} exceeds V_{IN_UV}
- V_{IN} is below V_{IN_OV}
- VIN_GD = 1
- t_{HOLD} ends
- AUTODPDM = 1, or FORCEDPDM is set

D+/D- detection includes the USB Battery Charging Specification 1.2 (BC1.2), non-standard adapter applications, and adjustable high-voltage adapter handshake. BC1.2 detection begins with data contact detection (DCD). If DCD detection is successful, the standard downstream port (SDP), dedicated charging port (DCP), and charging downstream port (CDP) are distinguished by primary and secondary detection. If the DCD timer expires, then non-standard adapter detection is initiated. Table 1 lists the criteria for non-standard adapter detection.

Table 1: Non-Standard Adaptor Detection

Adaptor Type	D+ Voltage	D- Voltage
Divider 1	V _{D+} within V _{2P0_TH}	V _{D-} within V _{2P7_TH}
Divider 2	V _{D+} within V _{2P7_TH}	V _{D-} within V _{2P0_TH}
Divider 3	V _{D+} within V _{2P7_TH}	V _{D-} within V _{2P7_TH}
Divider 4	V _{D+} within V _{1P2_TH}	V _{D-} within V _{1P2_TH}
Divider 5	V _{D+} within V _{2P7_TH}	V _{D-} > V _{2P7_TH}

Once a DCP is detected, the device is ready to detect a high-voltage adapter. Once a high-voltage adapter is detected, DPDM_STAT is set to 1001, an INT pulse is generated, and the

device is ready to configure the D+/D- pins via register 0Bh.

If AUTODPDM = 0, then D+/D- detection is bypassed and the DPDM_STAT bits remain set to 0000.

Table 2 lists the I_{IN_LIM} settings from D+/D- detection.

Table 2: Input Current Limit Setting by D+/D- Detection

D+/D- Detection	Input Current Limit
Not started	500mA
USB SDP	500mA
USB DCP	2A
USB CDP	1.5A
Divider 1	1A
Divider 2	2.1A
Divider 3	2.4A
Divider 4	2A
Divider 5	3A
Unknown	500mA
High-voltage adapter	2A

USB Type-C Sink Detection

In USB Type-C sink mode, the CC1 and CC2 pins are connected to AGND via a 5.1kΩ resistor (Rd). The CC1 and CC2 voltages are monitored. The sink power sub-state is determined by the monitored CC pin voltage (see Table 3).

Table 3: USB-C Sink Power Sub-States by CC Voltage

CC Detection Result	CC Voltage	Min	Max
Type-C default USB	vRd-USB	0.25V	0.61V
Type-C 1.5A current	vRd-1.5	0.70V	1.16V
Type-C 3A Current	vRd-3	1.31V	2.04V

Input Current Limit (I_{IN_LIM}) Setting

After input source type detection finishes, the following actions are executed:

- The CC1_SNK_STAT or CC2_SNK_STAT bits are updated
- The DPDM_STAT bits are updated
- I_{IN_LIM} is updated
- The VIN_RDY bit is set to 1

When the VIN_RDY bit is set, an INT pulse asserts and I_{IN_LIM} is updated (see Table 4). The host can overwrite the I_{IN_LIM} registers to modify I_{IN_LIM}.

Table 4: Input Current Limit Setting

CC Detection Result	Input Current Limit
Type-C default USB or CC_CFG is disabled	D+/D- detection result (500mA if AUTODPDM = 0)
Type-C 1.5A current	1.5A
Type-C 3A current	3A
vRa (V _{IN} is present, but no voltage is detected on the CC pin)	500mA

If the monitored CC pin changes after the USB Type-C resistor (Rp) change debounce time (t_{RP_CHANGE}) (typically 15ms), then I_{IN_LIM} updates. An INT pulse follows this action.

If the FORCEDPDM bit is set to 1, then D+/D- detection restarts. Once D+/D- detection finishes, the DPDM_STAT bits and I_{IN_LIM} updates. An INT pulse follows this action.

Input Voltage Limit (V_{IN_LIM}) Setting

The MP2722 supports a configurable input voltage limit (V_{IN_LIM}). If V_{IN} drops to V_{IN_LIM} due to the input source capability or a cable voltage drop, then the duty cycle is limited to prevent V_{IN} from dropping further. This reduces the converter's total output current.

If the EN_VIN_TRK bit is set to 0, then the absolute V_{IN_LIM} is set by the VIN_LIM register. If the EN_VIN_TRK bit is set to 1, then V_{IN_LIM} is the maximum value between the VIN_LIM register's setting and (V_{BATT} + 165mV).

Buck Converter and Charger Start-Up

After the VIN_RDY bit is set to 1, the buck converter soft starts if EN_BUCK = 1. The buck converter's switching frequency (f_{sw}) can be set between 750kHz and 1.5MHz. Peak current mode control is adopted to regulate the system voltage (V_{sys}), battery charge current, battery regulation voltage (V_{BATT_REG}), I_{IN_LIM}, V_{IN_LIM}, and the device die temperature loops.

If the EN_CHG bit is set to 1, the device automatically starts charging.

NVDC Battery MOSFET (BATTFET)

Using the NVDC structure, the BATTFET separates the system from the battery and controls the battery charging and discharging.

With power path management, the device prioritizes the system (SYS) output by utilizing the input source, battery, or both.

When the input source is absent, the BATTFET turns fully on to pass the battery power to the system via the ultra-low impedance path. When the input source is present and the buck converter has started up, the system output is related to V_{BATT} in the following ways:

1. When V_{BATT} is below the minimum system voltage setting (V_{SYS_MIN}), V_{SYS} is regulated to ($V_{SYS_MIN} + V_{TRACK}$), where V_{TRACK} is typically 150mV. Depending on V_{BATT} , the BATTFET works in linear mode to charge the battery with a trickle-charge, pre-charge, or fast charge current.
2. Once V_{BATT} exceeds V_{SYS_MIN} , the BATTFET turns on fully and the voltage difference between V_{SYS} and V_{BATT} is the BATTFET resistive voltage drop.
3. When charging is disabled or terminated, V_{SYS} is always regulated to V_{TRACK} plus the higher value between V_{SYS_MIN} and V_{BATT} . In this scenario, V_{TRACK} is typically 100mV.

The status register V_{SYS_STAT} indicates whether the system is in V_{SYS_MIN} regulation.

Figure 3 shows V_{SYS} regulation as V_{BATT} changes.

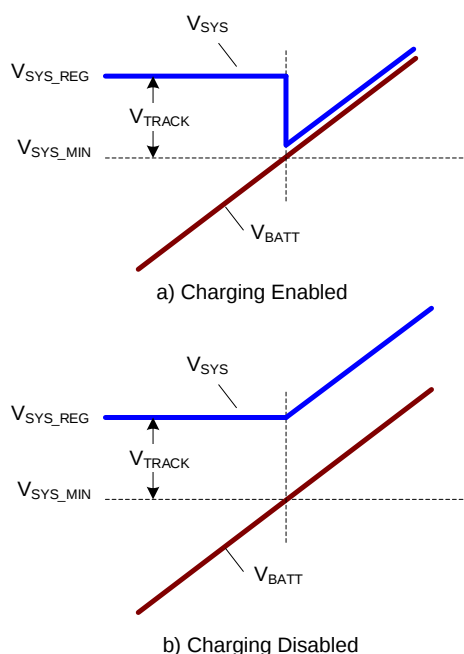


Figure 3: V_{SYS} Regulation with V_{BATT}

Dynamic Power Management

During the buck converter operation, the MP2722 continuously monitors the input current (I_{IN}) and V_{IN} . If I_{IN_LIM} or V_{IN_LIM} is reached, the charge current is reduced to prevent the input source from being overloaded.

If the charge current is reduced to 0A, V_{SYS} starts to drop due to input power limitation. Once the V_{SYS} falls below V_{BATT} , the IC automatically enters supplement mode.

If the converter operates in input current loop or input voltage loop, the $IINDPM_STAT$ or $VINDPM_STAT$ bit is set to 1, respectively. This is followed by a maskable INT pulse.

Supplement Mode

If V_{SYS} drops below V_{BATT} , the BATTFET turns on to prevent V_{SYS} from dropping further. In this scenario, the buck converter and the battery work together to provide power for the system.

Battery Charging

The MP2722 can autonomously run a charging cycle without host involvement. The host can also control the charge operations and parameters via the registers.

A new charge cycle starts when all of the below conditions are met:

- The buck converter has started up
- The NTC pin's (NTC1 and NTC2) voltages are within the acceptable ranges
- BATTFET is on ($BATTFET_DIS = 0$)
- Charging is enabled ($EN_CHG = 1$)

Charging Profile

The MP2722 detects V_{BATT} to provide four main charging phases: trickle-charge, pre-charge, constant-current charge, and constant-voltage charge (see Table 5).

Table 5: Charge Current Setting

Battery Voltage (V_{BATT})	Charge Current	Default Value	CHG_STAT
$V_{BATT} < V_{BATT_TC}$	$I_{TRICKLE}$	128mA	001
$V_{BATT_TC} \leq V_{BATT} < V_{BATT_PRE}$	I_{PRE}	240mA	010
$V_{BATT_PRE} \leq V_{BATT} < V_{BATT_REG}$	I_{CC}	2A	011
$V_{BATT} = V_{BATT_REG}$	$<I_{CC}$	-	100

Throughout the charging process, the actual charge current may be below the register setting due to other regulation loops, such as the input current loop, input voltage loop, or thermal regulation. In this scenario, charge termination is blocked and the charge timer counts at half of its usual speed. Figure 4 shows the battery charging profile.

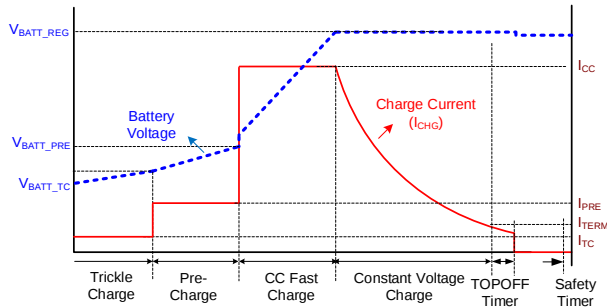


Figure 4: Battery Charging Profile

Charge Termination

If all the following conditions are met, charging is terminated:

- Termination is enabled ($EN_TERM = 1$)
- The charge current is below the termination threshold for t_{TERM_DGL} (about 250ms)
- The device is charging in the constant-voltage phase
- The device is not in an input current or input voltage loop
- The device is not in thermal regulation

After termination, the status register CHG_STAT is set to 101, the STAT pin indicator goes high, and an INT pulse is generated.

To restart a new charge cycle once charging terminates, re-plug in the input source or toggle the EN_CHG bit.

To fully charge the battery, a top-off timer can be applied after termination is detected. The $TOPOFF_TIMER$ bits set the top-off timer. The $TOPOFF_ACTIVE$ bit is 1 when the top-off timer is active. A maskable INT pulse is generated when entering and exiting the top-off time. During top-off timer operation, charging continues, while the CHG_STAT bits and the STAT pin both indicate that charging is done.

The top-off timer can be reset by any of the

conditions listed below:

- Charging changes from disabled to enabled
- Recharging begins
- The REG_RST bit is set

Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system supplement mode or self-discharge. When V_{BATT} discharges to the recharge threshold, the MP2722 automatically starts a new charging cycle without requiring a manual charge cycle restart, as long as the input power is valid. There is a deglitch timer (t_{RECH_DGL} , about 100ms) to detect whether V_{BATT} is below the recharge threshold. An INT pulse asserts when automatic recharging starts.

JEITA Thermistor Qualification

The device supports the JEITA profile to manage the charging parameters by continuously monitoring the NTC1 and NTC2 pin voltages. Two independent negative temperature coefficient (NTC) thermistors with temperature sensing and flexible configurations are provided. The NTC1 and NTC2 pins can be enabled and disabled by setting the $NTC1_ACTION$ and $NTC2_ACTION$ bit, respectively.

The EN_PG_NTC2 bit should be set to 1 to enable NTC2 channel. When EN_PG_NTC2 bit is set to 0, there is only one NTC monitor.

If the corresponding NTC channel is enabled, the voltage on the NTC pin must be within the V_{HOT} to V_{COLD} range to initiate a charge cycle. If the NTC pin voltage is outside the V_{HOT} to V_{COLD} range, then the MP2722 suspends charging and waits for the NTC voltage to return to the standard range.

In the cool temperature range (V_{COLD} to V_{COOL}), the charge current and/or charge voltage are reduced according to the $COOL_ACT$, $JEITA_ISET$, and $JEITA_VSET$ settings.

In the warm temperature range (V_{WARM} to V_{HOT}), the charge voltage and/or charge current are reduced according to the $WARM_ACT$, $JEITA_ISET$, and $JEITA_VSET$ settings.

The V_{COLD} , V_{COOL} , V_{WARM} , and V_{HOT} thresholds all have four configurable percentage levels.

The temperature conditions can be read in the NTC1_FAULT and/or NTC2_FAULT bits. An INT pulse is generated when NTC1 or NTC2 condition changes.

The NTC1 and NTC2 pins share the same configurable thresholds Table 6 shows the detection priority when the detection results between the two NTC inputs are different.

Table 6: JEITA Detection Priority

NTC1 \ NTC2	Hot	Warm	Normal	Cool	Cold
Hot	Hot	Hot	Hot	Hot	Hot
Warm	Hot	Warm	Warm	Warm	Cold
Normal	Hot	Warm	Normal	Cool	Cold
Cool	Hot	Warm	Cool	Cool	Cold
Cold	Hot	Cold	Cold	Cold	Cold

For battery temperature protection during boost mode, if the NTC1_ACTION or NTC2_ACTION bit is set to 1, the device compares the NTC1 and/or NTC2 pin voltage with the V_{COLD} and V_{HOT} thresholds. If the NTC pin voltage is outside of V_{COLD} to V_{HOT} range, then boost mode is suspended. The NTC1_FAULT or NTC2_FAULT bit is also set to report the condition.

The preset hot, cold, warm, and cool voltage thresholds are defined for a $\beta = 3435$ thermistor. It is recommended to use a pull-up resistor with a value that matches the thermistor's resistance at 25°C.

Figure 5 shows the JEITA voltage/current regulations with the following set-up: NTC1_ACTION = 1, NTC2_ACTION = 0, WARM_ACT = 01, COOL_ACT = 10, JEITA_VSET = 00, and JEITA_ISET = 00.

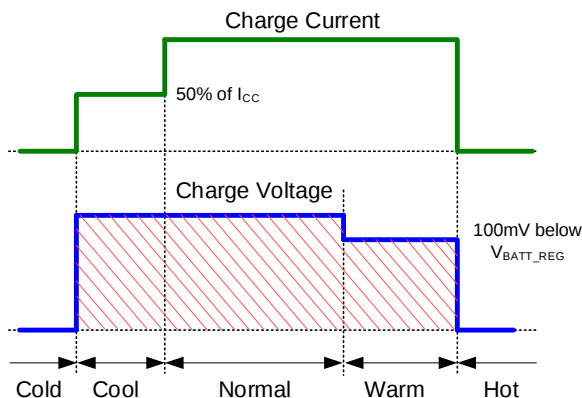


Figure 5: NTC Window under JEITA Control

Charging Safety Timer

The device has a built-in safety timer to prevent an extended charging cycle due to abnormal battery conditions. When V_{BATT} is below the V_{BATT_PRE} threshold, the safety timer is fixed to 2 hours. When V_{BATT} exceeds the V_{BATT_PRE} threshold, the safety timer is configured by CHG_TIMER bits. When the CHG_TIMER bits are set to 00, both the pre-charge timer and the fast-charge timer are disabled.

Charging is disabled after safety timer expires. Then the fault register's CHG_FAULT bit is set to 10, and an INT pulse is generated.

During an input current, input voltage, thermal regulation or JEITA cool/warm condition (when charge current reduction is enabled), the charge timer counts at half of its usual rate. This halved clock rate function can be disabled by setting the EN_TMR2X bit to 0.

The charging safety timer resets if any of the following conditions are met:

- The input source is unplugged
- EN_BUCK or EN_CHG is toggled
- The REG_RST bit is set

Remote Battery Voltage Sense

To minimize the parasitic trace resistance during charging, the BATTSENS pin can be connected to the actual battery pack's positive terminal. Remote sensing of the battery voltage accelerates the charging speed by helping the charger stay in constant-current charge mode for longer.

Shipping Mode

Entering Shipping Mode

When the host sets the BATTFET_DIS bit to 1, the MP2722 turns off the BATTFET immediately or after a delay time (t_{SHIP_DLY}), configured by the BATTFET_DLY bit.

Exiting Shipping Mode

When the MP2722 is in shipping mode (BATTFET_DIS = 1), either of the below events can wake up the BATTFET:

- An input source is applied
- The RST pin pulls low for t_{SHIPMODE}

BATTFET Reset

When the input source is absent, the system is powered by the battery through the BATTFET. The system can be forced to have a hardware power-on reset (POR) by changing the BATTFET status from on to off, then back to on.

For this function, the `RST` pin can be connected to the device's push-button. The `RST` pin is pulled up internally.

If the `RST` pin is driven low for t_{RST} while the input source is not plugged in and `BATTFET_DIS` = 0, the BATTFET turns off for t_{SYS_RST} , then it is enabled again (see Figure 6).

This function can be disabled by setting the `BATTFET_RST_EN` bit to 0.

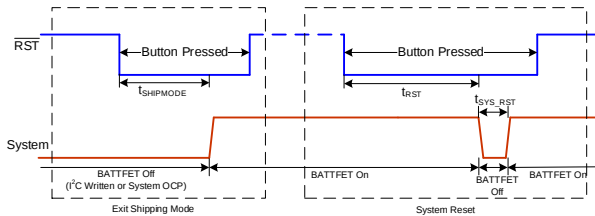


Figure 6: RST Timing

Power Good (PG) Indication

When `EN_PG_NTC2` is set to 0, the PG/NTC2 pin acts as the power good (PG) indicator. This pin goes low to indicate a good input source when all of the following conditions are met:

- V_{IN} exceeds V_{IN_UV}
- V_{IN} is below V_{IN_OV}
- The 15ms debounce timer has passed

STAT and IB Indication

When the `EN_STAT_IB` bit is set to 0, the charging status is indicated on the open-drain STAT/IB pin (see Table 7).

Table 7: STAT Indication

Charging State	STAT
Charging	Low
Charging is complete, top-off timer, boost mode, charging is disabled	High
Charging is suspended (due to battery OVP, input OVP, timer fault, or an NTC fault), boost mode is suspended (due to an NTC fault, OTP, or BATT_LOW)	Blinks at 1Hz

When `EN_STAT_IB` is set to 1, the STAT/IB pin acts as an analog current source output that indicates the value of the battery current flowing in or out of the battery. The current's direction can be read via the `BFET_STAT` bit. Connect a resistor load between the STAT/IB pin and AGND to sense the IB current. If `IB_EN` is set to 1, the IB output is always on. If `IB_EN` is set to 0, the IB output is only on when the device is switching.

The IB output voltage is between 0V and V_{CC} . The host can measure the IB voltage to make a software fuel gauge or monitor the peak discharge current.

Interrupts (INT)

A 256μs interrupt pulse is generated on the open-drain INT pin if any of the interrupt events occur. See the Interrupt List section on page 41 for more details.

Watchdog Functions (Bark and Bite)

After the first battery or V_{IN} start-up, the MP2722 operates with the default setup. The watchdog timer is expired by default when `WATCHDOG_FAULT` = 1. Writing 1 to `WATCHDOG_RST` starts the watchdog timer.

The watchdog timer has a bark function that generates an INT pulse when the watchdog timer is 3/4 of the way through its timer. The host can distinguish this condition by reading the `WATCHDOG_BARK` bit.

To maintain custom settings after the watchdog timer starts, write 1 to the `WATCHDOG_RST` bit before the watchdog timer expires. If the watchdog timer expires, the registers are reset according to the register table. After the watchdog timer expires, an INT pulse is sent and the `WATCHDOG_FAULT` bit is set to 1.

The watchdog timer can be disabled by setting the `WATCHDOG` bit to 00. If the watchdog timer is disabled, the registers keep their values until a POR.

Boost Mode

By boosting from the battery, the MP2722 is able to supply a regulated output at the IN pin. Boost mode starts once all of the following conditions are met:

- V_{IN} is below V_{IN_UV}

- The EN_BOOST bit is set to 1 by CC detection or by the host
- The voltages on the NTC pins (NTC1 and NTC2) are within the acceptable range
- V_{BATT} exceeds V_{BATT_UV}
- If BOOST_STP = 1, V_{BATT} must exceed V_{BATT_LOW}

The boost PWM's switching frequency is the same as the buck converter's setting.

The boost voltage loop regulates the PMID pin voltage at the value set by the VBOOST bits.

The boost output current loop limits the output current at the value set by the OLIM bits for the $V_{IN} > V_{BATT} + V_{HDMR}$ range.

The boost mode start-up sequence follows the steps below:

1. The converter soft starts and regulates the PMID voltage.
2. The blocking FET (Q_R) soft starts and regulates the discharge current from PMID to IN.
3. Once the IN pin starts up successfully, the boost is controlled to regulate the PMID voltage and the output current sensed through Q_R .

The boost converter's soft-start function allows the device to power into large capacitive loads on the IN pin.

USB Type-C Operation Modes

The MP2722 integrates a USB Type-C CC controller that supports multiple operation modes: sink-only, source-only, dual-role power (DRP), DRP with source preferred (try.SRC) and DRP with sink preferred (try.SNK). These operation modes can be configured with the CC_CFG bits. In addition to the modes being manually configurable, the MP2722 can function in any of the modes autonomously (without software intervention).

Sink Mode

The MP2722 can sink power from the input source, which presents R_d to AGND on the CC1 and CC2 pins. Set the CC_CFG bits to 000 to have the MP2722 act as a charger only, charging the battery once the input source is

detected by the IN pin.

The VIN_GD bit indicates whether a valid input source is detected. The CC1_SNK_STAT or CC2_SNK_STAT bits indicate the input source power advertisement.

Source Mode

Source mode is used for applications with the ability to start up external devices. The MP2722 can source power to the IN pin by boosting up from the battery. The device presents R_p pull-ups on the CC1 and CC2 pins. Set the CC_CFG bits to 001 to have the MP2722 generate a 5V output on the IN pin once a load is detected on either of the CC pins. The R_p value that advertises the source ability can be set via the RP_CFG bits.

The OTG_NEED bit indicates whether a valid external load is detected. The CC1_SRC_STAT or CC2_SRC_STAT bits can be read for the connection status on CC1 and CC2 pins.

DRP (Dual-Role Power) Mode

A DRP port can act as a sink or source. The MP2722 autonomously toggles between the sink (R_d) and source (R_p) on both the CC1 and CC2 pins for t_{DRP} (typically 80ms). t_{DRP} has a 50% duty cycle. The MP2722's role is determined automatically by the type of port plugged into it. The CC_CFG bits should be set to 010 for standard DRP mode.

In DRP mode, the same register bits and interrupts indicate the type of port that has been attached, as well as the source's power rating.

When the AUTOOTG is set to 1, the boost converter turns on/off via USB Type-C DRP detection, and the EN_BOOST bit is automatically updated. Writing 0 to the EN_BOOST bit can also turn off the boost converter during operation.

When the AUTOOTG bit is set to 0, the host turns the boost converter on/off by writing to the EN_BOOST bit. The host can determine the boost requirement with the OTG_NEED bit. This action is followed by an INT pulse.

Regardless of whether the MP2722 is operating in sink mode or source mode, the host can overwrite the EN_BOOST and/or EN_BUCK bit to turn the device on or off.

The debounced CC pin status can be read the in CC_SNK_STAT and CC_SRC_STAT bits. Any change in these bits is followed by a maskable INT pulse.

Forced Input Current Limit

When an input source is plugged in during sink mode, the MP2722 runs the start-up sequence and input source type detection. After detection finishes, I_{IN_LIM} is automatically generated. The I_{IN_LIM} result is returned by the IIN_LIM bits.

If the host does not want to use the automatically generated I_{IN_LIM} , there are two ways to set I_{IN_LIM} to different values via configuring either the IIN_MODE or IIN_LIM bits.

If the IIN_MODE bits are set to 000, the MP2722 runs with the automatically generated I_{IN_LIM} (returned by the IIN_LIM bits). However, once the VIN_RDY bit is set, the host can override the IIN_LIM bits to set I_{IN_LIM} to any value. This requires host involvement every time the converter starts up.

If the IIN_MODE bits are set to other values, I_{IN_LIM} is forced and fixed. For example, if the IIN_MODE bits are set to 101, the device always runs with a fixed 2000mA I_{IN_LIM} , ignoring the input source type detection.

Legacy Cable Detection

In sink mode, the MP2722 supports a legacy cable detection function. If the input source is plugged in through a Type-C to Type-C (C-C) cable, then V_{IN} is present after the CC1 and CC2 pins make contact for $\geq 100\text{ms}$. The adapter's Type-C port requires a debounce time ($t_{CC_DEBOUNCE}$) (between 100ms and 200ms) before it can turn on the V_{BUS} output. If a legacy Type-A to Type-C (A-C) cable is used, there is no debounce time.

A legacy cable timer (t_{LEGACY} , 75ms) starts once the CC1 or CC2 pin detects a v_{Rd} connect voltage ($>0.2\text{V}$). If an input source provides V_{BUS} before $t_{CC_DEBOUNCE}$ expires, or V_{IN} is present before the CC1 and CC2 pins make contact, then the LEGACYCABLE bit is set to 1 once a valid input source is detected (i.e. V_{IN} is between V_{IN_UV} and V_{IN_OV} after 15ms). This action is followed by a maskable an INT pulse. The LEGACYCABLE bit is reset to 0 if V_{IN} drops below V_{IN_UV} or exceeds V_{IN_OV} .

With legacy cable detection, the host can know the cable type. An advantage of this function is that if the legacy cable is non-compliant with the specification (e.g. if the CC pin is shorted to V_{BUS} or R_p is incorrect), the host can adjust the device's I_{IN_LIM} with the DPDM detection results.

Input Impedance Test

The MP2722 supports an input impedance testing function. By sourcing a current on the IN pin, the device can detect the impedance on the connector receptacle (water detection).

The host can write 1 to the VIN_SRC_EN bit to turn on the input impedance test by sourcing a current to the IN pin. The testing current can be configured via the IVIN_SRC bits. If V_{IN} rises to the threshold configured via the VIN_TEST bit, then VIN_TEST_HIGH is set to 1 and latched. This is followed by an INT pulse.

The host can write 0 to the VIN_SRC_EN bit to turn off the test current source and clear the VIN_TEST_HIGH bit.

The VIN_SRC_EN bit can only be effective when neither the buck nor boost is operating, and the current source's maximum pull-up voltage is 2.5V. If $V_{IN} > V_{IN_UV}$ is detected during the test, then the VIN_SRC_EN and VIN_TEST_HIGH bits are reset to 0 and the test ends immediately. If boost mode is enabled during the test, then the VIN_SRC_EN and VIN_TEST_HIGH bits are reset to 0 and the test ends immediately.

The advantage of the input impedance function is that the device can provide the information on the connector's impedance or moisture status. A Type-C connector can corrode when exposed to moisture, especially in source or DRP mode with a current on the CC pins. Software detects moisture conditions to allow the device to disable charging, the boost, or the Type-C block.

Lock Function

The MP2722 supports a lock function that limits the value of some key parameters (prevents accidental I²C writing). The battery regulation voltage, constant-current charge current, pre-charge current, and JEITA voltage/current settings are some of these parameters.

To enable the lock function, the host can set the above parameters to a target value, then write

the LOCK_CHG bit to 1. After these operations, these parameters can only be written to values below the previously set value.

Any of the following events can unlock the parameters:

- The host writes the LOCK_CHG bit to 0
- The host writes the REG_RST bit to 0
- The device shuts down

Protections

Battery Under-Voltage Protection (UVP)

If the battery is discharged below V_{BATT_UV} when the input source is absent, then the BATTFET turns off and all registers reset.

BATTFET Over-Current Protection (OCP)

The MP2722 monitors the BATTFET's current. If SYS is overloaded or experiences a short and the battery discharge current reaches the I_{BATT_OCP} threshold, then the BATTFET turns off and latches. In addition, the BATTFET_DIS bit is set to 1. To release the latch, apply one of the methods described in the Exiting Shipping Mode section on page 21.

Input Over-Voltage Protection (OVP)

The MP2722 provides input over-voltage protection (OVP) with a default rising threshold of 6.3V. If the IN pin senses a voltage above the V_{IN_OV} threshold, the buck converter stops working, the CHG_FAULT bits are set to 01, and an INT pulse is generated.

When V_{IN} returns to the normal range, the device runs the start-up sequence again and resumes normal operation. The CHG_FAULT bits are also cleared.

Battery Over-Voltage Protection (OVP)

The battery OVP threshold is 104% of V_{BATT_REG} . If a battery OV condition is detected, charging is disabled. Meanwhile, the fault register's CHG_FAULT bits are set to 11, and an INT pulse asserts.

Thermal Regulation and Thermal Shutdown

If the internal junction temperature reaches to the thermal regulation limit (T_{J_REG}) configured via the TREG bits (60°C to 120°C) during battery charging, then the charge current is reduced, charge termination is blocked, and the charge timer runs at half rate. The status

register's THERM_STAT bit is set to 1, followed by a maskable INT pulse.

If the internal junction temperature rises to the shutdown threshold (T_{J_SHDN} , about 150°C) at any time, both the converter and BATTFET turn off and all registers are reset. Once the junction temperature returns to T_{SHDN_HYS} (about 30°C) below T_{J_SHDN} (150°C), the MP2722 starts up again and resumes normal operation.

Boost Over-Voltage Protection (OVP)

If V_{IN} exceeds the regulation target and V_{BST_OVP} during boost operation, the device stops switching immediately. The BOOST_FAULT bits are set to 010, and an INT pulse is generated. Boost operation recovers once V_{IN} returns to its normal range.

Boost Overload Protection

If V_{IN} drops below the ($V_{BATT} + V_{HDMR}$) or V_{IN_UV} threshold due to a heavy load or short during boost operation, the blocking FET turns off and restarts after 500ms. If a total of 8 restarts are not successful, the boost converter stops and latches off. Then the BOOST_FAULT bits are set to 001 and an INT pulse is generated.

If the IN pin is shorted to GND before the boost converter starts, the blocking FET also restarts 8 times. If this is not successful, the boost converter stops and latches off.

Set the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Boost Battery Low Protection

The MP2722 can protect the battery from being over-drained and prevent a system shutdown during boost operation. If the BOOST_STP_EN bit is set to 1 and V_{BATT} falls below the BATT_LOW setting, boost operation automatically turns off and the MP2722 latches. The BOOST_FAULT bits are set to 100 and generate a maskable INT pulse. The BATTFET continues operating to provide power to SYS.

The battery low comparator has a 10ms debounce time. Change the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Boost Over-Temperature Protection

The MP2722 provides protection from over-temperature conditions in boost mode. If the BOOST_OTP_EN bit is set to 1 and the internal

junction temperature rises to the thermal regulation limit (T_{J_REG} , configured via the TREG bits), then boost operation stops and the MP2722 latches. The BOOST_FAULT bits are set to 011, followed by an INT pulse. In this scenario, the BATTFET continues operating to provide power to SYS.

Change the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Serial Interface

The MP2722 uses an I²C-compatible interface to flexibly set charging parameters and instantaneously report the device status. The I²C is a two-wire serial interface with two required bus lines: a serial data line (SDA) and a serial clock line (SCL). Both the SDA and SCL lines are open drains that must be connected to the positive supply voltage with a pull-up resistor.

The IC operates as a slave device and receives control inputs from the master device, such as a microcontroller (MCU). The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kbps) and fast mode (up to 400kbps).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the master. A start command is defined as a high-to-low transition on the SDA line while SCL is high. A stop command is defined as a low-to-high transition on the SDA line when the SCL is high (see Figure 7).

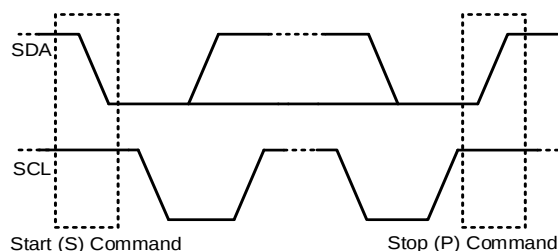


Figure 7: Start and Stop Commands

For data validity, the data on the SDA line must be stable during the high period of the clock.

The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 8). Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

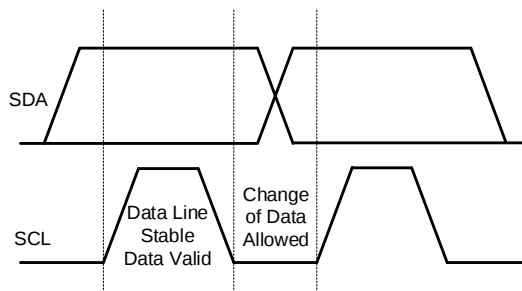


Figure 8: Bit Transfer on the I²C Bus

Each byte must be followed by an acknowledge (ACK) bit. The ACK bit is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low, which remains low during the high period of the 9th clock pulse.

If the SDA line is high during the 9th clock pulse, this is considered a not acknowledge (NACK) signal. The master can then generate either a stop command to abort the transfer or a repeated start (Sr) command to start a new transfer.

A slave address is sent after the start command. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 9 shows the address bit arrangement.

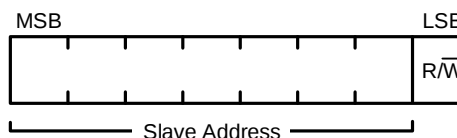


Figure 9: 7-Bit Addressing

Figure 10 shows a data transfer on the I²C bus.
 Figure 11 shows a single write sequence.
 Figure 12 shows a single read sequence.

Figure 13 shows a multi-write sequence. Figure 14 shows a multi-read sequence.

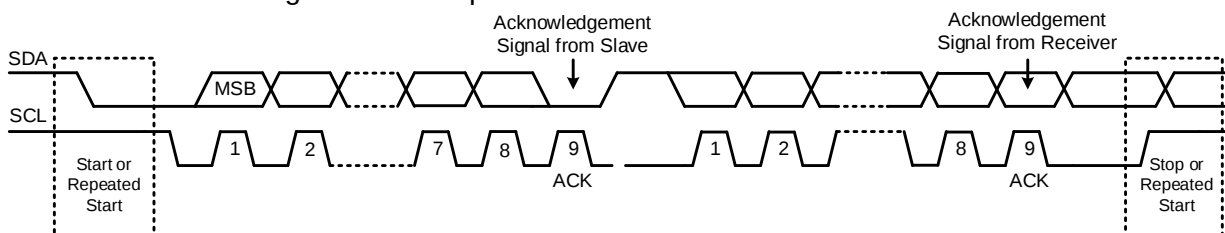


Figure 10: Data Transfer on the I²C Bus

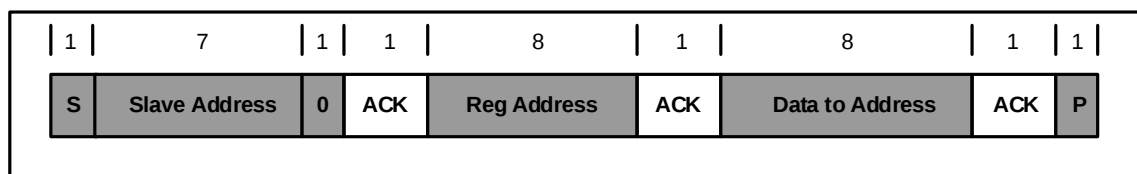


Figure 11: Single Write Sequence

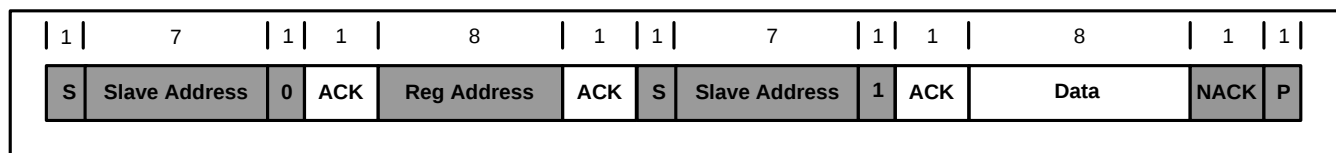


Figure 12: Single Read Sequence

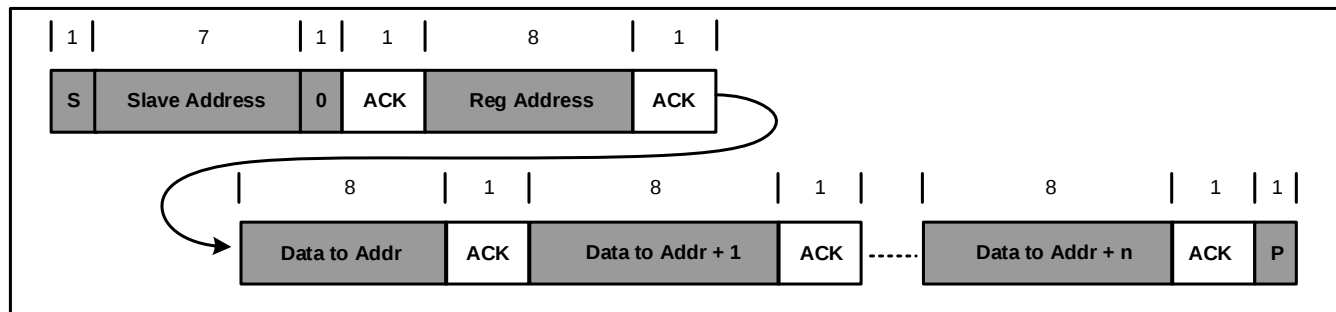


Figure 13: Multi-Write Sequence

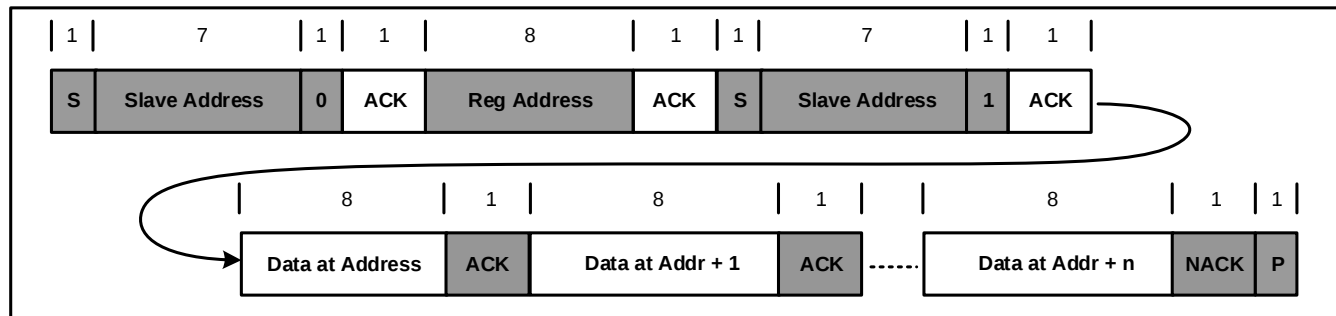


Figure 14: Multi-Read Sequence

REGISTER MAP

I²C Slave Address: 3Fh

Configuration Bytes: 00h~10h

Status Bytes: 11h~16h

CONFIGURATION BYTES (00h~10h)

Legend: POR = default value; WTD = watchdog; R/W = read/write; R = read-only, OTP-configurable = the register's default value can be configured via the OTP

REG00h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	REG_RST	0	-	R/W	Resets the register. 0: Keep the current setting 1: Reset the registers to their default values	This bit returns to 0 after it is written to 1.
6	EN_STAT_IB	0	No	R/W	0: The STAT/IB pin is configured as an open-drain status indicator (STAT) 1: The STAT/IB pin is configured as a battery current indicator (IB)	OTP-configurable.
5	EN_PG_NTC2	0	No	R/W	0: The PG/NTC2 pin is configured as an open-drain power good indicator (PG) 1: The PG/NTC2 pin is configured as a second thermistor input (NTC2)	To enable the NTC2 channel, this bit must be set to 1. OTP-configurable.
4	LOCK_CHG	0	No	R/W	0: Not locked 1: The VBATT[5:0], ICC[5:0], IPRE[3:0], JEITA_VSET[1:0], and JEITA_ISET[1:0] values are locked	After this bit is set to 1, any future writes to VBATT[5:0], ICC[5:0], IPRE[3:0], JEITA_VSET[1:0], and JEITA_ISET[1:0] can only reduce the set values.
3	HOLDOFF_TMR	1	Yes	R/W	0: Disable the hold-off timer 1: Enable the hold-off timer	OTP-configurable.
2	SW_FREQ[1]	0	No	R/W	00: 750kHz 01: 1MHz 10: 1.25MHz 11: 1.5MHz	Configures both the buck and boost operating frequencies. Default: 1MHz (01) OTP-configurable.
1	SW_FREQ[0]	1	No	R/W		
0	EN_VIN_TRK	1	No	R/W	0: V _{IN_LIM} is fixed 1: V _{IN_LIM} also tracks V _{BATT}	When this bit is set to 0, the VIN_LIM register sets the absolute input voltage limit (V _{IN_LIM}) value. When this bit is set to 1, V _{IN_LIM} is the maximum value between VIN_LIM[3:0] and (V _{BATT} + 165mV).

REG01h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	IIN_MODE[2]	0	No	R/W	000: Follow the IIN_LIM setting 001: Force I _{IN_LIM} to 100mA 010: Force I _{IN_LIM} to 500mA 011: Force I _{IN_LIM} to 900mA 100: Force I _{IN_LIM} to 1500mA 101: Force I _{IN_LIM} to 2000mA 110: Force I _{IN_LIM} to 3000mA	When setting these bits to 000, the input current limit (I _{IN_LIM}) follows the automatically generated I _{IN_LIM} value in IIN_LIM[4:0].
6	IIN_MODE[1]	0	No	R/W		When setting these bits to other values, I _{IN_LIM} is fixed.
5	IIN_MODE[0]	0	No	R/W		Default: 000
						OTP-configurable.
4	IIN_LIM[4]	0	No	R/W	1600mA.	Sets I _{IN_LIM} .
3	IIN_LIM[3]	0	No	R/W	800mA.	Range: 100mA to 3.2A Offset: 100mA Default: 500mA (00100)
2	IIN_LIM[2]	1	No	R/W	400mA.	
1	IIN_LIM[1]	0	No	R/W	200mA.	
0	IIN_LIM[0]	0	No	R/W	100mA.	This is automatically updated after input source type detection. The host can overwrite the I _{IN_LIM} value.

REG02h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	VPRE[1]	1	No	R/W	00: 2.4V 01: 2.6V 10: 2.8V 11: 3V	Sets the pre-charge to fast charge battery voltage threshold. Default: 3V (11)
6	VPRE[0]	1	No	R/W		
5	ICC[5]	0	Yes	R/W	2560mA.	Sets the fast charge current. Default: 2A (011001) OTP-configurable.
4	ICC[4]	1	Yes	R/W	1280mA.	
3	ICC[3]	1	Yes	R/W	640mA.	
2	ICC[2]	0	Yes	R/W	320mA.	
1	ICC[1]	0	Yes	R/W	160mA.	
0	ICC[0]	1	Yes	R/W	80mA.	

REG03h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	IPRE[3]	0	Yes	R/W	320mA.	Sets the pre-charge current Range: 80mA to 680mA Offset: 80mA Default: 240mA (0100) OTP-configurable.
6	IPRE[2]	1	Yes	R/W	160mA.	
5	IPRE[1]	0	Yes	R/W	80mA.	
4	IPRE[0]	0	Yes	R/W	40mA.	
3	ITERM[3]	0	Yes	R/W	240mA.	Sets the termination current. Range: 30mA to 480mA Offset: 30mA Default: 120mA (0011) OTP-configurable.
2	ITERM[2]	0	Yes	R/W	120mA.	
1	ITERM[1]	1	Yes	R/W	60mA.	
0	ITERM[0]	1	Yes	R/W	30mA.	

REG04h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	VRECHG	0	Yes	R/W	0: 100mV 1: 200mV	Sets the recharge threshold. Default: 100mV
6	ITRICKLE[2]	0	Yes	R/W	128mA.	Sets the trickle charge current. Range: 32mA to 256mA Offset: 32mA Default: 128mA (011) OTP-configurable.
5	ITRICKLE[1]	1	Yes	R/W	64mA.	
4	ITRICKLE[0]	1	Yes	R/W	32mA.	
3	VIN_LIM[3]	0	No	R/W	640mV.	Input voltage limit threshold Range: 3.88V to 5.08V Offset: 3.88V Default: 4.36V (0110)
2	VIN_LIM[2]	1	No	R/W	320mV.	
1	VIN_LIM[1]	1	No	R/W	160mV.	
0	VIN_LIM[0]	0	No	R/W	80mV.	

REG05h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	TOPOFF_TMR[1]	0	Yes	R/W	00: Disabled 01: 15 minutes 10: 30 minutes 11: 45 minutes	Timer to stop charging after charge termination.
6	TOPOFF_TMR[0]	0	Yes	R/W		
5	VBATT[5]	0	No	R/W	800mV.	Sets the battery regulation voltage (V _{BATT_REG}). Values above 101000 (4.6V) are clamped to 101000. Range: 3.6V to 4.6V Offset: 3.6V Default: 4.2V (011000) OTP-configurable.
4	VBATT[4]	1	No	R/W	400mV.	
3	VBATT[3]	1	No	R/W	200mV.	
2	VBATT[2]	0	No	R/W	100mV.	
1	VBATT[1]	0	No	R/W	50mV.	
0	VBATT[0]	0	No	R/W	25mV.	

REG06h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	VIN_OVP[1]	0	No	R/W	00: 6.3V 01: 11V 10: 14V 11: Disabled	Sets the input over-voltage protection (OVP) threshold. Default: 6.3V (00) OTP-configurable.
6	VIN_OVP[0]	0	No	R/W		
5	SYS_MIN[2]	1	No	R/W	000: 2.975V 001: 3.15V 010: 3.325V 011: 3.5V 100: 3.588V 101: 3.675V 110: 3.763V	Sets the system minimum regulation voltage (V _{SYS_MIN}). Default: 3.588V (100) The actual system regulation voltage is this value plus V _{TRACK} =150mV OTP-configurable.
4	SYS_MIN[1]	0	No	R/W		
3	SYS_MIN[0]	0	No	R/W		
2	TREG[2]	1	Yes	R/W	000: 60°C 001: 70°C 010: 80°C 011: 90°C 100: 100°C 101: 110°C 110: 120°C	Sets the thermal regulation threshold for charge mode, as well as the thermal protection threshold for boost mode. Default: 100°C (100)
1	TREG[1]	0	Yes	R/W		
0	TREG[0]	0	Yes	R/W		

REG07h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	IB_EN	0	Yes	R/W	0: IB outputs when the switcher is on 1: IB outputs all the time	Enables IB when only the battery is present, which uses about 3μA of battery current. Default: 0
6	WATCHDOG_RST	0	-	R/W	1: Reset the watchdog timer	After writing this bit to 1, the watchdog timer is reset, and this bit returns to 0.
5	WATCHDOG[1]	0	Yes	R/W	00: Disable timer 01: 40s 10: 80s 11: 160s	Default: 40s (01) OTP-configurable.
4	WATCHDOG[0]	1	Yes	R/W		
3	EN_TERM	1	Yes	R/W	0: Disable termination 1: Enable termination	Default: Enable termination (1)
2	EN_TMR2X	1	Yes	R/W	0: Disable 2x timer 1: Enable 2x timer	Default: Enable 2x timer (1)
1	CHG_TIMER[1]	1	Yes	R/W	00: Disable timer 01: 5hrs 10: 10hrs 11: 15hrs	Sets the charge safety timer. Default: 10hrs (10)
0	CHG_TIMER[0]	0	Yes	R/W		

REG08h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	BATTFET_DIS	0	No	R/W	0: Allow BATTFET to remain on 1: Turn off BATTFET	Shipping mode or OCP
6	BATTFET_DLY	1	No	R/W	0: Turn off BATTFET immediately 1: Turn off BATTFET after a 10s delay	Sets the delay after BATTFET_DIS is set to 1. Default: Turn off BATTFET after a 10s delay (1)
5	BATTFET_RST_EN	1	Yes	R/W	0: Disable the BATTFET reset function 1: Enable BATTFET reset function	Default: Enable the BATTFET reset function (1)
4	OLIM[1]	1	Yes	R/W	00: 500mA 01: 1.5A 10: 2.1A 11: 3A	Sets the boost output current limit. Default: 3A (11)
3	OLIM[0]	1	Yes	R/W		
2	VBOOST[2]	1	No	R/W	011: 5.35V 010: 5.3V 001: 5.25V 000: 5.2V 111: 5.15V 110: 5.1V 101: 5.05V 100: 5V	Sets the boost output voltage. Default: 5.15V (111) OTP-configurable.
1	VBOOST[1]	1	No	R/W		
0	VBOOST[0]	1	No	R/W		

REG09h

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	Reserved	0	No	R		
6	CC_CFG[2]	0	Yes	R/W	000: Sink only 001: Source only 010: DRP 011: DRP with Try.SNK 100: DRP with Try.SRC 101: Disabled	When the mode changes, the device resets to Unattached.SNK. Default: Sink only (000) OTP-configurable.
5	CC_CFG[1]	0	Yes	R/W		
4	CC_CFG[0]	0	Yes	R/W		
3	AUTOOTG	1	Yes	R/W	0: On-the-go (OTG) mode is controlled by the host 1: OTG is automatically controlled by CC detection	Default: 1 OTP-configurable.
2	EN_BOOST	0	Yes	R/W	0: Boost disabled 1: Boost enabled	When AUTOOTG = 1, the EN_BOOST bit is set/reset automatically, and boost mode is enabled/disabled. Writing 0 to EN_BOOST also turns off boost mode. When AUTOOTG = 0, the host can determine the boost requirement with the OTG_NEED bit. Writing 0 to EN_BOOST disables boost mode; writing 1 to EN_BOOST enables boost mode.
1	EN_BUCK	1	Yes	R/W	0: Buck disabled 1: Buck allowed	Set this bit to 0 to force the buck converter off.
0	EN_CHG	1	Yes	R/W	0: Charging disable 1: Charging allowed	Set this bit to 0 to force charging off.

REG0Ah

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	RESERVED	0	No	R	Reserved.	
5	AUTODPDM	1	Yes	R/W	0: D+/D- detection starts manually 1: D+/D- detection automatically starts after VIN_GD = 1 and the hold-off timer ends	Default: 1 OTP-configurable.
4	FORCEDPDM	0	-	R/W	0: Normal 1: Force D+/D- detection	This bit returns to 0 after 1 written
3	RP_CFG[1]	0	Yes	R/W	00: 80µA default USB 01: 180µA, USB Type-C 1.5A 10: 330µA, USB Type-C 3A	Sets the current rating advertisement in boost mode. Default: 01 OTP-configurable.
2	RP_CFG[0]	1	Yes	R/W		
1	FORCE_CC[1]	0	Yes	R/W	00: The CC1 and CC2 pins are automatically configured via CC_CFG 01: Forces the CC1 and CC2 pins to Rd 10: Forces the CC1 and CC2 pins to Rp (set by RP_CFG) 11: Forces the CC1 and CC2 pins into a high-impedance (Hi-Z) state	Default: 00 OTP-configurable.
0	FORCE_CC[0]	0	Yes	R/W		

REG0Bh

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	RESERVED	0	No	R	Reserved.	
5	RESERVED	0	No	R	Reserved.	
4	HVEN	1	No	R/W	0: Disables high-voltage adapter detection 1: Enables high-voltage adapter detection	Default: 1 OTP
3	HVUP	0	-	R/W	0: DP and DM do not change 1: DP = DM = 3.3V for 500µs	HVUP is only functional when DPDM_STAT = 1001 and HVREQ[1:0] = 11. This bit returns to 0 after being written to 1.
2	HVDOWN	0	X	R/W	0: DP DM unchanged 1: DP = DM = 0.6V for 500µs	HVDOWN is only functional when DPDM_STAT = 1001 and HVREQ[1:0] = 11. This bit returns to 0 after being written to 1.
1	HVREQ[1]	0	Y	R/W	00: DP = 0.6V, DM = Hi-Z 01: DP = 3.3V, DM = 0.6V 10: DP = 0.6V, DM = 0.6V 11: DP = 0.6V, DM = 3.3V	HVREQ is only functional when DPDM_STAT = 1001. This bit is reset to 00 once VIN_GD = 0.
0	HVREQ[0]	0	Y	R/W		

REG0Ch

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	NTC1_ACTION	1	No	R/W	0: Only generate INT when the NTC1 status changes 1: NTC1 is fully functional	The buck converter is not affected by this bit. Default: 1 OTP
5	NTC2_ACTION	0	No	R/W	0: Only generate INT when the NTC2 status changes 1: NTC2 is fully functional	The buck converter is not affected by this bit. Default: 0 OTP-configurable.
4	BATT_OVP_EN	1	Yes	R/W	0: Battery OVP is neglected 1: Battery OVP is enabled	Default: 1
3	BATT_LOW[1]	0	No	R/W	00: 3V falling 01: 3.1V falling 10: 3.2V falling 11: 3.3V falling	If V _{BATT} drops below BATT_LOW, an INT pulse is generated with a 10ms debounce time. Default: 3V (00)
2	BATT_LOW[0]	0	No	R/W		
1	BOOST_STP_EN	0	Yes	R/W	0: The BATT_LOW comparator only generates INT 1: The BATT_LOW comparator turns off boost operation and latches	Default: 0 OTP-configurable.
0	BOOST_OTP_EN	1	Yes	R/W	0: Boost OTP is ignored 1: Boost OTP occurs at TREG	Default: 1 OTP-configurable.

REG0Dh

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	WARM_ACT[1]	0	No	R/W	00: No action during an NTC warm condition 01: Reduce V _{BATT_REG} during an NTC warm condition 10: Reduce I _{CC} during an NTC warm condition 11: Reduce both V _{BATT_REG} and I _{CC} during an NTC warm condition	If both the NTC1_ACTION and NTC2_ACTION bits are set to 1, see Table 6 on page 21 for more details. Default: 01
6	WARM_ACT[0]	1	No	R/W		
5	COOL_ACT[1]	1	No	R/W	00: No action during an NTC cool condition 01: Reduce V _{BATT_REG} during an NTC cool condition 10: Reduce I _{CC} during an NTC cool condition 11: Reduce both V _{BATT_REG} and I _{CC} during an NTC cool condition	If both the NTC1_ACTION and NTC2_ACTION bits are set to 1, see Table 6 on page 21 for more details. Default: 10
4	COOL_ACT[0]	0	No	R/W		
3	JEITA_VSET[1]	0	Yes	R/W	00: V _{BATT_REG} - 100mV 01: V _{BATT_REG} - 150mV 10: V _{BATT_REG} - 200mV 11: V _{BATT_REG} - 250mV	Default: 00
2	JEITA_VSET[0]	0	Yes	R/W		
1	JEITA_ISET[1]	0	Yes	R/W	00: 50% of I _{CC} 01: 33% of I _{CC} 10: 20% of I _{CC}	Default: 00
0	JEITA_ISET[0]	0	Yes	R/W		

REG0Eh

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	VHOT[1]	1	Yes	R/W	00: 29.1% (50°C) 01: 25.9% (55°C)	Sets the hot falling threshold, as a percentage of V _{VRNTC} . Default: 23% (10)
6	VHOT[0]	0	Yes	R/W	10: 23% (60°C) 11: 20.4% (65°C)	
5	VWARM[1]	0	Yes	R/W	00: 36.5% (40°C) 01: 32.6% (45°C)	Sets the warm falling threshold, as a percentage of V _{VRNTC} . Default: 32.6% (01)
4	VWARM[0]	1	Yes	R/W	10: 29.1% (50°C) 11: 25.9% (55°C)	
3	VCOOL[1]	1	Yes	R/W	00: 74.2% (0°C) 01: 69.6% (5°C)	Sets the cool rising threshold, as a percentage of V _{VRNTC} . Default: 64.8% (10)
2	VCOOL[0]	0	Yes	R/W	10: 64.8% (10°C) 11: 59.9% (15°C)	
1	VCOLD[1]	0	Yes	R/W	00: 78.4% (-5°C) 01: 74.2% (0°C)	Sets the cold rising threshold, as a percentage of V _{VRNTC} . Default: 74.2% (01)
0	VCOLD[0]	1	Yes	R/W	10: 69.6% (+5°C) 11: 64.8% (+10°C)	

REG0Fh

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	VIN_SRC_EN	0	Yes	R/W	0: Normal 1: Source current to the IN pin	Enables the input impedance test.
5	IVIN_SRC[3]	0	Yes	R/W	0000: 5μA 0001: 10μA	Configures the input impedance test current source.
4	IVIN_SRC[2]	0	Yes	R/W	0010: 20μA 0011: 40μA	
3	IVIN_SRC[1]	0	Yes	R/W	0100: 80μA 0101: 160μA	
2	IVIN_SRC[0]	0	Yes	R/W	0110: 320μA 0111: 640μA 1000: 1280μA	
1	VIN_TEST[1]	0	Yes	R/W	00: 0.3V 01: 0.5V	Configures the input impedance test comparator threshold.
0	VIN_TEST[0]	0	Yes	R/W	10: 1V 11: 1.5V	

REG10h

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	RESERVED	1	No	R	Reserved.	
5	MASK_THERM	0	No	R/W	0: Enable the THERM_STAT INT pulse 1: Mask the THERM_STAT INT pulse	OTP-configurable.
4	MASK_DPM	0	No	R/W	0: Enable the VINDPM and IINDPM INT pulses 1: Mask the VINDPM and IINDPM INT pulses	
3	MASK_TOPOFF	0	No	R/W	0: Enable the TOPOFF timer INT pulse 1: Mask the TOPOFF timer INT pulse	
2	MASK_CC_INT	0	No	R/W	0: Enable the CC_SNK and CC_SRC INT pulses 1: Mask the CC_SNK and CC_SRC INT pulse	OTP-configurable.
1	MASK_BATT_LOW	0	No	R/W	0: Enable the BATT_LOW INT pulse 1: Mask the BATT_LOW INT pulse	
0	MASK_DEBUG_AUDIO	0	No	R/W	0: Allow DEBUGACC and AUDIOACC INT pulse 1: Mask DEBUGACC and AUDIOACC INT pulse	

STATUS BYTES (11h~16h)

Legend: POR = default value; R/W = read/write; R = read-only; INT = interrupt; YM = the interrupt can be masked

REG11h

Bits	Name	POR	R/W	INT	Description
7	DPDM_STAT[3]	-	R	No	Returns the input source D+/D- detection result.
6	DPDM_STAT[2]	-	R	No	0000: Not started (500mA) 0001: USB SDP (500mA) 0010: USB DCP (2A) 0011: USB CDP (1.5A)
5	DPDM_STAT[1]	-	R	No	0100: Divider 1 (1A) 0101: Divider 2 (2.1A) 0110: Divider 3 (2.4A) 0111: Divider 4 (2A)
4	DPDM_STAT[0]	-	R	No	1000: Unknown (500mA) 1001: High-voltage adapter (2A) 1110: Divider 5 (3A)
3	RESERVED	-	R	No	Reserved.
2	RESERVED	-	R	No	Reserved.
1	VINDPM_STAT	-	R	YM	0: Not in VINDPM 1: In VINDPM
0	IINDPM_STAT	-	R	YM	0: Not in IINDPM 1: In IINDPM

REG12h

Bits	Name	POR	R/W	INT	Description
7	RESERVED	-	R	No	Reserved.
6	VIN_GD	-	R	Yes	When $V_{VIN_UV} < V_{IN} < V_{VIN_OV}$ in buck mode, this bit is set to 1 and the PG pin is driven low (after a 15ms debounce time). 0: The input source is not valid 1: The input source is good
5	VIN_RDY	-	R	Yes	Indicates whether input source type detection has finished. IIN_LIM[4:0] is updated. 0: V_{IN} is not ready to charge 1: V_{IN} is ready to charge
4	LEGACYCABLE	-	R	YM	0: Normal 1: Legacy cable is detected (not valid in DRP mode)
3	THERM_STAT	-	R	YM	0: Not in thermal regulation 1: In thermal regulation
2	VSYS_STAT	-	R	No	0: $V_{BATT} < V_{SYS_MIN}$ 1: $V_{BATT} > V_{SYS_MIN}$
1	WATCHDOG_FAULT	-	R	Yes	0: Normal 1: The watchdog timer has expired
0	WATCHDOG_BARK	-	R	Yes	0: Normal 1: The 3/4 watchdog timer has expired

REG13h

Bits	Name	POR	R/W	INT	Description
7	CHG_STAT[2]	-	R	No	000: Not charging 001: Trickle charge 010: Pre-charge 011: Fast charge 100: Constant-voltage charge 101: Charging is done
6	CHG_STAT[1]	-	R	No	
5	CHG_STAT[0]	-	R	No	
4	BOOST_FAULT[2]	-	R	Yes	
3	BOOST_FAULT[1]	-	R	Yes	000: Normal 001: An IN overload or short (latch-off) has occurred 010: Boost over-voltage protection (OVP) (not latch) has occurred 011: Boost over-temperature protection (latch-off) has occurred 100: The boost has stopped due to BATT_LOW (latch-off)
2	BOOST_FAULT[0]	-	R	Yes	
1	CHG_FAULT[1]	-	R	Yes	00: Normal 01: Input OVP 10: The charge timer has expired 11: Battery OVP
0	CHG_FAULT[0]	-	R	Yes	

REG14h

Bits	Name	POR	R/W	INT	Description
7	NTC_MISSING	-	R	Yes	0: Normal 1: NTC is missing ($V_{NTC} > 95\%$ of V_{VRNTC})
6	BATT_MISSING	-	R	Yes	0: Normal 1: The battery is missing (2 terminations detected within 3 seconds)
5	NTC1_FAULT[2]	-	R	Yes	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot
4	NTC1_FAULT[1]	-	R	Yes	
3	NTC1_FAULT[0]	-	R	Yes	
2	NTC2_FAULT[2]	-	R	Yes	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot
1	NTC2_FAULT[1]	-	R	Yes	
0	NTC2_FAULT[0]	-	R	Yes	

REG15h

Bit	Name	POR	R/W	INT	Description
7	CC1_SNK_STAT[1]	0	R	YM	00: CC1 detects vRa 01: CC1 detects vRd-USB 10: CC1 detects vRd-1.5 11: CC1 detects vRd-3.0 A glitch in tPD_DEBOUNCE does not affect this result.
6	CC1_SNK_STAT[0]	0	R	YM	
5	CC2_SNK_STAT[1]	0	R	YM	00: CC2 detects vRa 01: CC2 detects vRd-USB 10: CC2 detects vRd-1.5 11: CC2 detects vRd-3.0 A glitch in tPD_DEBOUNCE does not affect this result.
4	CC2_SNK_STAT[0]	0	R	YM	
3	CC1_SRC_STAT[1]	0	R	YM	00: CC1 is vOPEN 01: CC1 detects vRd 10: CC1 detects vRa A glitch in tPD_DEBOUNCE does not affect this result.
2	CC1_SRC_STAT[0]	0	R	YM	
1	CC2_SRC_STAT[1]	0	R	YM	00: CC2 is vOPEN 01: CC2 detects vRd 10: CC2 detects vRa A glitch in tPD_DEBOUNCE does not affect this result.
0	CC2_SRC_STAT[0]	0	R	YM	

REG16h

Bits	Name	POR	R/W	INT	Description
7	RESERVED	-	R	No	Reserved.
6	TOPOFF_ACTIVE	-	R	YM	0: The top-off timer is not counting 1: The top-off timer is counting
5	BFET_STAT	-	R	No	0: The battery is charging or disabled 1: The battery is discharging
4	BATT_LOW_STAT	-	R	YM	The hysteresis = 200mV. 0: V _{BATT} is greater than BATT_LOW[1:0] 1: V _{BATT} is below BATT_LOW[1:0]
3	OTG_NEED	-	R	Yes	If the boost needs to be turned on/off by CC detection, this bit is set/reset with an INT pulse followed. 0: Boost should be disabled 1: Boost should be enabled
2	VIN_TEST_HIGH	-	R	Yes	0: V _{IN} is below the VIN_TEST threshold 1: V _{IN} has reached the VIN_TEST threshold
1	DEBUGACC	-	R	YM	0: Normal 1: Enters DebugAccessory.SNK state
0	AUDIOACC	-	R	YM	0: Normal 1: Enters AudioAccessory state

INTERRUPT LIST

INT Name	Related registers	Can be Masked	Event
VIN_GD	VIN_GD changes	No	A good input source has been detected.
DPDM_DET_DONE	DPDM_STAT[3:0] changes	No	DPDM detection is finished.
VIN_RDY	VIN_RDY 0→1	No	The input current limit has been updated; the buck converter starts.
CHG_DONE	CHG_STAT[2:0] any to 101	No	Charging has terminated.
RECHARGE	CHG_STAT[2:0] exits 101 and enter CC/CV charge	No	Recharging has been initiated.
THERM_STAT	THERM_STAT 0→1	Yes	The IC has entered charge thermal regulation.
WATCHDOG_FAULT	WATCHDOG_FAULT 0→1	No	A watchdog timeout has occurred.
WATCHDOG_BARK	WATCHDOG_BARK 0→1	No	A watchdog bark has occurred.
CHG_FAULT	CHG_FAULT[1:0] 00→01, 00→10, 00→11	No	One of the following charge faults has occurred: input OVP, battery OVP, or the charge timer has expired.
NTC_MISSING	NTC_MISSING changes	No	NTC is missing.
BATT_MISSING	BATT_MISSING changes	No	BATT is missing.
BOOST_FAULT	BOOST_FAULT[2:0] 000→001, 000→010, 010→000, 000→011, 000→100	No	One of the following boost fault has occurred: IN overload or short, boost OVP, boost OTP, the boost has stopped due to BATT_LOW.
NTC_FAULT	NTC1_FAULT[2:0] or NTC2_FAULT[2:0] changes	No	The NTC status has changed.
VINDPM_STAT	VINDPM_STAT 0→1	Yes	The V _{IN} regulation loop has been entered.
IINDPM_STAT	IINDPM_STAT 0→1		The I _{IN} regulation loop has been entered.
TOPOFF_TMR	TOPOFF_ACTIVE changes	Yes	The TOPOFF timer has started and ended.
CC_SNK	CC1_SNK_STAT[1:0] or CC2_SNK_STAT[1:0] changes	Yes	vRd connect has been detected or the source current advertisement has changed.
CC_SRC	CC1_SRC_STAT[1:0] or CC2_SRC_STAT[1:0] changes		vRd or vRa has been detected.
BATT_LOW	BATT_LOW_STAT 0→1	Yes	V _{BATT} has dropped to the BATT_LOW threshold.
OTG_NEED	OTG_NEED changes	No	The host has to turn enable/disable boost.
VIN_TEST_HIGH	VIN_TEST_HIGH 0→1	No	V _{IN} has reached the VIN_TEST threshold during the input impedance test.
DEBUGACC	DEBUGACC changes	Yes	DebugAccessory.SNK state entry/exit
AUDIOACC	AUDIOACC changes		AudioAccessory state entry/exit
HVCHARGER	DPDM_STAT[3:0] Any → 1001	No	A high-voltage charger has been detected.

OTP MAP

The MP2722 has a one-time-programming (OTP) function to configure the default values for certain registers. The OTP map below shows the OTP-configurable commands.

#	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00h	N/A	EN_STAT_IB	EN_PG_NTC2	N/A	HOLDOFF_ TMR	SW_FREQ[1:0]		N/A
01h	IIN_MODE			N/A	N/A	N/A	N/A	N/A
02h	N/A	N/A	ICC[5:0]					
03h	IPRE[3:0]				ITERM[3:0]			
04h	N/A	ITRICKLE[2:0]			N/A			
05h	N/A	N/A	VBATT[5:0]					
06h	VIN_OVP[1:0]		SYS_MIN[2:0]			N/A	N/A	N/A
07h	N/A	N/A	WATCHDOG[1:0]		N/A	N/A	N/A	N/A
08h	N/A	N/A	N/A	N/A	N/A	VBOOST[2:0]		
09h	N/A	CC_CFG[2:0]			AUTOOTG	N/A	N/A	N/A
0Ah	N/A	N/A	AUTODPDM	N/A	RP_CFG[1:0]		FORCE_CC[1:0]	
0Bh	N/A	N/A	N/A	HVEN	N/A	N/A	N/A	N/A
0Ch	N/A	NTC1_ACTI ON	NTC2_ACTION	N/A	N/A	N/A	BOOST_ STP_ EN	BOOST_O TP_ EN
10h	N/A	N/A	MASK_THERM	N/A	N/A	MASK_CC_ INT	N/A	N/A

ONE-TIME PROGRAMMABLE (OTP) DEFAULT

OTP Items	Default
EN_STAT_IB	0: STAT
EN_PG_NTC2	0: PG
HOLDOFF_TMR	1: Enable the hold-off timer
SW_FREQ[1:0]	01: 1MHz
IIN_MODE[2:0]	000: Follow IIN_LIM setting
ICC[5:0]	011001: 2A
IPRE[3:0]	0100: 240mA
ITERM[3:0]	0011: 120mA
ITRICKLE[2:0]	011: 128mA
VBATT[5:0]	011000: 4.2V
VIN_OVP[1:0]	00: 6.3V
SYS_MIN[2:0]	100: 3.588V
WATCHDOG[1:0]	01: 40s
VBOOST[2:0]	111: 5.15V
CC_CFG[2:0]	000: Sink only
AUTOOTG	1: OTG is controlled automatically
AUTODPDM	1: D+/D- detection automatically starts after VIN_GD = 1 and the hold-off timer ends
RP_CFG[1:0]	01: 180uA (USB Type-C 1.5A)
FORCE_CC[1:0]	00: CC1 and CC2 are configured automatically
HVEN	1: Enable HV adaptor detection
NTC1_ACTION	1: Active
NTC2_ACTION	0: INT only
BOOST_STP_EN	0: The BATT_LOW comparator only generates INT
BOOST_OTP_EN	1: Boost operation stops if over-temperature protection occurs
MASK_THERM	0: Allow INT
MASK_CC_INT	0: Allow INT

APPLICATION INFORMATION

Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A lower-value inductor corresponds to a smaller size, but also results in a higher current ripple, higher magnetic hysteretic losses, and higher output capacitances. A higher-value inductor results in a lower ripple current and smaller output filter capacitors, but it also results in higher inductor DC resistance (DCR) loss.

The required inductance can be estimated with Equation (1):

$$L = \frac{V_{IN} - V_{SYS}}{\Delta I_{L_MAX}} \times \frac{V_{SYS}}{V_{IN} \times f_{SW}} \quad (1)$$

Where V_{IN} is the input voltage, V_{SYS} is the converter output voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is typically designed to be 20% to 40% of the maximum load current.

Choose an inductor that does not saturate under the worst-case load condition, which can be calculated with Equation (2):

$$I_{SAT} > I_{LOAD} + \frac{\Delta I_{L_MAX}}{2} \quad (2)$$

Where I_{SAT} is the inductor saturation current, I_{LOAD} is the buck converter's maximum load.

Selecting the PMID Capacitor (C_{PMID})

The PMID capacitor (C_{PMID}) decouples the switching buck converter and absorbs the switching ripple current. Select C_{PMID} based on the demand for the PMID current ripple. The input current ripple can be calculated with Equation (3):

$$I_{RMS_MAX} = I_{LOAD} \times \frac{\sqrt{V_{SYS} \times (V_{IN} - V_{SYS})}}{V_{IN}} \quad (3)$$

Use low-ESR ceramic capacitors with an X7R or X5R rating for C_{PMID} . This capacitor should be placed as close to the PMID and PGND pins as possible. The capacitor's voltage rating must exceed V_{IN} , and it is recommended to consider the plug-in overshoot voltage. A capacitor rated for at least 25V is recommended for applications with a 15V V_{IN} . Generally, a capacitance of 10 μ F is considered a sufficient starting value.

PCB Layout Guidelines

PCB layout is important to meet specified noise, efficiency, and stability requirements. For the best results, refer to Figure 15 and follow the guidelines below:

1. Place the PMID capacitor as close to the PMID and PGND pins as possible using a short copper plane connection. Place the PMID capacitor on the same layer as the IC.
2. Minimize the high-frequency current path loop between the PMID capacitor and the buck converter power MOSFETs (from the PMID pin to the capacitor to ground).
3. Place the inductor's input terminal as close to the SW pin as possible.
4. Minimize the copper area of the inductor's input terminal trace to reduce electrical and magnetic field radiation, but ensure that the trace is wide enough to carry the charging current.
5. Minimize parasitic capacitance from the inductor input terminal to any other trace or plane.

6. Place decoupling capacitors (e.g. the VCC pin capacitor) as close to the IC pins as possible, and make the connection as short as possible.
7. Connect the IC's power pin to as many copper planes as possible to conduct heat away from the IC.
8. Ensure that the number and physical size of the vias are sufficient for a current path.

Figure 15 shows a high-frequency current path. In this figure, the high-frequency path (the high-side MOSFET, low-side MOSFET and the PMID capacitor) must be minimized.

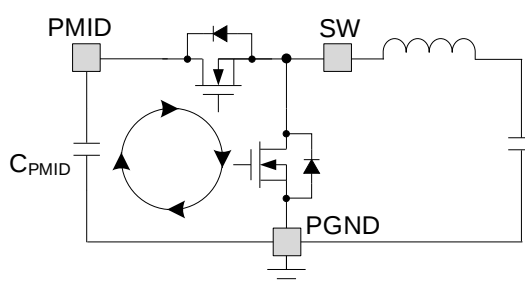


Figure 15: High-Frequency Current Path

TYPICAL APPLICATION CIRCUIT

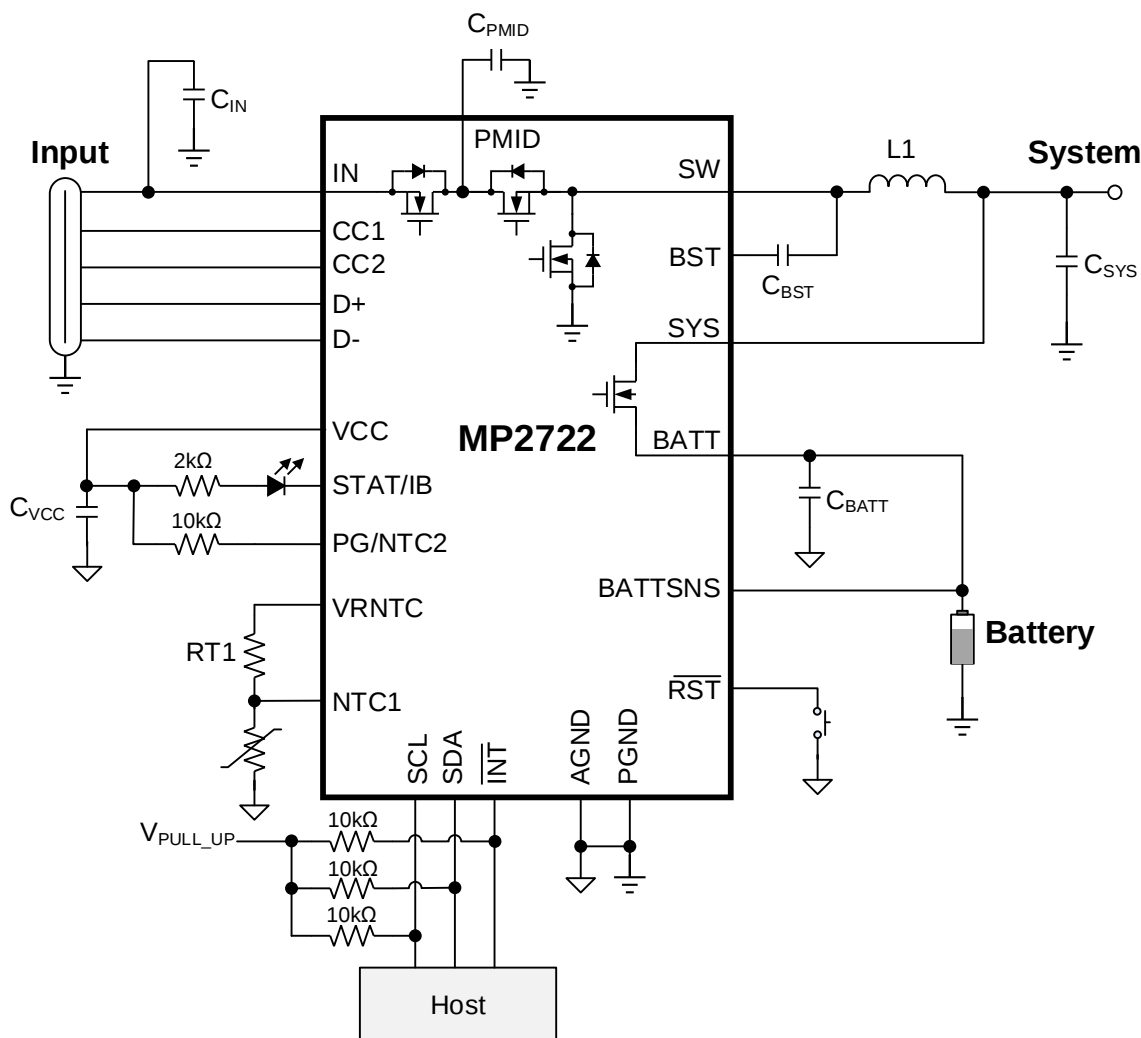


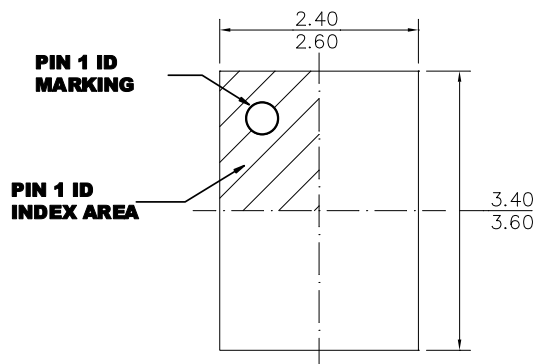
Figure 16: Typical Application Circuit

Table 8: Key BOM of Figure 16

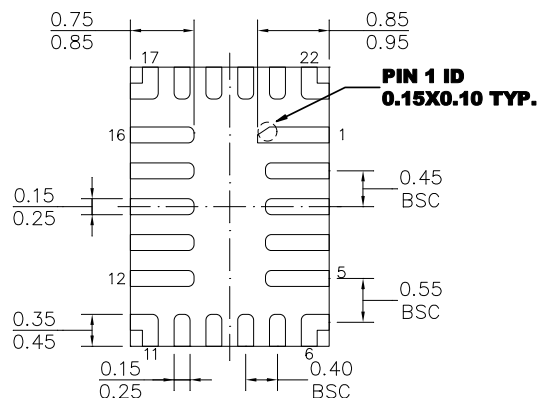
Qty	Ref	Value	Description	Package	Manufacturer
1	C _{IN}	1μF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C _{PMID}	10μF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
2	C _{SYS}	10μF x 2	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C _{BATT}	10μF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C _{VCC}	4.7μF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C _{BST}	22nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	1μH	Inductor, 1μH, low DCR	SMD	Any
1	RT1	10kΩ	Film resistor, 1%, same value as the NTC resistance at 25°C	0603	Any

PACKAGE INFORMATION

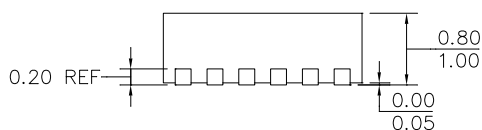
QFN-22 (2.5mmx3.5mm)



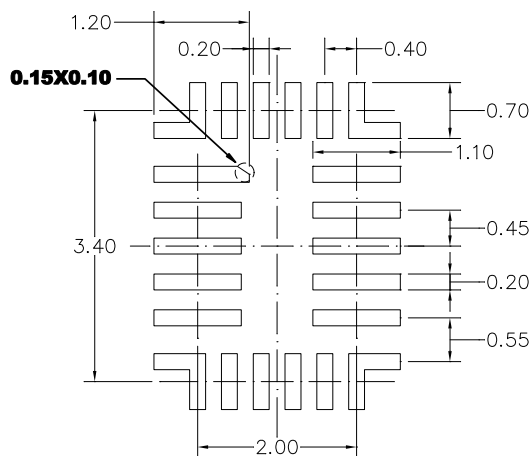
TOP VIEW



BOTTOM VIEW



SIDE VIEW

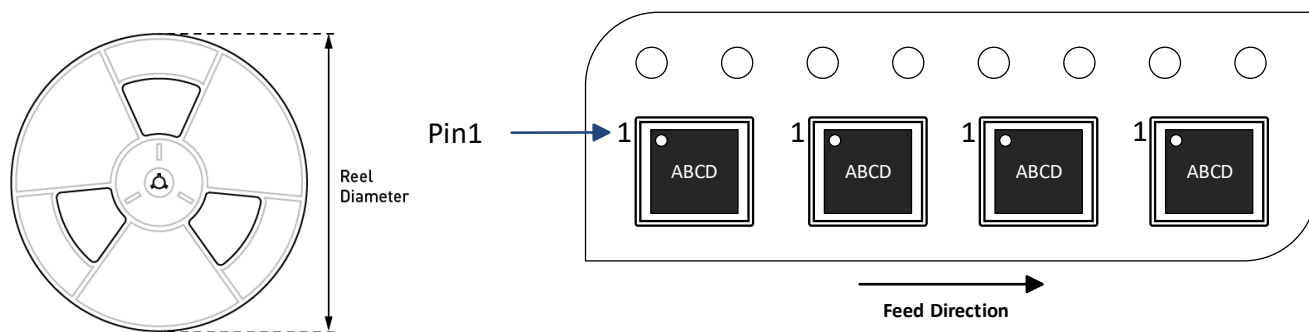


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2722GRH- xxxx-Z	QFN-22 (2.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/3/2022	Initial Release	-

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