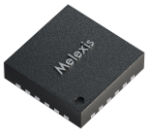
1 General description

1.1 Features and benefits

- Absolute Angle Position and Speed Tracking up to 200,000 rpm
- On-Chip Signal Processing with Latency Compensation for High-Speed operation and Accurate Absolute Positions Sensing
- On-Chip Self-Calibration for End of Line and In-Operation
- 5 V and 3.3 V supply compatible
- Triaxis® Hall Technology
- Programmable Linear Transfer Characteristic with up to 16 points
- Compliant to ASIL-B
- Dual-Die capable for ASIL-D concepts
- AEC-Q100 qualified (Grade 0) [1]
- Output modes:
  - SPI/SSI/PWM
  - Single-ended and differential ABI/UVW
  - Synchronized readout of multiple devices via SPI
- Packages RoHS compliant
- Single-Die - QFN-24
- Dual-Die - TSSOP-16/ TSSOP-16_EP
- 360° Stray Field Immunity up to 4 kA/m



QFN-24

TSSOP-16/ TSSOP-16_EP

1.2 Application examples

- Absolute Rotary Position Sensor
- Incremental Rotary Position Sensor
- High Speed Encoder
  - Automotive
  - Robotics
  - E-Mobility
  - Industrial Motors
- E-Steering Motor Position Sensor
- E-Braking Motor Position Sensor

1.3 Description

The MLX90382 is a monolithic magnetic position sensor IC that integrates a Triaxis® Hall magnetic front end, an analog-to-digital converter, digital hardware for high-speed signal processing and conditioning, as well as several output drivers.

The MLX90382 is sensitive to three components of the magnetic flux density applied to the IC (i.e. Bx, By, and Bz) and a differential magnetic field in the Z-axis. By programming the sensor, the user can select which axis pair will be used to determine an angle. This flexibility, combined with the appropriate magnetic design, allows the MLX90382 to calculate both the absolute and incremental position of any rotating magnet.

MLX90382 devices are factory-trimmed for immediate use. For tighter accuracy, end-of-line calibration includes multi-point linearization and self-calibration. In-Operation drift tracking maintains high-speed angle accuracy over assembly tolerances, temperature, and aging.

MLX90382 offers five output modes: 1) an industry-standard single-ended and differential ABI interface for incremental angular output, 2) a single-ended and differential UVW signal emulation for BLDC motors, 3) a PWM interface, and 4-5) SPI and SSI interfaces with configurable content that support functional safety requirements. Additionally, the SPI protocol includes a multi-slave synchronized readout capability.

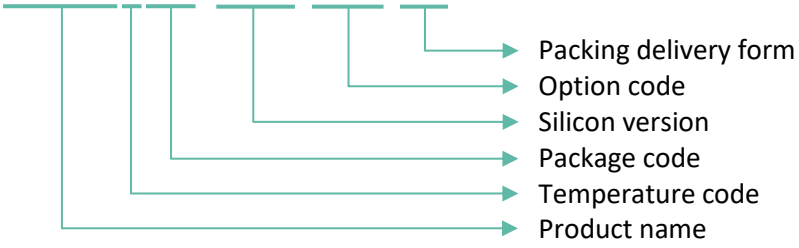
Figure 1: MLX90382 application examples

2 Ordering information

Ordering Code	Temperature range (°C)	Package	System Die	Pack-ing	Magnetic Configuration
MLX90382LLW-BAA-000-RE	-40 to 150	QFN-24	Single	Reel	Rotary Mode (mid-field)
MLX90382LLW-BAA-100-RE	-40 to 150	QFN-24	Single	Reel	Rotary Mode (high-field)
MLX90382LLW-BAA-600-RE	-40 to 150	QFN-24	Single	Reel	Stray Field Immune Ro-tary Mode
MLX90382LGO-BAA-000-RE	-40 to 150	TSSOP-16_EP	Dual	Reel	Rotary Mode (mid-field)
MLX90382LGO-BAA-100-RE	-40 to 150	TSSOP-16_EP	Dual	Reel	Rotary Mode (high-field)
MLX90382LGO-BAA-602-RE	-40 to 150	TSSOP-16	Dual	Reel	Stray Field Immune Ro-tary Mode

Table 1: MLX90382 Ordering Codes

MLX90382Lxx-BAA-x00-RE



Temperature Code:	**L**: -40 °C to 150 °C
Package Code:	**LW:** QFN-24 package (Single-Die) **GO**: TSSOP-16 (Dual-Die) and TSSOP-16_EP package (Dual-Die)
Silicon version	**BAA**-100: **Silicon version** ▪ **BAA**: MLX90382BA production version
Option Code - Magnetic Configuration	BAA-**1**00: **Magnetic Configuration** ▪ **0:** Rotary Mode for mid-field magnetic range ▪ **1:** Rotary Mode for high-field magnetic range ▪ **6:** 360 deg Stray Field Immune Rotary Mode
Option Code - Package Configuration	BAA-00**2**: **Package Configuration** ▪ **0:** Package with exposed pad ▪ **2:** Package without exposed pad
Packing Form:	**RE**: Tape & Reel ▪ 5000 pcs/reel for (Single-Die), LW package code ▪ 4500 pcs/reel for (Dual-Die), GO package code

Table 2: Ordering Codes Information

3 Contents

4 Block diagram and pin description

4.1 Block diagram

4.1.1 MLX90382 QFN-24 (Single-Die)

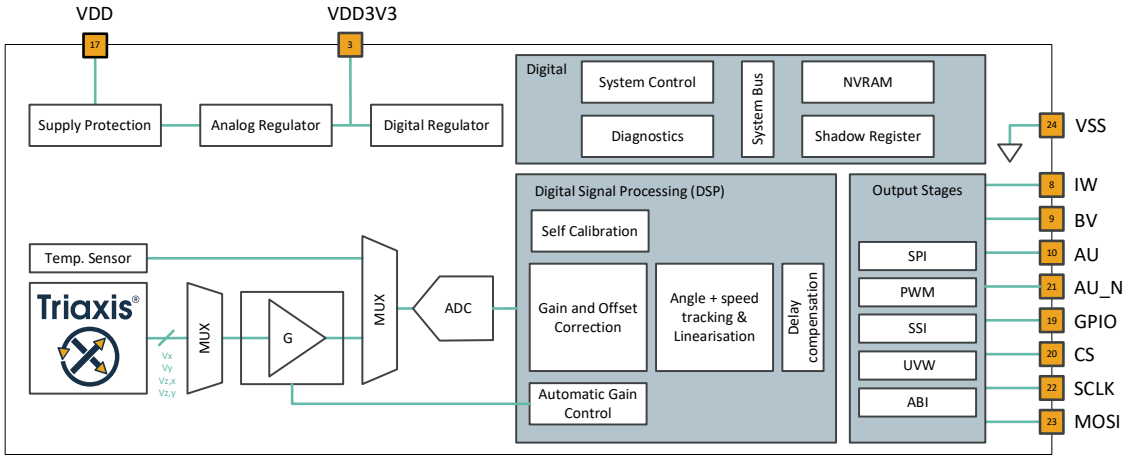


Figure 2: MLX90382 QFN-24 block diagram

4.1.2 MLX90382 TSSOP-16 / TSSOP-16_EP (Dual-Die)

The isolation resistance between the two dies is specified in Section 5.3.

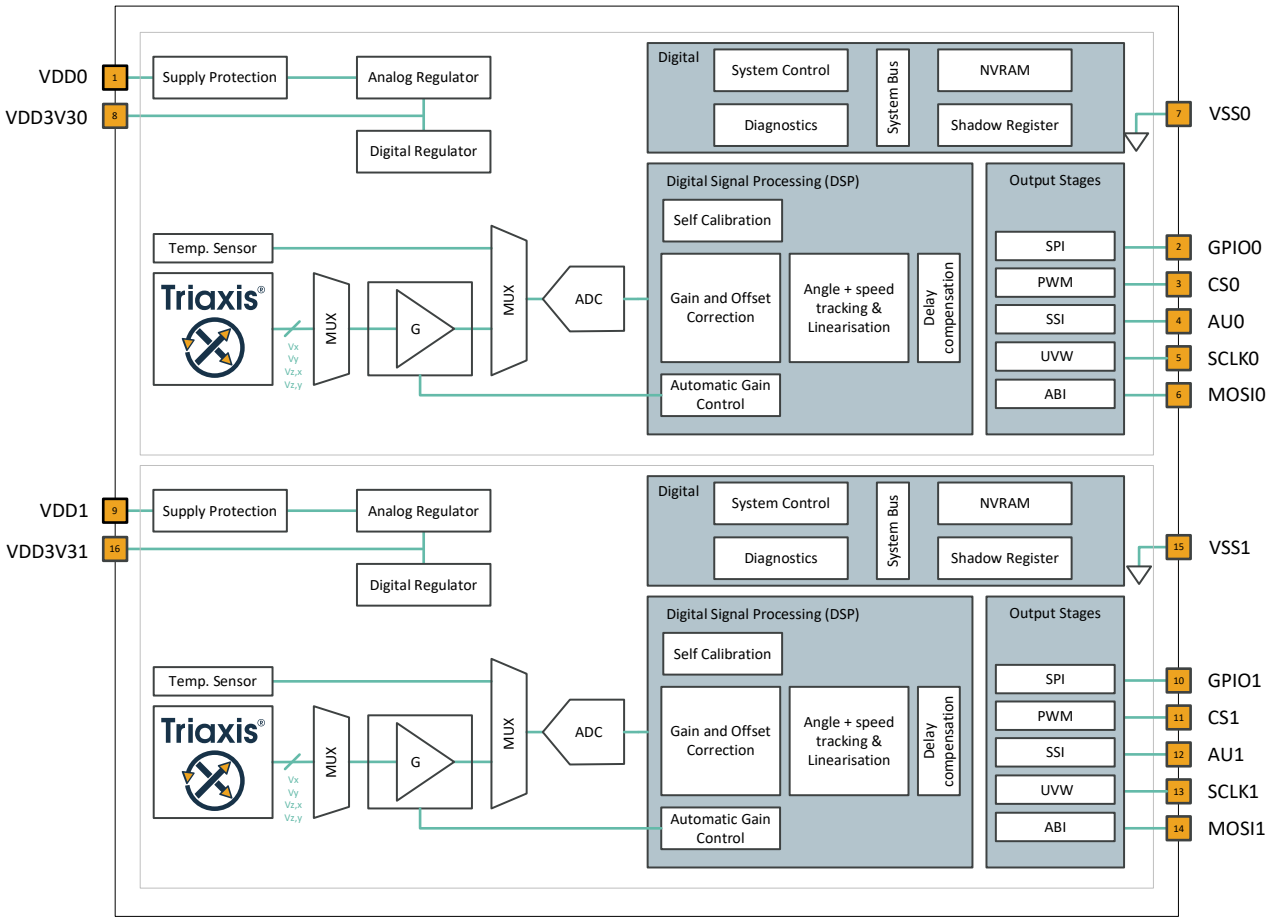


Figure 3: MLX90382 TSSOP-16 and TSSOP-16_EP block diagram

4.2 Pin description

4.2.1 Pin description for QFN-24 package

For optimal EMC and ESD behaviour, connect the unused pins to VSS. CS is the exception and should be tied to VDD when unused.

Pins CS and SCLK include internal pull-up resistors. If one of these pins is unused, disable their internal pull-ups to avoid additional current consumption (see Section 8.1.1).

The output driver mode of unused output pins must be set to “Hi-Z”. See Section 8.1.2.

The pin function options (the different modes in which the interface can be configured via programming) are described in Section 8.1.4.

Pin	Name (1)	I/O (2)	Mode (configurable by programming)					
			A0	A1	A2	A3	A4	A5
1	N.C.							
2	VDD3V3	S	Pin for decoupling capacitor for 5 V configuration To be shorted to VDD for 3.3 V configuration					
3..7	N.C.							
8	IW	O	ABI: I	UVW: W	ABI: I	UVW: W	ABI: I	UVW: W
9	BV	O	ABI: B	UVW: V	ABI: B	UVW: V	ABI: B	UVW: V
10	AU	O	ABI: A	UVW: U	ABI: A	UVW: U	ABI: A	UVW: U
11..16	N.C.							
17	VDD	S	Supply for 5 V To be shorted to VDD3V3 for 3.3 V configuration					
18	N.C.							
19	GPIO	O	SPI: MISO		SSI: DATA		PWM	
20	CS	I	SPI: Active low SPI chip select					
21	AU_N	O	Hi-Z				ABI: A_N	UVW: U_N
22	SCLK	I/O	SPI: SCLK		SSI: SCLK		ABI: B_N	UVW: V_N
23	MOSI	I/O	SPI: MOSI		Hi-Z		ABI: I_N	UVW: W_N
24	VSS	G	Ground					

Table 3: QFN-24 package pinout

Note:
(1): The postfix _N refers to logical inverted signals
(2): [S] Supply, [G] Ground, [I] Input, [O] Output

4.2.2 Pin description for TSSOP-16 and TSSOP-16_EP package

For optimal EMC and ESD behaviour, connect the unused pins to VSS0/VSS1. CS0/1 are the exception and should be tied to VDD when unused.

Pins CS0/1 and SCLK0/1 include internal pull-up resistors. If one of these pins is unused, disable their internal pull-ups to avoid additional current consumption (see Section 8.1.1).

The output driver mode of unused output pins must be set to “Hi-Z”. See Section 8.1.2.

The pin function options (the different modes in which the interface can be configured via programming) are described in Section 8.1.5.

Pin	Name	I/O (1)	Mode (configurable by programming) A0	A1	A2	A3
Die 0 (Bottom die)						
1	VDD0	S	Supply for 5 V To be shorted to VDD3V30 for 3.3 V configuration			
2	GPIO0	O	SPI: MISO	SSI: DATA	PWM	PWM
3	CS0	I	SPI: Active low SPI chip select			
4	AU0	O	Hi-Z	Hi-Z	ABI: A	UVW: U
5	SCLK0	I/O	SPI: SCLK	SSI: SCLK	ABI: B	UVW: V
6	MOSI0	I/O	SPI: MOSI	Hi-Z	ABI: I	UVW: W
7	VSS0	G	Ground			
8	VDD3V30	S	Pin for decoupling capacitor for 5 V configuration To be shorted to VDD0 for 3.3 V configuration			
Die 1 (Top die)						
9	VDD1	S	Supply for 5 V To be shorted to VDD3V31 for 3.3 V configuration			
10	GPIO1	O	SPI: MISO	SSI: DATA	PWM	PWM
11	CS1	I	SPI: Active low SPI chip select			
12	AU1	O	Hi-Z	Hi-Z	ABI: A	UVW: U
13	SCLK1	I/O	SPI: SCLK	SSI: SCLK	ABI: B	UVW: V
14	MOSI1	I/O	SPI: MOSI	Hi-Z	ABI: I	UVW: W
15	VSS1	G	Ground			
16	VDD3V31	S	Pin for decoupling capacitor for 5 V configuration To be shorted to VDD1 for 3.3 V configuration			

Table 4: TSSOP-16 and TSSOP-16_EP package pinout

Note:
(1): [S] Supply, [G] Ground, [I] Input, [O] Output

5 Conditions and specifications

5.1 Absolute maximum ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions may affect the device reliability.

Parameter	Symbol	Min.	Max.	Unit	Condition
Supply Voltage at VDD Pin	V_{DD}	-0.3	6.2	V	
Supply Voltage at VDD3V3 Pin	V_{DD}	-0.3	4.0	V	
I/O Pin Voltage	V_{PIN}	-0.3	V_{DD}+0.3	V	
ESD CDM Robustness	V_{CDM}	-500	500	V	All pins, except package corner pins, according to JEDEC JS-002
		-750	750	V	Package corner pins, according to JEDEC JS-002
ESD HBM Robustness	V_{HBM}	-2.0	2.0	kV	
Die to Die Voltage	$V_{SS0-SS1}$	-12.0	12.0	V	VSS0 to VSS1
Operating Temperature	T_{AMB}	-40.0	150.0	°C	
Junction Temperature	T_J		+175	°C	
Storage Temperature	T_{st}	-55	+170	°C	
Magnetic Flux Density	B_{max}	-1	1	T	
NVRAM erase/write cycles			100,000	Cycles	At 25 °C

Table 5: Absolute maximum ratings

5.2 Electrical operating conditions and specifications

5.2.1 3.3 V operating mode supply

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{DD}		3.3		V	Pin VDD and VDD3V3 shorted
		-5		+5	% V_{DD}	
Supply Current	I_{DD}			10.0	mA	IMC, excluding output I/F
				11.0	mA	Stray Field Immune mode, excluding output I/F
Under Voltage Detection Level On	$V_{UVD\_LH\_3V3}$	2.7	2.825	2.95	V	Supply voltage V_{DD} falling
Under Voltage Detection Level Off	$V_{UVD\_HL\_3V3}$	2.75	2.875	3.0	V	Supply voltage V_{DD} rising
Under Voltage detection Hysteresis	$V_{UVD\_Hyst\_3V3}$	0.02	0.05	0.15	V	
Over Voltage Detection Level On	$V_{OVD\_LH\_3V3}$	3.6	3.75	3.9	V	Supply voltage V_{DD} rising
Over Voltage Detection Level Off	$V_{OVD\_HL\_3V3}$	3.50	3.65	3.8	V	Supply voltage V_{DD} falling
Over Voltage Detection Hysteresis	$V_{OVD\_Hyst\_3V3}$	0.05	0.1	0.20	V	

Table 6: Electrical operating conditions in 3.3 V operating mode

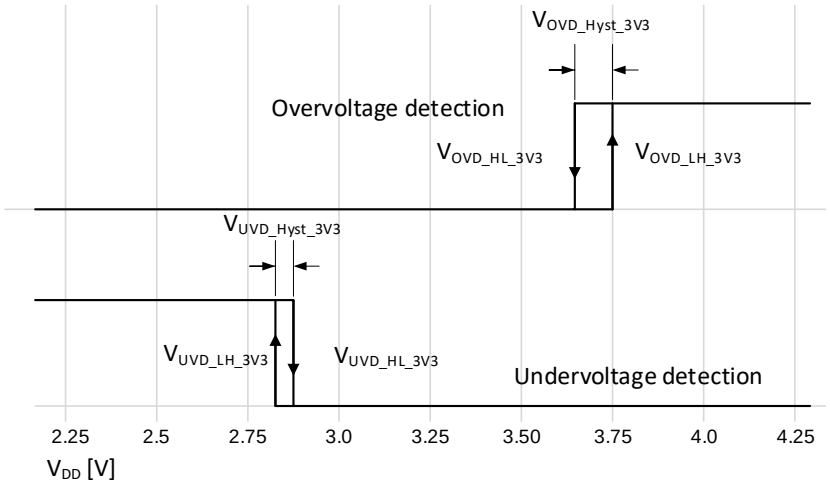


Figure 4: Over- and under voltage signal detection logic for typical condition in VDD 3.3V mode

5.2.2 5 V operating mode supply

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{DD}		5.0		V	
		-10		+10	% V_{DD}	
Supply Current	I_{DD}			10.0	mA	IMC, excluding output I/F
				11.0	mA	Stray Field Immune mode, excluding output I/F
Under Voltage Detection Level Off	$V_{UVD\_HL\_5\ V}$	4.1	4.25	4.4	V	Supply voltage V_{DD} rising
Under Voltage Detection Level On	$V_{UVD\_LH\_5\ V}$	3.85	4.0	4.15	V	Supply voltage V_{DD} falling
Under Voltage Detection Hysteresis	$V_{UVD\_Hyst\_5\ V}$	0.1	0.25	0.4	V	
Over Voltage Detection Level Off	$V_{OVD\_HL\_5\ V}$	5.5	5.65	5.80	V	Supply voltage V_{DD} falling
Over Voltage Detection Level On	$V_{OVD\_LH\_5\ V}$	5.75	5.9	6.2	V	Supply voltage V_{DD} rising
Over Voltage Detection Hysteresis	$V_{OVD\_Hyst\_5\ V}$	0.1	0.25	0.4	V	

Table 7: Electrical operating conditions in 5 V operating mode

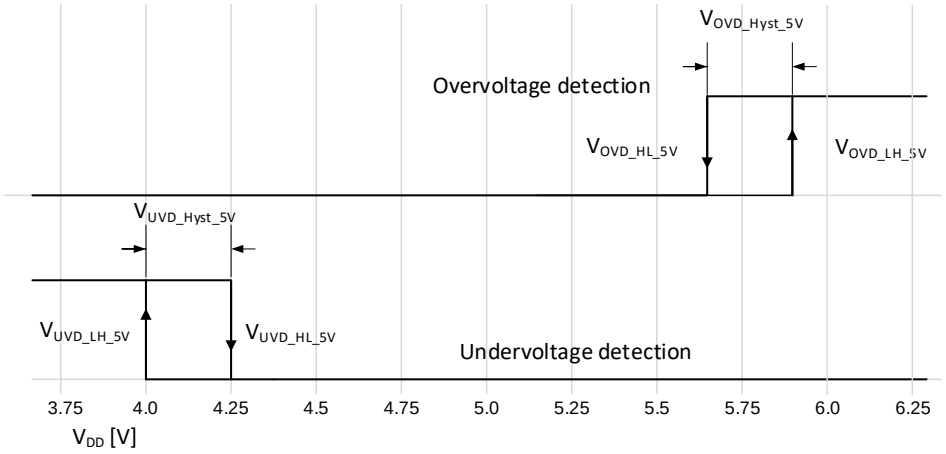


Figure 5: Over- and under voltage signal detection logic for typical cond. in VDD 5V mode

5.3 Isolation specification

The specified isolation resistance is only valid for the TSSOP-16 and TSSOP-16_EP package (code GO).

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Die 0 to Die 1 Isolation Leakage Current	I_{isol}			3.0	µA	Between dies, measured between VSS0 and VSS1 with +/-12 V bias

Table 8: Electrical isolation specifications for TSSOP-16 and TSSOP-16_EP

5.4 Dynamic operating specifications and conditions

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Rotational Speed (electrical)	v_{el}	-200		200	krpm	
Rotational Acceleration (electrical)	a_{el}	-10000		10000	krpm/s	Dynamic behaviour see Section 6.5.

Table 9: Angle operating specifications and conditions

5.5 Timing specifications

5.5.1 General timing specifications

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C, specified nominal supply voltage and supply voltage rise time from 0 V to 3.3 V or 5 V in 100 µs.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Main Clock Frequency	f_{RCO}		20.0		MHz	Trimmed. Including thermal and lifetime drift.
		-5		5	% f_{RCO}	
Application Clock Frequency	f_{AC}		f_{RCO}		MHz	Trimmed. Including thermal and lifetime drift.
Fault Handling Time Interval	FHTI			1.0	ms	See Section 7
System Start-up Time	T_{Start}			1.6	ms	Adaptive loop filter enabled (see Section 6.5)

Table 10: General timing specifications

5.5.2 Signal processing timing specification

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Processing Delay	τ_P	-333.0		333.0	ns	With delay compensation, excluding output interface. *DSP_DRIFT_DIS* = 0.
				6.0	µs	No delay compensation, excluding output interface. *DSP_DRIFT_DIS* = 1.

Table 11: Signal processing timing specification

5.6 Magnetic field specifications

5.6.1 Clarifications

For Rotary mode variants (option codes -000 and -100), the angle is calculated from magnetic flux density.

For Stray Field Immune devices, the angle is calculated from magnetic flux density gradient. The amplitude of the differential signal is directly dependent on the Hall Plate Spacing.

To convert magnetic a flux density gradient (in Stray Field Immune rotary mode devices) to magnetic flux density in Z direction, following relation can be used:

$$B_Z = \frac{\Delta B_Z}{\Delta XY} \cdot d_{HE}/2$$

where: B_Z represents to magnetic flux density, $\frac{\Delta B_Z}{\Delta XY}$ represents magnetic flux density gradient and d_{HE} is the Hall Plate Spacing. For example, a magnetic flux density gradient of 30 mT/mm corresponds to a magnetic flux density of 23.3 mT, with a Hall Plate Spacing of 1.554 mm.

5.6.2 Rotary mode - mid-field variant (option code -000)

Unless otherwise specified, the magnetic field specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Number of Magnetic Poles	N_P		2			
Magnetic Flux Density Norm (Medium Field IMC)	B_{NORM}	10			mT	$\sqrt{{B_x}^2 + {B_y}^2}$ (x-y mode) $\sqrt{{B_x}^2 + \left(\frac{1}{G_{IMC}} B_z\right)^2}$ (x-z mode) $\sqrt{{B_y}^2 + \left(\frac{1}{G_{IMC}} B_z\right)^2}$ (y-z mode)
Magnetic Flux Density in X-Y plane	B_X, B_Y			70	mT	$\sqrt{{B_x}^2 + {B_y}^2}$
Magnetic Flux Density in Z direction	B_Z			130	mT	
IMC Gain coefficient	G_{IMC}		1.15			

Table 12: Magnetic field specification for Rotary Mode mid-field Variant (Option Code -000)

5.6.3 Rotary mode - high-field variant (option code -100)

Unless otherwise specified, the magnetic field specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Number of Magnetic Poles	N_P		2			
Magnetic Flux Density (high-field IMC)	B_{NORM}	40			mT	$\sqrt{{B_x}^2 + {B_y}^2}$ (x-y mode) $\sqrt{{B_x}^2 + \left(\frac{1}{G_{IMC}} B_z\right)^2}$ (x-z mode) $\sqrt{{B_y}^2 + \left(\frac{1}{G_{IMC}} B_z\right)^2}$ (y-z mode)
Magnetic Flux Density in X-Y plane	B_X, B_Y			120	mT	$\sqrt{{B_x}^2 + {B_y}^2}$
Magnetic Flux Density in Z direction	B_Z			200	mT	
IMC Gain coefficient	G_{IMC}		0.53			

Table 13: Magnetic field specification for rotary mode high-field variant (Option Code -100)

5.6.4 Stray Field Immune rotary mode (dBz) (option code -60x)

Unless otherwise specified, the magnetic field specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Number of Magnetic Poles	N_P		2			
Magnetic Flux Density Gradient	$\frac{\Delta B_Z}{\Delta XY}$	10		128	$\frac{\mathrm{mT}}{\mathrm{mm}}$	dBz mode
Magnetic Flux Density in Z direction	B_Z	7.7		100	mT	
Hall Plate Spacing (see details in section 10.1.1.3 and 10.1.3.3)	d_{HE}		1.554		mm	

Table 14: Magnetic field specification for Stray Field Immune rotary mode (Option Code -60x)

5.7 Angular accuracy specifications

5.7.1 Performance conditions

The MLX90382 accuracy specifications are defined for two different ranges of performance conditions, nominal (see Section 5.7.5) and limited (see Section 5.7.6) performance, which are defined by the ambient temperature and the magnetic flux density/gradient range (see Figure 6).

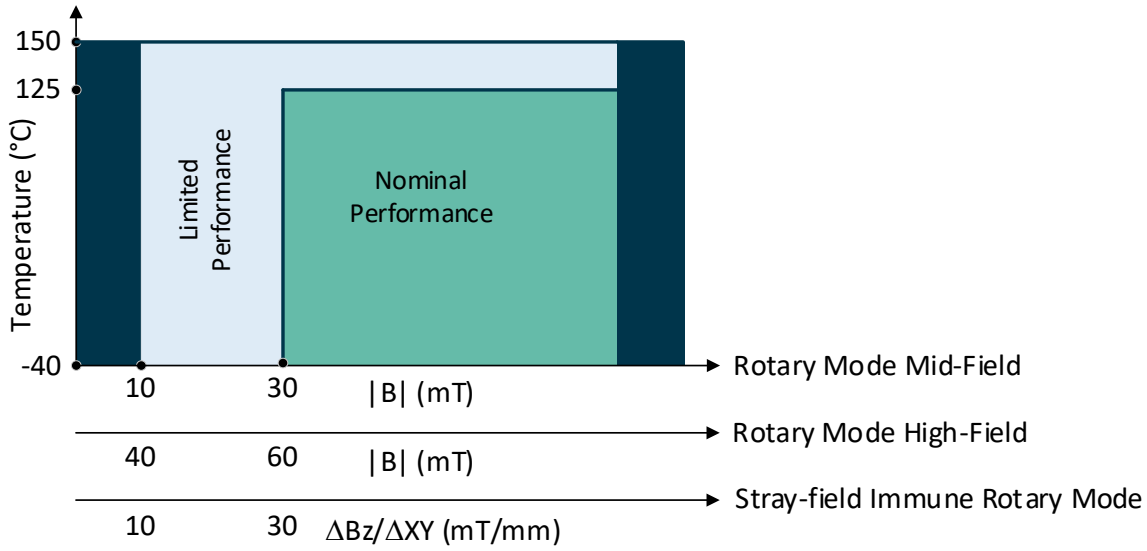


Figure 6: Performance condition definition for rotary mode with different variants

5.7.2 Definitions

This section defines several parameters, which are used for the magnetic specifications.

5.7.2.1 Intrinsic linearity error

The Intrinsic linearity error LE accounts for various error sources within the IC, such as offset, sensitivity mismatch and orthogonality error, assuming an ideal magnetic field. In cases of speed and acceleration, an additional dynamic angular offset (θ_{vel,τ_p}) to the Intrinsic Linearity Error is to be expected. When integrated into a sensor module and its associated mechanical and magnetic tolerances, the overall output linearity error (INL-integral nonlinearity) increases. The overall output linearity error can be reduced through I/Q mismatch calibration (see Section 6.6) and 16-Point Linearization (see Section 6.6.3). Consequently, once properly calibrated, this error is not the critical factor in most applications.

5.7.2.2 Total drift

After End of Line (EoL) calibration, variation due to temperature and ageing effects are referred to as the total drift $\partial\theta_{TT}$:

$$\partial\theta_{TT} = \max\{\theta(\theta_{IN}, T, t) - \theta(\theta_{IN}, T_{RT}, t_0)\}$$

where θ_{IN} represents the input angle, T is the operating temperature, T_{RT} is the room temperature, and t is the elapsed time since calibration. t_0 represents the start of the sensor's operational life. Note that the total drift $\partial\theta_{TT}$ is always measured relative to the angle at room temperature. In this datasheet, T_{RT} is typically defined at 35 °C, unless stated otherwise. The total drift specification is valid for all angles.

5.7.3 Performance optimization

The MLX90382 has internal mechanisms to optimize angular performance:

- An automatic bandwidth-adaptation loop tunes the angular-tracking filter in real time (see Section 6.5). When acceleration is low, the loop narrows the bandwidth to suppress noise and preserve high angular resolution (up to 14 bits RMS), producing smooth angle feedback. When acceleration increases, it opens the bandwidth as needed to follow fast motion without loss of accuracy.
- The MLX90382 contains a self-calibration function applicable to both end-of-line (EoL) calibration and In-Operation drift compensation (see Section 6.6.3). When applied, it significantly lowers the assembled sensor module's overall output linearity error and maintains performance over its lifetime.

5.7.4 General performance

Unless otherwise specified, valid before EoL calibration and for all applications under the temperature range of [-40, 150] °C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Dynamic Angular Offset	θ_{vel,τ_P}	-0.1		0.1	deg	v_{el} = 50 krpm, the value is proportional to the occurring processing delay. $\theta_{Vel,\tau\_p} = 6\ \tau_p\ v_{el.}$
Dynamic Eddy-Current related Angular Error in presence of Bz-component	$\theta_{vel,EC,dyn}$		±0.1		deg	v_{el} = 50 krpm *DSP_LFC_HI* = 0
			±0.4		deg	v_{el} = 50 krpm *DSP_LFC_HI* = 5
			±0.15		deg	v_{el} = 200 krpm *DSP_LFC_HI* = 0
			±1.5		deg	v_{el} = 200 krpm *DSP_LFC_HI* = 5

Table 15: General accuracy performance specifications

Note: The Dynamic Eddy-Current related Angular Error can scale due to different magnet alignments and conductive material close to the sensor plane. It appears in general in presence of B-field component in Z-direction. The disturbance appears mainly as a second-harmonic component of the angular error. By tightening the phase-tracking loop's bandwidth, this disturbance can be smoothed, leaving a minor residual noise. (see Section 6.5 for further details on bandwidth configuration).

5.7.5 Nominal performance

A homogeneous magnetic field is utilized to define magnetic performance specification. The performance may decrease with other magnetic sources.

5.7.5.1 Rotary mode

Unless otherwise specified, all values are valid before EoL calibration and for all applications under following nominal performance conditions: Temperature range [-40, 125] °C, $v_{el} \leq 50$ krpm, Magnetic flux density $|B| \geq 30$ mT (IMC-mid-field) and $|B| \geq 60$ mT (IMC-high-field).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
XY – Intrinsic Linearity Error, IMC	LE_{IMC_XY}	-0.5		0.5	deg	*SENSING_MODE* = 0
XZ – Intrinsic Linearity Error, IMC	LE_{IMC_XZ}	-1.0		1.0	deg	*SENSING_MODE* = 1
YZ – Intrinsic Linearity Error, IMC	LE_{IMC_YZ}	-1.0		1.0	deg	*SENSING_MODE* = 2
XY – Total Drift, IMC	$\partial\theta_{TT\_XY}$	-0.3		0.3	deg	*SENSING_MODE* = 0 T_{RT} = 35 °C
XZ, YZ – Total Drift, IMC	$\partial\theta_{TT\_XZ\_YZ}$	-0.4		0.4	deg	*SENSING_MODE* = 1/2 T_{RT} = 35 °C
Magnetic Hysteresis, IMC mid-field	$\theta_{EMH\_IMC\_MF}$			0.1	deg	Rotary Mode (mid-field variant)
Magnetic Hysteresis, IMC high-field	$\theta_{EMH\_IMC\_HF}$			0.1	deg	Rotary Mode (high-field variant)
Angular noise, RMS	θ_{STD}		0.025		deg	*DSP_LFC_HI* = 0
			0.035		deg	*DSP_LFC_HI* = 3

Table 16: Accuracy specifications for rotary mode at nominal performance conditions

5.7.5.2 Stray Field Immune rotary mode

Unless otherwise specified, all values are valid before EoL calibration and for all applications under the following conditions: Temperature range [-40, 125] °C, $v_{el} \leq 50$ krpm, Magnetic flux gradient $\Delta Bz/\Delta XY \geq 30$ mT/mm.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
XY – Intrinsic Linearity Error, dBz	LE_{DBZ_XY}	-0.7		0.7	deg	*SENSING_MODE* = 0
XY – Total Drift, dBz	$\partial\theta_{TT\_DBZ\_XY}$	-0.6		0.6	deg	*SENSING_MODE* = 0 T_{RT} = 35 °C
Stray Field Immunity	θ_{SF}	-0.15		0.15	deg	QFN-24: In accordance with ISO11452-8:2015 [2], at 30 °C with stray field of 4 kA/m from any direction
		-0.25		0.25	deg	TSSOP-16: In accordance with ISO11452-8:2015 [2], at 30 °C with stray field of 4 kA/m from any direction
Angular noise, RMS	θ_{STD}		0.025		deg	*DSP_LFC_HI* = 0
			0.050		deg	*DSP_LFC_HI* = 3

Table 17: Accuracy specifications for Stray Field Immune mode at nominal performance conditions

5.7.6 Limited performance

A homogeneous magnetic field is utilized to define magnetic performance specification. The performance may decrease with other magnetic sources.

5.7.6.1 Rotary mode

Unless otherwise specified, all values are valid before EoL calibration and for all applications under the following conditions: Temperature range [-40, 150] °C, $v_{el} \leq 50$ krpm, Magnetic flux $|B| \geq 10$ mT (IMC-mid-field) and $|B| \geq 40$ mT (IMC-high-field).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
XY - Intrinsic Linearity Error, IMC	LE_{IMC_XY}	-1.0		1.0	deg	*SENSING_MODE* = 0
XZ - Intrinsic Linearity Error, IMC	LE_{IMC_XZ}	-2.0		2.0	deg	*SENSING_MODE* = 1
YZ - Intrinsic Linearity Error, IMC	LE_{IMC_YZ}	-2.0		2.0	deg	*SENSING_MODE* = 2
XY - Total Drift, IMC	$\partial\theta_{TT\_IMC\_XY}$	-0.8		0.8	deg	*SENSING_MODE* = 0 T_{RT} = 35 °C
XZ, YZ - Total Drift, IMC	$\partial\theta_{TT\_IMC\_XZ\_YZ}$	-0.8		0.8	deg	*SENSING_MODE* = 1/2 T_{RT} = 35 °C
Magnetic Hysteresis, IMC mid-field	$\theta_{EMH\_IMC\_MF}$			0.2	deg	Rotary Mode (mid-field variant)
Magnetic Hysteresis, IMC high-field	$\theta_{EMH\_IMC\_HF}$			0.2	deg	Rotary Mode (high-field variant)
Angular noise, RMS	θ_{STD}		0.04		deg	*DSP_LFC_HI* = 0
			0.10		deg	*DSP_LFC_HI* = 3

Table 18: Accuracy specifications for rotary mode at limited performance conditions

5.7.6.2 Stray Field Immune rotary mode

Unless otherwise specified, all values are valid before EoL calibration and for all applications under the following conditions: Temperature range [-40, 150] °C, vel ≤ 50 krpm, Magnetic flux gradient ΔBz/ΔXY ≥ 10 mT/mm.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
XY - Intrinsic Linearity Error, dBz	LE_{DBZ_XY}	-1.4		1.4	deg	*SENSING_MODE* = 0
XY - Total Drift, dBz	$\partial\theta_{TT\_DBZ\_XY}$	-1.0		1.0	deg	*SENSING_MODE* = 0 T_{RT} = 35 °C
Stray Field Immunity	θ_{SF}	-0.40		0.40	deg	QFN-24: In accordance with ISO11452- 8:2015 [2], at 30 °C with stray field of 4 kA/m from any direction
		-0.70		0.70	deg	TSSOP-16: In accordance with ISO11452- 8:2015 [2], at 30 °C with stray field of 4 kA/m from any direction
Angular noise, RMS	θ_{STD}		0.05		deg	*DSP_LFC_HI* = 0
			0.15		deg	*DSP_LFC_HI* = 3

Table 19: Accuracy specification for Stray Field Immune mode at limited performance conditions

6 Functional description

6.1 System overview

The MLX90382 is a high-speed magnetic position sensor designed for absolute and incremental rotary position sensing. The block diagrams are shown in Figure 2 and Figure 3. The primary signal processing blocks of the position sensor consist of the Triaxis Hall elements, signal multiplexing and amplification, the Analog-To-Digital Conversion (ADC), the Digital Signal Processing (DSP) and output interfaces providing the output signals.

The MLX90382 supports the following features:

- Automatic gain control.
- Factory trimmed magnetic compensations for offset and I/Q gain mismatch over temperature in all magnetic modes.
- On-chip self-calibration: supports end-of-line trimming and continuous In-Operation drift compensation for I/Q gain and orthogonality mismatch.
- Computation for 16-bit angular position and 16-bit speed values with adjustable noise suppression or step responses. This includes an adjustable filter bandwidth and overshoot in the angular domain, ranging between 500 Hz to 100 kHz. An optional adaptive loop filter (ALF) optimizes the filter bandwidth, balancing noise suppression and regulation offset (due to magnetic acceleration). The upper and lower bandwidth limits are adjustable.
- Angular linearization using 16 equidistant correction points over 360 degrees, with linear interpolation. The 16-Point Linearization can be calibrated at low speeds or in static conditions and functions independently from the filter setting across the full-speed range.
- Processing delay compensation for both internal and external delays (adjustable) by compensation of the speed-dependent angular offset. The signal processing timing specifications are listed in Table 11.
- Flexible signal conditioning for the 16-bit angular output, allowing:
    - Selection of input range (clamping),
    - Adjustment of angular offset,
    - Definition of output range for transmission via SPI, SSI and PWM interfaces,
    - Specification of a fault band value to indicate a fail-safe state.

6.2 Automatic gain control

The automatic gain control (AGC) controls the common amplifier stage of the analog I and Q signals to keep the peak signal amplitude within 50% to 60% of the ADC full-scale range. The total available gain range is between 10 dB and 29 dB and can be limited or fixed using the register *AGC_GAIN_MIN[5:0]* and *AGC_GAIN_MAX[5:0]*. The current setting of the AGC can be read from *AGC_GAIN[5:0]*. Gain limiting is effective for values from 0 to 47 LSB. If *AGC_GAIN_MIN[5:0]* or *AGC_GAIN_MAX[5:0]* is programmed to a value above 47 LSB, the device internally treats it as 63 LSB.

6.3 Temperature sensing

The MLX90382 provides onboard temperature sensing, which can be read out via *TEMP[11:0]*. The physical value is encoded as defined in the SENT standard, Section A.5.3.2, in the range [200.125 : 0.125 : 711] [K].

$$T[°C] = \frac{TEMP[11:0]}{8} + 200[K] - 273.15$$

6.4 Digital signal processing overview

After digitalization of the analog I/Q signals, they are conditioned by factory calibrated, temperature-dependent offset compensation, as well as sensitivity and orthogonality correction. The customer can access intermediate processing values via DSP registers (see Section 11.2). The signal processing chain is illustrated in Figure 7. Compared to the output angle at the interface, these values have an internal update frequency of

f_{ac}/26. The sensitivity, orthogonality and offset compensated I/Q values can be read-out as averaged values trough *GC_I*[15:0] and *GC_Q[15:0].*

The averaging window used to calculate the mean $\overline{GC\_X}$ is configured by *DSP_GC_AVG[2:0]* as follows:

$$\overline{GC\_X} = \begin{cases} \dfrac{GC\_X}{4^{\,DSP\_GC\_AVG[2:0]}}, & DSP\_GC\_AVG[2:0] < 7 \\ \dfrac{GC\_X}{8}, & DSP\_GC\_AVG[2:0] = 7 \end{cases}$$

When *DSP_GC_AVG[2:0]* > 0, the start of the averaging can be triggered by reading out *GC_Q*. The averaged values can then be accessed via *GC_I* and *GC_Q* after the waiting period of t_{avg}, calculated as:

$$t_{avg} = \begin{cases} DSP\_GC\_AVG[2:0] \cdot \dfrac{26}{f_{ac}}, & DSP\_GC\_AVG[2:0] < 7 \\ 8 \cdot \dfrac{26}{f_{ac}}, & DSP\_GC\_AVG[2:0] = 7 \end{cases}$$

In addition, an optional on-chip self-calibration continuously adapts sensitivity, orthogonality, and offset during normal operation and EoL calibration to suppress 2nd-harmonic residues and angle drift over temperature, ageing, and mechanical tolerances. The angular phase and speed are tracked using a phase tracking loop, which operates by monitoring an error signal derived from the I/Q signals. The integration time is configurable to balance noise suppression and dynamic performance (refer to Section 6.5). The linearized phase can be read from register *LIN_PHASE[15:0]*, and the 16-bit speed value can be read via *SPEED[15:0]*. The phase tracking is followed by the compensation of internal processing delays. The delay-compensated values, accessible through *DRIFTC_PHASE[15:0]*, include an optional angular offset that can be applied via *PHASE_OFS[15:0]* for zero-angle calibration. Signal conditioning allows the adaptation of the internal 16-bit angle value to the bit width required by the output protocol. Before the angular value is provided as DSP_DATA to the output interface, its update frequency is scaled up to f_{ac} by linear interpolation.

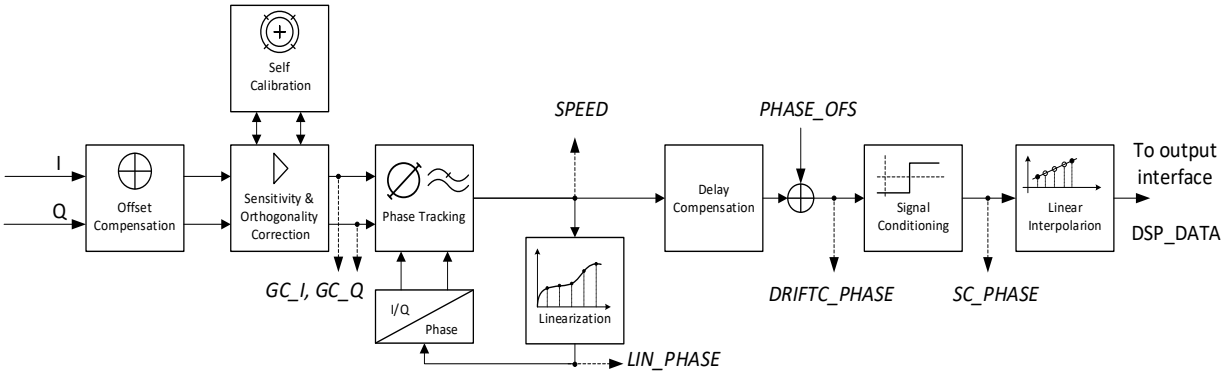


Figure 7: Digital signal processing architecture

6.5 High-dynamic performance

The phase-tracking loop bandwidth can be adapted to match application-specific dynamic behaviour. Two parameters control this behaviour: the loop filter constant (LFC) and the step-response overshoot (OS). Together they define the trade-off between fast tracking of angle changes and noise suppression.

The registers *DSP_LFC_LO[2:0]* and *DSP_LFC_HI[2:0]* define the allowed range of LFC values used for automatic bandwidth adaptation. Within this range, the device adjusts the effective loop bandwidth during operation according to the measured angular acceleration. Narrower bandwidth improves noise filtering and but increases the response time to fast angle changes. Wider bandwidth enables better tracking of rapid dynamics but makes the output more sensitive to noise. Setting *DSP_LFC_LO[2:0]* and *DSP_LFC_HI[2:0]* to the same value fixes the LFC and therefore disables automatic bandwidth adaptation.

The step-response overshoot is configured via *DSP_SROS[1:0]*. Lower overshoot settings provide a more damped, monotonic response with minimal ringing, while higher overshoot settings yield a faster response at the expense of transient overshoot in the angle output.

The step response behaviour and the angular error due to acceleration at different LFC and OS values are shown Figure 8 and Figure 9, using simulated results.

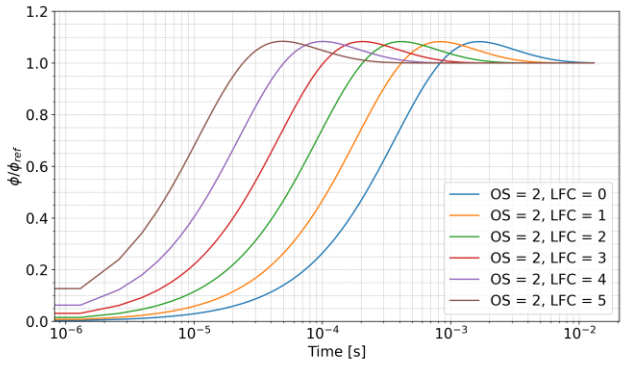


Figure 8: Step response ϕ/ϕ_{ref} over loop filter bandwidth LFC

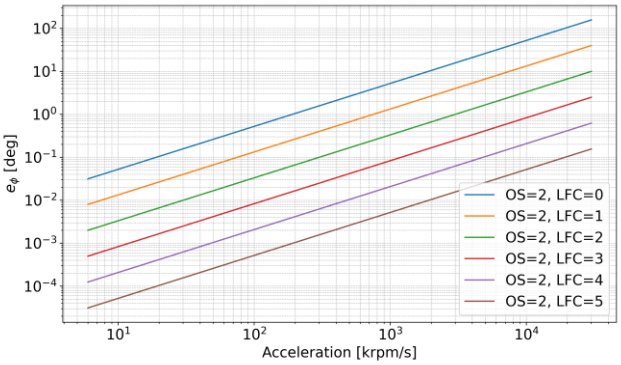


Figure 9: Angular error e_ϕ over acceleration and loop filter bandwidth LFC

OS	Overshoot (%)
0	2.7
1	5.1
2	8.9
3	15.2

Table 20: Overshoot in % over OS

LFC	Cutoff frequency f_{-3dB} (Hz)			
	OS = 0	OS = 1	OS = 2	OS = 3
0	495	509	539	595
1	990	1020	1079	1193
2	1989	2049	2168	2396
3	4010	4132	4374	4835
4	8158	8410	8906	9852
5	16914	17450	18500	20498

Table 21: Cut-off frequency over LFC and OS

6.6 Calibration and linearization

6.6.1 Impact of calibration and linearization on internal diagnostics

The phase tracking loop contains a safety monitor (DIAG_ALF) that observes the angular acceleration error in the phase tracking loop (PLL) between the PLL feedback and the I/Q input signal. It provides a safeguard against situations where excessive phase error builds up due to rapid changes in magnet speed or signal disturbances. Non-linearities (INL) that cannot be calibrated or linearized out (or remain uncalibrated) introduce harmonic content into the electrical angle. These harmonics appear to DIAG_ALF as periodic acceleration and can therefore trigger the monitor. Refer to the MLX90382 Application Note [6] and the MLX90382 Safety Manual [3] for the correct configuration of *DIAG_ALF_THD* to prevent false-positive triggers during EoL calibration and in operation.

6.6.2 I/Q sensitivity and orthogonality calibration

The sensitivity and orthogonality between the I-channel and Q-channel are factory calibrated but can change within the application. A common example is off-axis positioning of the IC with different field amplitudes in X-Y and Z directions. The relative sensitivity and orthogonality between the I-channel and Q-channel can be adjusted via *S_QQ[15:0]* and *S_IQ[15:0]*, respectively, minimizing the angular error over a full electrical period

before applying the 16-Point Linearization. This correction is applied to the *GC_I* and *GC_Q* values (see Figure 7) during the sensitivity and orthogonality correction step as follows:

$$\begin{bmatrix} GC_I \\ GC_Q \end{bmatrix} = \begin{bmatrix} 1 & S\_IQ/2^{15} \\ 0 & S\_QQ/2^{15} \end{bmatrix} * \begin{bmatrix} I \\ Q \end{bmatrix}$$

6.6.3 Self-calibration

The MLX90382 provides an optional self-calibration method that measures and tracks relative sensitivity and orthogonality of the I/Q signals during motion. The tracked sensitivity can be read out via *RMM_AS_QQ*[15:0] and the orthogonality via *RMM_AS_IQ[15:0].* Self-calibration is enabled by setting *DE_DSP_RMM[1:0] = 0*.

The method can be applied to remove mismatch from the IC and due to mechanical misalignment. During EoL calibration, device-specific trim values for relative sensitivity and orthogonality can be self-calibrated by the IC and programmed to the NVRAM manually. During operation, the routine continuously tracks and corrects residual drift of relative sensitivity and orthogonality. This significantly improves angle accuracy over temperature, mechanical tolerances and lifetime.

Figure 10 shows an example of the angular error after start-up of the self-calibration routine with sensitivity and orthogonality correction enabled, for an end of shaft scenario (1 mm lateral displacement, 1 deg tilt, Neodym magnet: d = 12 mm, h = 6 mm). The compensation of the 2nd harmonic in the angular signal converges to its optimal result after several electrical rotations, leaving only a residual 1st harmonic. For the programming procedure and recommended settings for all self-calibration related registers, refer to the MLX90382 Application Note [6]. The achievable accuracy depends on the magnet and mechanical tolerances.

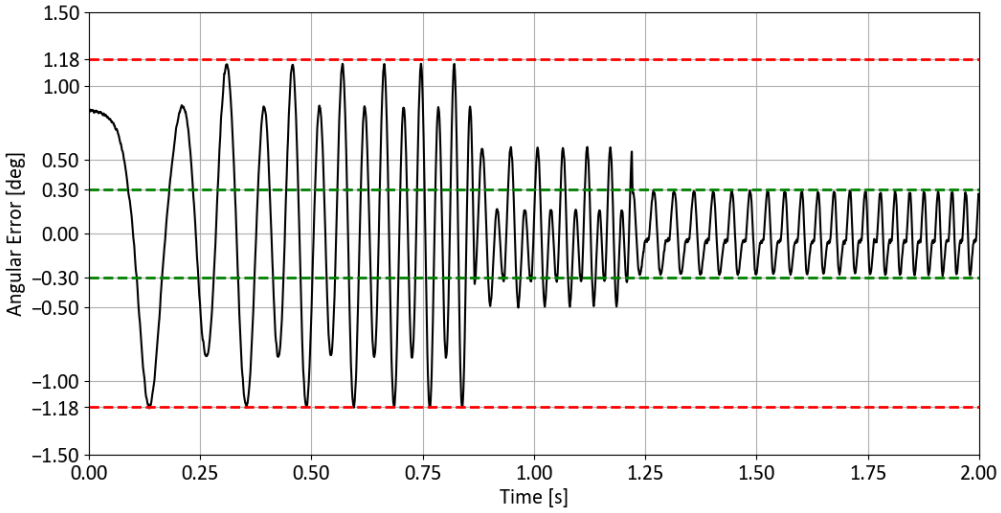


Figure 10: Example of a self-calibration scenario

6.6.4 16-Point Linearization and zero position adjustment

The 16-Point Linearization feature allows compensation for angular deviations caused by asymmetries in the sensor system, which includes the magnet and the sensor IC. The 8-bit signed equalization values (*PEQ00[7:0]* to *PEQ15[7:0]*) define an angular error curve at angular sample points of 360/16 degrees * [00 .. 15]. All intermediate values are linearly interpolated, as shown in Figure 11. After equalization, the residual error curve is the difference between the input error curve and the interpolated equalization curve. The angular error curve should be measured with quasi-static rotation.

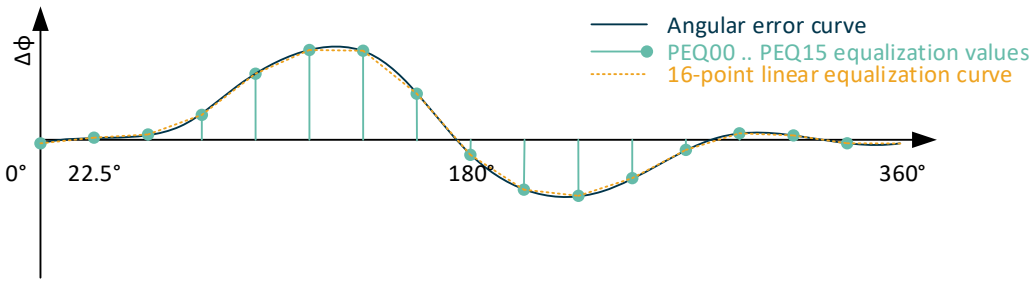


Figure 11: 16-Point Linearization of angular error curve

The equalization strength versus resolution can be adjusted using *PEQ_GAIN[2:0]*. If *PEQ_GAIN* is set to 0, no equalization is applied. For *PEQ_GAIN[2:0]* = [1..7], the error curve is adjusted per sample point as follows:

$$\Delta\varphi(xx) = signed(PEQxx[7:0]) * 2^{PEQ\_GAIN[2:0]-17} * 360[deg.]$$

The signed equalization values *PEQ00[7:0]* to *PEQ15[7:0]* range from -127 to 127. Table 23 details the equalization range and resolution for each sample point. In Figure 11, the adjustable range for the programmable linearization is illustrated.

PEQ_GAIN[2:0]	Resolution [deg]	Range (+/-) [deg]
0	0	0
1	0.0055	0.70
2	0.011	1.40
3	0.022	2.79
4	0.044	5.58
5	0.088	11.16
6	0.176	22.32
7	0.352	44.65

Table 22: Equalization range and resolution per sample point for PEQ_GAIN

Additionally, the angle of the magnet that results in a zero output value can be adjusted by setting the field *PHASE_OFS[15:0]*. This value is systematically added to the position value calculated by the phase tracking loop.

6.7 Delay compensation

The speed signal provided by the phase tracking loop is used to compensate for phase errors caused by system latency in case of angular speed. The compensation can be disabled by setting *DSP_DRIFTC_DIS = 1.* Furthermore, the register *DELAY_CUS[7:0]* can be used to compensate for additional delays, such as related to filter networks in between the MLX90382 and the MCU, in steps of (26/64)/f_{RCO}.

6.8 Signal conditioning

The signal conditioning function maps the 16-bit electrical angle to the desired output range used by SPI/SSI or PWM. The input is the 16-bit measured angle value *DRIFTC_PHASE* (see Figure 7), after delay compensation and phase offset adjustment. It is configured with four two's-complement parameters: *SC_X1[15:0]*, *SC_X2[15:0]* (input stage) and *SC_Y1[15:0]*, *SC_Y2[15:0]* (output stage). Figure 12 shows the calculation steps of the procedure.

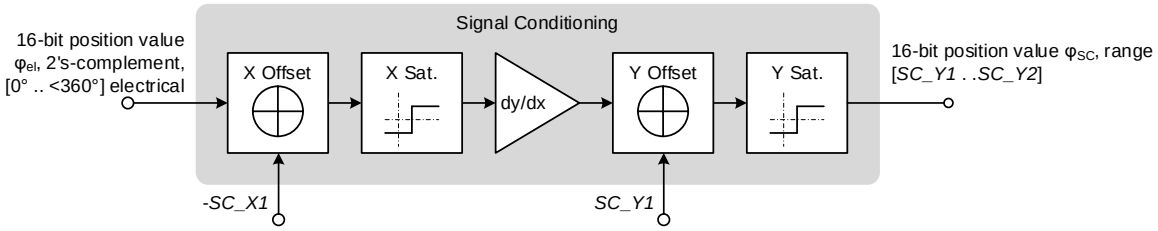


Figure 12: Signal Conditioning Functional Block Diagram

The input stage selects the angle range of interest by defining a window with *SC_X1* and *SC_X2* and saturates any measured angle outside [*SC_X1 … SC_X2*]. There is no constraint on the ordering of *SC_X1* and *SC_X2*, so the selected range may wrap across the zero point.

The output stage adds the offset *SC_Y1* and limits the result to [min(*SC_Y1, SC_Y2*) … max(*SC_Y1, SC_Y2*)]. If *SC_X1* < *SC_X2* but *SC_Y1* > *SC_Y2*, the transfer characteristic is inverted. Either stage can be bypassed by setting its values to [0, 0] or to full scale [0, 2^16−1]. Within the saturated region, the position of the transition between *SC_Y1* and *SC_Y2* is shifted by *SC_HL[7:0]*, which specifies an offset from the window center (*SC_X1*+*SC_X2*)/2 steps of 360°/2^8. The resolution of the angle after signal conditioning $\Delta\varphi_{sc}$ can be calculated with:

$$\Delta\varphi_{sc}[deg.] = \frac{360}{2^{16}} * \max\left(1, \frac{|unwrap(SC\_X2 - SC\_X1)|}{|SC\_Y2 - SC\_Y1|}\right)$$

SC_YE[15:0], defines a fault-band on the output. If the angular values fall inside this band, the device asserts the fail-safe state SS3 (see the MLX90382 Safety Manual [3]). Figure 14 illustrates an example with an unrestricted input range and a defined output range including a fault band.

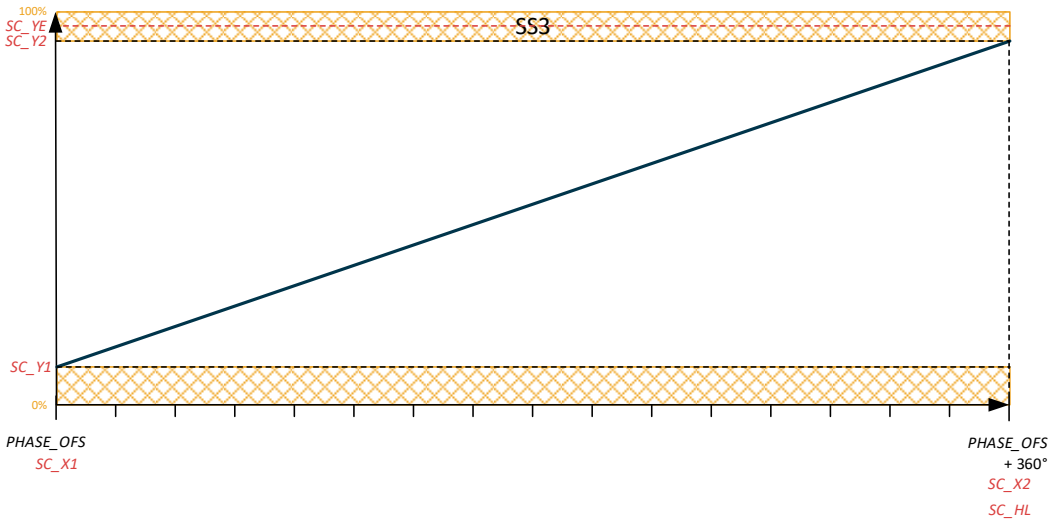


Figure 13: 360° application with signal conditioning

7 Functional safety

According to ISO26262 [7]/IEC61508 [8], the MLX90382 achieves ASIL-B/SIL-2. This section provides a brief overview. The technical safety concept is described in detail in the MLX90382 Safety Manuals [3] [4] [5].

7.1 Top technical safety requirement

The following top-technical safety requirement is covering the main-mission of the MLX90382. For further details refer to the MLX90382 Safety Manual [3].

Item	Definition
Top Technical Safety Requirement MLX90382	The MLX90382 shall detect faults leading to an angular error higher than the angle error safety specification and, in case of fault detection, switch into a fail-safe state within the specified FHTI time.
ASIL	B
Angle error safety specification	± 4°
Operating conditions	The MLX90382 shall work under the operating conditions defined in the datasheet (e.g. operating range, speed, temperature profile, magnetic conditions, power-supply …)
FHTI, max	1 ms
Fail-Safe States	SS2 or SS3 according to the programmed fault reporting modes (see Table 24)
HW architectural metric targets	• SPFM > 90% • LFM > 60% • PMHF < 10 FIT (according to IEC/TR 62380)

Table 23: MLX90382 Top technical safety requirement

7.2 Safety mechanism overview

Built-in monitors in the MLX90382 cover the main IC domains and signal path. Supply monitors continuously check the external VDD for over/undervoltage and the internal analog/digital supplies for over/undervoltage. Wire-break on VDD/VSS is also detected. A temperature monitor compares die temperature against programmable thresholds. Magnetic signal amplitude is monitored by the AGC amplitude window and gain-clamping diagnostics. ADC linearity and conversion are also monitored. Motion dynamics are monitored via a DSP speed threshold, while adaptive loop-filter diagnostics trigger on tracking/phase errors. Digital robustness is covered by NVRAM CRC/ECC and DSP process checks.

7.3 Fault Reporting

In case of random internal failure detection that violates the angle error safety specification, the MLX90382 transitions to one of its fail-safe states SS2 or SS3.

7.3.1 Fault categories

Two categories of faults are defined:

- **Critical faults**, that potentially interrupt the communication function (SS2 fail-safe state). They are typically caused by failures in (1) the external or internal supply voltage and (2) the digital part or the non-volatile memory.
- **Non-critical faults**, arising from the external environment and the analog sensing circuit, which potentially corrupt or affect the accuracy of the calculated angle. Such faults lead to a warning information in SPI(SSI) frames (SS3 fail-safe state). They are typically caused by failures in (1) the environment, (2) the analogue sensing parts and (3) the digital signal processing circuits.

Both types of faults can violate the top technical safety requirement. The fault reporting mode depends on the kind of fault.

7.3.2 Reporting of critical faults (SS2)

Critical faults are immediately reported by setting the MLX90382 to fail-safe state SS2. When reaching fail-safe state, any transmission is interrupted and all outputs except SPI output are set to high-impedance (tristate).

The SS2 fail-safe state allows a fix using the remaining working SPI communication.

7.3.3 Reporting of non-critical faults (SS3)

A non-critical fault leads to different possible fail-safe states, depending on the options programmed in the NVRAM.

Mode	NVRAM configuration	SS3 OUT state
ABI/UVW	Independent from ABI/UVW interface configuration	Hi-Z (like SS2)
PWM	*SC_YE* configured as: *SC_YE* < min(*SC_Y1, SC_Y2*) or *SC_YE* > max(*SC_Y1, SC_Y2*)	Fault Band
	SC_YE configured as: min(*SC_Y1, SC_Y2*) < *SC_YE* < max(*SC_Y1, SC_Y2*)	Hi-Z (like SS2)
SPI	*SC_YE* configured as: *SC_YE* < min(*SC_Y1, SC_Y2*) or *SC_YE* > max(*SC_Y1, SC_Y2*) *SPI_FRFSEN* = 1	Inverted Frame Start Byte and Fault Band
	SC_YE configured as: min(*SC_Y1, SC_Y2*) < *SC_YE* < max(*SC_Y1, SC_Y2*) *SPI_FRFSEN* = 0	Hi-Z (like SS2)
	SC_YE configured as: min(*SC_Y1, SC_Y2*) < *SC_YE* < max(*SC_Y1, SC_Y2*) *SPI_FRFSEN* = 1	Inverted Frame Start Byte
	SC_YE configured as: *SC_YE* < min(*SC_Y1, SC_Y2*) or *SC_YE* > max(*SC_Y1, SC_Y2*) *SPI_FRFSEN* = 0	Fault Band
SSI	*SC_YE* configured as: *SC_YE* < min(*SC_Y1, SC_Y2*) or *SC_YE* > max(*SC_Y1, SC_Y2*)	Fault Band
	SC_YE configured as: min(*SC_Y1, SC_Y2*) < *SC_YE* < max(*SC_Y1, SC_Y2*)	Hi-Z (like SS2)

Table 24: Reporting of non-critical failures

8 Interfaces

8.1 I/O architecture and interface selection

The interface stage features several input and output channels that can be selected by customers according to Table 3: QFN-24 package pinout and Table 4: TSSOP-16 and TSSOP-16_EP package pinout.

8.1.1 Digital input channel

Each input channel contains an optional low-pass filter with cut-off frequency INP_{LPF3dB} to further improve EMC robustness. The filter can be individually enabled on CS, MOSI, and SCLK by setting *PHY_RC_EN[2:0]*. The specifications for the input channels are listed in Table 25. The input channel includes internal pull-up resistors R_{INT_CS} and R_{INT_SCLK} on pins CS and SCLK (see Table 25) to maintain stable logic levels. These pull-ups can be disabled by setting *PHY_CS_RPU_DIS* = 1 and *PHY_BV_RPU_DIS* = 1.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Low Voltage Detection Level		25.0	35.0	42.0	% V_{DD}	
Input High Voltage Detection Level		52.0	60.0	75.0	% V_{DD}	
Input Hysteresis Level		18.0	25.0	42.0	% V_{DD}	
Input Voltage Range		0		100	% V_{DD}	
Input EMC Filter Cut-Off Frequency	INP_{LPF3dB}	3.5	6.0	10.5	MHz	Setting *PHY_RC_EN[2:0]* to enable EMC filter.
Internal pull-up resistor CS	R_{INT_CS}	8.0	14.0	28.0	kΩ	Internal pull-up resistor for input pins: (1) CS in QFN-24 and (2) CS0/1 in TSSOP-16/ TSSOP-16_EP. The resistor can be disabled via *PHY_CS_RPU_DIS* = 1.
Internal pull-up resistor SCLK	R_{INT_SCLK}	8.0	14.0	28.0	kΩ	Internal pull-up resistor for input pins: (1) SCLK in QFN-24 and (2) SCLK0/1 in TSSOP-16/ TSSOP-16_EP/ The resistor can be disabled via *PHY_CS_RPU_DIS* = 1.

Table 25: Input channel specifications

8.1.2 Digital output channel

The output driver strength for all driver stages in 5 V supply mode is factory trimmed to limit the maximum output current as specified in Table 26 and Table 27 for pin mapping. The driver strengths can be changed by programming *GPIO_CFG[2:0]* and *ABI_CFG[2:0]*, but must not exceed the factory trimmed value in 5 V supply mode. In 3.3 V mode, however, the maximum driver strength configuration is recommended.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Maximum output short circuit current per channel	$I_{OS,max}$	5.0	15.0	30.0	mA	3.3 V supply mode. *GPIO_CFG[2:0]* = 7 and *ABI_CFG[2:0]* = 7.
		9.0	25.0	55.0	mA	5V supply mode. Factory trimmed settings for *GPIO_CFG[2:0]* and *ABI_CFG[2:0]*.

Table 26: Maximum output short circuit current per channel

NVRAM Field	Pins (QFN-24)	Pins (TSSOP-16 and TSSOP-16_EP)
GPIO_CFG	GPIO	GPIOx
ABI_CFG	AU, IW, BV (AU_N, SCLK and MOSI) for differential ABI/UVW	AUx, SCLKx, MOSIx

Table 27: Pin mapping for GPIO_CFG and ABI_CFG

The driver for the output pins can be configured in different modes listed in Table 28 via *GPIO_CFG[4:3]* and *ABI_CFG[4:3]*. Each output pin voltage ranges from 0 V to VDD external supply. See Table 27 for the pin mapping.

GPIO_CFG[4:3]/ABI_CFG[4:3]	Output Driver Mode
00	Hi-Z
01	Open drain p-MOS
10	Open drain n-MOS
11	Push-pull

Table 28 Output driver modes

8.1.3 Activation of SPI interface

If CS is set to low, the SPI communication is always activated without considering the interface selection in *GPIO_IF[1:0]*.

8.1.4 Interface selection for QFN-24

The interface function of the GPIO, AU_N, SCLK, MOSI and AU/BV/IW pins can be selected by setting *GPIO_IF[1:0], ABI_IF, ABI_DIFF* and *ABI_PORT*.

The individual configuration is listed in Table 29 referring to the pin description in Table 3.

By setting *ABI_PORT* = 0, the ABI/UVW and SPI interface signals share the same physical pins on the single-die QFN24 package (see Table 29). This allows seamless switching between ABI/UVW output during normal operation and SPI communication during programming mode, with the same set of pins being used for both interfaces without external reconfiguration.

Mode	NVRAM settings				Pin configuration							
	GPIO_IF	*ABI_IF*	*ABI_DIFF*	*ABI_PORT*	AU	BV	IW	GPIO	CS	AU_N	SCLK	MOSI
A0	2	1	0	1	A	B	I	SPI: MISO	SPI:CS	Hi-Z	SPI: SCLK	SPI: MOSI
	2	1	0	0	Hi-Z	Hi-Z	Hi-Z	SPI: MISO	0	Hi-Z	SPI: SCLK	SPI: MOSI
	2	1	0	0	Hi-Z	Hi-Z	Hi-Z	SPI: MISO	1	A	B	I
A1	2	0	0	1	U	V	W	SPI: MISO	SPI:CS	Hi-Z	SPI: SCLK	SPI: MOSI
	2	0	0	0	Hi-Z	Hi-Z	Hi-Z	SPI: MISO	0	Hi-Z	SPI: SCLK	SPI: MOSI
	2	0	0	0	Hi-Z	Hi-Z	Hi-Z	SPI: MISO	1	U	V	W
A2	1	1	0	1	A	B	I	SSI: DATA	SPI:CS	Hi-Z	SSI: SCLK	Hi-Z
A3	1	0	0	1	U	V	W	SSI: DATA	SPI:CS	Hi-Z	SSI: SCLK	Hi-Z
A4	0	1	0	1	A	B	I	PWM	SPI:CS	Hi-Z	Hi-Z	Hi-Z
	0	1	1	1	A	B	I	PWM	SPI:CS	A_N	B_N	I_N
A5	0	0	0	1	U	V	W	PWM	SPI:CS	Hi-Z	Hi-Z	Hi-Z
	0	0	1	1	U	V	W	PWM	SPI:CS	U_N	V_N	W_N

Table 29: Interface mode selection for QFN-24

8.1.5 Interface Selection for TSSOP-16 and TSSOP-16_EP

The interface function of the GPIO0/1, AU0/1, SCLK0/1 and MOSI0/1 pins can be selected by setting *GPIO_IF[1:0], ABI_IF[0]* and must be set individually for each of the two IC's inside the TSSOP-16 and TSSOP-16_EP package. The individual configuration is listed in Table 30 referring to the pin description in Table 4.

Mode	NVRAM settings		Pin configuration				
	GPIO_IF	*ABI_IF*	GPIOx	CSx	AUx	SCLKx	MOSIx
A0	2	x	SPI: MISO	SPI:CS	Hi-Z	SPI: SCLK	SPI: MOSI
A1	1	x	SSI: DATA		Hi-Z	SSI: SCLK	Hi-Z
A2	0	1	PWM		A	B	I
A3	0	0	PWM		U	V	W

Table 30: Interface mode selection for TSSOP-16 and TSSOP-16_EP

8.2 SPI slave interface

8.2.1 General Description

The SPI slave interface for customer programming allows read/write access to all registers and memories, including the sensor position data. It operates up to 10 MHz SPI clock full-duplex and is designed to support functional safety, continuous readout, and multi-slave synchronization. The SPI supports all standard clock and phase modes for data exchange, which can be selected using *SPI_MODE[1:0]*.

8.2.2 SPI Timing Specifications

The capacitance C_L refers to the max. load on the signal wire.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SPI Clock Frequency	f_{SCLK}	0.04		10.0	MHz	*PHY_RC_EN[2:0]* = 0 (Input EMC Filter Off), 5 V mode, $C_L \leq 20$ pF
		0.04		6.5	MHz	*PHY_RC_EN[2:0]* = 0 (Input EMC Filter Off), 3.3 V mode, $C_L \leq 50$ pF
		0.04		4.0	MHz	*PHY_RC_EN[2:0]*=1 (Input EMC Filter On), $C_L \leq 50$ pF
SPI Idle time	SPI_{tIDLE}	1.0			$1/f_{SCLK}$	Idle time between consecutive SPI transactions. $\overline{CS}$ is at high state.
SPI CS inactive delay after SCLK active edge	SPI_{tCS1}	4.0			$1/f_{AC}$	SPI Write
		1.0			$1/f_{AC}$	SPI Read and SPI Frame Read
SPI CS active until SCLK active edge delay	SPI_{tCS0}	0.5			$1/f_{SCLK}$	*SPI_DBNC_CS[3:0]* = 0, *SPI_DBNC[3:0]* = 0
SPI MISO disable delay after CS_B rising edge	SPI_{tOD}			100.0	ns	
SPI MISO enable delay after CMD byte	SPI_{tOE}			100.0	ns	*SPI_DBNC_CS[3:0]* = 0, CMD OK
MISO Data Delay	SPI_{tSDO}			40.0	ns	C_L = 20 pF, SCLK edge to MISO 70% VDD for 5 V mode.
				80.0	ns	C_L = 50 pF, SCLK edge to MISO 70% VDD for 3.3 V mode.
MOSI Setup Time	SPI_{tSU_MOSI}	0.25			$1/f_{SCLK}$	*SPI_DBNC[3:0]* = 0
MOSI Hold Time	SPI_{tHD_MOSI}	0.25			$1/f_{SCLK}$	*SPI_DBNC[3:0]* = 0

Table 31: SPI timing specification

8.2.3 SPI Transaction for Register Read/Write Access

Data exchange is possible with three different SPI protocol variants: Register Read (RR), Register Write (RW) and Frame Read (FR). The structure of the protocols is shown in Figure 14. All transactions start with a command byte. For Register Read and Register Write, the 6-bit command pattern shall match exactly. In case of mismatch, the device always responds as in Frame Read mode. RR and RW modes are active while CS = 0 ignoring the *GPIO_IF[1:0]* setting. Using FR mode needs a configuration of *GPIO_IF[1:0]* = 2 (SPI-Bus mode). The address byte ADR refers to the IC address space shown in Section 11. As the LSB of the 9-bit address ADR is always “0”, only the upper 8-bit part of the address is used for RR, RW and FR operations.

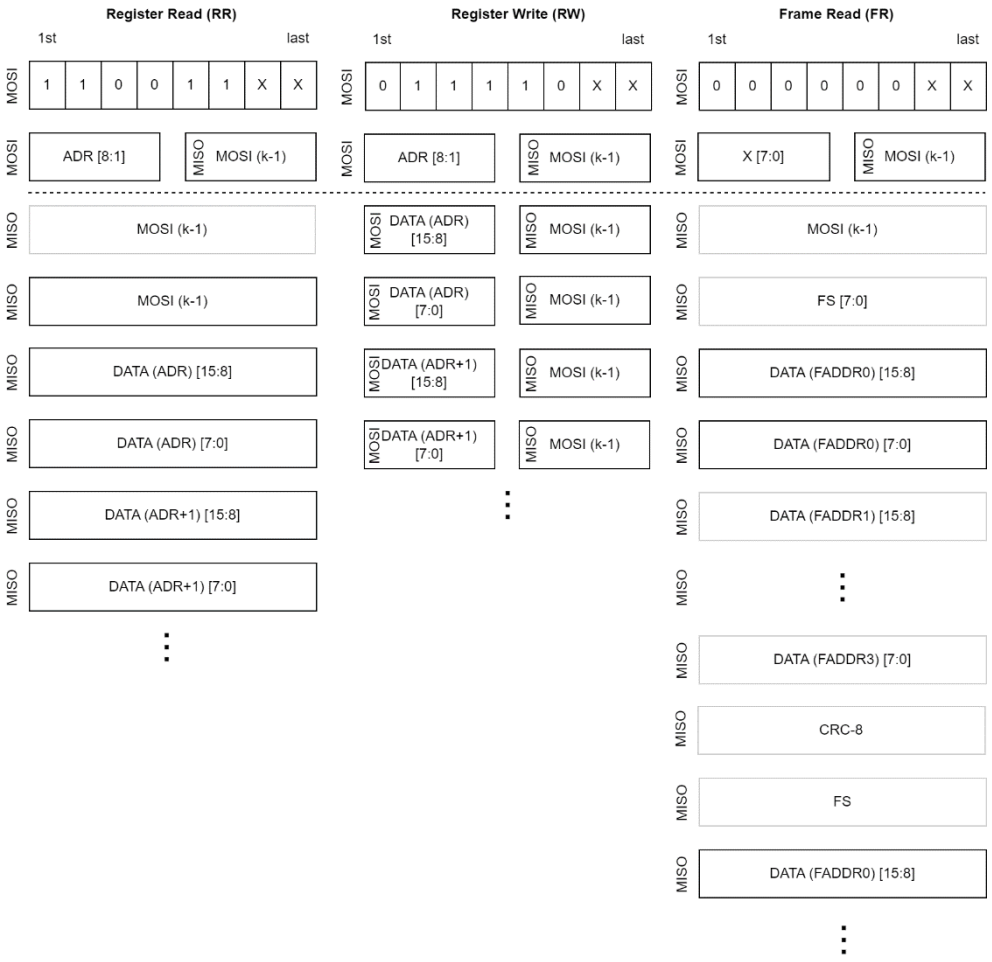


Figure 14: SPI Protocols for Read/Write and Frame Read

8.2.3.1 Register Read (RR)

The register read operation begins by sending the command byte, followed by the aligned address byte. An optional third byte can be used to adjust the word alignment of the data transfer, which can be enabled using the *SPI_DMY* bit. The subsequent byte is a dummy byte. The signal timing constraints for the register read operation are shown in Figure 15.

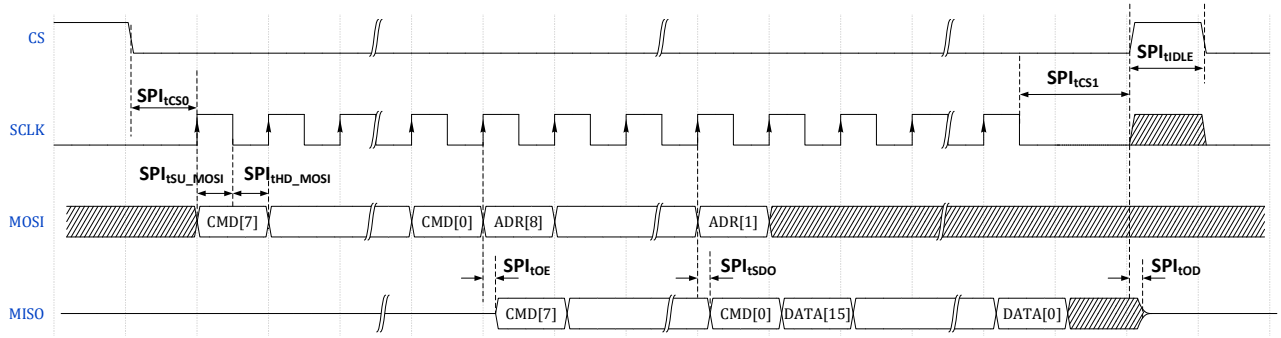


Figure 15: Timing for SPI Register Read with SPI Mode 1 (CPOL = 0, CPHA = 1)

Multiple bytes can be read sequentially during EOL calibration and non-safety related applications. This read option must not be used for safety related applications (e.g. ASIL, SIL). The multiple bytes read enables a fast and efficient communication. Starting from the provided address, multiple bytes can be read sequentially. The register *DE_SR[2:0]* = 3 must be set before reading a larger number of registers. Once the read attempt is complete, the register must be reset to its default value. The angular value must not be used during this procedure.

Register	Address	Bit	R/W	Default	Description
DE_SR	0x0BE	[3:1]	R/W	0	Disable Shadow Register Monitor. If 3, register monitor is disabled.

Table 32: MLX90382 register address for disabling shadow register monitor

8.2.3.2 Register Write (RW)

The register write operation begins by sending the command byte, followed by the aligned address byte. This allows access to all device registers. Multiple registers can be written sequentially, starting from the provided address. The signal timing constraints for the register write operation are shown in Figure 16.

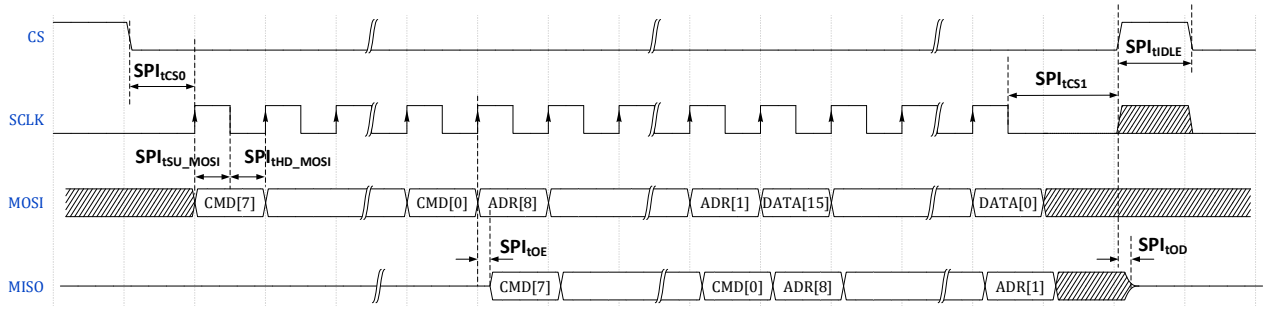


Figure 16: Timing for SPI Register Write with SPI Mode 1 (CPOL = 0, CPHA = 1)

8.2.3.3 Frame Read (FR)

When operating in Frame Read (FR) mode, the device transmits the content of up to four register addresses. This transmission can be initiated by an optional Frame Start (FS) byte and terminated by an optional CRC-8 byte. The FS byte is enabled via the *SPI_FRFSEN* bit and consists of a configurable content (*SPI_FRFS[3:0]*) and a rolling counter. The rolling counter, which defines a nibble of the optional FS byte, allows the MCU to detect desynchronization that may result from lost SCLK edges. The composition of the FS byte is shown in Table 33.

Bit	7	6	5	4	3	2	1	0
Content	*SPI_FRFS*				Rolling Counter			

Table 33: Frame start byte in Frame Read

The second byte of the FR frame is ignored but still transmitted to prevent bus congestion in half-duplex mode and to allow command fail checks by the MCU. An optional third dummy byte can be enabled via the *SPI_DMY* bit to adjust the word alignment of the data transfer. The content of register addresses for readout can be configured by setting *SPI_FADDR0..3*. If *SPI_FADDR0[7:0]* is set to 0x00, the angular value will be transmitted (see Section 8.2.4.1). If one of the *SPI_FADDR1..3* register is set to 0x00, its content will not be transmitted and will not part of the frame. The length of the FR frame is defined as:

$$L_{Frame}[byte] = SPI\_FRFSEN + 2 \cdot (1 + (SPI\_FADDR1 > 0) + (SPI\_FADDR2 > 0) + (SPI\_FADDR3 > 0)) + SPI\_FRCRCEN.$$

The optional CRC-8 byte, which can be activated using the *SPI_FRCRCEN* bit, protects the data fields. An additional method for detecting transmission errors is provided via binary inversion. By setting the bit position “x” in field *SPI_FRINV[3:0],* the byte of content *DATA(FADDR”x”)* will be binary inverted. A comparison between inverted and non-inverted DATA allows error detection.

8.2.4 SPI Data Sample Timing

8.2.4.1 Angle Data Sampling in Frame Read Mode

By setting *SPI_FADDR0* = 0x00, the angle value is sampled from digital signal processing with a maximum distance of (*SPI_CPTLT[2:0]* + 0.5) * 1/f_{SCLK} [s] before the *DATA(FADDR0)* word. To ensure correct internal data acquisition, it is necessary to adjust *SPI_CPTLT* accordingly:

$$SPI\_CPTLT \geq 5 \cdot \frac{f_{SCLK}}{f_{ac}} - 0.5$$

8.2.4.2 Data Sampling

All registers, in FR mode for *SPI_FADDR0* != 0x00, will be captured in the beginning of the previous byte transfer.

8.2.5 SPI Transaction for Synchronous Read Access of Multiple Slaves

The SPI interface allows synchronous capturing and sequential transmission of angular data with multiple SPI slaves on a shared SPI interface. The Super Frame Read (SFR) mode defines a delayed transmission of the FR response frame, facilitating a time-division-multiple-access (TDMA) scheme on the MISO line. This setup supports up to 16 SPI slaves, allowing them to capture or measure synchronized data and transmit it sequentially on the shared MISO bus. A common use case for the SFR is the Dual-Die product configuration, as shown in Section 4.2. The configuration of the SFR is described in the following sections.

8.2.5.1 Time-division multiple access via Super Frame Read mode

The time-division multiple access (TDMA) mechanism is controlled through *SPI_SFRDLY[7:0]* in the slave device(s). This configuration defines the delay, in bytes, between the start of the first byte in the SFR frame and the beginning of the specific slave device's first byte within the SFR frame.

8.2.5.2 Angular capture point

The capture point of the angular value can be synchronized across all slave devices by setting bit *SPI_SFR_SCPT = 1*. This ensures that the capture point is aligned with the position of the very first *DATA(FADDR0)[15:8]* byte within the entire Super Frame. To ensure synchronization, *SPI_CPTLT[2:0]* should be identical on all slave devices to capture the angular data at the same position before the first *DATA(FADDR0)[15:8]* in the Super Frame. If bit *SPI_SFR_SCPT* = 0, the angular position is captured before each individual slave device's *DATA(FADDR0)[15:8]*. The synchronization options are illustrated in Figure 17 and the timing behaviour is described in Section 8.2.4.1.

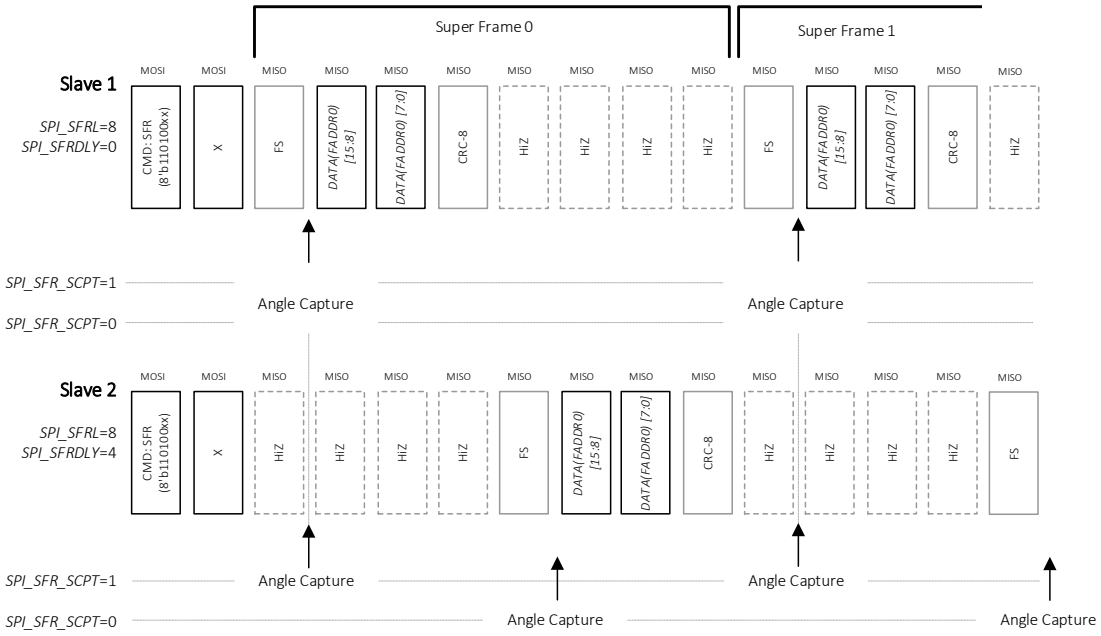


Figure 17: Angle capture synchronization in Super Frame Mode with example FR configuration

8.2.5.3 Super Frame length alignment

The Super Frame length (L_{SFrame}) must be set as the sum of all bytes composed of the individual frame (see Section 8.2.3.3) of each slave device, using *SPI_SFRL[7:0]*. The frame length of each slave can differ. The total frame length can be calculated as:

$$L_{SFrame}[byte] = SPI\_SFRL = \sum_{i=1}^{N} L_{Frame}(i)$$

8.2.6 SPI EMC debounce filter

The SPI inputs SCLK, CS and MOSI have dedicated digital symmetric debounce filter with programmable filter depth. *SPI_DBNC[3:0]* and *SPI_DBNC_CS[3:0]* configure the debouncing delay for SCLK (τ_{SCLK}), MOSI (τ_{MOSI}) and CS (τ_{CS}) respectively as follows:

$$\tau_{CS}\,[s] = SPI\_DBNC\_CS[3:0] * \frac{2}{f_{RCO}}$$

$$\tau_{MOSI}, \tau_{SCLK}[s] = \frac{SPI\_DBNC[3:0]}{f_{RCO}}$$

It is important to consider that SPI_{tOD}, SPI_{tOE} and SPI_{tSDO} will accumulate with the defined debouncing delay. Next to this, the setting of *SPI_DBNC[3:0]* > 0 limits the maximum SCLK frequency.

8.3 SSI output

In SSI mode, the angular value is transmitted as a 16-bit data word with in a 16-bit frame, with a clock period of T = $1/f_{SCLK}$. The MCU provides the SSI clock and controls the pause time T_P between two consecutive frames. After each frame, the device requires a minimum pause time T_M to recognize that the transmission is complete T_M is configured via *SSI_TM[7:0]* as follows:

$$T_M[s] = (SSI\_TM[7:0] + 1) \cdot \frac{8}{f_{ac}}$$

The pause time (T_P) must consider T_M and a minimum idle time, such that: $T_P \geq T_M + 0.5$ µs. A Data line high level during the pause period T_P, following the timeout period T_M, requires a pull-up resistor on the Data line, as shown in the recommended example application diagrams in Chapter 0.

If the MCU triggers 16 or more clocks (without any clock violation), the last transmitted word is repeated, starting with the MSB. The diagram in Figure 18 illustrates two consecutive readouts of the same angular value, followed by a third readout of a new angular value activated after a clock timing violation. The timing specifications are list in Table 31.

8.3.1 SSI Timing Specification

The capacitance C_L refers to the max. load on the signal wire.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SSI Clock Frequency	f_{SCLK}	0.04		10.0	MHz	*PHY_RC_EN[2:0]* = 0 (Input EMC Filter Off), 5 V mode, $C_L \leq 20$ pF
		0.04		6.5	MHz	*PHY_RC_EN[2:0]* = 0 (Input EMC Filter Off), 3.3 V mode, $C_L \leq 50$ pF
		0.04		4.0	MHz	*PHY_RC_EN[2:0]*=1 (Input EMC Filter On), $C_L \leq 50$ pF
SSI Data Delay	SSI_{tSDO}			40.0	ns	C_L = 20 pF, SCLK rising edge to Data 70% VDD for 5 V mode.
				80.0	ns	C_L = 50 pF, SCLK rising edge to Data 70% VDD for 3.3 V mode.

Table 34: SSI timing specification

8.3.2 SSI Data Sample Timing

The DSP output is sampled based on the configuration of *SSI_CPT[14]*, as listed in Table 35.

- If *SSI_CPT[14]* = 1, the data is always captured at the rising edge of T_M. Consequently, the age of the angular information in the next SSI clock sequence is T_P - T_M. It should be noticed that the data at the first clock sequence after start-up contains no valid information, as no capture event was triggered before this point.
- If *SSI_CPT[14]* = 0, the data is always captured at the first falling edge of SCLK.

SSI_CPT[14]	Description	Condition
0	The data will always be captured at the first falling edge of SCLK	SCLK ≤ 2MHz
1	The data will always be captured after T_M	

Table 35: Configuration of SSI angle capture point

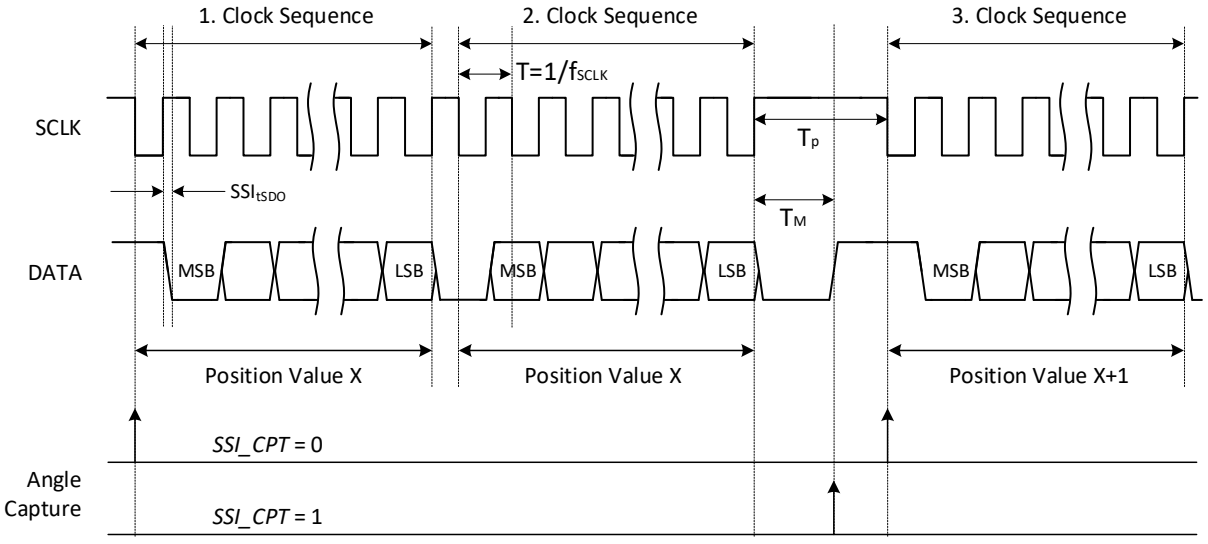


Figure 18: SSI timing diagram

8.3.3 SSI Interface Configuration

If SSI mode is selected by setting *GPIO_IF[1:0]* = 1, the field *SPI_MODE[1:0]* must be set to 1. If further SPI communication is required, the SPI master must be configured accordingly.

8.3.4 SSI Parity Bit

If *SSI_PARPOS[3:0]* < 9, an optional odd parity bit of all bits before the parity bit position can be transmitted within the 16-bit frame. With the parity bit applied, the maximum transmittable angular output resolution is 15 bits. *SSI_PARPOS[3:0]* specifies the position of the parity bit within the 16-bit frame and allows adjustment of the SSI frame width as all following content after the parity bit can be ignored. The frame transmission can be stopped immediately after the transmission of the parity bit. The SSI frame is composed as shown in Table 36, with the scaled angular value φ_{sc} and the parity bit.

Bit Position	15 … *SSI_PARPOS*+1	*SSI_PARPOS*	*SSI_PARPOS*-1 … 0
Content	$\varphi_{sc}[15:SSI\_PARPOS+1]$	Parity-Bit	to be ignored

Table 36: MLX90382 SSI frame composition with parity bit

Signal conditioning need to be applied (refer to Section 6.8) to scale the angular value into the desired range $\varphi_{sc}[15:SSI\_PARPOS+1]$. Following constraints must be fulfilled to avoid placing the parity bit into the scaled output data range of φ_{sc}:

In case $SC\_YE \leq max(SC\_Y1, SC\_Y2)$:

$$SSI\_PARPOS[3:0] \leq 15 - ceil(log2(max(SC\_Y1, SC\_Y2)))$$

In case $SC\_YE > max(SC\_Y1, SC\_Y2)$:

$$SSI\_PARPOS[3:0] \leq 15 - ceil(log2(SC\_YE))$$

8.4 PWM output

8.4.1 PWM Definition

The MLX90382 generates pulse width modulation (PWM) signals with a time resolution of $1/f_{ac}$. The interface supports a freely programmable period T_{PWM}, configured via *PWM_PERIOD[15:0]*:

$$T_{PWM} = \frac{PWM\_PERIOD[15:0]}{f_{ac}}$$

The PWM polarity can be inverted using the *PWM_INV* bit.

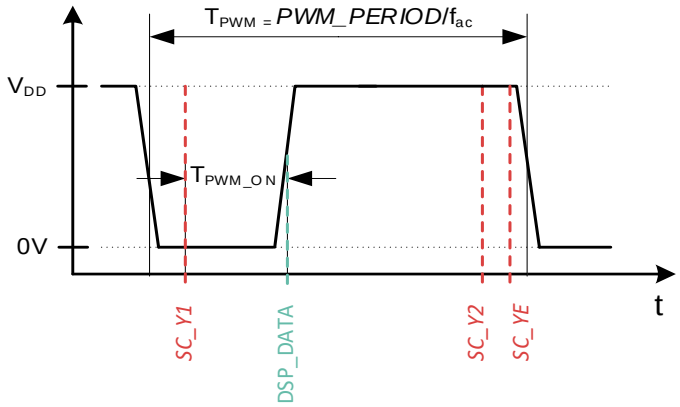


Figure 19: PWM signal definitions with PWM_INV = 0

The PWM duty cycle (T_{PWM_ON}) is proportional to the angular value after signal conditioning and interpolation, which is captured at the beginning of each PWM period. The upper and lower limit of the on-time, T_{PWM_ON},

are defined by the output of the signal conditioning via *SC_Y1[15:0]* and *SC_Y2[15:0]* (see Section 6.8). Figure 19 illustrates a PWM configuration, including the defined on-time. DSP_DATA represents the output data after interpolation (see Section 6.4). *SC_YE[15:0]* refers to the fault band indication that is described in the MLX90382 safety manual [3]. It is important to note that the following constraint must be considered for setting the PWM period by *PWM_PERIOD[15:0]*:

$$PWM\_PERIOD[15:0] > max(SC\_Y1, SC\_Y2, SC\_YE)$$

The PWM Output resolution R_{PWM} depends on the ratio between the application clock frequency and the PWM frequency and can be calculated as follows:

$$R_{PWM} = log2\left(\frac{f_{ac}}{f_{PWM}}\right)$$

To compensate for mismatch between rising and falling edge delays, the signed value *PWM_DC_OFS[8:0]* allows to adjust the T_{PWM_ON} time as follows:

$$\Delta T_{PWM\_ON} = \frac{PWM\_DC\_OFS[8:0]}{f_{ac}}$$

8.4.2 PWM performance characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
PWM Output Resolution	R_{PWM}		12.0	16.0	Bit	
PWM Frequency	f_{PWM}	305		5000	Hz	
PWM Frequency Tolerance	Δf_{PWM}	-5.0		5.0	% f_{PWM}	
PWM Duty Cycle Jitter	J_{DC}			0.03	%	f_{PWM} = 2 kHz; DC = 50%, normalized to the period
PWM Period Jitter	J_{PWM}			500.0	ns	f_{PWM} = 2 kHz

Table 37: PWM performance characteristics

8.5 ABI incremental encoder output

The MLX90382 features an incremental encoder output interface with three signals (see Figure 21). Signals A and B are quadrature signals, where the period represents an angular increment of $4 \cdot \Delta\theta$. The I signal is a reference signal that indicates one complete electrical revolution. In the positive rotation direction, the rising edge of the I-channel marks the zero position, while in the negative direction, the falling edge indicates the zero position.

The direction of rotation is determined by the phase relationship between signals A and B, which corresponds to the sign of the angular velocity. When signal A leads signal B, the angular velocity is considered positive. If signal B leads signal A, the angular velocity is negative.

The ABI interface includes an adjustable hysteresis, which allows to balance noise versus accuracy (See Figure 20). The hysteresis can be configured over a wide range by *ABIUVW_HYS[3:0]*. The direction of rotation can be reversed using the *ABIUVW_DIR* bit setting. It is recommended to set the hysteresis value higher than the expected peak noise. A good estimation is 3 * RMS angular noise. The hysteresis HYS_{ABI_UVW}, expressed in degrees, can be calculated as follows:

$$HYS_{ABI\_UVW}[deg] = \pm floor\left(2^{ABIUVW\_HYS[3:0]-1}\right) \cdot \frac{360}{2^{16}}$$

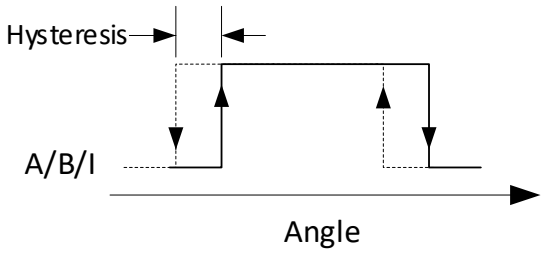


Figure 20: ABI Hysteresis

8.5.1 ABI performance characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Angular Resolution	$\Delta\theta$	0.02			deg	*ABI_LOG2N[3:0]*=12

Table 38: ABI performance characteristics

8.5.2 ABI Configuration of Angular Resolution

The number of counts (N_{ABI_COUNTS}) within one electrical revolution is defined by *ABI_LOG2N[3:0]* and the following equation:

$$N_{ABI\_COUNTS} = 4 \cdot 2^{ABI\_LOG2N[3:0]}$$

The maximum setting for *ABI_LOG2N[3:0]* is 12. The angular output resolution $\Delta\theta$ is defined by:

$$\Delta\theta[deg] = \frac{360}{N_{ABI\_COUNTS}}$$

Be aware that the defined hysteresis HYS_{ABI_UVW} will limit the angular resolution. Therefore, the constraint for the hysteresis setting is as follows:

$$ABIUVW\_HYS[3:0] \leq (13 - ABI\_LOG2N[3:0])$$

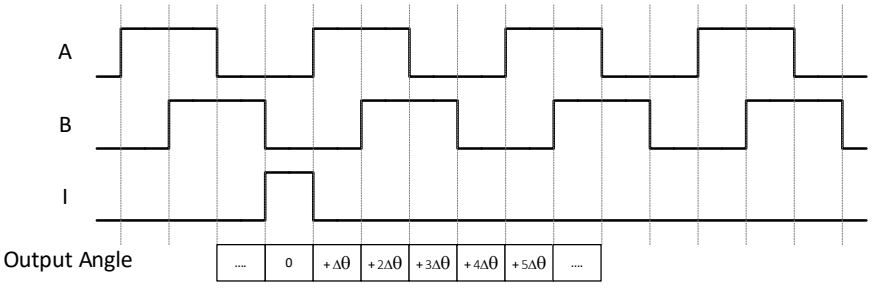


Figure 21: ABI signal definition

8.5.3 ABI I-Pulse duration configuration

In presence of high noise, the internal angle can step over the index pulse (I-pulse) trigger range. To make the I-pulse generation more robust, the duration and the starting point of the I-Pulse can be adjusted by *ABI_I_LEN[0]*. With *ABI_I_LEN* = 1, the I-pulse is a three-count index that starts with the last count on the previous turn plus two counts on the new turn. With *ABI_I_LEN* = 0, the I-pulse is a single count index starting on the wrap. The resulting effect is illustrated in Figure 22.

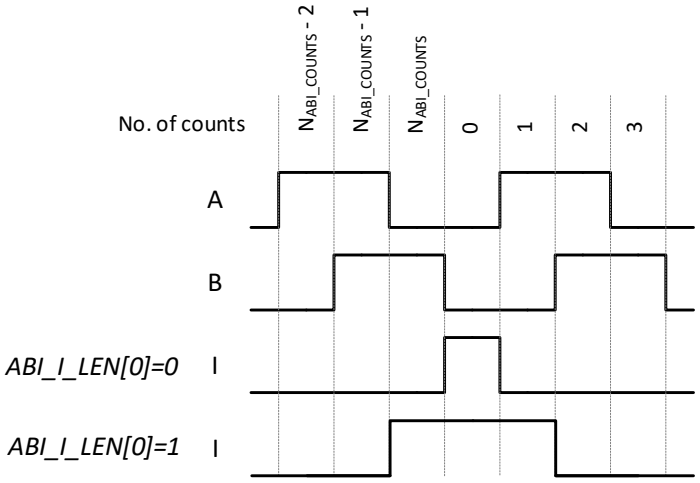


Figure 22: ABI I-pulse duration configuration

8.5.4 ABI Constraints on Configuration

The configuration of *ABI_LOG2N[3:0]* and *ABIUVW_HYS[3:0]* is constraint by the maximum angular speed (v_{el}). To ensure valid encoding of the ABI signals relative to angular speed, the following constraint must be considered:

$$max(v_{el}[Hz]) < (2^{14-ABI_{LOG2N}-ABIUVW_{HYS}-1}) \cdot \frac{f_{ac}}{2^{16}}$$

8.6 UVW commutation output

The MLX90382 UVW interface emulates the U, V and W signals typically generated by three Hall switches in Brushless DC (BLDC) motors. These three signals are electrically phase-shifted by 120 degrees and switch at the position where the mechanical angle indicates a pole change in the motor. The number of pole pairs N_{pp} can be set from 1 to 32 pairs through N_{pp} = *UVW_PP[4:0]* + 1.

Additionally, the MLX90382 includes a dedicated hysteresis setting, configurable via *ABIUVW_HYS[3:0].* It prevents incorrect transitions. This setting is adjustable over a wide range to optimize the balance between noise and accuracy. The calculation of the hysteresis HYS_{ABI_UVW} is detailed in Section 8.5.

The direction of rotation can be reversed by setting bit *ABIUVW_DIR.* Figure 23 shows and example of UVW signals with N_{pp} = 3, along with the corresponding mechanical angle θ.

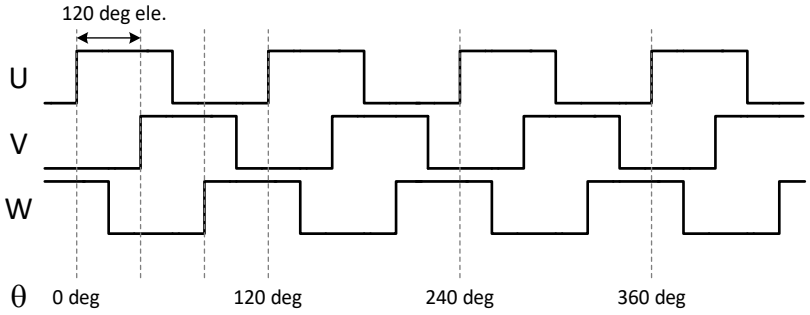


Figure 23: UVW signal definition with 3 pole pairs

8.6.1 UVW performance characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Number of pole pairs	N_{pp}	1		32		

Table 39: UVW performance characteristics

8.7 Differential ABI and UVW output (QFN-24)

The QFN-24 package provides a differential ABI and UVW interface output, meaning the ABI/UVW signals are logical inverted, with signal levels ranging between VSS and VDD. By configuring *ABI_DIFF[0]* to 1, the inverted signals A/U_N, B/V_N and I/W_N are provided at the AU_N, SCLK and MOSI pins, respectively (see Table 29).

9 Application information

This section provides a non-exhaustive list of application examples for the QFN-24, and TSSOP-16/ TSSOP-16_EP packages. For simplicity, Supply configurations are described once per package type, and the recommended values for pull-up/ pull-down resistors, as well as termination resistors are mentioned in the tables below.

Component	Min.	Typ.	Max.	Unit	Comment
R_{PU}/ R_{PD}	5			kΩ	Push-pull mode. Applicable for all outputs.
R_{PU}/ R_{PD}	1			kΩ	Open drain mode in 5 V mode derived at 90% VDD and 10% VDD
	2			kΩ	Open drain mode in 3.3 V mode derived at 90% VDD and 10% VDD

Table 40: Recommended component values pull-up/ pull-down resistors

Component	Min.	Typ.	Max.	Unit	Comment
R_{TR}	660			Ω	In 5V supply mode
	560			Ω	In 3.3V supply mode

Table 41: Recommended component values for termination resistors for differential ABI/ UVW interface

9.1 Example application diagrams with MLX90382 in QFN-24 package

9.1.1 Supply configurations for QFN-24 devices

Figure 24 shows the connection diagram for a QFN-24 device in 5V supply mode, while Figure 25 depicts 3.3 V supply mode. Please note that these supply modes can be applied to any of the following application diagrams with QFN-24 devices. Values for the capacitors are listed in Table 42.

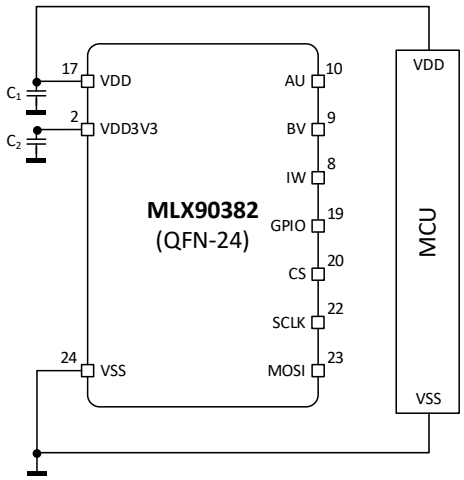


Figure 24 : Example depicting 5 V supply mode

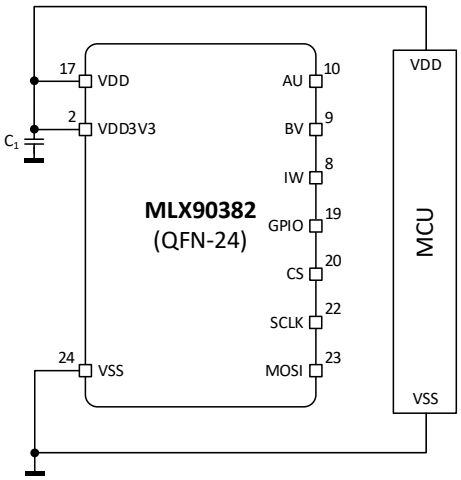


Figure 25 : Example depicting 3.3 V supply mode

Component	Min.	Typ.	Max.	Unit	Comment
C_1		330		nF	Close to the IC pin
C_2		100		nF	Close to the IC pin, $C_2 \leq C_1$

Table 42: Recommended component values for QFN-24 with 5 V and 3.3 V configuration

9.1.2 SPI interface with MLX90382 in QFN-24 package

Figure 26 shows the application diagram for the QFN-24 device, connected via SPI to the MCU. The pull-up/ pull-down resistors R_{PU}/ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40).
This configuration can be used for both operating and programming the device.

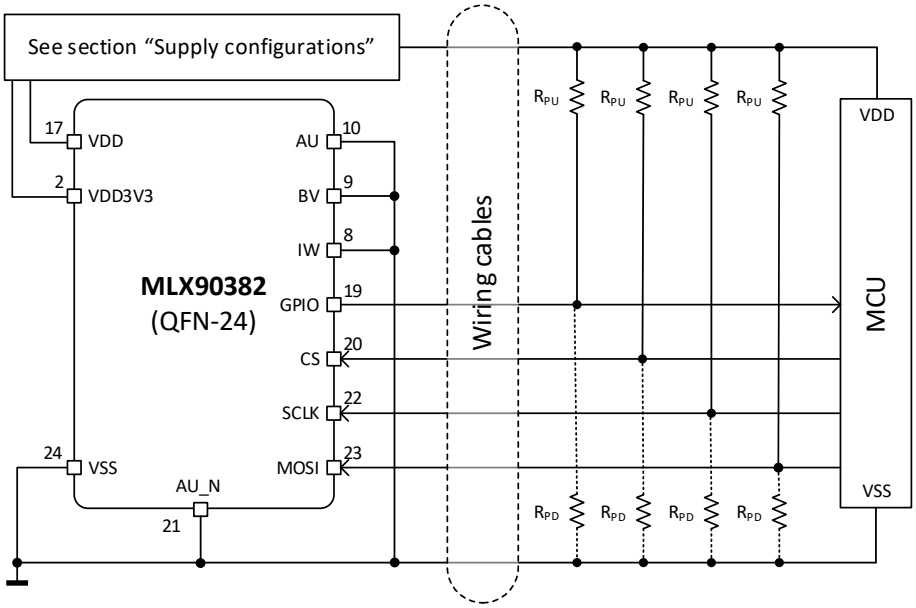


Figure 26: Example application diagram for SPI interface

9.1.3 SSI interface with MLX90382 in QFN-24 Package

Figure 27 shows the application diagram for the QFN-24 device, connected via SSI to the MCU. The pull-up/ pull-down resistors R_{PU}/ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40).
In order to support programming of the device, SPI interface shall be connected as shown in chapter 9.1.2.

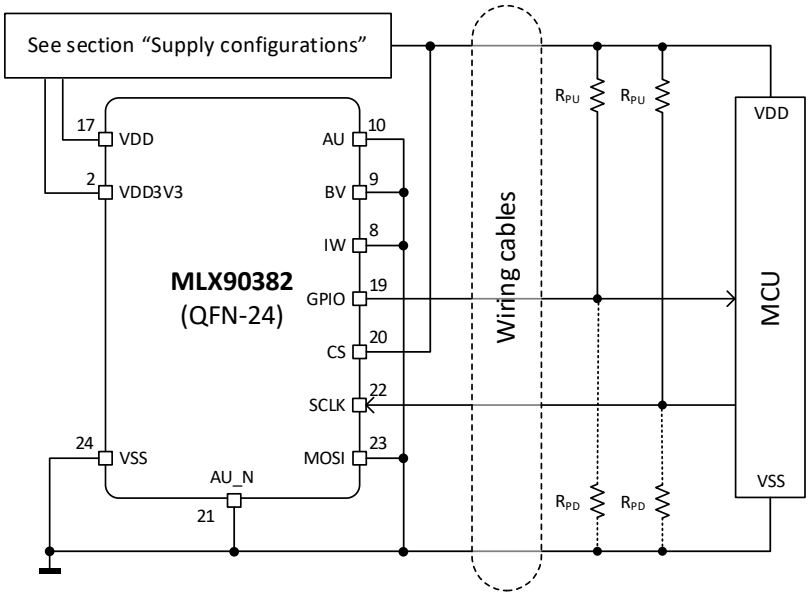


Figure 27: Example application diagram for SSI interface

9.1.4 PWM interface with MLX90382 in QFN-24 Package

Figure 28 shows the application diagram for the QFN-24 device, connected via PWM to the MCU. The pull-up/ pull-down resistors $R_{PU/}$ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40).
In order to support programming of the device, SPI interface shall be connected as shown in chapter 9.1.2.

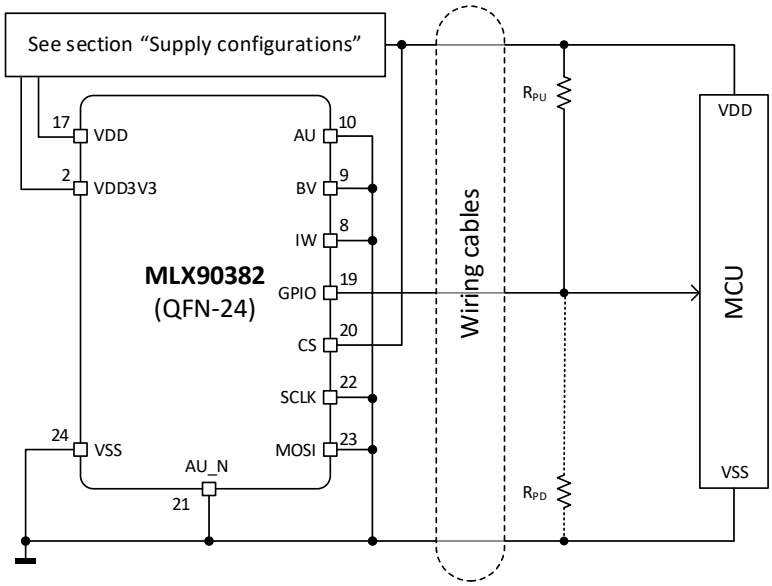


Figure 28: Example application diagram for PWM interface

9.1.5 ABI/UVW interface with MLX90382 in QFN-24 Package

Figure 29 shows the application diagram for the QFN-24 device, connected via ABI/UVW to the MCU. The pull-up/ pull-down resistors $R_{PU/}$ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40).
In order to support programming of the device, SPI interface shall be connected as shown in chapter 9.1.2.

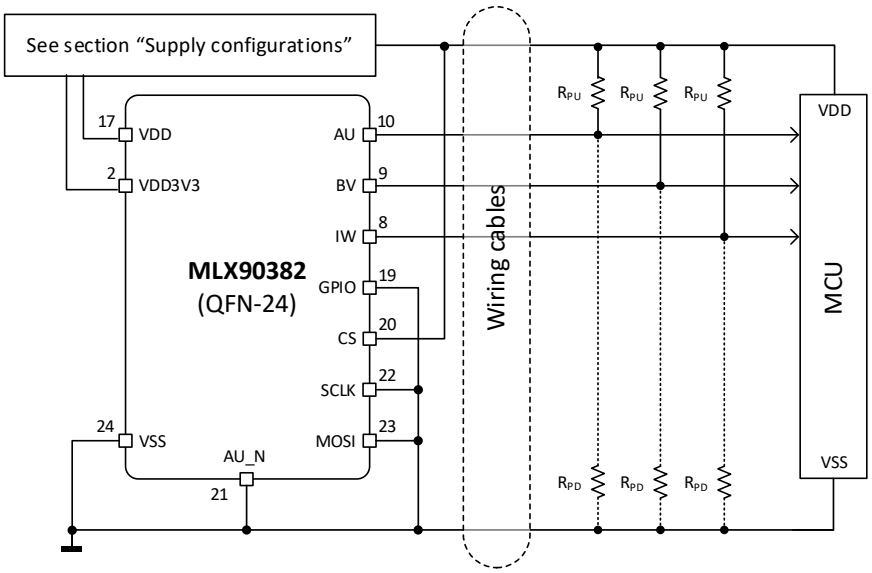


Figure 29: Example application diagram for ABI/ UVW interface.

9.1.6 Differential ABI/ UVW interface with MLX90382 in QFN-24 Package

Figure 30 shows the application diagram for the QFN-24 device, connected via differential ABI/ UVW to the MCU. The termination resistors R_{TR} are specified differently for the 3.3 V and 5 V supply modes (see Table 41).

In order to support programming of the device, SPI interface shall be connected as shown in chapter 9.1.2.

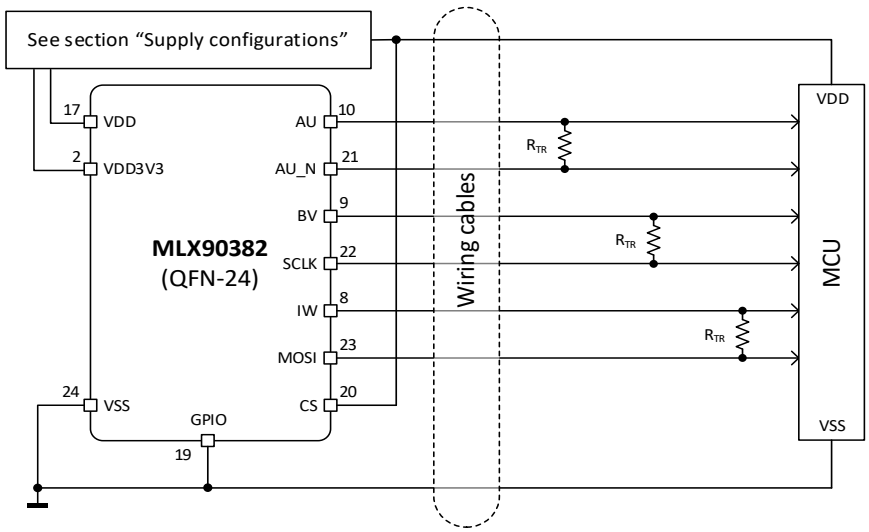


Figure 30: Example application diagram for differential ABI/ UVW interface

9.2 Example application diagrams with MLX90382 in TSSOP-16/TSSOP-16_EP package

9.2.1 Supply configurations for TSSOP-16/ TSSOP-16_EP devices

Figure 31 shows the connection diagram for a TSSOP-16/ TSSOP-16_EP device in 5 V supply mode, while Figure 32 depicts 3.3 V supply mode. Do note that these supply modes can be applied to any of the following application diagrams with TSSOP-16/ TSSOP-16_EP device devices. Values for the capacitors are mentioned inTable 43.

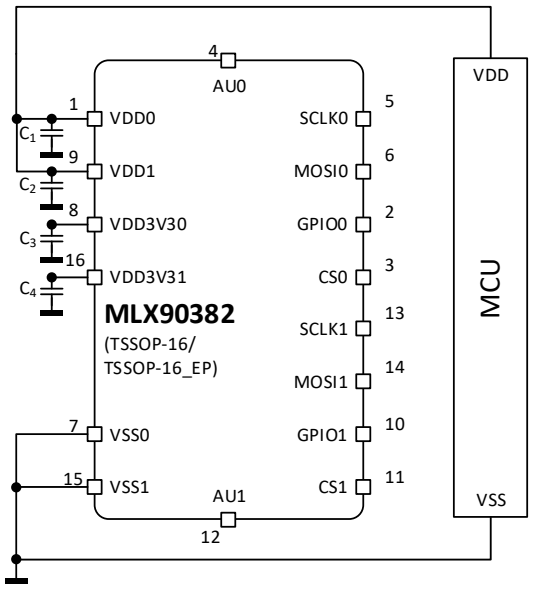


Figure 31 : Example depicting 5 V supply mode for TSSOP-16/ TSSOP-16_EP devices

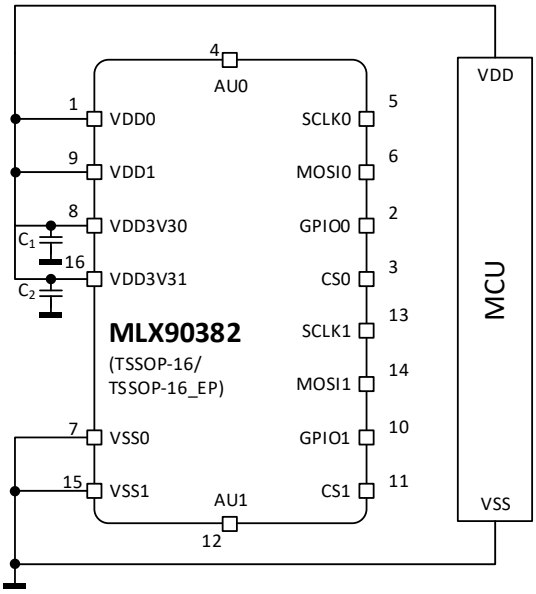


Figure 32 : Example depicting 3.3 V supply mode for TSSOP-16/ TSSOP-16_EP devices

Component	Min.	Typ.	Max.	Unit	Comment
C_1, C_2		330		nF	Close to the IC pin
C_3, C_4		100		nF	Close to the IC pin, C_3, $C_4 \leq C_1$, C_2

Table 43: Recommended component values for TSSOP-16/ TSSOP-16_EP with 5 V and 3.3 V configuration

9.2.2 SPI interface with MLX90382 in TSSOP-16/ TSSOP-16_EP package

Figure 33 shows the application diagram for the TSSOP-16/ TSSOP-16_EP device, connected via SPI to the MCU. The pull-up/ pull-down resistors R_{PU}/ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40).

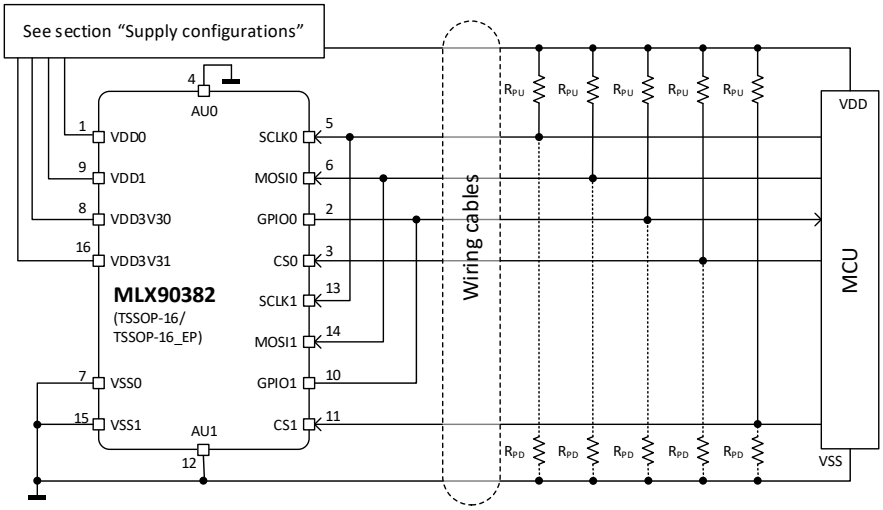


Figure 33: Example application diagram for SPI interface.

9.2.3 SSI interface with MLX90382 in TSSOP-16/ TSSOP-16_EP package

Figure 34 shows the application diagram for the TSSOP-16/ TSSOP-16_EP device, connected via SSI to the MCU. The pull-up/ pull-down resistors R_{PU}/ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40).

In order to support programming of the device, SPI interface shall be connected as shown in chapter 9.2.2 .

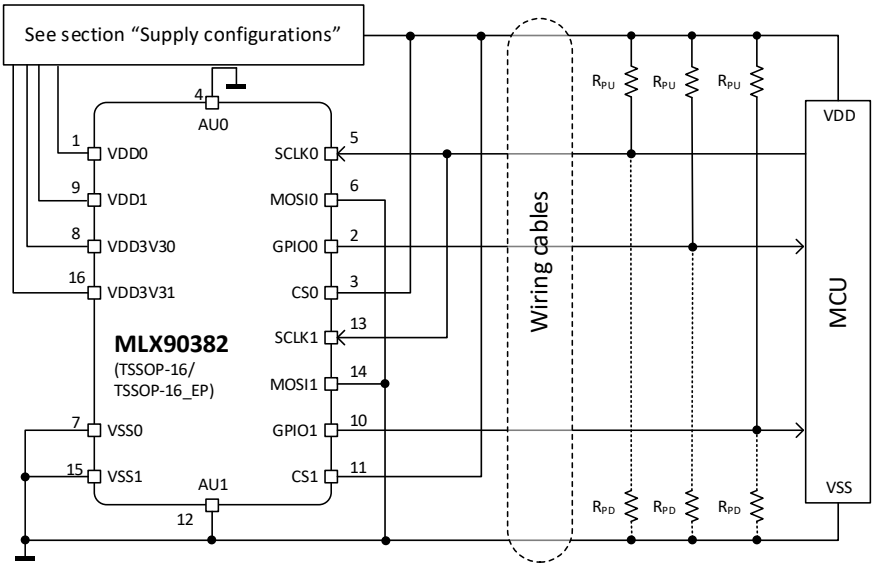


Figure 34: Example application diagram for SSI interface

9.2.4 PWM interface with MLX90382 in TSSOP-16/ TSSOP-16_EP package

Figure 35 shows the application diagram for the TSSOP-16/ TSSOP-16_EP device, connected via PWM to the MCU. The pull-up/ pull-down resistors $R_{PU/}$ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40). In order to support programming of the device, SPI interface shall be connected as shown in chapter 9.2.2 .

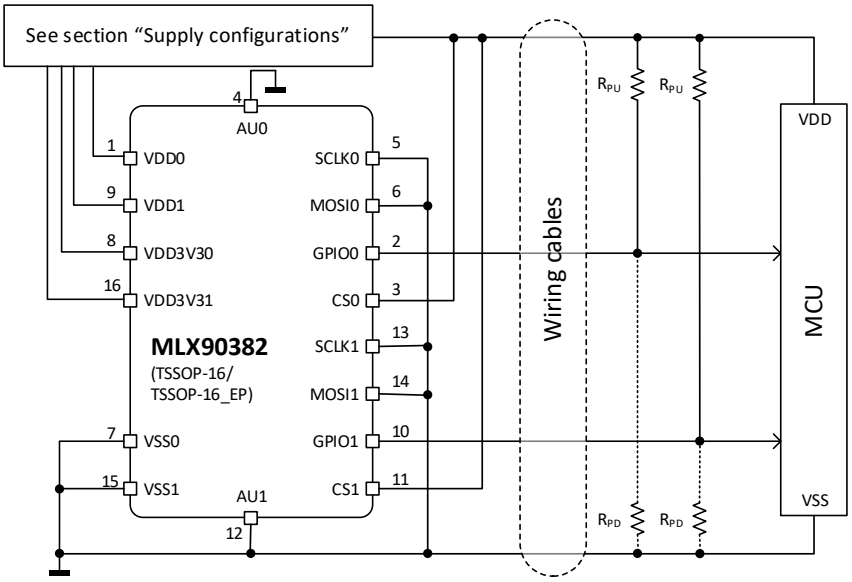


Figure 35: Example application diagram for PWM interface

9.2.5 ABI/UVW interface with MLX90382 in TSSOP-16/ TSSOP-16_EP package

Figure 36 shows the application diagram for the TSSOP-16/ TSSOP-16_EP device, connected via ABI/UVW to the MCU. The pull-up/ pull-down resistors $R_{PU/}$ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40).

In order to support programming of the device, SPI interface shall be connected as shown in chapter 9.2.2 .

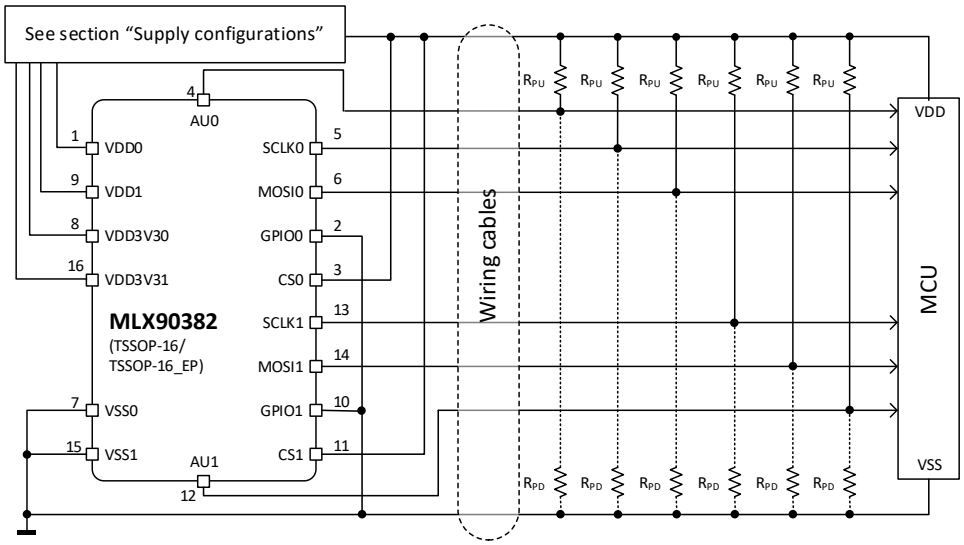


Figure 36: Example application diagram for ABI/ UVW interface

9.3 Example application diagram for concurrent interfaces

It is possible to use some interfaces concurrently (combined), Figure 37 shows an example application diagram for concurrent usage of SPI and ABI interface. An overview of the supported concurrent interface combinations and their configuration is given in Table 29 and Table 30. The pull-up/ pull-down resistors $R_{PU/}$ R_{PD} are specified differently for the 3.3 V and 5 V supply modes (see Table 40).

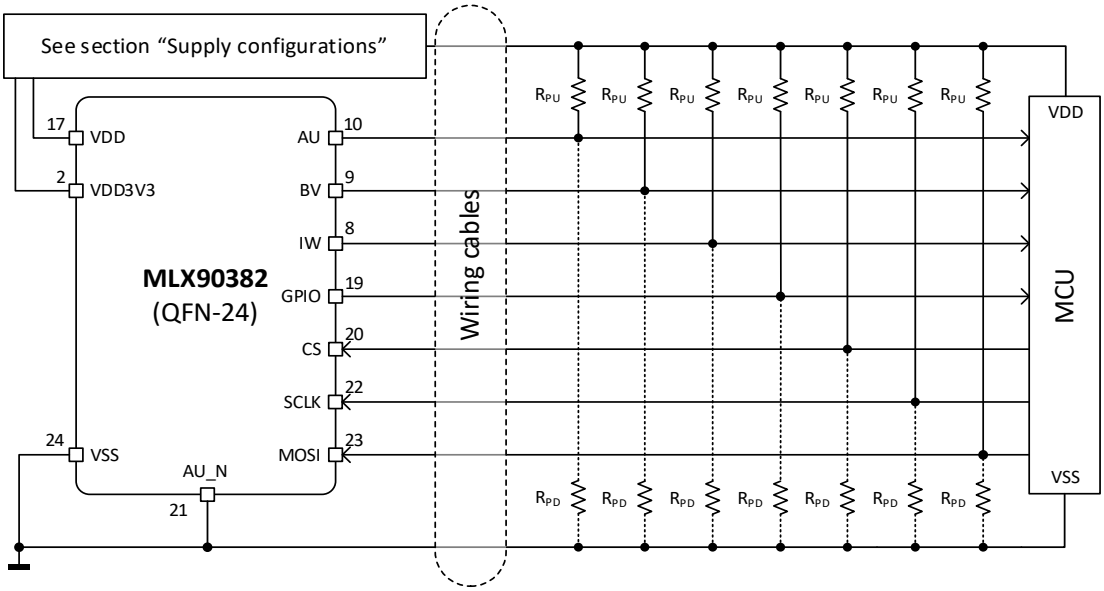


Figure 37: Example application diagram for concurrent usage of SPI and ABI with a QFN-24 package

9.4 Magnetic Sensing modes

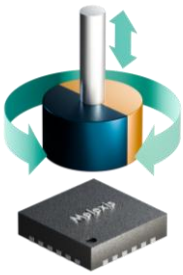
From an application perspective, the different sensing modes correspond to the measurement of the angular position of the magnet as projected within one of the three planes of the spatial reference frame, as illustrated in Figure 38. These modes can be configured with the setting in *SENSING_MODE[2:0].* The *SENSING_MODE[2:0]* parameter is only available for Rotary Mode for mid- and high-field magnetic range not for the 360-degree Stray Field Immune Rotary Mode.

Figure 38: Spatial reference frame of the packages. Left: QFN-24. Right: TSSOP-16 and TSSOP-16_EP

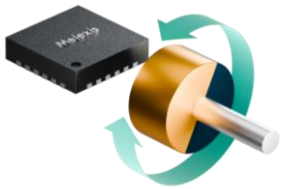
9.4.1 Application scenario end of shaft

A diametral magnetisation is assumed for the illustration of the following application modes. The position of the magnet is assumed to be centred to the shaft-axis to achieve the optimal angular accuracy.

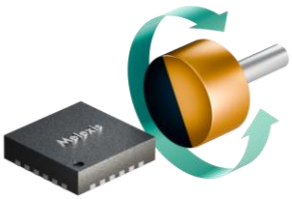
9.4.1.1 End of shaft (QFN-24)



X-Y mode
BAA-000, -100 and -600



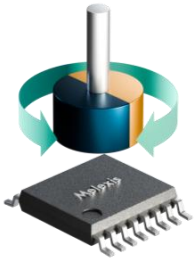
X-Z mode
BAA-000 and -100



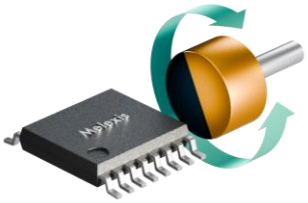
Y-Z mode
BAA-000 and -100

Figure 39: Exemplary illustration for end of shaft applications (QFN-24)

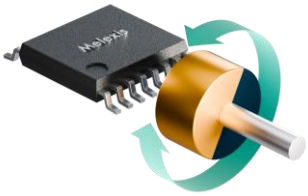
9.4.1.2 End of shaft (TSSOP-16_EP)



X-Y mode
BAA-000 and -100



X-Z mode
BAA-000 and -100

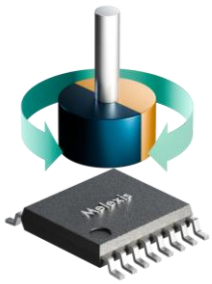


Y-Z mode
BAA-000 and -100

Figure 40: Exemplary illustration for end of shaft application modes (TSSOP-16_EP)

9.4.1.3 End of shaft (TSSOP-16)

The TSSOP-16 package variant supports only the X-Y magnetic sensing mode for Stray Field Immune measurement.



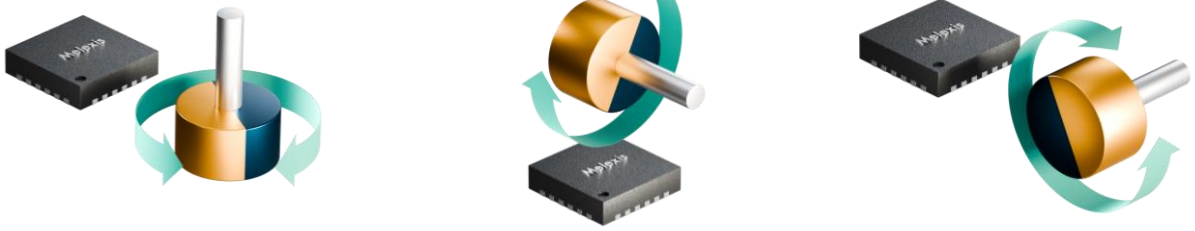
X-Y Mode
BAA-602

Figure 41: Exemplary illustration for end of shaft application modes (TSSOP-16)

9.4.2 Side/through shaft

9.4.2.1 Side/through shaft (QFN-24)

The position of the magnet can vary within the depicted plane.



X-Y Mode
BAA-000 and -100

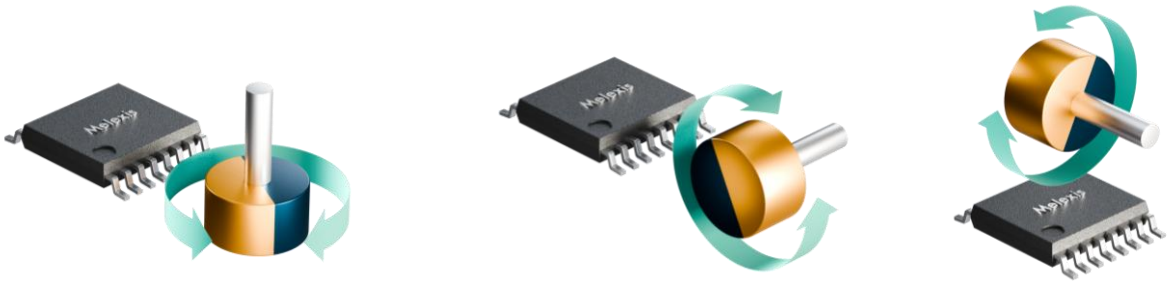
X-Z Mode
BAA-000 and -100

Y-Z Mode
BAA-000 and -100

Figure 42: Exemplary illustration for side/through shaft application modes (QFN-24)

9.4.2.2 Side/through shaft (TSSOP-16_EP)

The position of the magnet can vary within the depicted plane.



X-Y Mode
BAA-000 and -100

X-Z Mode
BAA-000 and -100

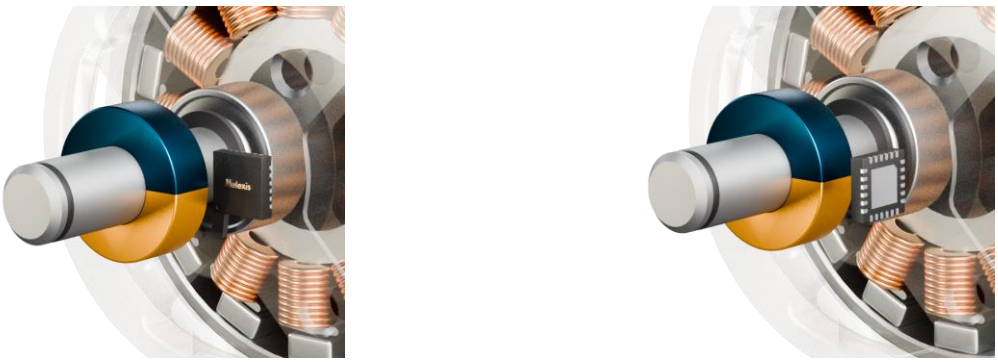
Y-Z Mode
BAA-000 and -100

Figure 43: Exemplary illustration for side/through shaft application modes (TSSOP-16_EP)

9.4.3 Through shaft magnet ring

9.4.3.1 Through shaft magnet ring (QFN-24), dual-pole magnet

The illustration of the following application modes depicts a single pole pare magnet and a QFN-24 device.



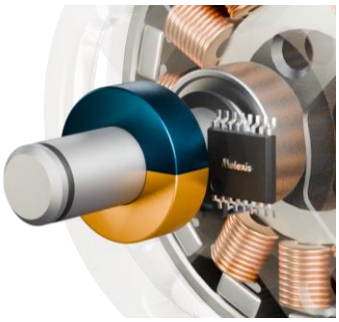
X-Z Mode
BAA-000 and -100

Y-Z Mode
BAA-000 and -100

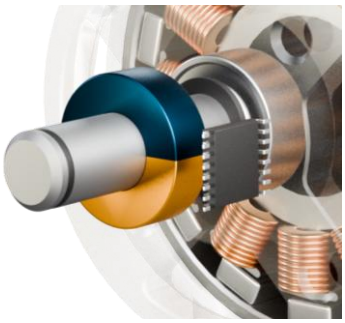
Figure 44: Exemplary application for through shaft magnet ring (QFN-14), dual-pole magnet

9.4.3.2 Through shaft magnet ring (TSSOP-16_EP), dual-pole magnet

The illustration of the following application modes depicts a single pole pair magnet and a TSSOP-16_EP device.



X-Z Mode
BAA-000 and -100



Y-Z Mode
BAA-000 and -100

Figure 45: Exemplary illustration for through shaft magnet ring (TSSOP-16_EP), dual-pole magnet

9.4.3.3 Through shaft magnet ring (QFN-24), multipole magnet

The illustration of the following application modes depicts a six-pole pair magnet and a QFN-24 device, but is also valid for other multipole pair magnets.

X-Z Mode
BAA-000 and -100

Y-Z Mode
BAA-000 and -100

Figure 46: Exemplary application for through shaft magnet ring (QFN-14), six-pole magnet

9.4.3.4 Through shaft magnet ring ((TSSOP-16_EP), multipole magnet

The illustration of the following application modes depicts a six-pole pair magnet and a TSSOP-16_EP device, but is also valid for other multipole pair magnets.

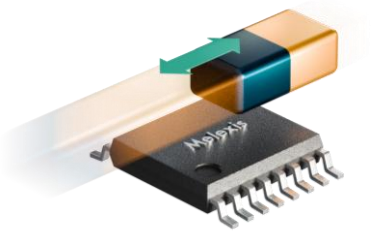
X-Z Mode
BAA-000 and -100

Y-Z Mode
BAA-000 and -100

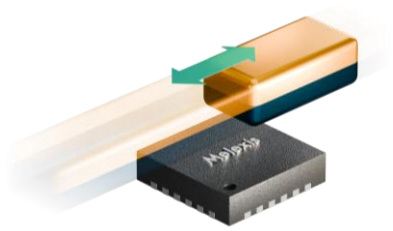
Figure 47: Exemplary illustration for through shaft magnet ring (TSSOP-16_EP), six-pole magnet

9.4.4 Linear magnet motion

The illustration of the following application modes depicts a single pole pair magnet, but is also valid for a multipole pair magnet.



Y-Z Mode
BAA-000 and -100



X-Z Mode
BAA-000 and -100

Figure 48: Exemplary illustration for linear application modes

10 Package, IC handling and assembly

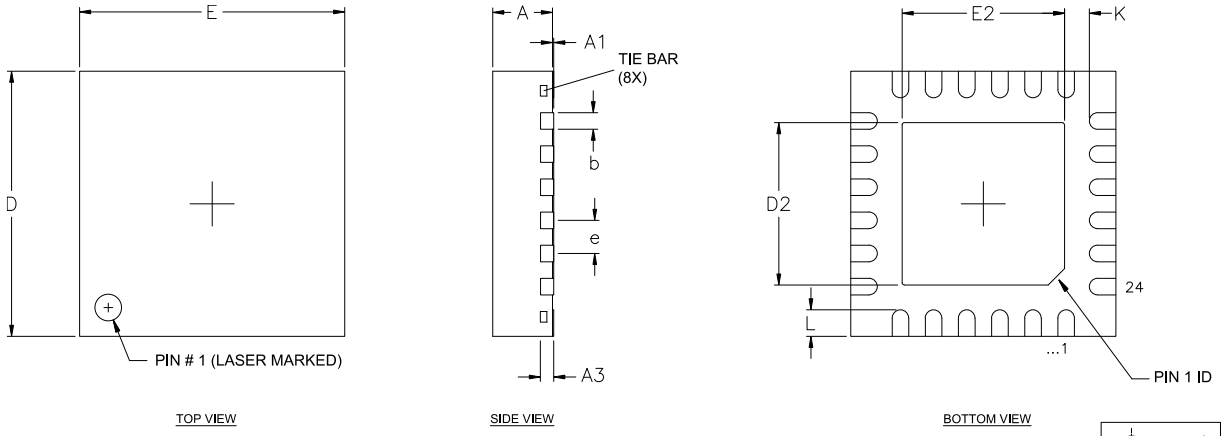
10.1 Package information

Variant Code Marking	Definition (Option Code)
M	Rotary Mode mid-field (-000)
H	Rotary Mode high-field (-100)
N	Stray Field Immune Rotary Mode (-60x)

Table 44: Definition of the device variant marking on the package

10.1.1 Package QFN-24 4x4

10.1.1.1 Package QFN-24 dimensions



NOTE :
1. EXPOSED TIE BAR SHOULD BE KEPT FREE FROM SOLDER.
2. (OPTIONAL) SIDE WALL IMMERSION TIN PLATING MIN 1um THICK.

SYMBOL	ALL DIMENSION ARE IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.35	2.45	2.55
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
K	0.20	---	---
b	0.18	0.25	0.30
e		0.50 BSC	

Figure 49: Package QFN-24 dimensions

10.1.1.2 Package QFN-24 pinout and marking

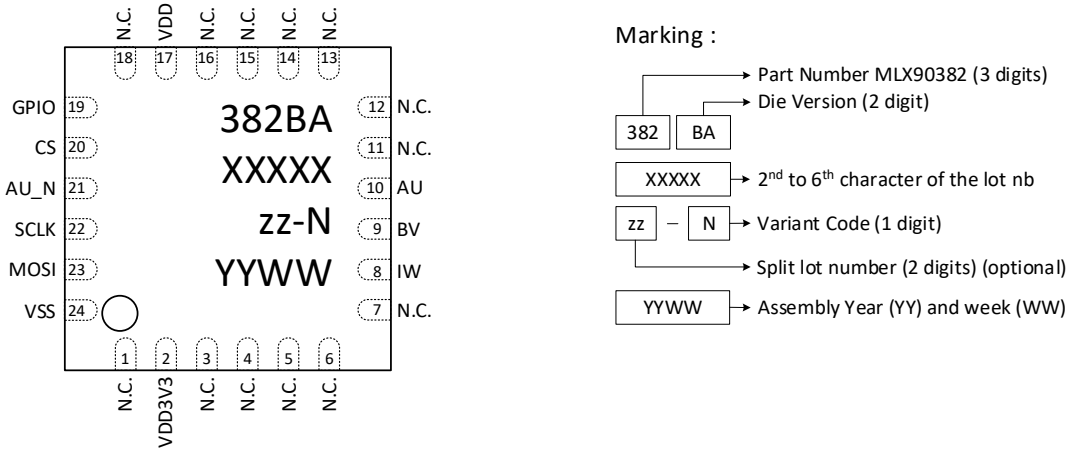


Figure 50: Package QFN-24 pinout and marking

10.1.1.3 Package QFN-24 magnetic sweet-spot

The location of the hall plates used for the Stray Field Immune rotary mode are market as green rectangles.

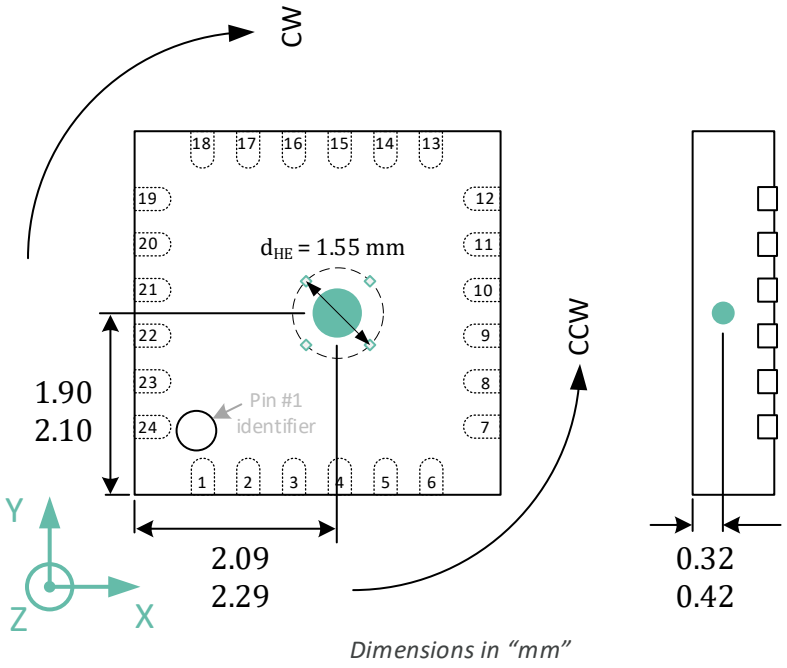
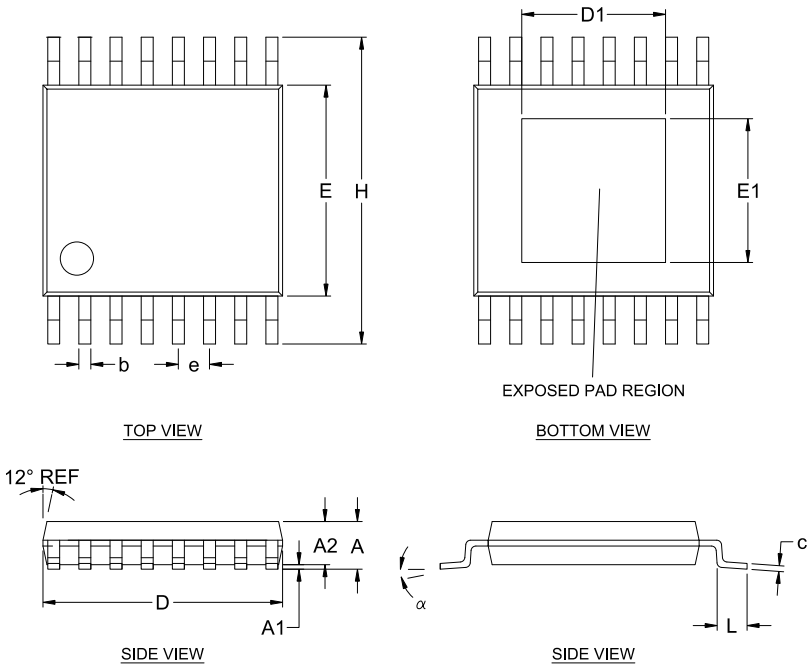


Figure 51: Package QFN-24 magnetic sweet-spot

10.1.2 Package TSSOP-16_EP

10.1.2.1 Package TSSOP-16_EP dimensions



SYMBOL	MINIMUM	MAXIMUM
A	---	1.10
A1	0.05	0.15
A2	0.85	0.95
D	4.90	5.10
E	4.30	4.50
D1	2.90	3.10
E1	2.90	3.10
H	6.40 REF	
L	0.50	0.75
b	0.19	0.30
c	0.09	0.20
e	0.65 BSC	
α	0°	8°

NOTE :
1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTERLEADS FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.08 mm.
5. LEAD COPLANARITY SHALL BE MAXIMUM 0.1 mm.

Figure 52: Package TSSOP-16_EP dimensions

10.1.2.2 Package TSSOP-16_EP pinout and marking

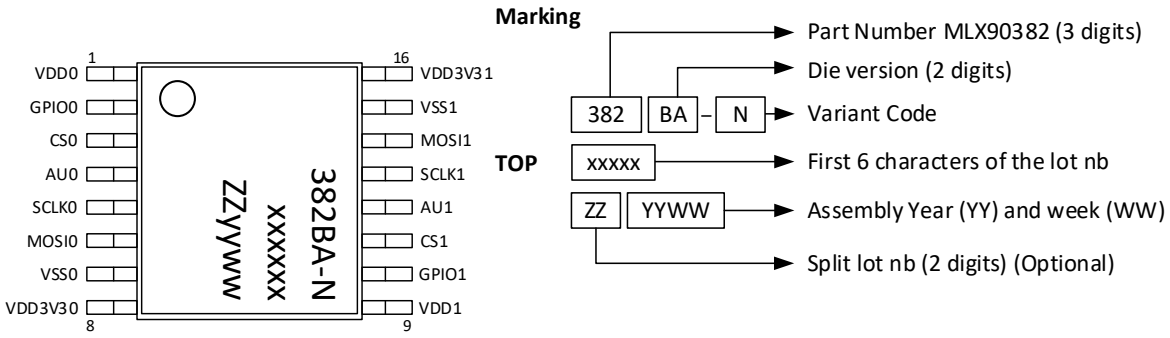
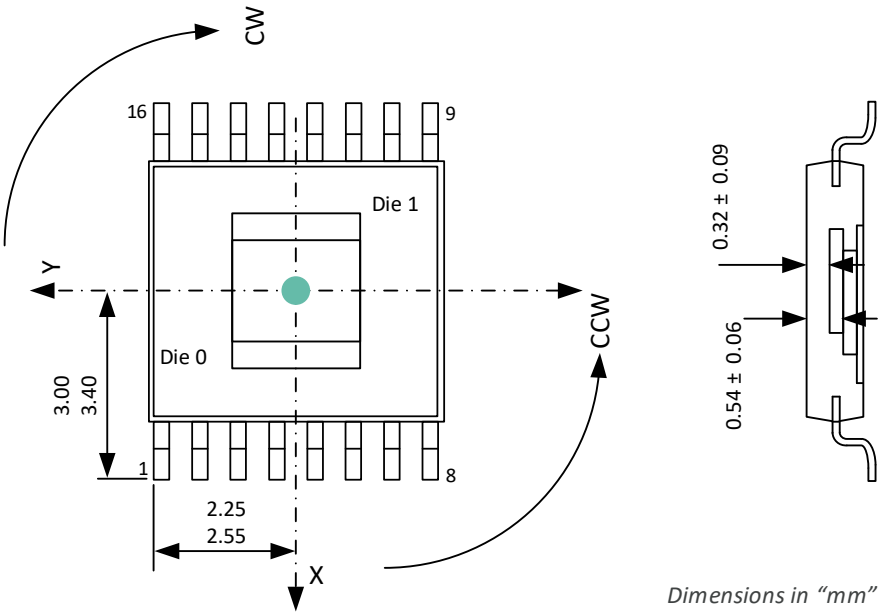


Figure 53: Package TSSOP-16_EP pinout and marking

10.1.2.3 Package TSSOP-16_EP magnetic sweet spot

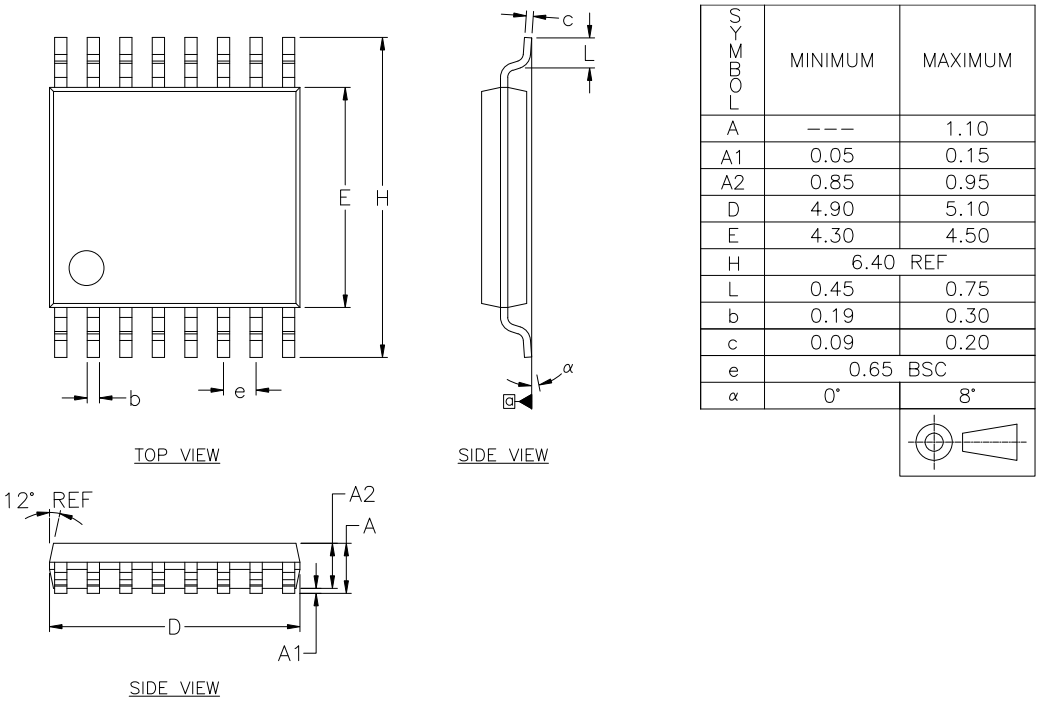


Dimensions in "mm"

Figure 54: Package TSSOP-16_EP magnetic sweet spot

10.1.3 Package TSSOP-16

10.1.3.1 Package TSSOP-16 dimensions



SYMBOL	MINIMUM	MAXIMUM
A	---	1.10
A1	0.05	0.15
A2	0.85	0.95
D	4.90	5.10
E	4.30	4.50
H	6.40 REF	
L	0.45	0.75
b	0.19	0.30
c	0.09	0.20
e	0.65 BSC	
α	0°	8°

NOTE :
1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTERLEADS FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.08 mm.
5. LEAD TO LEAD COPLANARITY MAX 0.100 MILLIMETERS (mm) WITH RESPECT TO SEATING PLANE a.

Figure 55: Package TSSOP-16 dimensions

10.1.3.2 Package TSSOP-16 pinout and marking

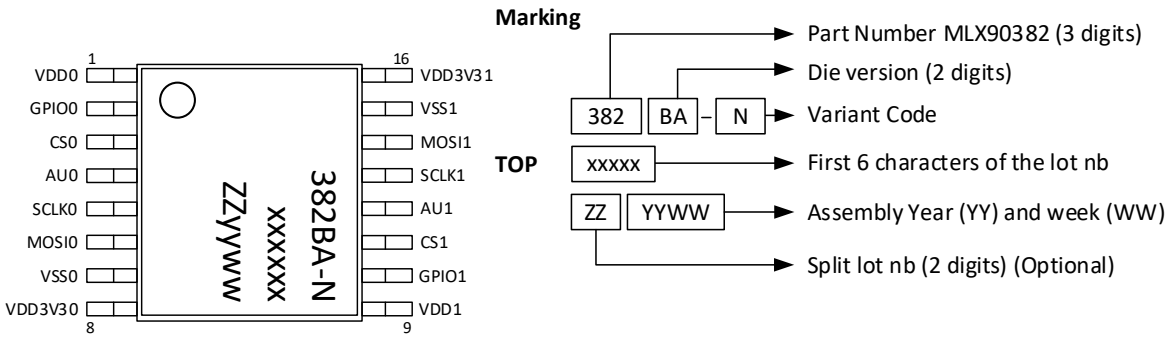


Figure 56: Package TSSOP-16 pinout and marking

10.1.3.3 Package TSSOP-16 magnetic sweet spot

The location of the hall plates used for the Stray Field Immune rotary mode are market as green rectangles.

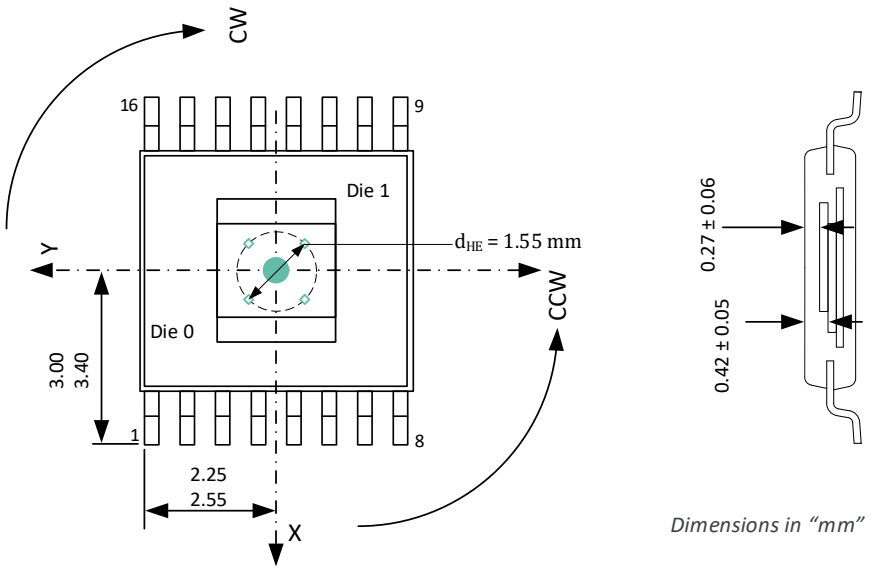


Figure 57: Package TSSOP-16 magnetic sweet spot

10.2 Package thermal performance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Thermal resistance - junction to ambient	R_{thja}		28		K/W	QFN-24 package with soldered exposed pad
			76		K/W	QFN-24 package with non-soldered exposed pad
			102		K/W	TSSOP-16 package
			55		K/W	TSSOP-16_EP package with soldered exposed pad
			107		K/W	TSSOP-16_EP package with non-soldered exposed pad
Thermal resistance - junction to case	R_{thjc}		2		K/W	QFN-24 package
			27		K/W	TSSOP-16 package
			31		K/W	TSSOP-16_EP package

Table 45: Thermal resistance specification (based on simulation)

10.3 Storage and handling of plastic encapsulated ICs

Plastic encapsulated ICs shall be stored and handled according to their MSL categorization level (specified in the packing label) as per J-STD-033 [9]. Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). The component assembly shall be handled in EPA (Electrostatic Protected Area) as per ANSI S20.20 [10].
For more information refer to Melexis *Guidelines for storage and handling of plastic encapsulated ICs* [1]

[1] https://www.melexis.com/en/tech-info/ic-handling-and-assembly

10.4 Assembly of encapsulated ICs

For Surface Mounted Devices (SMD, as defined according to JEDEC norms), the only applicable soldering method is reflow.

For Through Hole Devices (THD), the applicable soldering methods are reflow, wave, selective wave and robot point-to-point. THD lead pre-forming (cutting and/or bending) is applicable under strict compliance with Melexis *Guidelines for lead forming of SIP Hall Sensors* [(1)].

Melexis products soldering on PCB should be conducted according to the requirements of IPC/JEDEC and J-STD-001 [9]. Solder quality acceptance should follow the requirements of IPC-A-610 [11].

For PCB-less assembly refer to the relevant application notes [(1)] or contact Melexis.

Electrical resistance welding or laser welding can be applied to Melexis products in THD and specific PCB-less packages following the *Guidelines for welding of PCB-less devices*[(1)].

Environmental protection of customer assembly with Melexis products for harsh media application, is applicable by means of coating, potting or overmolding considering restrictions listed in the relevant application notes [(1)]

For other specific process, contact Melexis via www.melexis.com/technical-inquiry

10.5 Environment and sustainability

Melexis is contributing to global environmental conservation by promoting non-hazardous solutions. For more information on our environmental policy and declarations (RoHS, REACH…) visit www.melexis.com/environmental-forms-and-declarations

11 User programmable items

The MLX90382 provides programming capability via SPI interface. It is designed and factory-programmed to require a minimal configuration setup. Both reading and writing operations of registers are supported. When configuring the registers, any unused (Not used) bits must be set to "0", otherwise the NVRAM shadow register monitor causes triggering a fail-safe state (see MLX90382 Safety Manuals).

Values of reserved bits shall not be changed.

11.1 MLX90382 address space

The MLX90382 address space is organized in read/writeable volatile DSP register and NVRAM register.

Address - Range		Description
0x000	0x110	R/W volatile DSP register
0x200	0x25E	Customer R/W NVRAM register

Table 46: MLX90382 address space organization

11.2 DSP register

Register	Address	Bit	R/W	Default	Description
NVOP_KEY	0x010	[3:0]	R/W	0	8 bits KEY to unlock non-volatile operation.
Not used		[15:4]	R	0	
IN _APPLICATION	0x024	[1:0]	R/W	2	2: Application mode off, else: application running
DE_NVM_CRC		2	R/W	0	1: Disable NVRAM CRC calculation
Not used		[15:3]	R	0	
CRC	0x026	[15:0]	R	0	NVRAM CRC calculation result
CRC_CALC_STRT	0x028	0	W	N/A	Start NVRAM checksum computation
CRC_CALC_DONE		1	R	0	If 1, NVRAM checksum computation finished, CRC updated in 0x026
Reserved		2	R/W	0	Reserved, don't change
Not used		[15:3]	R	0	
STATE	0x02C	[7:0]	R	8	0x08: Norm state 0x10: Safe-State SS2 (NVRAM failure) 0x20: Safe-State SS2 0x40: Safe-State SS3
Not used		[15:8]	R	0	
AGC_GAIN	0x034	[5:0]	R	23	Read current AGC gain setting
Reserved		6	R	0	Reserved, don't change
Not used		[15:7]	R	0	
AGC_AMP	0x036	[12:0]	R	0	AGC measured amplitude (used for AGC and AGC monitoring)
Not used		[15:13]	R	0	
TEMP	0x038	[11:0]	R	0	Temperature range [200.125:0.125:711] [K]
Not used		[15:12]	R	0	
LIN_PHASE	0x03A	[15:0]	R	0	Angular value after linearization, resolution $360/2^{16}$ deg; Before delay compensation
SPEED	0x03C	[15:0]	R	0	v[Hz] = signed(SPEED) / 2^{22} * f_{ac}/26; v[rpm] = v[Hz] * 60; range ±6009,43

Register	Address	Bit	R/W	Default	Description
DRIFTC_PHASE	0x042	[15:0]	R	0	Angular value after delay compensation and zero-point offset correction, resolution $360/2^{16}$ deg
SC_PHASE	0x044	[15:0]	R	0	Angular value after signal conditioning
GC_I	0x048	[15:0]	R	0	Gain-compensated I component (Averaging result)
GC_Q	0x04E	[15:0]	R	0	Gain-compensated Q component (Averaging result)
RMM_ASIQ	0x062	[15:0]	R	SC_IQ	Adaptive orthogonality correction value AS_IQ
RMM_ASQQ	0x064	[15:0]	R	SC_QQ	Adaptive sensitivity correction value AS_SQ
PWM_PCNT	0x10A	[15:0]	R	0	PWM period counter (PWM_PCNT_ON = 1)

Table 47: DSP register

11.3 NVRAM register

11.3.1 Magnetic sensing mode configuration

Register	Address	Bit	R/W	Default	Description
SENSING_MODE	0x200	[2:0]	R/W	0	Magnetic sensing modes: 0: X-Y (default) 1: X-Z 2: Y-Z

Table 48: Magnetic sensing mode configuration register

11.3.2 Interface configuration

Register	Address	Bit	R/W	Default	Description
GPIO_IF	0x200	[4:3]	R/W	2	GPIO protocol: 0: PWM/Differential ABI or UVW; 1: SSI; 2: SPI bus mode
ABI_IF		5	R/W	1	ABI / UVW protocol: 0: UVW; 1: ABI
ABI_DIFF		6	R/W	0	ABI/UVW differential mode: 0: single ended mode, 1: differential mode
GPIO_CFG		[11:7]	R/W	28	<u>GPIO output driver strength:</u> GPIO_CFG[2:0]: Do not change or overrides factory trimming for **5V mode** only. Use max. driving strength for **3.3V mode** only. <u>GPIO Output driver-mode:</u> GPIO_CFG[4:3]: 0: off, 1: open-drain p-MOS, 2: open-drain n-MOS 3: push-pull
Not used		[15:12]	R	0	

Register	Address	Bit	R/W	Default	Description
ABI_CFG	0x202	[4:0]	R/W	28	ABI output driver strength: ABI_CFG[2:0] Do not change or Overrides factory trimming for **5V mode** only. Use max. driving strength for **3.3V mode** only. ABI Output driver-mode: ABI_CFG[4:3] 0: off, 1: open-drain p-MOS, 2: open-drain n-MOS 3: push-pull Applies to ABI single-ended port (ABI_1) only
EH_MIN_SS_PERIOD		[7:5]	R/W	2	Minimum fail-safe state period. Please refer to the MLX90382 safety manual for details.
Not used		[15:12]	R	0	
ABI_LOG2N	0x204	[3:0]	R/W	3	ABI number of counts per revolution with: $4 * 2^{ABI\_LOG2N}$
UVW_PP		[8:4]	R/W	0	UVW pole pairs
ABIUVW_DIR		9	R/W	0	ABI / UVW rotation direction
ABIUVW_HYS		[13:10]	R/W	6	ABI / UVW hysteresis: $\pm floor(2^{(ABIUVW\_HYS-1)})$
ABI_I_LEN		14	R/W	1	ABI I-pulse length selection
ABI_PORT		15	R/W	1	QFN-24 ABI/UVW pin group selection: 0: select pin group AU_N, SCLK and MOSI 1: select pin group AU, BV and IW
PWM_INV	0x206	0	R/W	0	PWM waveform inversion
PWM_PCNT_ON		1	R/W	0	PWM period counter (PWM_PCNT), 0: period counter off, 1: PWM counter running despite GPIO_IF setting
Reserved		[7:2]	R/W	61	Reserved, don't change.
Not used		[15:8]	R	0	
PWM_PERIOD	0x22E	[15:0]	R/W	4095	PWM period
PWM_DC_OFS	0x248	[8:0]	R/W	0	PWM duty cycle offset trimming
Not used		[15:9]	R	0	
SPI_FADDR0	0x230	[7:0]	R/W	0	SPI FR address 0
SPI_FADDR1		[15:8]	R/W	60	SPI FR address 1
SPI_FADDR2	0x232	[7:0]	R/W	0	SPI FR address 2

Register	Address	Bit	R/W	Default	Description
SPI_FADDR3		[15:8]	R/W	0	SPI FR address 3
SPI_FRFS	0x234	[3:0]	R/W	10	SPI FR frame start pattern
SPI_FRFSEN		[4]	R/W	1	SPI FR frame start enable
SPI_FRCRCEN		[5]	R/W	1	SPI FR CRC enable
SPI_FRINV		[9:6]	R/W	0	SPI FR data inversion
SPI_MODE		[11:10]	R/W	0	SPI Mode selection Mode / SPI_MODE[11:10] (CPOL, CPHA) 0: 0, 0 1: 0, 1 2: 1, 0 3: 1, 1
SPI_DMY		[13:12]	R/W	0	SPI output optional word alignment SPI_DMY[13] = 1: Add additional dummy byte transfer after byte 2 in RR mode SPI_DMY[12] = 1: Add additional dummy byte transfer after byte 2 in FR mode
Not used		[15:14]	R	0	
SPI_SFRL	0x236	[7:0]	R/W	12	SPI super frame length, in bytes
SPI_SFRDLY		[15:8]	R/W	0	SPI FR delay within super frame Default is 6 for Die 1 in TSSOP-16/ TSSOP-16_EP package
SPI_CPTLT	0x238	[2:0]	R/W	0	SPI capture lead time synchronous (SPI_CPTLT + 1) * TSCLK before the DATA(FADDR0)[15:8] byte
SPI_SFR_SCPT		3	R/W	1	Synchronize the angle capture time point on all slaves to the position of the DATA(FADDR0)[15:8] byte with SPI_SFRDLY = 0
SPI_DBNC_CS		[7:4]	R/W	0	SPI CS debounce filter τ_{CS} = SPI_DBNC_CS*2/f_{RCO}
SPI_DBNC		[11:8]	R/W	0	SPI SCLK/MOSI debounce filter $\tau_{SCLK/MOSI}$ = SPI_DBNC/f_{RCO}
Not used		[15:12]	R	0	
SSI_PARPOS	0x23A	[3:0]	R/W	0	SSI parity bit position for odd parity: ≤ 8: parity of angle[15:SSI_PARPOS+1] transmitted at bit position SSI_PARPOS > 8: no parity bit - SSI data: angle[15:0]
SSI_TM		[11:4]	R/W	0	SSI timeout, T_M = (SSI_TM+1)*8/f_{ac}

Register	Address	Bit	R/W	Default	Description
SSI_CPT		12	R/W	1	In SSI mode, the DSP output shall be sampled at rate f_{ac} depending on SSI_CPT (CUS, default: 0) as follows: SSI_CPT = 0: falling edge on SCLK after start-up and falling edge auf pause pulse (T_P) SSI_CPT = 1: T_M after rising edge of pause pulse (T_P)
Not used		[15:13]	R	0	
PHY_RC_EN	0x23C	[2:0]	R/W	0	EMC RC filter enable: Bit[0]: pin CS Bit[1]: pin IW (QFN-24)/pin MOSI (TSSOP-16/ TSSOP-16_EP) Bit[2]: pin BV (QFN-24)/pin SCLK (TSSOP-16/ TSSOP-16_EP)
PHY_CS_RPU_DIS		3	R/W	0	Pin CS pull-up disable
PHY_BV_RPU_DIS		4	R/W	0	BV Pad pull-up disable (SCK)
Reserved		[6:5]	R/W	0	Reserved, don't change.
Not used		[15:7]	R	0	

Table 49: Interface configuration register

11.3.3 Safety mechanism configuration and reporting

The content of the following registers will affect the safety hardware metrics and shall not be modified unless a proper impact analysis is conducted. For further information refer to the MLX90382 Safety Manual [3].

Register	Address	Bit	R/W	De-fault	Description
EH_MIN_SS_PERIOD	0x202	[7:5]	R/W	2	Minimum fail-safe state period. See Table 49 for description of address 0x202
SC_YE	0x22A	[15:0]	R/W	32766	Signal conditioning: Protocol fault band value in SS3
DIAG_TEMP_THD_LO	0x24A	[7:0]	R/W	14	Temperature threshold for under-temperature diagnostic, unit 2*[K]
DIAG_TEMP_THD_HI		[15:8]	R/W	117	Temperature threshold for over-temperature diagnostic, unit 2*[K]
DIAG_TEMP_THD_MAX	0x24C	[7:0]	R/W	122	Threshold for maximum temperature diagnostic, unit 2*[K]
Reserved		8	R/W	0	Reserved, don't change
Not used		[15:9]	R		
DIAG_SPEED_THD	0x24E	[7:0]	R/W	254	Speed monitoring limit
DIAG_ALF_THD		[10:8]	R/W	2	Phase tracking error limit
Not used		[15:11]	R	0	
DIAG_AGC_THD_LO	0x252	[7:0]	R/W	2	AGC monitoring limit (lower bound)
DIAG_AGC_THD_HI		[15:8]	R/W	250	AGC monitoring limit (upper bound)
DE_OV_VDD	0x25A	0	R/W	0	Disable VDD overvoltage monitor
DE_UV_VDD		1	R/W	0	Disable VDD undervoltage monitor
DE_OV_VDDD		2	R/W	0	Disable VDDD overvoltage for monitor

DE_VDDA		3	R/W	0	Disable VDDA over-/undervoltage monitor
DE_VAUX		4	R/W	0	Disable VAUX over-/undervoltage monitor
DE_AGC		5	R/W	0	Disable AGC monitor
DE_DSP		6	R/W	0	Disable DSP related monitor
DE_RCO		7	R/W	0	Disable RCO monitor
DE_ADC_LIN		8	R/W	0	Disable ADC linearity monitor
DE_ADC		9	R/W	0	Disable ADC monitor
DE_ADC_OVF		10	R/W	0	Disable ADC overflow monitor
DE_AFE_REF		11	R/W	0	Disable AFE reference monitor
DE_TEMP		12	R/W	0	Disable over/under temperature monitor
DE_TEMP_MAX		13	R/W	0	Disable maximum temperature monitor
DE_SPEED		14	R/W	0	Disable speed monitor
DE_DSP_ALF		15	R/W	0	Disable DSP ALF monitor

Table 50: Safety mechanism related register

11.3.4 Miscellaneous

Register	Address	Bit	R/W	Default	Description
CUS_CRC	0x25E	[15:0]	R/W	N/A	CUS area checksum (CRC16 CCITT)
USER_ID0	0x23E	[7:0]	R/W	0	Reserved for customers for traceability
USER_ID1		[15:8]	R/W	0	Reserved for customers for traceability
USER_ID2	0x240	[7:0]	R/W	0	Reserved for customers for traceability
USER_ID3		[15:8]	R/W	0	Reserved for customers for traceability
USER_ID4	0x242	[7:0]	R/W	0	Reserved for customers for traceability
USER_ID5		[15:8]	R/W	N/A	Reserved for customers for traceability

Table 51: Miscellaneous register

11.3.5 Signal conditioning, calibration and processing

Register	Address	Bit	R/W	Default	Description
AGC_GAIN_MIN	0x208	[5:0]	R/W	0	AGC minimum gain, range [0..63]. Values above 47 LSB are treated as 63 LSB
AGC_GAIN_MAX		[11:6]	R/W	63	AGC maximum gain, range [0..63]. Values above 47 LSB are treated as 63 LSB
Not used		[15:12]	R	0	
PEQ_GAIN	0x20A	[2:0]	R/W	0	Linearization gain. If > 0, phase offsets per reference point angle are POFSxx[15:0] = signed(PEQxx) * $2^{(PEQ\_GAIN-1)}$, else 0
Not used		[15:3]	R	0	
PEQ00	0x20C	[7:0]	R/W	0	Phase Equalizer value at 0/16 * 360 deg
PEQ01		[15:8]	R/W	0	Phase Equalizer value at 1/16 * 360 deg
PEQ02	0x20E	[7:0]	R/W	0	Phase Equalizer value at 2/16 * 360 deg
PEQ03		[15:8]	R/W	0	Phase Equalizer value at 3/16 * 360 deg
PEQ04	0x210	[7:0]	R/W	0	Phase Equalizer value at 4/16 * 360 deg
PEQ05		[15:8]	R/W	0	Phase Equalizer value at 5/16 * 360 deg
PEQ06	0x212	[7:0]	R/W	0	Phase Equalizer value at 6/16 * 360 deg

Register	Address	Bit	R/W	Default	Description
PEQ07		[15:8]	R/W	0	Phase Equalizer value at 7/16 * 360 deg
PEQ08	0x214	[7:0]	R/W	0	Phase Equalizer value at 8/16 * 360 deg
PEQ09		[15:8]	R/W	0	Phase Equalizer value at 9/16 * 360 deg
PEQ10	0x216	[7:0]	R/W	0	Phase Equalizer value at 10/16 * 360 deg
PEQ11		[15:8]	R/W	0	Phase Equalizer value at 11/16 * 360 deg
PEQ12	0x218	[7:0]	R/W	0	Phase Equalizer value at 12/16 * 360 deg
PEQ13		[15:8]	R/W	0	Phase Equalizer value at 13/16 * 360 deg
PEQ14	0x21A	[7:0]	R/W	0	Phase Equalizer value at 14/16 * 360 deg
PEQ15		[15:8]	R/W	0	Phase Equalizer value at 15/16 * 360 deg
S_IQ	0x21C	[15:0]	R/W	0	Relative cross-sensitivity from in-phase to quadrature phase component, range $[-2^{15},+2^{15})$; overrides factory trimming, if non-zero
S_QQ	0x21E	[15:0]	R/W	32768	Relative sensitivity for quadrature component, range $[0,2^{16}-1)$; overrides factory trimming if not 2^{15}.
PHASE_OFS	0x220	[15:0]	R/W	0	Phase/Angle offset before signal conditioning, resolution $360/2^{16}$ deg (signed 2th-complement)
SC_X1	0x222	[15:0]	R/W	0	Signal conditioning: X1, input range low
SC_X2	0x224	[15:0]	R/W	0	Signal conditioning: X2, input range high
SC_Y1	0x226	[15:0]	R/W	1	Signal conditioning: Y1, output range low
SC_Y2	0x228	[15:0]	R/W	32765	Signal conditioning: Y2, output range high
SC_YE	0x22A	[15:0]	R/W	32766	Signal conditioning: output fault band level
SC_HL	0x22C	[8:0]	R/W	128	Signal conditioning: Transition point for clamping high to clamping low as offset from center point of X range; resolution 360 deg/2^8.
Not used		[15:9]	R	0	
DELAY_CUS	0x244	[7:0]	R/W	0	Customer processing delay, range [0:255] * 26/64 / f_{RCO}
Not used		[15:8]	R	0	
DSP_IQNEG	0x246	[1:0]	R/W	0	I/Q sign inversion: Bit[0]: 0: GC_I, 1: -GC_I Bit[1]: 0: GC_Q, 1: -GC_Q
DSP_GC_AVG		[4:2]	R/W	0	GC averaging control: 0: Averaging off, 1…6: sum(k = 1..4^DSP_GC_AVG, gc_x/4^DSP_GC_AVG) 7: sum(k = 1..8, gc_x/8)
DSP_DRIFTC_DIS		5	R/W	0	1: Disable delay compensation
Reserved		6	R/W	1	Reserved, don't change.
DSP_LFC_LO		[10:8]	R/W	0	Lowest DSP loop filter bandwidth; adaptive loop filter enabled, if DSP_LFC_LO < DSP_LFC_HI
DSP_LFC_HI		[13:11]	R/W	5	Upper DSP loop filter bandwidth
DSP_SROS		[15:14]	R/W	2	Phase tracking step response overshoot

Register	Address	Bit	R/W	Default	Description
RMM_FAST	0x256	[2:0]	R/W	4	Settling configuration for Self-Calibration after start up
RMM_LFC		[5:3]	R/W	2	Settling constant for the Self-Calibration tracking filter
RMM_AVG_MIN		[7:6]	R/W	0	Minimum value for Self-Calibration averaging
RMM_AVG_MAX		[9:8]	R/W	3	Maximum value for Self-Calibration averaging
Reserved		[14:10]	R/W	0	Reserved, don't change.
Not used		15	R	0	
RMM_ASQQ_MIN	0x258	[4:0]	R/W	0	Self-Calibration minimum ASQQ clamping value
RMM_ASQQ_MAX		[9:5]	R/W	0	Self-Calibration maximum ASQQ clamping value
RMM_ASIQ_MAX		[14:10]	R/W	0	Self-Calibration maximum absolute ASIQ clamping value
Reserved		15	R/W	0	Reserved, don't change.
Reserved	0x25C	[0:6]	R/W	0	Reserved, don't change.
DE_DSP_RMM		[8:7]	R/W	3	bit[0] – 1: Disable sensitivity Self-Calibration bit[1] – 1: Disable orthogonality Self-Calibration
Reserved		9	R/W	1	Reserved, don't change.
Not used		[14:10]	R	0	
Reserved		15	R/W	0	Reserved, don't change.

Table 52: Signal conditioning and processing register

12 Glossary of terms and references

12.1 Glossary

Term	Description
ABI	Incremental Output Interface (Quadrature A/B and Index outputs)
ADC	Analog-to-Digital Converter
ASIL	Automotive Safety Integrity Level
CDM	Charged Device Mode
CRC	Cyclic Redundancy Check
CS	Chip Select
CPHA	Clock Phase
CPOL	Clock Polarity
dBz mode	Stray Field Immune Mode
DSP	Digital Signal Processing
ECC	Error Correction Code
EMC	Electro-Magnetic Compatibility
EoL	End of Line
ESD	Electrostatic discharge
FR	Frame Read
HBM	Human Body Model
IC	Integrated Circuit
IMC	Integrated Magnetic Concentrator
INL / DNL	Integral Non-Linearity / Differential Non-Linearity
LFC	Low-pass Filter Constant
LE	Linearity Error
MCU	Microcontroller Unit
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Bit
MUX	Multiplexer
N.C.	Not Connected
NVRAM	Non-Volatile RAM
LSB/MSB	Least Significant Bit / Most Significant Bit
OV/UV	Overvoltage / Undervoltage
OS	Overshoot
PWM	Pulse Width Modulation
RAM	Random-Access Memory
RMS	Root Mean Square
RPM	Revolutions Per Minute
RR	Register Read
RW	Register Write
SCLK	Serial Clock
SFR	Super-Frame Read
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TDMA	Time Division Multiple Access
Tesla (T)	SI derived unit for the magnetic flux density (Vs/m2)
UVW	Brushless Motor Output

12.2 References

Following documents are referred to in this document:

[1] Automotive Electronics Council, *Failure Mechanism Based Stress Test Qualification for Integrated Circuits, AEC-Q100,* 2014.
[2] *ISO 11452-8:2015, Road vehicles — Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 8: Immunity to magnetic fields.*
[3] *MLX90382 Safety Manual (single die).*
[4] *MLX90382 Safety Manual Addendum for IEC61508 compliance.*
[5] *MLX90382 dual-die Safety Manual Addendum.*
[6] *MLX90382 Application Note.*
[7] *ISO 26262:2018, Road vehicles — Functional safety.*
[8] *IEC 61508:2010, Functional safety of electrical/electronic/programmable electronic safety-related.*
[9] *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices, IPC J-STD-033.*
[10] *ANSI/ESD S20.20-2021: Protection of Electrical and Electronic Parts.*
[11] *IPC J-STD-001H, Requirements for Soldered Electrical and Electronic Assemblies, IPC.*
[12] *IPC-A-610H, Acceptability of Electronic Assemblies.*

The application note “MLX90382 programming and EoL calibration via SPI” can be accessed through the MyMelexis platform: www.melexis.com/mymelexis. To gain access to www.melexis.com/mymelexis and to the MLX90392 Safety Manuals, please contact your local sales representative.

The descriptions in this document overrule the descriptions in the referred documents.

12.3 List of Tables

12.4 List of Figures

13 Revision history

Revision	Date	Change history
1.0	17.11.2025	Initial version

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