Microchip Timing Module for Data Center Servers

MD-990-0011-B Data Sheet

General Description

The MD-990-0011-B is a Microchip Timing Module for Data Center Servers that provides a modular system design approach. The MD-990-0011-B is a custom product that is designed to be used only within specific Intel-based system architecture reference designs. Please consult Microchip to confirm if this product fits your Intel-based system.

Features

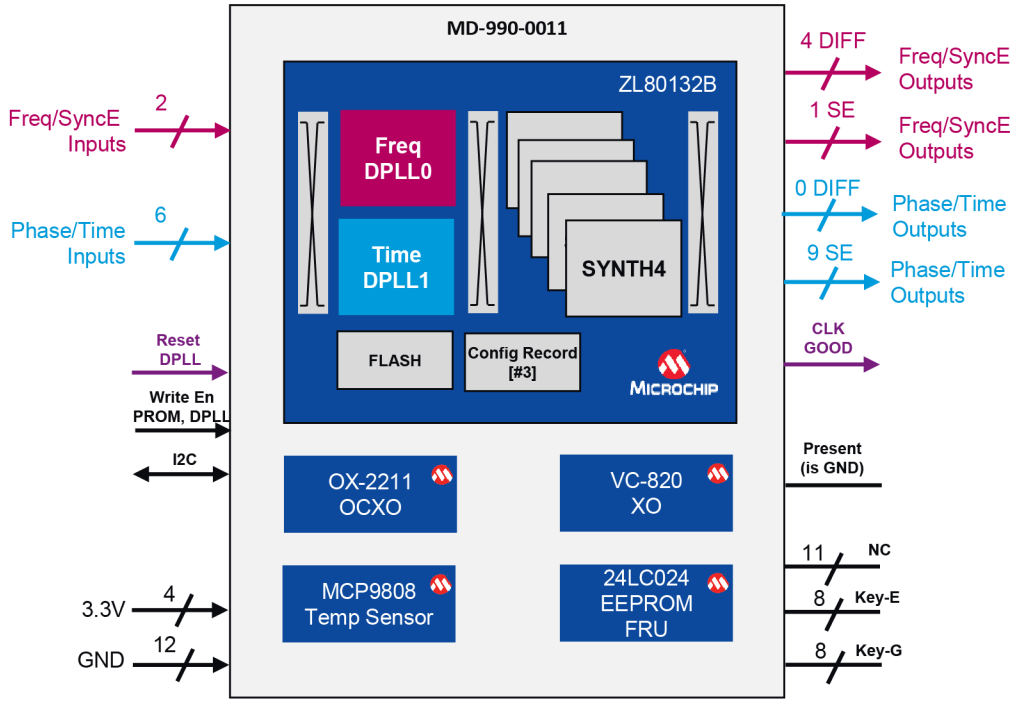
- Two independent channels: one for Time and one for Frequency
- Multiple options for 1.5µs holdover: from 4 to 8 hours
- Standard M.2 E-Key connector

Applications

- Data center compute servers
- Provides synchronization for a server including an OCP NIC, PCIe NIC, or motherboard with Intel Xeon processor

Block Diagram

Figure 1. Block Diagram



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1. Functional Description

1.1. Form Factor

- 70mm x 30mm incl. M.2 connector 75 position (2x28 Pins)

1.2. Hardware DPLL

- Two independent channels
  - Typical use is one channel for Frequency (i.e. EEC supporting SyncE)
  - Typical use is one channel for Time (i.e., PEC supporting TIME or GNSS)
- Eight independent inputs
  - Typical use is two for Frequency candidates
  - Typical use is six for Time candidates
- Eighteen outputs
  - Typical use is four differential pair clocks and one single-ended clock from Frequency domain
  - Typical use is nine single-ended clocks from Time domain
  - Outputs sourced from SYNTH0 (typically SyncE domain) are available within 20ms after power-up reset
- Core operation
  - Frequency domain is compliant with ITU-T G.8262, G.8262.1, as well as legacy Telecom standards from ITU-T G.813 and GR-1244-CORE, amongst others.
  - Time domain is capable of synchronizing to GNSS 1PPS signal, as well as operation controlled from external software (using NCO).
  - Supports the ability to measure per-input phase error compared with DPLL
  - The per-input phase error is typically around 0 nanoseconds for DPLL1 (configured for phase/time synchronization) and will *not* be around 0 nanoseconds for DPLL0 (configured for frequency synchronization)
- Programmability
  - Bandwidth filtering for physical input clocks from sub-1mHz to over 100Hz
  - Fast locking to physical input clocks, as low as 10 seconds to 1PPS input candidate
  - Holdover engine for long-term loss of TIME or GNSS inputs, including programmable holdover filtering and holdover storage delay
  - Automatic (unmanaged) selection of candidates based on availability and pre-programmed priority table
- See Microchip's ZL80132B data sheet for more details

1.3. Firmware DPLL

- The firmware version is stored in register 0x005 and is 0x1BC4
- The custom_config_ver 0x0007-0x000A is 0x00-0x0B-0x00-0x00 for MD-990-0011-B with 0x0007 reserved for user use/variants
- The firmware program and configuration may be upgraded using devlink
  - https://git.kernel.org/pub/scm/linux/kernel/git/torvalds/linux.git/tree/drivers/dpll/zl3073x?h=v6.18
- The firmware upgrade processes may typically take 150 seconds at 100kHz I^2C interface speed

1.4. Software DPLL Netlink Functionality

- Netlink support has been upstream to Linux kernel
  - https://git.kernel.org/pub/scm/linux/kernel/git/torvalds/linux.git/tree/drivers/dpll/zl3073x?h=v6.18

1.5. Hardware System Clock

- Low-jitter system oscillator. One of the following three XO may be populated, based on Microchip's manufacturing preference.
  - VC-820-9021-114M285000
  - VC-820-9022-114M285000
  - VC-820-9024-114M285000

1.6. Hardware OCXO

- Holdover (freewheeling) capability up to 8 hours without external software compensation
  - 1.5µs over 4 hours: OX-2211-EAE-1090-10M0000000
  - 1.5µs over 8 hours: OX-2211-EAE-5000-10M0000000
- See Microchip's OX-2211-EAE-1090-10M0000000 and OX-2211-EAE-5000-10M0000000 data sheets for more details

1.7. Software OCXO

- I^2C option
- See Microchip's OX-2211-EAE-1090-10M0000000 and OX-2211-EAE-5000-10M0000000 data sheets for more details

1.8. Hardware Temperature Sensor

- See Microchip's MCP9808 data sheet for more details

1.9. Software Temperature Sensor

- I^2C access to the temperature sensor is available through the M.2 I^2C interface.
- See Microchip's MCP9808 data sheet for more details

1.10. Hardware EEPROM

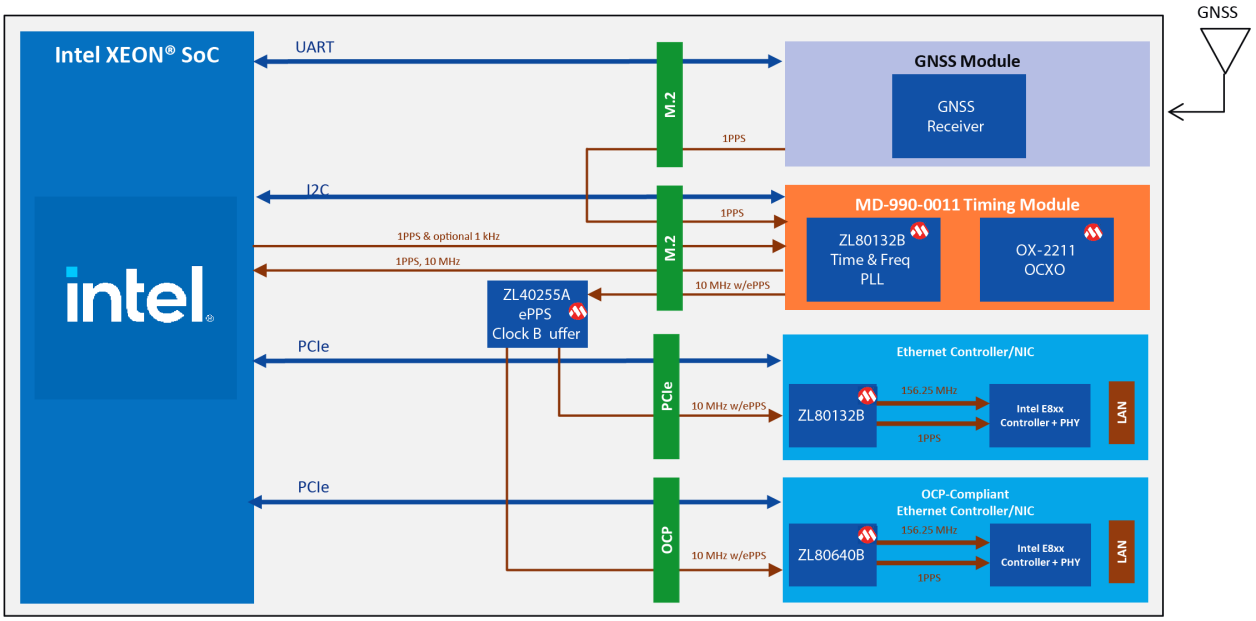
- See Microchip's 24LC024 data sheet for more details

1.11. Software EEPROM

- Contains FRU content as shown in this document
- I^2C access to 2kBit EEPROM is available through the M.2 I^2C interface
- Write Enable pin available
- See Microchip's 24LC024 data sheet for more details

1.12. Typical Use Case

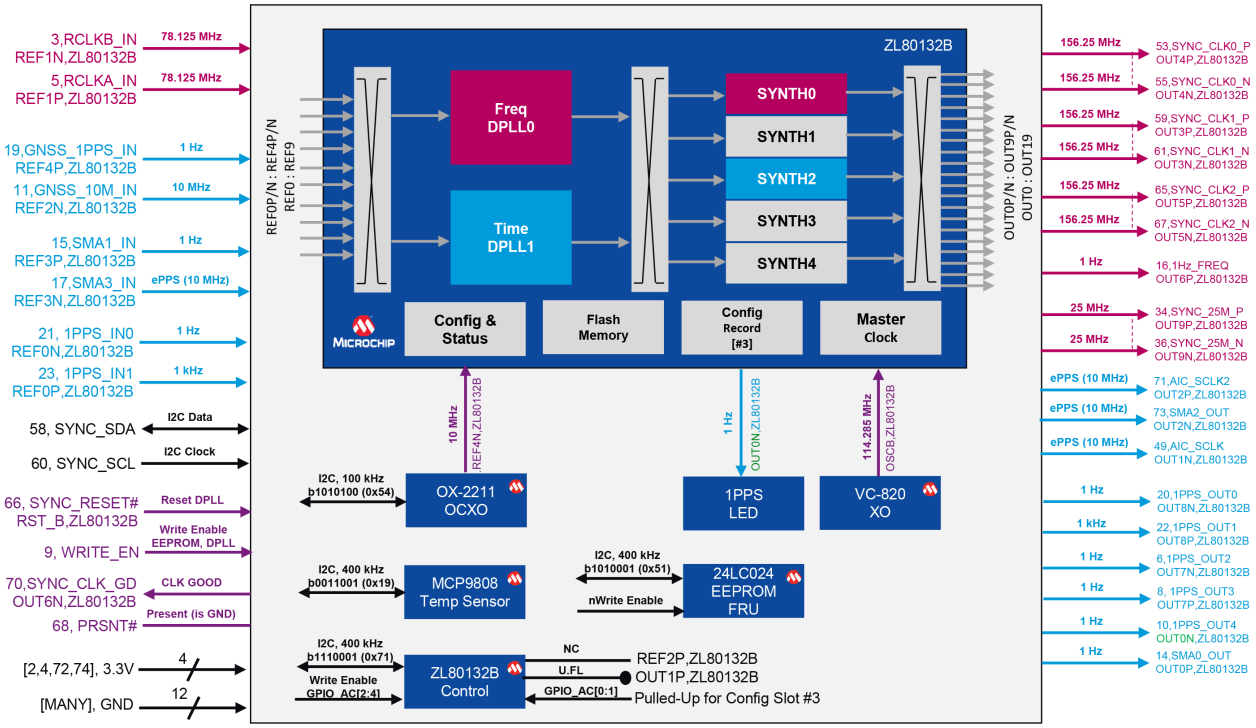
Figure 1-1. Typical Use Case



In the use case above, the computer server has access to a GNSS signal and may synchronize the MD-990-0011 using the recovered GNSS 1PPS. If the GNSS 1PPS signal fails, the MD-990-0011-B may be reconfigured to fall back to the TIME as the synchronization source for the Server.

1.13. Detailed Block Diagram

Figure 1-2. Detailed Block Diagram

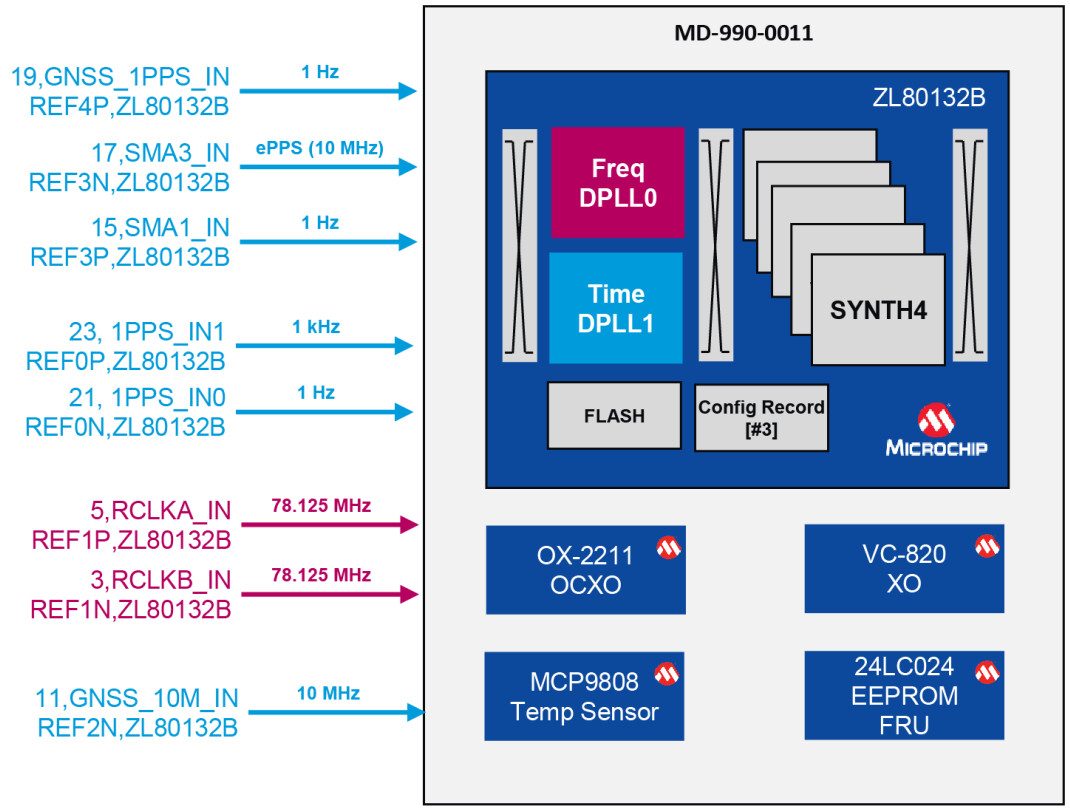


1.14. Input Clocking Use Case

Table 1-1. Input Pin Definitions

Input	ZL80132B	Default Frequency	Alternate Frequency	Time DPLL1 Priority	Freq DPLL0 Priority	Typical Source
GNSS_1PPS_IN	REF4P	1Hz	Menu (see below)	0	0	GNSS Receiver
SMA3_IN	REF3N	ePPS	Menu (see below)	2	2	External SMA
SMA1_IN	REF3P	1Hz	Menu (see below)	3	3	External SMA
1PPS_IN1 + 1PPS_IN0	REF0P + REF0N	1kHz + 1Hz	Menu (see below)	6	DNU	MB CPU
1PPS_IN1	REF0P	1kHz	Menu (see below)	6	DNU	MB CPU
1PPS_IN0	REF0N	1Hz	Menu (see below)	7	DNU	MB CPU
RCLKA_IN	REF1P	78.125MHz	Menu (see below)	10	10	SyncE PHY
RCLKB_IN	REF1N	78.125MHz	Menu (see below)	11	11	SyncE PHY
GNSS_10M_IN	REF2N	10MHz	Menu (see below)	DNU	DNU	GNSS Receiver

Figure 1-3. Block Diagram: Input Clocking Use Case



DPLL processes inputs via priority table

- Priority 0 is highest, Priority 15 is DNU

DPLL will automatically select best input

- ZL80132B will reconfigure its settings based on input selected

Users may manually change the clock frequency configuration using I^2C registers

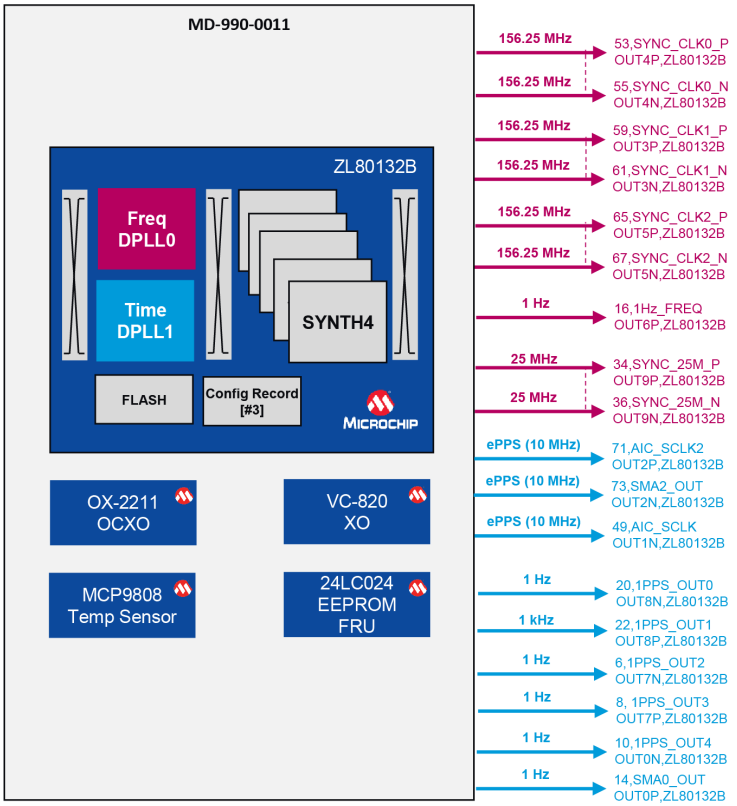
- Frequency source clocks: 62.5MHz, 78.125MHz, 100MHz
- Phase source clocks: 1Hz, 25Hz, 100Hz, 1kHz, 10MHz, 25MHz, ePPS (10MHz)

1.15. Output Clocking Use Case

Table 1-2. Output Pin Definitions

Output	ZL80132B	Default Frequency	Alternate Frequency	Source DPLL	Typical Use
1PPS_OUT0, 1PPS_OUT1	OUT8N, OUT8P	1Hz, 1kHz	Menu (see below)	Time DPLL1	Ref-Sync pairs
1PPS_OUT2, 1PPS_OUT3	OUT7N, OUT7P	1Hz, 1Hz	Blocked	Time DPLL1	MB CPU
1PPS_OUT4	OUT0N	1Hz	Menu (see below)	Time DPLL1	—
SMA0_OUT	OUT0P	1Hz	Menu (see below)	Time DPLL1	External SMA
AIC_SCLK	OUT1N	ePPS	Blocked	Time DPLL1	Plug-in cards (e.g. OCP)
SMA2_OUT	OUT2N	ePPS	Blocked	Time DPLL1	External SMA
AIC_SCLK2	OUT2P	ePPS	Blocked	Time DPLL1	Additional plug-in cards (e.g. OCP)
SYNC_CLK0_P/N	OUT4_P/N	156.25MHz	Blocked	Freq DPLL0	SyncE PHY (SyncE traceable)
SYNC_CLK1_P/N	OUT3_P/N	156.25MHz	Blocked	Freq DPLL0	
SYNC_CLK2_P/N	OUT5_P/N	156.25MHz	Blocked	Freq DPLL0	SYS clock for MB CPU
SYNC_25M_P/N	OUT9_P/N	25MHz	Blocked	Freq DPLL0	PTP host clock freerun source
1Hz_FREQ	OUT6P	1Hz	Blocked	Freq DPLL0	Not ToD aligned

Figure 1-4. Block Diagram: Output Clocking Use Case



DPLL power-up configuration has a fixed relationship between outputs, synthesizers, and DPLL, as shown in the table.

Outputs are pairs that limit combinations on the P/N pins.

- P must be the same or higher frequency than N
- P and N must have the same ePPS configuration

Other:

- OUT0N is driving the LED on the M.2 card and is also brought out to the connector
- OUT1P attaches to the local U.FL on the M.2 card and is not brought out to the connector
- OUT6N is SYNC_CLK_GD and is brought out to the connector

The user may manually change the clock frequency configuration using I^2C registers.

- Frequency output clocks: 156.25MHz
- Phase output clocks: 1Hz, 25Hz, 100Hz, 1kHz, 10MHz, 25MHz, ePPS (10MHz)

1.16. Main Components

Table 1-3. Main Components: MD-990-0011-BA01

Part	Vendor	Function	I²C Address	I²C Speed
ZL80132BLDG1Q0GT	Microchip	PLL	b1110001	100kHz, 400kHz
OX-2211-EAE-1090-10M0000000	Microchip	OCXO	b1010100	100kHz
MCP9808	Microchip	Temp. Sensor	b0011001	100kHz, 400kHz
24LC024	Microchip	EEPROM	b1010001	100kHz, 400kHz
VC-820-9021-114M285000 VC-820-9022-114M285000 VC-820-9024-114M285000	Microchip	XO	N/A	N/A

Table 1-4. Main Components: MD-990-0011-BC01

Part	Vendor	Function	I²C Address	I²C Speed
ZL80132BLDG1Q0GT	Microchip	PLL	b1110001	100kHz, 400kHz
OX-2211-EAE-5000-10M0000000	Microchip	OCXO	b1010100	100kHz
MCP9808	Microchip	Temp. Sensor	b0011001	100kHz, 400kHz
24LC024	Microchip	EEPROM	b1010001	100kHz, 400kHz
VC-820-9021-114M285000 VC-820-9022-114M285000 VC-820-9024-114M285000	Microchip	XO	N/A	N/A

1.17. Pin Connections: ZL80132B to M.2 Connector

Figure 1-5. Pin Connections Between ZL80132B and M.2 Connector

M.2 Pin #	M.2 Signal Name	M.2 Signal Direction (Module Perspective)	Clock Frequency	Signal Format / Voltage Level	ZL80132B Pin #	ZL80132B Pin Name	ZL80132B Domain	ZL80132B PLL#	ZL80132B Synth#	In CLK Frequency Default	In CLK Frequency Alternate	In CLK DPLL1 Priority	In CLK DPLL0 Priority	Out CLK Frequency Default	Out CLK Frequency Alternate	Delay
68	PRSNT#	Output, Single-Ended	Grounded on Module	3.3 V	—	—	—	—	—	—	—	—	—	—	—	—
9	WRITE_EN	Input	—	3.3 V	47,46,45	GPIO[2:4]_AC[2:4]	—	—	—	—	—	—	—	—	—	—
66	SYNC_RESET#	Input	—	3.3 V	16	RST_B	—	—	—	—	—	—	—	—	—	—
60	SYNC_SCL	Input	<400kHz	3.3 V	36	SCK_SCL, GPIO[0]_AC[0]	—	—	—	—	—	—	—	—	—	—
58	SYNC_SDA	Bidirectional	<400kHz	3.3 V	35	SI_SDA, GPIO[1]_AC[1]	—	—	—	—	—	—	—	—	—	—
23	1PPS_IN1	Input	1kHz	3.3 V	12	REF0P	TIME	DPLL1	SYNTH2	1kHz	Menu	6	DNU	—	—	129ps
21	1PPS_IN0	Input	1PPS	3.3 V	13	REF0N	TIME	DPLL1	SYNTH2	1Hz	Menu	7	DNU	—	—	129ps
5	RCLKA_IN	Input	78.125MHz	3.3 V	10	REF1P	SyncE	DPLL0	SYNTH0	78.125MHz	Menu	10	10	—	—	146ps
3	RCLKB_IN	Input	78.125MHz	3.3 V	11	REF1N	SyncE	DPLL0	SYNTH0	78.125MHz	Menu	11	11	—	—	146ps
—	—	—	—	—	8	REF2P	NONE	NONE	NONE	DIS	Menu	DNU	DNU	—	—	—
11	GNSS_10M_IN	Input	10MHz	3.3 V	9	REF2N	TIME	DPLL1	SYNTH2	10MHz	Menu	DNU	DNU	—	—	143ps
15	SMA1_IN	Input	Up to 10MHz	3.3 V	6	REF3P	TIME	DPLL1	SYNTH2	1Hz	Menu	3	3	—	—	2349ps
17	SMA3_IN	Input	Up to 10MHz	3.3 V	7	REF3N	TIME	DPLL1	SYNTH2	ePPS	Menu	2	2	—	—	2344ps
19	GNSS_1PPS_IN	Input	1PPS	3.3 V	4	REF4P	TIME	DPLL1	SYNTH2	1Hz	Menu	0	0	—	—	155ps
—	—	—	—	—	5	REF4N	OCXO	ALL	ALL	10MHz	Menu	DNU	DNU	—	—	—
14	SMA0_OUT	Output, Single-Ended	Up to 10MHz	3.3 V	52	OUT0P	TIME	DPLL1	SYNTH2	—	—	—	—	1Hz	Menu	2432ps
10	1PPS_OUT4	Output, Single-Ended	1PPS	3.3 V	51	OUT0N	TIME	DPLL1	SYNTH2	—	—	—	—	1Hz	Menu	248ps
—	—	—	—	—	55	OUT1P	TIME	DPLL1	SYNTH2	—	—	—	—	Blocked	Blocked	—
49	AIC_SCLK	Output, Single-Ended	10MHz/ePPS	3.3 V	54	OUT1N	TIME	DPLL1	SYNTH2	—	—	—	—	ePPS	Blocked	159ps
71	AIC_SCLK2	Output, Single-Ended	10MHz/ePPS	3.3 V	58	OUT2P	TIME	DPLL1	SYNTH2	—	—	—	—	ePPS	Blocked	137ps
73	SMA2_OUT	Output, Single-Ended	10MHz/ePPS	3.3 V	57	OUT2N	TIME	DPLL1	SYNTH2	—	—	—	—	ePPS	Blocked	141ps
59	SYNC_CLK1_P	Output, Differential	156.25MHz	LVDS (AC-coupled)	61	OUT3P	SyncE	DPLL0	SYNTH0	—	—	—	—	156.25MHz	Blocked	133ps
61	SYNC_CLK1_N	Output, Differential	156.25MHz	LVDS (AC-coupled)	60	OUT3N	SyncE	DPLL0	SYNTH0	—	—	—	—	156.25MHz	Blocked	137ps
53	SYNC_CLK0_P	Output, Differential	156.25MHz	LVDS (AC-coupled)	64	OUT4P	SyncE	DPLL0	SYNTH0	—	—	—	—	156.25MHz	Blocked	115ps
55	SYNC_CLK0_N	Output, Differential	156.25MHz	LVDS (AC-coupled)	63	OUT4N	SyncE	DPLL0	SYNTH0	—	—	—	—	156.25MHz	Blocked	121ps
65	SYNC_CLK2_P	Output, Differential	156.25MHz	LVPECL (AC-coupled)	17	OUT5P	SyncE	DPLL0	SYNTH0	—	—	—	—	156.25MHz	Blocked	90ps
67	SYNC_CLK2_N	Output, Differential	156.25MHz	LVPECL (AC-coupled)	18	OUT5N	SyncE	DPLL0	SYNTH0	—	—	—	—	156.25MHz	Blocked	99ps
16	1Hz_FREQ	Output, Single-Ended	1PPS	3.3 V	20	OUT6P	SyncE	DPLL0	SYNTH0	—	—	—	—	1Hz	Blocked	2344ps
70	SYNC_CLK_GD	Output, Single-Ended	GPO	3.3 V	21	OUT6N	SyncE	DPLL0	SYNTH0	—	—	—	—	GPO: GOOD	Blocked	104ps
8	1PPS_OUT3	Output, Single-Ended	1PPS	3.3 V	23	OUT7P	TIME	DPLL1	SYNTH2	—	—	—	—	1Hz	Blocked	147ps
6	1PPS_OUT2	Output, Single-Ended	1PPS	3.3 V	24	OUT7N	TIME	DPLL1	SYNTH2	—	—	—	—	1Hz	Blocked	152ps
22	1PPS_OUT1	Output, Single-Ended	1kHz	3.3 V	26	OUT8P	TIME	DPLL1	SYNTH2	—	—	—	—	1kHz	Menu	147ps
20	1PPS_OUT0	Output, Single-Ended	1PPS	3.3 V	27	OUT8N	TIME	DPLL1	SYNTH2	—	—	—	—	1Hz	Menu	139ps
34	SYNC_25M_P	Output, Differential	25MHz	LVPECL (AC-coupled)	29	OUT9P	SyncE	DPLL0	SYNTH0	—	—	—	—	25MHz	Blocked	133ps
36	SYNC_25M_N	Output, Differential	25MHz	LVPECL (AC-coupled)	30	OUT9N	SyncE	DPLL0	SYNTH0	—	—	—	—	25MHz	Blocked	139ps

1.18. EEPROM (FRU) Memory Map

The image below is a sample of the FRU Memory Map. The complete map can be downloaded by logging into MyMicrochip and navigating to the appropriate page.

Figure 1-6. EEPROM (FRU) Memory Map

IPMI Area	Start Byte (dec)	End Byte (dec)	Start Byte (hex)	End Byte (hex)	Length (Bytes)	IPMI Field	MD-990 Custom Field	Field Value	Field Value Description	Field Value (Binary as Little Endian, Padding is ZERO 0x20)
Common Header	0	0	0x0	0x0	1	Common Header Format Version		fixed		0x01
Common Header	1	1	0x1	0x1	1	Internal User Area Starting Offset		fixed	<unused>	0x00
Common Header	2	2	0x2	0x2	1	Chassis Info Area Starting Offset		fixed	<unused>	0x00
Common Header	3	3	0x3	0x3	1	Board Area Starting Offset		fixed	offset to board info area (byte 8 is 1*8 bytes)	0x01
Common Header	4	4	0x4	0x4	1	Product Info Area Starting Offset		fixed	offset to product info area (byte 64 is 8*8 bytes)	0x08
Common Header	5	5	0x5	0x5	1	MultiRecord Area Starting Offset		fixed		0x00
Common Header	6	6	0x6	0x6	1	PAD		fixed	PAD, write as 00h	0x00
Common Header	7	7	0x7	0x7	1	Comon Header Checksum		fixed	"zero checksum"	0xF6
Internal User Area						<unused>		fixed	<unused>	<unused>
Chassis Info Area						<unused>		fixed	<unused>	<unused>
Board Info Area	8	8	0x8	0x8	1	Board Area Format Version		fixed		0x01
Board Info Area	9	9	0x9	0x9	1	Board Area Length		fixed	board info area is 56 bytes (56 is 7*8 bytes)	0x07
Board Info Area	10	10	0xA	0xA	1	Language Code		fixed	English (d25)	0x19
Board Info Area	11	13	0xB	0xD	3	Manufacturing Date / Time		computed	Number of minutes from 0:00 hrs 1/1/96. 00 00 00h = unspecified	addr 0x0D-0C-0B e.g. 0x[redacted]
Board Info Area	14	14	0xE	0xE	1	Board Manufacturer T/L		fixed	8-bit ASCII + Latin 1, length 9	0xC9
Board Info Area	15	23	0xF	0x17	9	Board Manufacturer		fixed	"MICROCHIP"	addr 0x0F-10-11-12-13-14-15-16-17 only 0x4D-49-43-52-4F-43-48-49-50
Board Info Area	24	24	0x18	0x18	1	Board Product Name T/L		fixed	8-bit ASCII + Latin 1, length 11	0xCB
Board Info Area	25	35	0x19	0x23	11	Board Product Name		part-specific	e.g. "MD-990-0011"	addr 0x19-1A-1B-1C-1D-1E-1F-20-21-22-23 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31
Board Info Area	36	36	0x24	0x24	1	Board Serial Number T/L		fixed	binary, length 3	0x03
Board Info Area	37	39	0x25	0x27	3	Board Serial Number		computed	MD-990 M.2 serial number	addr 0x27-26-25 e.g. 0x[redacted]
Board Info Area	40	40	0x28	0x28	1	Board Part Number T/L		fixed	8-bit ASCII + Latin 1, length 19	0xD3
Board Info Area	41	59	0x29	0x3B	19	Board Part Number		part-specific	e.g. "MD-990-0011-AA01" e.g. "MD-990-0011-AB01" e.g. "MD-990-0011-AC01" e.g. "MD-990-0011-BA01" e.g. "MD-990-0011-BA01-02"	addr 0x29-2A-2B-2C-2D-2E-2F-30-31-32-33-34-35-36-37-38-39-3A-3B e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-41-41-30-31-20-20-20 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-41-42-30-31-20-20-20 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-41-43-30-31-20-20-20 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-42-41-30-31-20-20-20 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-42-41-30-31-2D-30-32
Board Info Area	60	60	0x3C	0x3C	1	FRU File ID T/L		fixed	binary, length 1	0x01
Board Info Area	61	61	0x3D	0x3D	1	FRU File ID		fixed	FRU file version 1	0x01
Board Info Area	62	62	0x3E	0x3E	1	End		fixed		0xC1
Board Info Area	63	63	0x3F	0x3F	1	Board Info Area Checksum		computed	"zero checksum"	0x[redacted]
Product Info Area	64	64	0x40	0x40	1	Product Area Format Version		fixed		0x01
Product Info Area	65	65	0x41	0x41	1	Product Area Length		fixed	product info area is 168 bytes (168 is 21*8 bytes)	0x15
Product Info Area	66	66	0x42	0x42	1	Language Code		fixed	English (d25)	0x19
Product Info Area	67	67	0x43	0x43	1	Manufacturer Name T/L		fixed	8-bit ASCII + Latin 1, length 9	0xC9
Product Info Area	68	76	0x44	0x4C	9	Manufacturer Name		fixed	"MICROCHIP"	addr 0x44-45-46-47-48-49-4A-4B-4C only 0x4D-49-43-52-4F-43-48-49-50
Product Info Area	77	77	0x4D	0x4D	1	Product Name T/L		fixed	8-bit ASCII + Latin 1, length 11	0xCB
Product Info Area	78	88	0x4E	0x58	11	Product Name		part-specific	e.g. "MD-990-0011"	addr 0x4E-4F-50-51-52-53-54-55-56-57-58 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31
Product Info Area	89	89	0x59	0x59	1	Product Part/Model Number T/L		fixed	8-bit ASCII + Latin 1, length 19	0xD3
Product Info Area	90	108	0x5A	0x6C	19	Product Part/Model Number		part-specific	e.g. "MD-990-0011-AA01" e.g. "MD-990-0011-AB01" e.g. "MD-990-0011-AC01" e.g. "MD-990-0011-BA01" e.g. "MD-990-0011-BA01-02"	addr 0x5A-5B-5C-5D-5E-5F-60-61-62-63-64-65-66-67-68-69-6A-6B-6C e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-41-41-30-31-20-20-20 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-41-42-30-31-20-20-20 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-41-43-30-31-20-20-20 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-42-41-30-31-20-20-20 e.g. 0x4D-44-2D-39-39-30-2D-30-30-31-31-2D-42-41-30-31-2D-30-32
Product Info Area	109	109	0x6D	0x6D	1	Product Version T/L		fixed	binary, length 2	0x02
Product Info Area	110	111	0x6E	0x6F	2	Product Version		part-specific	e.g. rev 0x0A ENG e.g. rev 0x00 production	addr 0x6F-6E e.g. 0x00-0A e.g. 0x00-0B
Product Info Area	112	112	0x70	0x70	1	Product Serial Number T/L		fixed	binary, length 3	0x03
Product Info Area	113	115	0x71	0x73	3	Product Serial Number		computed	MD-990 M.2 serial number	addr 0x73-72-71 e.g. 0x[redacted]
Product Info Area	116	116	0x74	0x74	1	Asset Tag T/L		fixed	binary, length 1	0x01
Product Info Area	117	117	0x75	0x75	1	Asset Tag		fixed	unused	0x00
Product Info Area	118	118	0x76	0x76	1	FRU File ID T/L		fixed	binary, length 1	0x01
Product Info Area	119	119	0x77	0x77	1	FRU File ID		fixed	FRU file version 1	0x01
Product Info Area	120	120	0x78	0x78	1	Custom product info area fields XYZ T/L	Product Base ClockIdentity	fixed	binary, length 8	0x08
Product Info Area	121	128	0x79	0x80	8	Custom product info area fields XYZ	Product Base ClockIdentity	computed	MCHP DUI: 00-A0-87 MCHP INTERNAL (1-bit format, 2-bit version, 5-bit family, 4-bit DPLL, 4-bit DNU) 0x00-A0-87-02-00-[redacted]	addr 0x80-7F-7E-7D-7C-7B-7A-79 e.g. 0x00-A0-87-02-00-[redacted]
Product Info Area	129	129	0x81	0x81	1	Custom product info area fields XYZ T/L	Sensor Part Number	fixed	8-bit ASCII + Latin 1, length 10	0xCA
Product Info Area	130	139	0x82	0x8B	10	Custom product info area fields XYZ	Sensor Part Number	part-specific	e.g. "MCP9808"	addr 0x82-83-84-85-86-87-88-89-8A-8B e.g. 0x4D-43-50-39-38-30-38-[redacted]
Product Info Area	140	140	0x8C	0x8C	1	Custom product info area fields XYZ T/L	Sensor I2C Address	fixed	binary, length 1	0x01
Product Info Area	141	141	0x8D	0x8D	1	Custom product info area fields XYZ	Sensor I2C Address	part-specific	b001'1001	0x19
Product Info Area	142	142	0x8E	0x8E	1	Custom product info area fields XYZ T/L	PLL Part Number	fixed	8-bit ASCII + Latin 1, length 10	0xCA
Product Info Area	143	152	0x8F	0x98	10	Custom product info area fields XYZ	PLL Part Number	part-specific	e.g. "ZL80132B"	addr 0x8F-90-91-92-93-94-95-96-97-98 e.g. 0x5A-4C-38-30-31-33-32-42-[redacted]
Product Info Area	153	153	0x99	0x99	1	Custom product info area fields XYZ T/L	PLL I2C Address	fixed	binary, length 1	0x01
Product Info Area	154	154	0x9A	0x9A	1	Custom product info area fields XYZ	PLL I2C Address	part-specific	b111'0001	0x71
Product Info Area	155	155	0x9B	0x9B	1	Custom product info area fields XYZ T/L	OCXO Part Number	fixed	8-bit ASCII + Latin 1, length 32	0xE0
Product Info Area	156	187	0x9C	0xBB	32	Custom product info area fields XYZ	OCXO Part Number	part-specific	e.g. "OX-2211-EAE-1090-10M0000000" e.g. "OX-2281-EAE-5000-10M000" e.g. "OX-2211-EAE-5000-10M0000000"	addr 0x9C-9D-9E-9F-A0-A1-A2-A3-A4-A5-A6-A7-A8-A9-AA-AB-AC-AD-AE-AF-B0-B1-B2-B3-B4-B5-B6-B7-B8-B9-BA-BB e.g. 0x4F-58-2D-32-32-30-31-2D-45-41-45-2D-35-30-30-30-2D-31-30-4D-30-30-30-30-20-20-20-20 e.g. 0x4F-58-2D-32-32-38-31-2D-45-41-45-2D-35-30-30-30-2D-31-30-4D-30-30-30-20-20-20-20-20-20-20-20 e.g. 0x4F-58-2D-32-32-31-31-2D-45-41-45-2D-35-30-30-30-2D-31-30-4D-30-30-30-30-30-30-30-30-20-20-20-20
Product Info Area	188	188	0xBC	0xBC	1	Custom product info area fields XYZ T/L	OCXO I2C Address	fixed	binary, length 1	0x01
Product Info Area	189	189	0xBD	0xBD	1	Custom product info area fields XYZ	OCXO I2C Address	part-specific	b101'0100	0x54
Product Info Area	190	190	0xBE	0xBE	1	Custom product info area fields XYZ T/L	OCXO nominal holdover duration (minutes)	fixed	binary, length 2	0x02
Product Info Area	191	192	0xBF	0xC0	2	Custom product info area fields XYZ	OCXO nominal holdover duration (minutes)	part-specific	holdover duration (minutes)	addr 0xC0-BF e.g. 0x00-F0 or 240 minutes e.g. 0x01-E0 or 480 minutes e.g. 0x01-E0 or 480 minutes
Product Info Area	193	193	0xC1	0xC1	1	Custom product info area fields XYZ T/L	OCXO nominal holdover phase error (nanoseconds)	fixed	binary, length 2	0x02
Product Info Area	194	195	0xC2	0xC3	2	Custom product info area fields XYZ	OCXO nominal holdover phase error (nanoseconds)	part-specific	holdover phase error (nanoseconds)	addr 0xC3-C2 e.g. 0x05-DC or 1500 ns e.g. 0x05-DC or 1500 ns e.g. 0x05-DC or 1500 ns
Product Info Area	196	196	0xC4	0xC4	1	Custom product info area fields XYZ T/L	OCXO nominal holdover temperature change (°C)	fixed	binary, length 1	0x01
Product Info Area	197	197	0xC5	0xC5	1	Custom product info area fields XYZ	OCXO nominal holdover temperature change (°C)	part-specific	holdover temperature change (°C)	e.g. 0x05 or 5 °C e.g. 0x03 or 3 °C e.g. 0x02 or 2 °C
Product Info Area	198	198	0xC6	0xC6	1	Custom product info area fields XYZ T/L	Input Clock Board Delay Array	fixed	binary, length 10	0x0A

1.19. Reset and Configuration Pins

- GPIO[0:4]_AC[0:4]
  - Please pay close attention to the use of SYNC_SCL, SYNC_SDA, and WRITE_EN because they are dual purpose with GPIO and impact start-up operation or configuration.
- SYNC_SCL and SYNC_SDA
  - SYNC_SCL and SYNC_SDA have pull-up resistors on the MD-990-0011 module
  - SYNC_SCL and SYNC_SDA have dual uses, as both I^2C bus and the power-up configuration of the M.2 module
  - SYNC_SCL and SYNC_SDA must be high on the rising edge of SYNC_RESET# for normal operation of the ZL80132B
  - SYNC_SCL and SYNC_SDA must be high on the rising edge of SYNC_RESET# for the firmware upgrade operation of the ZL80132B
  - The status of SYNC_SCLK and SYNC_SDA at the last SYNC_RESET# rising edge may be read from ZL80132B register 0x0019 bits 1:0
  - If SYNC_SCLK or SYNC_SDA at the last SYNC_RESET# are not high, the MD-990-0011 module will continue to work properly due to duplicate backups for combinations of 00, 01, and 10. These duplicate backups may be changed in the future revisions of the MD-990-0011 hardware.
- WRITE_EN
  - WRITE_EN has a weak pull-down resistor (12kΩ) on the MD-990-0011 module
  - WRITE_EN must be low on the rising edge of SYNC_RESET# for normal operation of the ZL80132B
  - WRITE_EN must be high on the rising edge of SYNC_RESET# for the firmware upgrade operation of the ZL80132B

1.20. Reprogramming Configuration Slots

Related to the "Reset and Configuration Pins" section about the selection of configurations slots within the ZL80132B. If the user reprograms the configuration slots, it is recommend to rewrite the slots #0 to #6 with the same data.

1.21. Power-Up Setup

Please note that the OCXO may move quickly during the first few minutes after power-up. For optimal fast lock of the PLL—due to automatic operation of the PLL immediately on power-up and quick selection of the best available reference by the PLL—the OCXO should be powered for three minutes prior to connecting input reference clocks or taking the PLL out of reset.

Otherwise, if the OCXO is not stable prior to PLL reference selection, the lock time may be significantly longer.

1.22. Pin Termination/Impedance/Assumption

- See the ZL80132B data sheet and configuration for how output drivers are configured in ZL80132B
- See the MD-990-0011 schematics for passive components on the input and output clock traces between the M.2 connector and the ZL80132B

2. Electrical and Environmental Characteristics

Table 2-1. Temperature Ranges

Parameter	Min.	Typ.	Max.	Units	Conditions
Operating Temperature Range	–40	—	+85	°C	—
Storage Temperature Range	–40	—	+125	°C	—

Table 2-2. Power

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	3.14	3.3	3.47	VDC	—
Power Consumption	—	—	1260	mA	At $V_{S(NOM)}$ and +25°C
	—	—	1560	mA	At $V_{S(NOM)}$ and –40°C
	—	—	1860	mA	During OCXO warm-up

Table 2-3. Environmental and Product Classification

Mechanical Shock	MIL-STD-202, Method 213B Condition C: 100g, 6ms, 6 shocks in each direction
Vibration Sine	JESD22-B103, Condition 2: 10g, 10Hz to 2000Hz 4x in each 3 axis 4 min. sweep time
Moisture Sensitivity Level	1
Temperature Cycling	JESD22-A104, Condition G: 1000 cycles, –40 to +125°C, cycle time 30 min.
High Temperature Operating Life	MIL-STD-202, Method 108A Condition C: 1000 hours @ +105°C under voltage
Low Temperature Operating Life	IEC 60068-2-1, Condition Ae: T_A = –40°C, >1000 hours with bias for OCXO
RoHS Compliance	EU-RoHS(2011/65/EU) + amendment RoHS3(2015/863)
FIT-Rate: $\lambda\ in$ 10^9 h	444
MTBF = 1/FIT	257 years

3. Mechanical Information

3.1. Outline Drawing and Enclosure

Figure 3-1. Enclosure Drawing

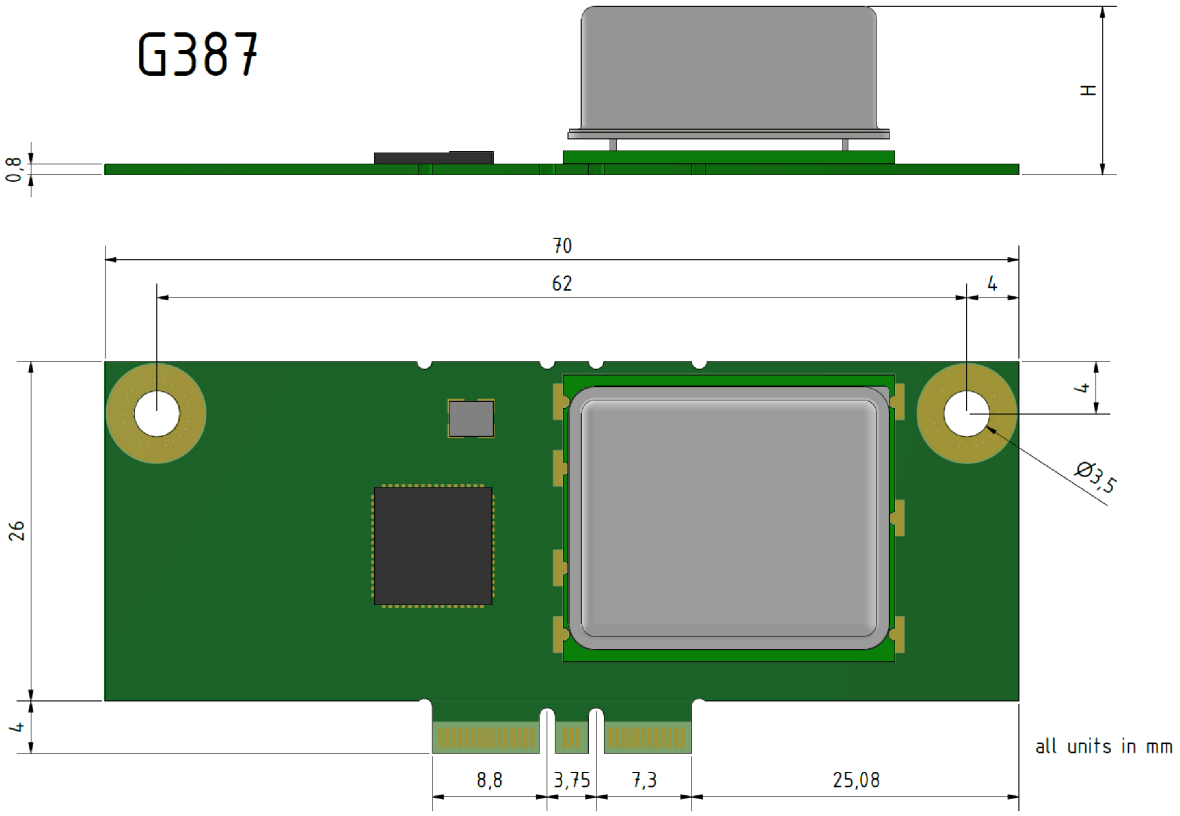


Table 3-1. Dimensions and Weight

Parameter	Value
Height	12.9mm ±0.35mm
Weight (MD-990-0011-AA01 & MD-990-0011-AC01)	14g

3.2. M.2 Connector Pinout

Table 3-2. M.2 Connector Pinout

Pin #	Signal	Signal	Pin #
74	3.3V	GND	75
72	3.3V	SMA2_OUT	73
70	SYNC_CLK_GD	AIC_CLK2	71
68	PRSNT#	GND	69
66	SYNC_RESET#	SYNC_CLK2_N	67
64	NC	SYNC_CLK2_P	65
62	NC	GND	63
60	SYNC_SCL	SYNC_CLK1_N	61
58	SYNC_SDA	SYNC_CLK1_P	59
56	NC	GND	57
54	NC	SYNC_CLK0_N	55
52	NC	SYNC_CLK0_P	53
50	NC	GND	51
48	NC	AIC_SCLK	49
46	Card Key-G	GND	47
44	Card Key-G	Card Key-G	45
42	Card Key-G	Card Key-G	43
40	Card Key-G	Card Key-G	41
38	GND	Card Key-G	39
36	SYNC_25M_N	NC	37
34	SYNC_25M_P	NC	35
32	GND	GND	33
30	Card Key-E	Card Key-E	31
28	Card Key-E	Card Key-E	29
26	Card Key-E	Card Key-E	27
24	Card Key-E	Card Key-E	25
22	1PPS_OUT1	1PPS_IN1	23
20	1PPS_OUT0	1PPS_IN0	21
18	GND	GNSS_1PPS_IN	19
16	1Hz_FREQ	SMA3_IN	17
14	SMA0_OUT	SMA1_IN	15
12	NC	NC	13
10	1PPS_OUT4	GNSS_10M_IN	11
8	1PPS_OUT3	WRITE_EN	9
6	1PPS_OUT2	GND	7
4	3.3V	RCLKA_IN	5
2	3.3V	RCLKB_IN	3
—	—	GND	1

4. Product Marking Information

4.1. Product Marking

Figure 4-1. Module Backside with Label

Table 4-1. Label Information

Product Name	MD-990-0011-Bxxx
Serial Number	MD: xxxx OX: yyyy
Date Code	AYYWW
Country of Origin	Made in Germany
Data Matrix Content	Product Name Serial Number, Module Serial Number, OCXO Date Code

4.2. Label Size

Figure 4-2. Sample Picture of the Label

4.3. Data Matrix Code Example

Figure 4-3. Data Matrix Code Example

The data matrix contains: Product Name; Module Serial Number; OCXO Serial Number, A Date Code.

Example: MD-990-0011-BC01;9;116;A2542

4.4. Shipping Information

Figure 4-4. Picture of Open Inner Box

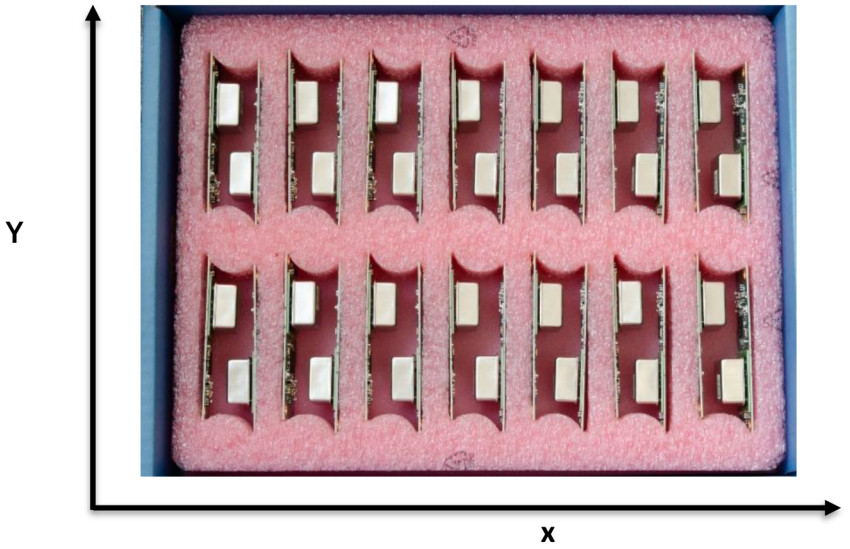


Table 4-2. Inner Box Dimensions

Quantity per Box	28 Units per box [14 (x) * 2 (y)]
Inner Size	250mm x 191mm x 64mm (L x W x H)
Outer Size	270mm x 200mm x 70mm (L x W x H)
Box Weight (28 modules per box, MD-990-0011-BA01; MD-990-0011-BC01)	530g
ESD Compliant	Yes
Recyclable	Yes

Table 4-3. Outer Box Dimensions

Quantity per Box	Up to 12 ESD boxes
Outer Size	400mm x 380mm x 400mm (L x W x H)
Recyclable	Yes

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Section	Description
DS00006363B	04/2026	Section 1.6	Corrected instances of “OX-2211-EAE-5000-10M000” to the full part number of “OX-2211-EAE-5000-10M0000000”.
		Section 1.7	
		Table 1-4	
		Figure 4-1, Figure 4-2	Updated image.
DS00006363A	02/2026	—	Initial Release of MD-990-0011-B - Microchip Timing Module for Data Center Servers

6. Product Identification System

XX	-XXX-XXXX	-X	X	XX	-XX
Product Family	Product Series	Chipset Version	Oscillator Model	Additional Function Code	Extended Warranty

Product Family:	MD = Module
Product Series:	990-0011 = Single populated board, 30mm x 40mm, including M.2 connector
Chipset Version:	B = ZL80132BLDG1Q0GT
Oscillator Model:	A = OX-2211-EAE-1090-10M0000000 C = OX-2211-EAE-5000-10M0000000
Additional Function Code:	01 = Standard
Extended Warranty:	<blank> = Standard 1 year warranty 02 = 1 year extended warranty 03 = 2 year extended warranty 04 = 3 year extended warranty

Table 6-1. Module Chipset/Oscillator Configuration

Chipset/Oscillator Version	Chipset	Oscillator	Holdover Performance	Performance Code
BA01	ZL80132BLDG1Q0GT	OX-2211-EAE-1090-10M0000000	1.5µs over 4 hours	Standard
BC01	ZL80132BLDG1Q0GT	OX-2211-EAE-5000-10M0000000	1.5µs over 8 hours	Standard

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