High-Performance, General Purpose PMIC for MPUs

MCP16503

General Description

The MCP16503 is an optimally integrated PMIC, for general purpose eMPUs (Embedded Microprocessor Units), requiring Dynamic Voltage Scaling (DVS). The regulators' Start-up voltages are adjustable using selection resistors, and the regulators can be fully adjusted by using I^2C. The MCP16503 integrates four DC-DC Buck regulators and two auxiliary LDOs, and provides a comprehensive interface to the MPU, which includes an interrupt flag and a 1 MHz I^2C interface.

All Buck channels can support loads up to 1A and are 100% duty cycle capable. Two 300 mA LDOs are provided such that sensitive analog loads can be supported. Unlike MCP16502, the MCP16503 comes with a simple logic level EN pin, which simplifies the start-up procedure, being able to start even when the input voltage ramps slowly or when the input voltage is unstable and suddenly drops below UVLO. After the initial Start-up, the PMIC can be shutdown and started by the MPU, using the PWRHLD pin. This method allows greater precision in the output voltage setting by eliminating inaccuracies due to external feedback resistors while minimizing external component count. The voltage selection set allows easy migration across different generations of memory. The default power channel sequencing is built-in according to the requirements of the MPU, starting from buck1 and LDOx, buck2, buck3, and buck4. A dedicated pin (LPM) facilitates the transition to Low-Power mode and the implementation of Backup mode with DDR in self-refresh (Hibernate mode). The MCP16503 features a low no-load operational quiescent current and it draws less than 10 µA in full shutdown. Active discharge resistors are provided on each output. All Buck channels support safe start-up into pre-biased outputs. The MCP16503 is available in a 32-pin 5 × 5 mm VQFN package with an operating junction temperature range from −40°C to +125°C.

Features

- Input Voltage: 2.7V to 5.5V
- Four 1A Output Current Buck Channels with 100% Maximum Duty Cycle Capability
- 2MHz Buck Channels PWM Operation
- Two Auxiliary 300mA Low Dropout Linear Regulators (LDOs)
- ±1 Voltage Accuracy Suitable to Power the DDR, Core and CPU Voltage Rails
- Resistor Selectable Output Voltage for the Default Start-up
- I^2C Output Voltage Configuration Following System Startup (DVS)
- Adjustable Output Voltage from 0.6V to 1.85V (Only for buck2, buck3 and buck4)
- Adjustable Output Voltage from 1.2V to 3.7V (Only for buck1, LDO1 and LDO2)
- Shutdown Input Pin (EN)
- MPU-specific Built-in Default Channel Sequencing and nRSTO Assertion Delay
- Support of MPU Hibernate, Low-Power and High-Performance Modes with DVS
- 1MHz I^2C Interface for Programming and Diagnostics
- Low Noise, Forced PWM (FPWM) and Low IQ, Light Load, High-efficiency Mode Available
- I^2C-selectable Displacement (±16.5%) of PWM Switching Frequency
- Leakage-free Interfacing to MPU in Any Operating Condition through Optimized ESD Protection

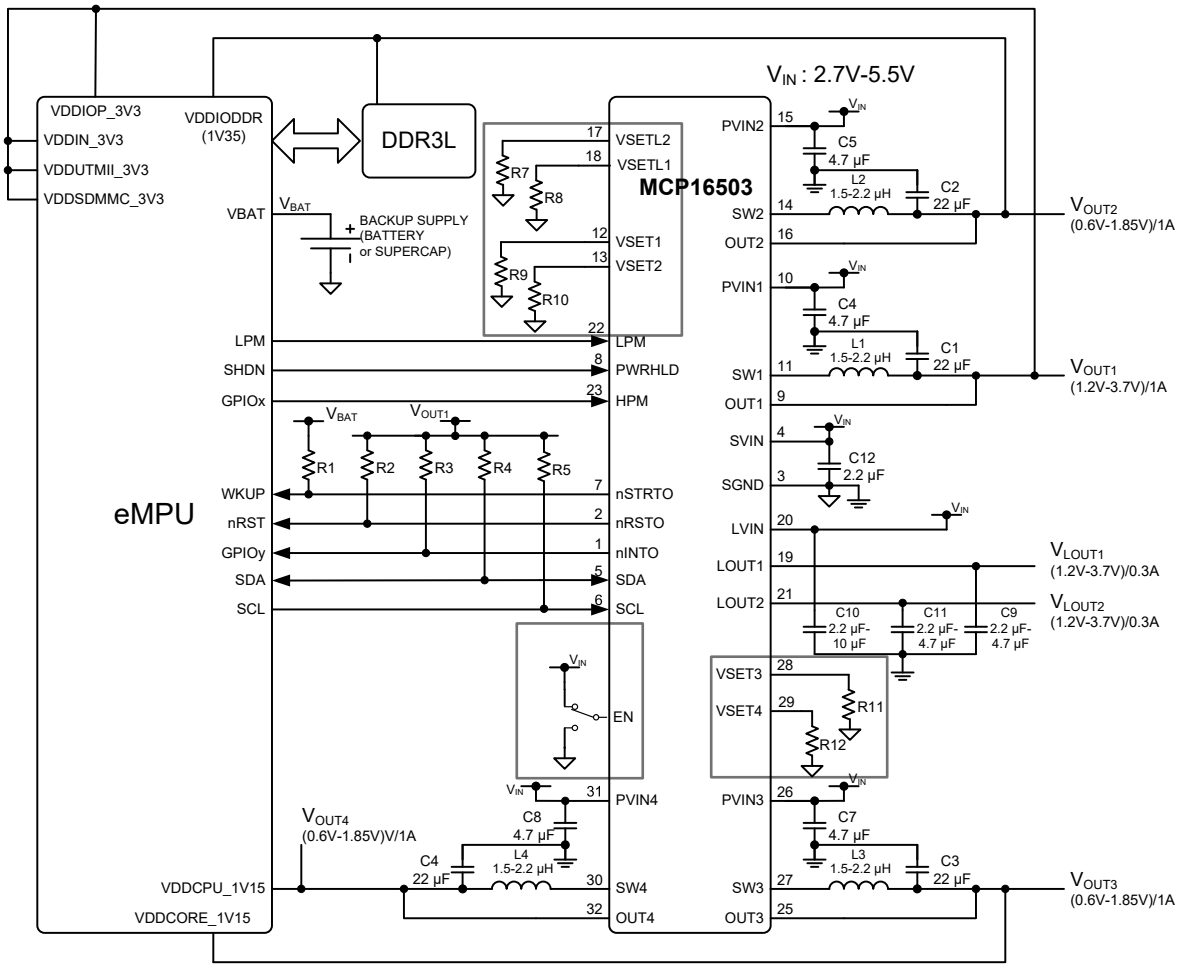
- Less than 300µA Low-power Mode Typical Quiescent Current Bucks and LDO1 ON, No Load
- 10µA Maximum Shutdown Current (V_{IN} = 4.5V, T_J = +105°C)
- Cost and Size-optimized BOM
- Thermal Shutdown and Current Limit Protection
- User-programmable Overcurrent Fault Response
- 32-Pin 5mm × 5mm VQFN Package
- −40°C to +125°C Junction Temperature Range

Applications

- High-performance, General Purpose MPUs
- µC/µP, FPGA and DSP Power

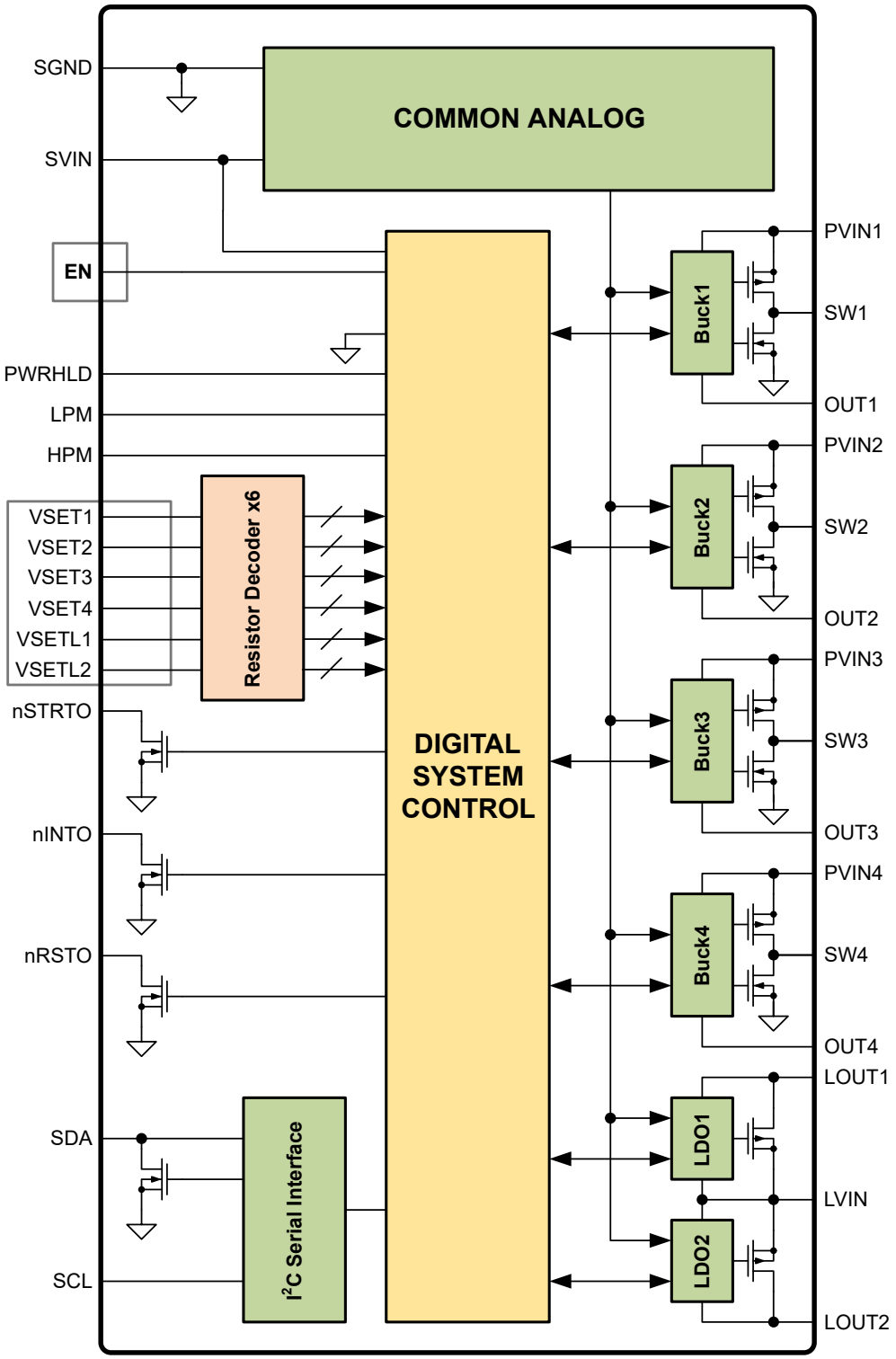
Typical Application

Figure 1. MCP16503



Functional Block Diagram

Figure 2. MCP16503



1. Pin Descriptions

Pin Number	Pin Name	Pin Function
1	nINTO	Active low, open-drain interrupt output.
2	nRSTO	Active low, open-drain reset output.
3	SGND	Signal ground. Connect to reference ground plane.
4	SVIN	Input voltage for the analog control circuitry. Decouple SVIN to SGND with a 1µF (minimum) ceramic capacitor.
5	SDA	I^2C interface serial data.
6	SCL	I^2C interface serial clock.
7	nSTRTO	Active low, open-drain START event output. The nSTRTO signal is asserted LOW whenever the EN is detected to be HIGH.
8	PWRHLD	Power hold input. Typically asserted high by the MPU to maintain power after the initial startup triggered by EN. PWRHLD will be asserted low by the MPU to initiate a PMIC shutdown sequence.
9	OUT1	Output sensing for buck channel 1. Connect to the regulation point for V_{OUT1}.
10	PVIN1	Power input voltage of buck channel 1. Connect a ceramic capacitor from PVIN1 to ground, to localize pulsed currents loops and decouple switching noise.
11	SW1	Switch node of buck channel 1. Internal power MOSFET switches and external inductor connection.
12	VSET1	Connect a resistor on this pin to ground to define the start-up voltage of the buck channel 1.
13	VSET2	Connect a resistor on this pin to ground to define the start-up voltage of the buck channel 2
14	SW2	Switch node of buck channel 2. Internal power MOSFET switches and external inductor connection.
15	PVIN2	Power input voltage of buck channel 2. Connect a ceramic capacitor from PVIN2 to ground, to localize pulsed currents loops and decouple switching noise.
16	OUT2	Output sensing for buck channel 2. Connect to the regulation point for V_{OUT2}.
17	VSETL2	Connect a resistor on this pin to ground to define the start-up voltage of the LDO2.
18	VSETL1	Connect a resistor on this pin to ground to define the start-up voltage of the LDO1.
19	LOUT1	LDO1 output. Decouple LOUT1 to ground with a 2.2µF (minimum) ceramic capacitor.
20	LVIN	Input voltage for LDO1 and LDO2. Decouple LVIN to ground with a 2.2µF (minimum) ceramic capacitor.
21	LOUT2	LDO2 output. If LDO2 is in use, decouple LOUT2 to SGND with a 2.2µF (minimum) ceramic capacitor.
22	LPM	Low-power mode input pin. In combination with PWRHLD and HPM, this pin defines the power mode status of the MCP16503.
23	HPM	High-performance mode input pin. In combination with PWRHLD and LPM, this pin defines the power mode status of the MCP16503. Connect to ground if not used.
24	EN	Enable input. Drive EN high to initiate a start-up sequence at power up or after a power down triggered by EN.
25	OUT3	Output sensing for buck channel 3. Connect to the regulation point for V_{OUT3}.
26	PVIN3	Power input voltage of buck channel 3. Connect a ceramic capacitor from PVIN3 to ground, to localize pulsed currents loops and decouple switching noise.
27	SW3	Switch node of buck channel 3. Internal power MOSFET switches and external inductor connection.
28	VSET3	Connect a resistor on this pin to ground to define the start-up voltage of the buck channel 3.
29	VSET4	Connect a resistor on this pin to ground to define the start-up voltage of the buck channel 4.

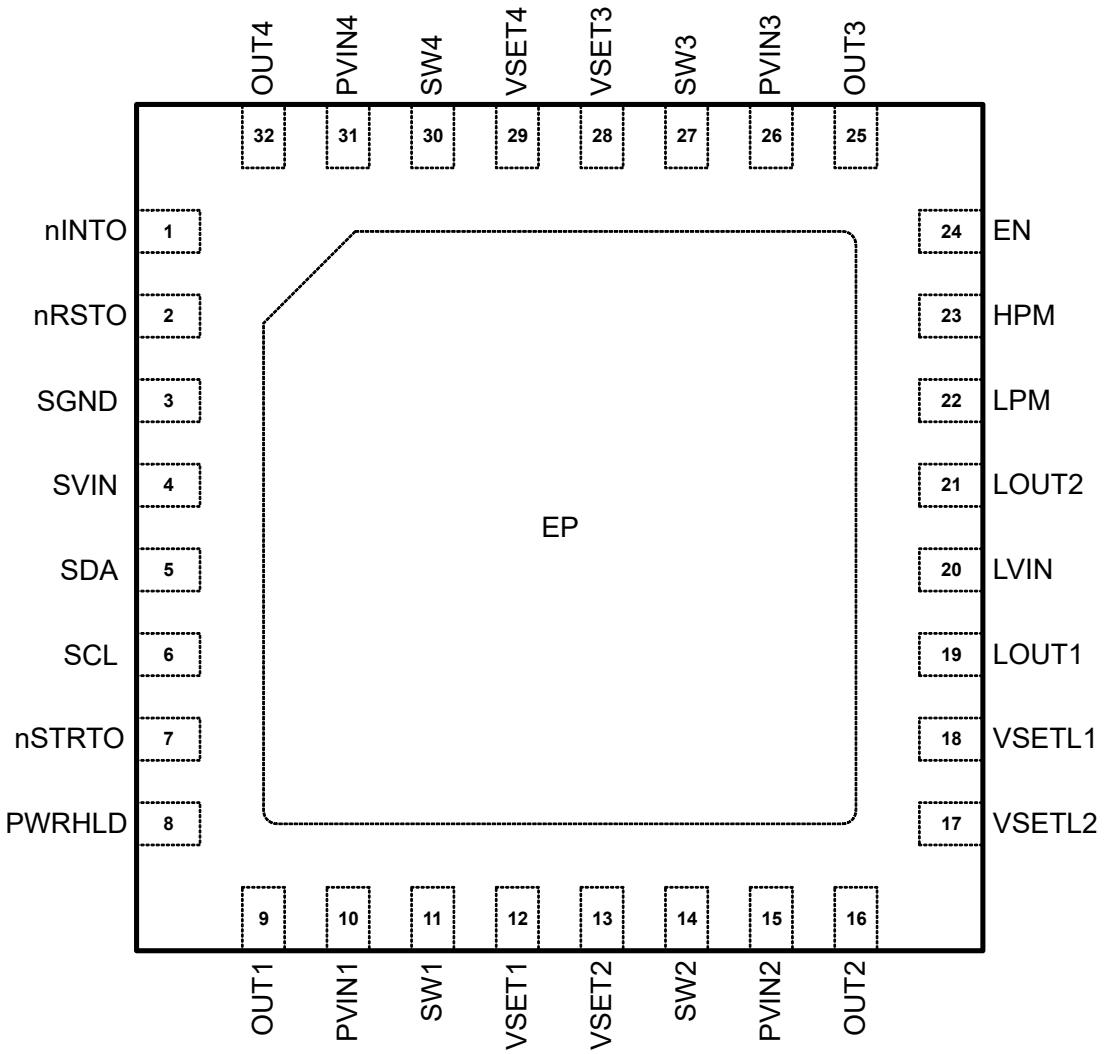
Pin Descriptions (continued)

Pin Number	Pin Name	Pin Function
30	SW4	Switch node of buck channel 4. Internal power MOSFET switches and external inductor connection.
31	PVIN4	Power input voltage of buck channel 4. Connect a ceramic capacitor from PVIN4 to ground, to localize pulsed currents loops and decouple switching noise.
32	OUT4	Output sensing for buck channel 4. Connect to the regulation point for V_{OUT4}.
—	EP	Exposed pad (ePad). Connect to ground plane with vias to ensure good thermal properties.

Note: The PVINx pins, SVIN pin and the LVIN pin shall be supplied from the same input voltage rail.

1.1. Package Type

Figure 1-1. MCP16503 Pinout Configuration (32-pin, 5 × 5 mm, VQFN – Top View)



2. Functional Description

2.1. Buck Channels and Related External Components

The MCP16503 buck channels are based on peak-current-mode control architecture and have internal frequency compensation for the voltage regulation loop. The slope compensation is optimized for inductors in the 1.5µH to 2.2µH range. A minimum output capacitor of 22µF is required for stable operation. Output capacitance can be increased if necessary, however the maximum output capacitance value should be limited to avoid engaging hiccup-mode overcurrent protection during the initial soft-start ramp and during DVS operation. Further details are given in section Maximum Simultaneous Capacitive and DC Loading in Soft-Start and DVS

The buck channels of the MCP16503 also feature a negative inductor current limit protection when operating in forced PWM mode. This prevents dangerous current levels in the power train. If the inductor current reaches the low-side negative peak current limit (I_{LIM_NEGx}) while the low-side MOSFET is conducting, the low-side MOSFET is turned off and the inductor current is pushed to the input voltage, either through the body diode of the high-side MOSFET (if OFF) or its channel (when turned ON by the control loop). Since this feature is only intended to protect the device in some particular transient conditions (such as a large decrease of the output voltage setting associated with an extremely large capacitive load), it is only reported through I^2C, but it does not cause the assertion of the nRSTO (RESET) signal.

This protection should never be exercised continuously and/or without a very large bulk capacitor, because it may quickly destroy the device.

When this protection is engaged, energy is pumped back from the output into the input voltage. If the input supply has no sinking capability and/or the input bulk decoupling cap is not large enough, the input voltage will rise to the point where the device is permanently damaged.

LDOs are protected against short-circuits by a linear constant-voltage, constant-current (i.e., brick-wall) output characteristic. The output current under short-circuit conditions is not intermittent. Therefore, the internal power dissipation in the MCP16503 can reach high levels under LDO short-circuit conditions. The current limit condition of each LDO is also reported through I^2C. The intervention of the LDO current limit protection does not cause the assertion of the nRSTO (RESET) signal.

The recommended input decoupling capacitance on each buck channel is 4.7µF.

The buck channels can operate either in forced PWM mode (continuous inductor current mode), where the inductor current is allowed to go negative, or in automatic PFM mode, where the inductor current is not allowed to go negative through zero-current detection (ZCD) and diode emulation of the low-side MOSFET.

The switching frequency in forced PWM mode is nominally 2MHz and can be displaced through I^2C by ±16.5% to prevent interference with other sensitive system blocks.

Recommended part numbers are given in section Recommended External Components.

2.2. LDO Channels and Related External Components

The MCP16503 LDOs are designed for operation with low-ESR ceramic output capacitors of 2.2 µF (minimum value) for loads up to 150 mA, and of 4.7 µF (minimum value) for loads up to 300 mA. The total rail capacitance should not exceed 50 µF.

The LDOs can be used with an input voltage (V_{LVIN}) less or equal to the voltage at pin SVIN. As such, they can operate as post-regulators cascaded to a buck channel output, if its output voltage is programmed above 2.7V.

Recommended capacitors part numbers are given in section Recommended External Components.

2.3. Control Signals and Power States

2.3.1. Interfacing Signals

The MCP16503 is interfaced to the host MPU by means of the following signals: nSTRTO (open-drain output), nRSTO (open-drain output), nINTO (open-drain output), PWRHLD (input), LPM (input) and HPM (input). SDA and SCL are I^2C interface pins. The MCP16503 is a target-only device without clock-stretching capability and therefore the SCL pin is an input only. Further details about the I^2C interface of the MCP16503 are given in section I^2C Interface Description.

The ESD protection on each interfacing signal is purposely designed to prevent any leakage from the MPU IOs, even in the case where the main input power is removed from the MCP16503.

2.3.2. EN, nSTRTO, PWRHLD Functionality

After a Power-On Reset (POR), when the EN pin is detected HIGH, the MCP16503 initiates the power-up sequence and transitions to Start-up mode.

Once the first power-up sequence is successfully completed, an internal status bit PSEQ_DONE is set. This bit indicates that the PMIC has completed its start-up sequence.

After PSEQ_DONE is set, the EN pin HIGH alone will no longer trigger a transition to Start-up mode. From this point onward, startup and shutdown operations can be controlled using the PWRHLD pin.

The PSEQ_DONE bit is cleared only under the following conditions:

- The device is power cycled.
- The EN pin goes LOW and the defined timeout expires (please refer to Power-Up/Power-Down/HIBERNATE Sequences and Timings).
- The EN pin is LOW while the IC is in OFF mode.

The PSEQ_DONE bit is set when all regulators enabled during the start-up sequence have successfully ramped up, which occurs at the end of time t_4, as shown in EN Power Start-up Scenario: EN Short to VIN.

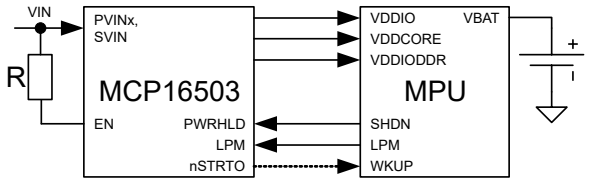
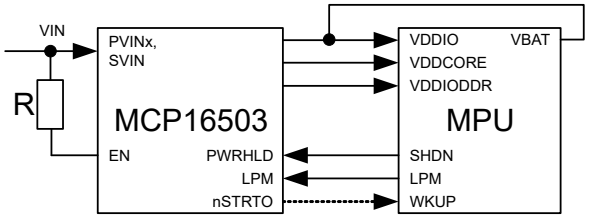
nSTRTO signal is asserted LOW whenever the EN is detected to be HIGH and t_1 is not expired. In case t_1 is configured to be 0, nSTRTO is asserted LOW for 10 µs as long as EN pin is detected HIGH. The pin is high-Z otherwise (typically nSTRTO has an external pull-up resistor). The only exception to this input (EN) /output (nSTRTO) relationship is the so-called Automatic Wake-Up Pulse (AWKP). Please refer to section Restart Aequence After Fault During HIBERNATE: Automatic Wake-up Pulse (AWKP) Generation for the detailed timing diagram.

After the start-up sequence has been initiated, MCP16503 expects the assertion of the PWRHLD signal (Power-Hold) from the MPU to validate the sequence.

PWRHLD could be already HIGH in a typical application using a backup supply. If PWRHLD has NOT been asserted HIGH by the MPU before the completion of the start-up sequence (i.e. when nRSTO is about to be asserted high), the MCP16503 will automatically initiate a turn-off sequence.

2.3.3. EN/PWRHLD Typical Use Cases

Depending on the presence of a Back-Up supply, two different scenarios can be defined for the turn-on of the MCP16503, as described in the following table.

Applications With a Backup Bupply	Applications Without a Backup Supply
 The application starts when VIN ramps up above the UVLO threshold as the EN pin is pulled up to VIN. Note that PWRHLD (= SHDN from MPU) was set to 1 at the time the battery was mounted on the PCB, i.e. at the time of manufacturing. The power channels of MCP16503 are turned off by the MPU by setting SHDN = 0. The MPU is then in backup mode. If supported, the DDR can also be placed in backup self-refresh mode (BSR) by setting LPM = 1 before SHDN = 0. To wake up the application from backup mode, a wake-up event must be generated for the SHDWC (Shutdown and Wake-Up Controller) of the MPU. This can be an internal event (e.g. RTC, RTT alarm, TAMPER detection) or an event on a I/O of the SHDWC (e.g. wake-up from a wireless module). The MPU will then set SHDN = 1 and the low-to-high transition of PWRHLD will cause the MCP16503 to restart. If VIN is cycled while the MPU is in backup mode (SHDN=0), the MCP16503 restarts automatically and sends a wake-up event to the MPU on nSTRTO (WKUP). If this wake-up event was not enabled in the MPU SHDWC configuration, SHDN will stay low and the MCP16503 will turn off at the end of the start-up sequence, because PWRHLD has not been set high. If this wake-up event was enabled, SHDN will immediately go high thus confirming the start-up sequence for the MCP16503, and the application will restart.	 The application starts when VIN ramps up above the UVLO threshold as the EN pin is pulled up to VIN. PWRHLD (= SHDN from MPU) is set to 1 as soon as VBAT (= VDDIO) is above its internal POR threshold (around 1.5V). The power channels of MCP16503 are turned off by the MPU by setting SHDN = 0. In this case, the MPU is NOT in backup mode, it is simply completely OFF. Hibernate mode cannot be used because PWRHLD cannot be set to 0. Doing so would cause the PMIC to shut down and it would not restart, as the battery is not present. Without the battery, the VBAT voltage drops to 0 V immediately after the PMIC shuts down. From the OFF state, the application can only be restarted by cycling power on VIN.

PWRHLD, LPM and HPM define different power states which are illustrated in the following Table 2-1. These are default definitions for the targeted typical application scenario of an MPU when powering DDR memories and therefore may be different for other application configurations.

The logic value of HPM input pin is masked (seen by the internal logic as “0”) until a specific I^2C command is issued (HPMPEN bit must be set to “1”) only after PSEQ_DONE bit is set and start-up sequence is completed. The reason is the HPM is a generic GPIO, whose status at the MPU power-up time could be undefined. The HPMPEN bit is reset only through power cycling or an EN pin high to low transition in OFF mode.

After the software has issued the unmask HPM command through I^2C, it is safe to assume that the HPM status is well defined and the HPM signal can be used to enter/exit High-Performance Mode. All the following power states assume that EN is already HIGH.

Table 2-1. Default Power States Definition

PWRHLD	LPM	HPM	Buck1	Buck2	Buck3	Buck4	LDO1	LDO2	nRSTO	Power State
0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	LOW	OFF
0	1	0	OFF	ON Auto PFM	OFF	OFF	OFF	OFF	LOW	HIBERNATE
1	1	0	ON Auto PFM	ON Auto PFM	ON Auto PFM	ON Auto PFM	ON	ON	High-Z	Low-Power Mode
1	0	0	ON FPWM	ON FPWM	ON FPWM	ON FPWM	ON	ON	High-Z	Active
1	0	1	ON FPWM	ON FPWM	ON FPWM	ON FPWM	ON	ON	High-Z	High-Performance Mode

Other logic combinations of PWRHLD, LPM and HPM (after HPM unmasking) are forbidden.

The initial state is the OFF state (shutdown).

The process by which the MCP16503 abandons the OFF state and enters the other possible power states is defined as the Power-Up Sequence, which is described in the relevant section Typical Power-Up Sequence and Timing.

The following state diagram shown in Figure 2-1 illustrates the power states of MCP16503 and their typical and/or permissible dynamic transitions. **Special care must be taken when performing power mode transitions**, as the PMIC supports different output voltage levels in each mode. During a transition from OFF to Low-Power mode, the device **necessarily passes through Active mode**, causing the output voltage to first rise to the voltage configured for Active mode. The device then transitions to Low-Power mode, during which the output voltage changes again to the voltage configured for Low-Power mode. **If the voltage settings for Active and Low-Power modes differ, this results in multiple output voltage changes during the transition, which must be carefully considered during system design.**

2.3.4. Power Channel Default Start-up Voltage

In MCP16503, the default start-up voltage of all power channels can be configured through pin VSETx and VSETLy. By connecting a resistor on those pins against ground, or shorting the pins to ground or SVIN, 16 start-up voltage options can be configured for each channel. The table below shows an overview of all configurations. The option “short the pin to ground” is reserved for disabling the corresponding power channel in a start-up sequence. The other 15 options define 15 different start-up voltages. The PMIC only reads (decodes) the resistors connected to the VSETx and VSETLx pins during power-up. After start-up, the user can then change the output voltage through I^2C (see section VSET[5:0] Codes Definition).

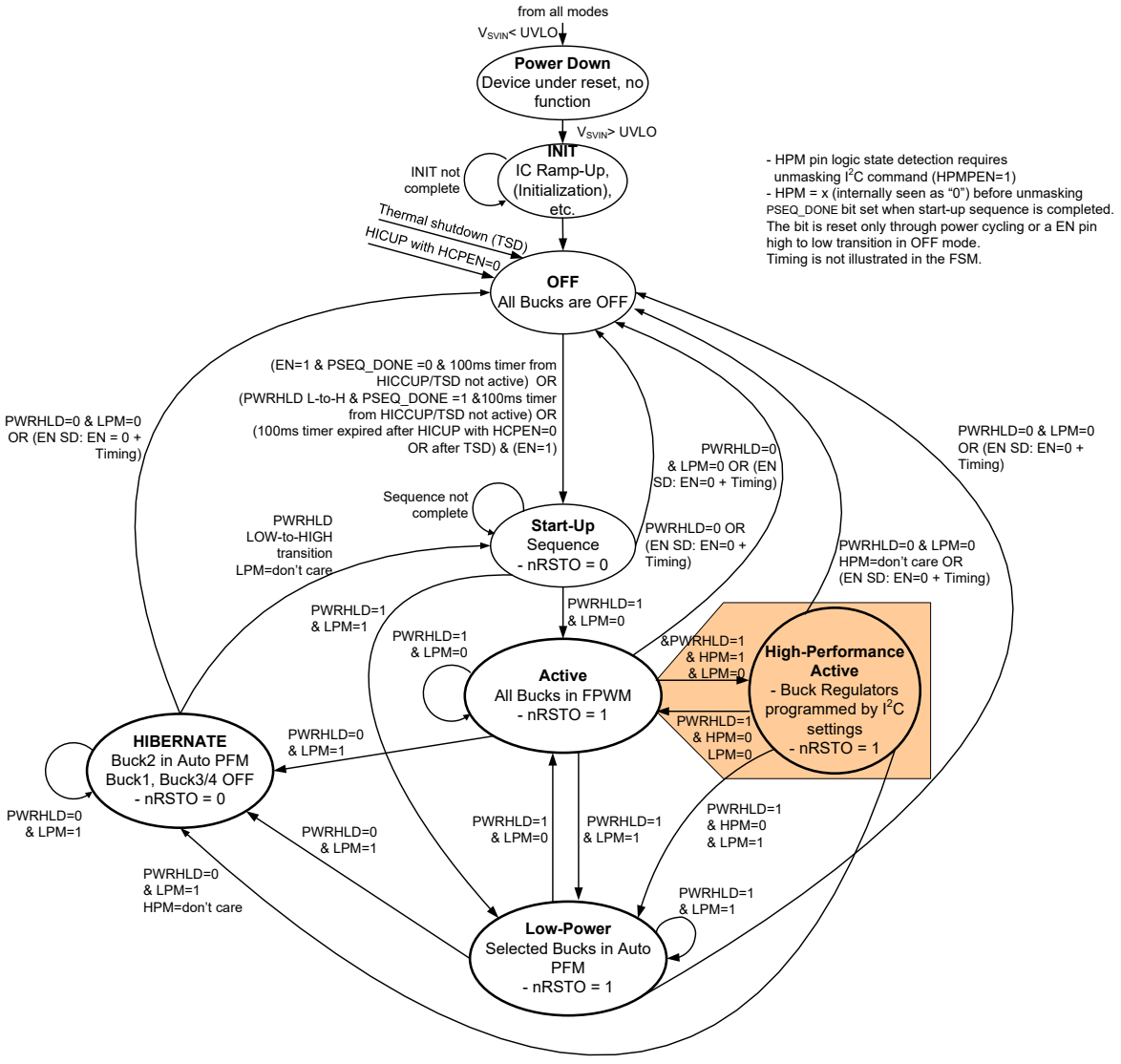
Table 2-2. Configuring MCP16503 Default Start-Up Voltage

R (Ω)	BCK1	BCK2	BCK3	BCK4	LDO1	LDO2
Short to GND	Disabled during sequencing					
187	1.2V	0.6V	0.6V	0.6V	1.2V	1.2V
487	1.25V	0.8V	0.8V	0.8V	1.25V	1.25V
976	1.3V	0.9V	0.9V	0.9V	1.3V	1.3V
1740	1.35V	1V	1V	1V	1.35V	1.35V
2940	1.4V	1.05V	1.05V	1.05V	1.4V	1.4V
4870	1.5V	1.1V	1.1V	1.1V	1.5V	1.5V
8060	1.6V	1.15V	1.15V	1.15V	1.6V	1.6V
13000	1.8V	1.2V	1.2V	1.2V	1.8V	1.8V

Table 2-2. Configuring MCP16503 Default Start-Up Voltage (continued)

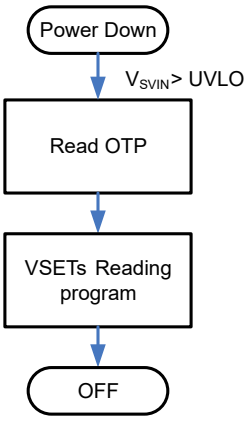
R (Ω)	BCK1	BCK2	BCK3	BCK4	LDO1	LDO2
21000	2.5V	1.25V	1.25V	1.25V	2.5V	2.5V
34000	2.8V	1.275V	1.275V	1.275V	2.8V	2.8V
54900	3.0V	1.35V	1.35V	1.35V	3.0V	3.0V
86600	3.15V	1.375V	1.375V	1.375V	3.15V	3.15V
140000	3.3V	1.4V	1.4V	1.4V	3.3V	3.3V
226000	3.4V	1.5V	1.5V	1.5V	3.4V	3.4V
Short to SVIN	3.6V	1.8V	1.8V	1.8V	3.6V	3.6V

Figure 2-1. Finite State Machine (FSM) States Diagram for MCP16503



The figure below illustrates a simplified flow chart for INIT mode.

Figure 2-2. INIT Mode Simplified Flow Chart



The identified default start-up voltage configurations are memorized in the corresponding VSET[5:0] registers in OUTx-A, LDOx-A registers and copied into VSET[5:0] in OUTx-LPM, OUTx- HIB, OUTx-HPM, LDOx-LPM, LDOx- HIB and LDOx-HPM.

2.3.5. nINTO (Interrupt Output) Pin

Pin nINTO is an active-low, open-drain Interrupt output pin. The nINTO pin goes low every time a fault is detected, and the corresponding Interrupt masking bit is cleared.

By default, all Interrupt generating events are masked (xxxMSK bits are “1” by default) and the end user needs to unmask those to enable Interrupt generation on faults.

Only one Interrupt generation event is always enabled and cannot be disabled. The Enable (EN) timeout described in section Typical Power-Down Sequence and Timing also shows this.

2.3.6. nRSTO (RESET Output) Pin

Pin nRSTO is an active-low, open-drain output pin that keeps the MPU in RESET state. The nRSTO pin is released (i.e. goes High-Z) with a programmable delay upon successful completion of a Start-Up Sequence. The RESET delay is programmable over a wide range of values, as shown in section Reset Assertion Delay (t_4) Programming Bits, and the default is 4 ms. nRSTO is immediately asserted low when either the SVIN voltage falls below the UVLO threshold, or a fault condition is detected at system level (such a Thermal Shutdown) or an overcurrent condition is detected on the Buck channels. Please see section Protections for more details on the faults that would cause the nRSTO signal low assertion. nRSTO goes also low when the HIBERNATE mode is entered.

2.4. Power-Up/Power-Down/HIBERNATE Sequences and Timings

2.4.1. Typical Power-Up Sequence and Timing

The start-up sequence can be initiated in two different ways, also depending on the presence of a back-up supply in the application:

1. **EN event (EN pin pulled HIGH) with PSEQ_DONE bit cleared, maintained by PWRHLD assertion**
   In applications with backup battery, the PWRHLD signal is typically already high before the EN event.
2. **A low-to-high transition of the PWRHLD signal with PSEQ_DONE bit set**, regardless of the EN event. This is only possible in applications with backup supply. This mode is typically originated by an external wake-up event asserted by a peripheral device to the MPU Shutdown and Wakeup Controller (SHDWC), which is still powered in backup mode.

Note that the event 1 and 2 needs the assertion of PWRHLD to have the power-up sequence completed successfully. If PWRHLD is not yet HIGH at the time nRSTO is supposed to be asserted, the PMIC automatically initiates a turn-off sequence, without any positive glitches on nRSTO.

Delay t_1 acts as a de-bouncing delay of the EN event. Therefore, EN must be detected HIGH continuously during t_1 to validate the start-up event and initiate the first sequence step. EN pin shall stay high, otherwise it can trigger a power down sequence when timing condition is fulfilled. Please refer to the next section for the details.

The following timing diagrams show the typical sequence for the first case:

Figure 2-3. EN Power Start-up Scenario: EN Short to VIN

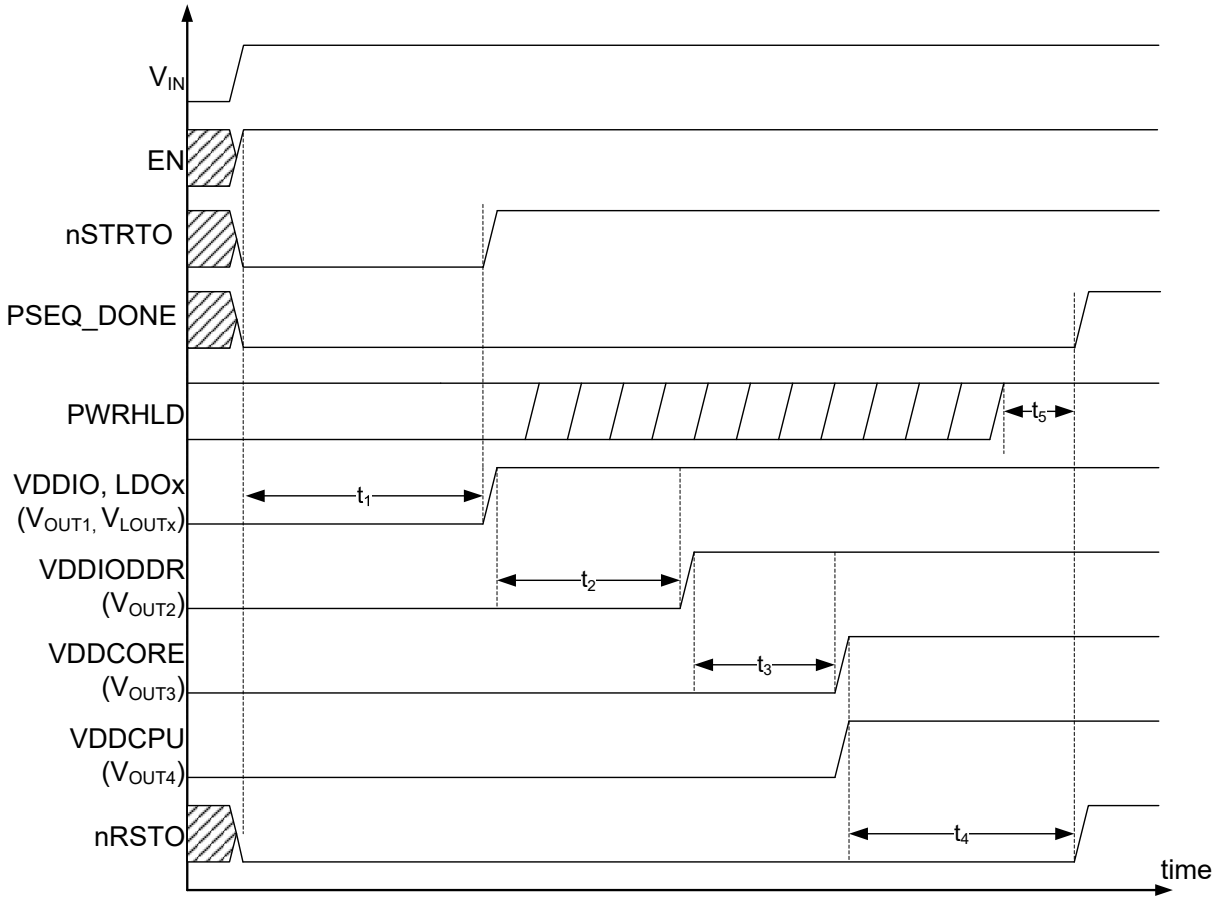
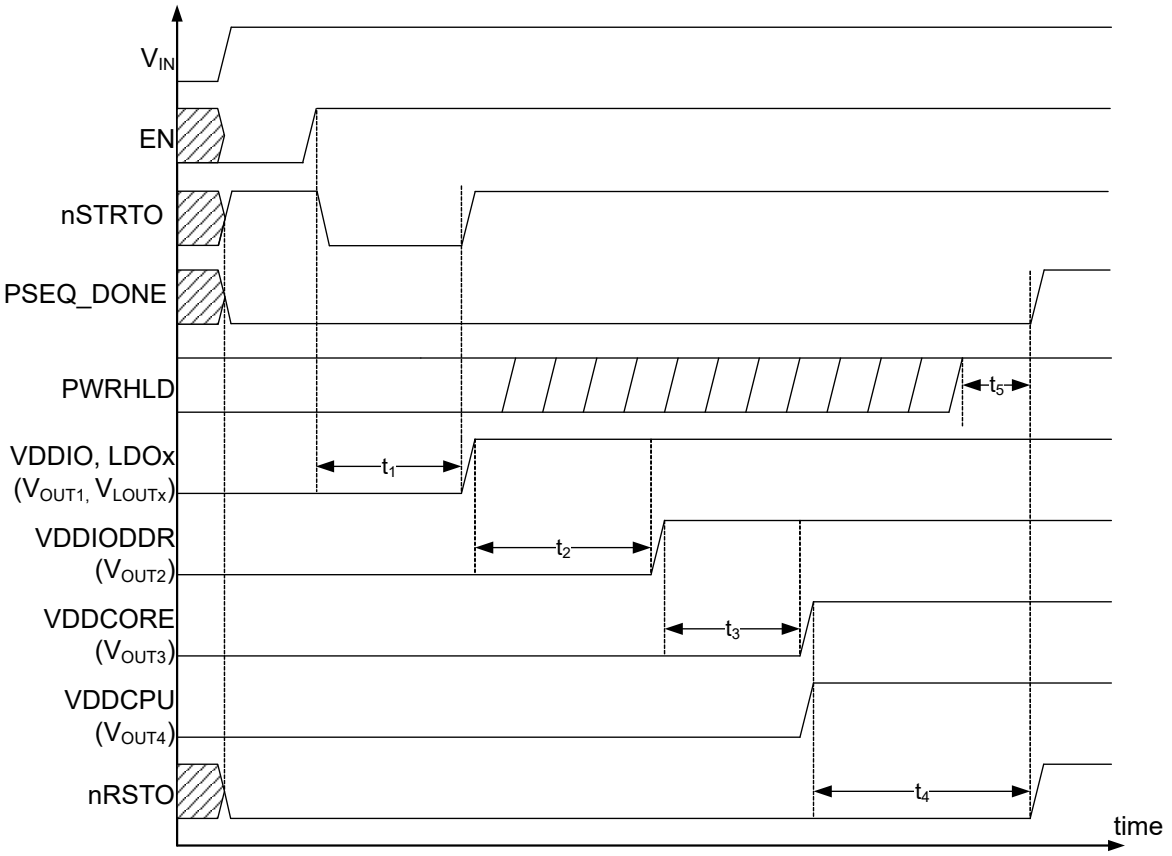


Figure 2-4. EN Power Start Scenario: EN Delayed



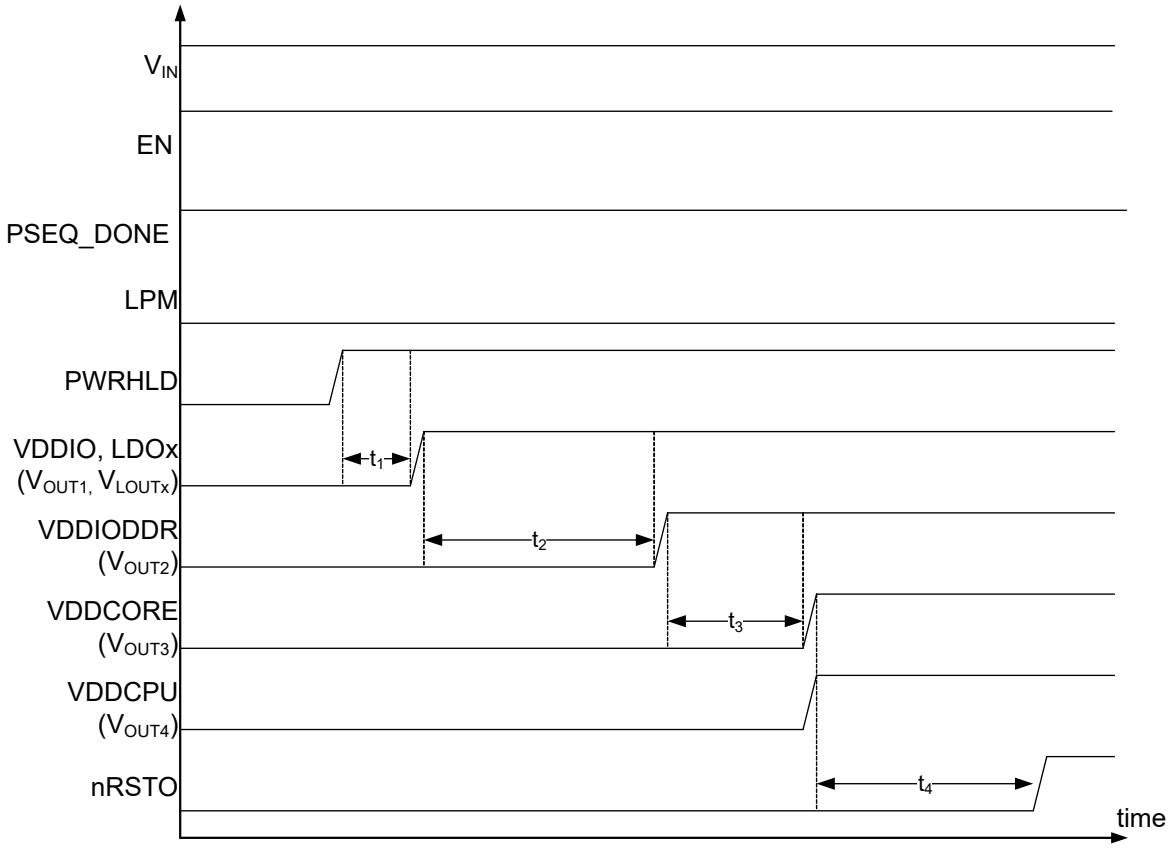
Where:

- t_1 = delay from EN rising to first output, V_{OUT1} starting (SEQ[1:0] = 00, default DELAY[2:0] = 001 i.e. 0.5 ms + device wake-up time)
- t_2 = time from V_{OUT1} established to V_{OUT2} starting (SEQ[1:0] = 01, default DELAY[2:0] = 101 i.e. 8 ms)
- t_3 = time from V_{OUT2} established to V_{OUT3}, V_{OUT4} starting (SEQ[1:0] = 10, default DELAY[2:0] = 100 i.e. 4 ms)
- t_4 = time from V_{OUT3} established to nRSTO de-assertion (default RSTDLY[2:0] = 100 i.e. 16 ms)
- t_5 = setup/hold times, min. 0 ms (internal filtering applies)
- “established” means the relevant power channel POK bit has gone HIGH
- t_1 to t_3 are programmable through DELAY[2:0] bits, t_4 is programmable through RSTDLY[2:0] bits

For power supplies starting at t_1, the DELAY[2:0] value is the additional delay time interval added to the minimum achievable wake-up time.

The following timing diagram of Figure 2-5 shows the typical sequence for the second case:

Figure 2-5. Start-Up From PWRHLD Timing Diagram



Where:

- t_1 = delay from PWRHLD asserted to first output V_{OUT1} starting (SEQ[1:0] = 00, default DELAY[2:0] = 001 i.e. 0.5 ms + device wake-up time)
- t_2 = time from V_{OUT1} established to V_{OUT2} starting (SEQ[1:0] = 01, default DELAY[2:0] = 101 i.e. 8 ms)
- t_3 = time from V_{OUT2} established to V_{OUT3}, V_{OUT4} starting (SEQ[1:0] = 10, default DELAY[2:0] = 100 i.e. 4 ms)
- t_4 = time from V_{OUT3} established to nRSTO de-assertion (default RSTDLY[2:0] = 100 i.e. 16 ms)
- “established” means the power channel POK bit has gone HIGH

For all the sequences described above, LPM can be assumed to be LOW. The MPU will assert LPM after some time, based on software decision, to enter the Low-Power modes.

2.4.2. Power-up Sequence Programming and Flowchart

The power-up sequence management is flexible enough to accommodate other Power-Up sequences than the typical one.

The start-up sequence is divided into three steps, and each regulator (Bucks and LDOs) is included in the start-up sequence ONLY if its SEQEN bit is set. Each regulator is then assigned to a specific sequence step:

1. (SEQ[1:0] = 00): enabled (bit SEQEN = 1) regulator(s) are started after a delay (t_1) since the start-up event. If the start-up event is no longer valid at the instant t_1 expires, the start-up sequence is aborted before the first regulator is started;
2. (SEQ[1:0] = 01): enabled (bit SEQEN = 1) regulator(s) are started after a delay (t_2) since the completion of the sequence step 1 (all regulators enabled at step 1 have been powered up correctly);
3. (SEQ[1:0] = 1x): enabled (bit SEQEN = 1) regulator(s) are started after a delay (t_3) since the completion of the sequence step 2 (all regulators enabled at steps 1 and 2 have been powered up correctly).

Note that if more than one regulator is assigned to power up at a given sequence step, their DELAY[2:0] bits might still be different. Therefore, they might initiate their Soft-Start ramps at different times, even if they are assigned to the same sequence step. This is useful to reduce input inrush currents at start-up and allow for even more sequencing flexibility.

The subsequent assertion of nRSTO is determined only by the status of all regulators that have been turned ON during the Power-Up Sequence (SEQEN = 1). Their status is checked before starting counter t_4 and again checked at the expiration of t_4 to have nRSTO asserted.

The status of the regulators that have NOT been turned ON during the Power-Up sequence (SEQEN = 0) is not taken into account for the assertion of nRSTO.

After the completion of the Power-Up sequence, i.e. at the time instant nRSTO is asserted high, the MCP16503 will enter the Power Modes state machine operation defined by LPM, HPM and PWRHLD signals and the content of registers 0x10-0x13, 0x20-0x23, 0x30-0x33, 0x40-0x43, 0x50-0x53, 0x60-0x63 applies.

Note that there might be a conflict between the enable status of regulator(s) which have been powered-up (SEQEN = 1) or left OFF (SEQEN = 0) during the start-up sequence, and their EN bit (ON or OFF state) in the power modes states (i.e. bit 7 of registers 0x10-0x13, and so on).

For example, LDO2 might not have been enabled to turn-on during the Power-Up sequence (SEQEN = 0), but it is defined as ON in the power modes definition registers 0x60-0x63.

In that case, the power modes definition of register 0x60-0x63 prevails as soon as the Power-Up sequence is completed. So LDO2 will be turned ON immediately after nRSTO has been asserted high.

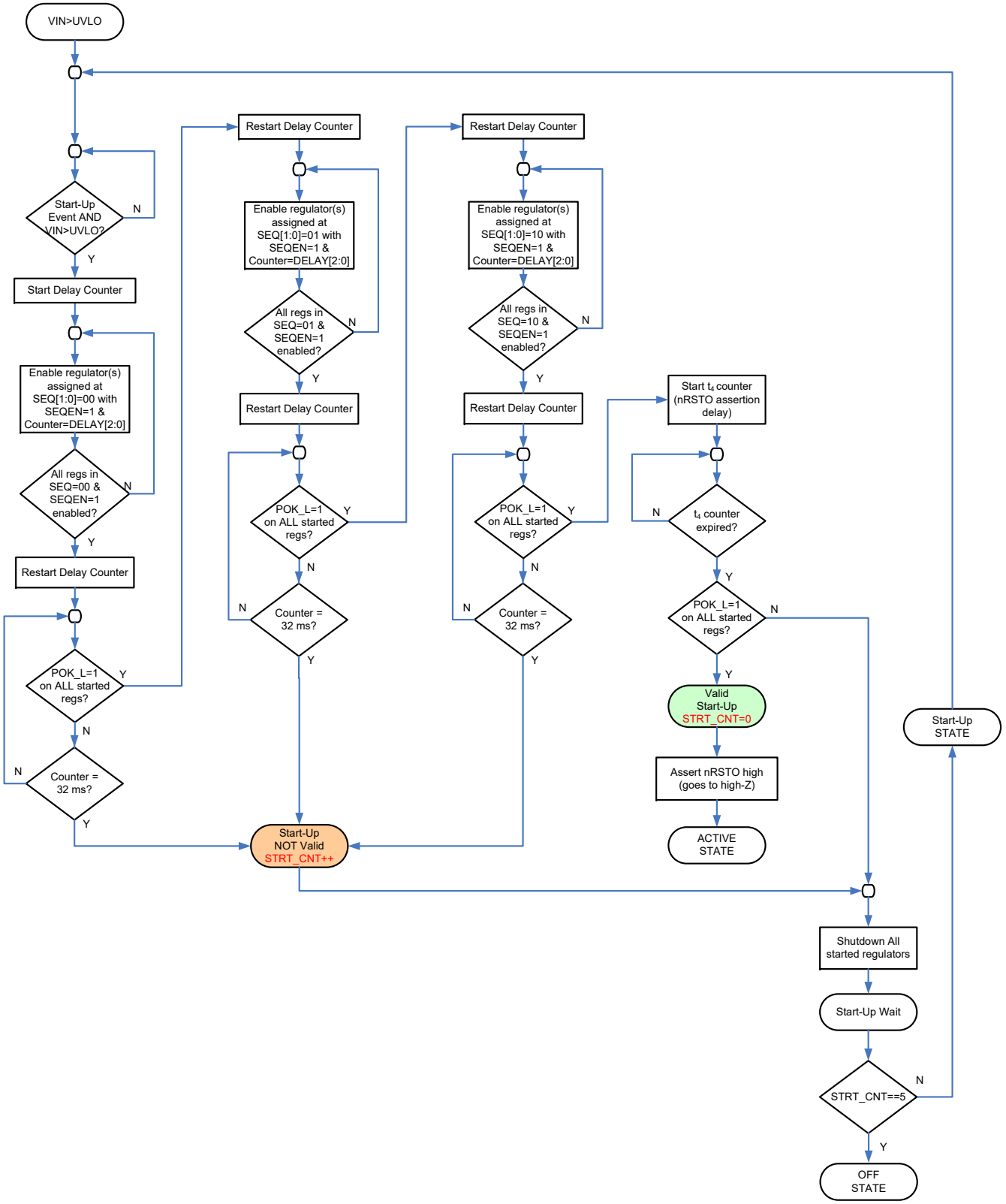
Some regulators which are supposed to turn-ON in the Power-up sequence may fail to power-up correctly.

In this case, the sequencing engine adds a 32 ms wait time to allow the affected regulators to recover. After the expiration of the 32 ms period, if the affected regulators have still not recovered, the STRT_CNT counter is incremented.

Once the MCP16503 detects 5 invalid start-up attempts, the STRTF flag is set. This flag is automatically cleared when EN = 0 is detected, when the IC enters OFF mode, after a power cycle, or upon any successful start-up. The device will remain in OFF mode until the counter is reset.

The start-up sequence flowchart is described in the following Figure 2-6.

Figure 2-6. Start-Up Sequence Flowchart



2.4.3. Dropout-Safe Start-Up Sequence Feature

The start-up sequence management of the MCP16503 ensures predictable timing between subsequent steps even in the case that some power channels may operate in dropout conditions with moderate loading.

This is the case for Buck1 or LDOs, because their achievable output voltage range (up to 3.7V) overlaps the input supply range (2.7V-5.5V).

This operating condition in frequently encountered in battery-powered applications. For example, some loads designed for 3.3V nominal supply voltage may not be able to withstand the fully charged battery voltage (around 4.2V) and therefore they would require a front-end regulator, but they could still operate when the battery voltage has decreased low enough to push their front-end regulator into dropout.

For example, if the battery voltage was around 3.1V and the Buck1 output voltage was also set at 3.3V, it is desirable to still start Buck1 and proceed throughout the start-up sequence even if the POK (Power OK) threshold for Buck1 may not be reached, since Buck1 will still be delivering a voltage within the I/O operating voltage range. This would allow a better exploitation of the battery, because the cut-off voltage is no longer dictated by the onset of the dropout of the 3.3V regulator (Buck1) and by its POK threshold.

By means of a dedicated circuit that monitors the input-output differential during start-up of the potentially affected regulators, the MCP16503 can still ensure a proper start-up and report an out-of-regulation condition of the relevant voltage rail (i.e. POK = 0) after the start-up sequence has been completed. The MPU can then detect the anomaly and decide either to continue operation or shut down the system.

The relevant EC Table parameter that defines the acceptable level of input-output differential to continue through the start-up sequence in lack of the normal POK is the Start-up POK Bypass Threshold.

2.4.4. Typical Power-Down Sequence and Timing

The power-down (shutdown) sequence can be initiated in two ways:

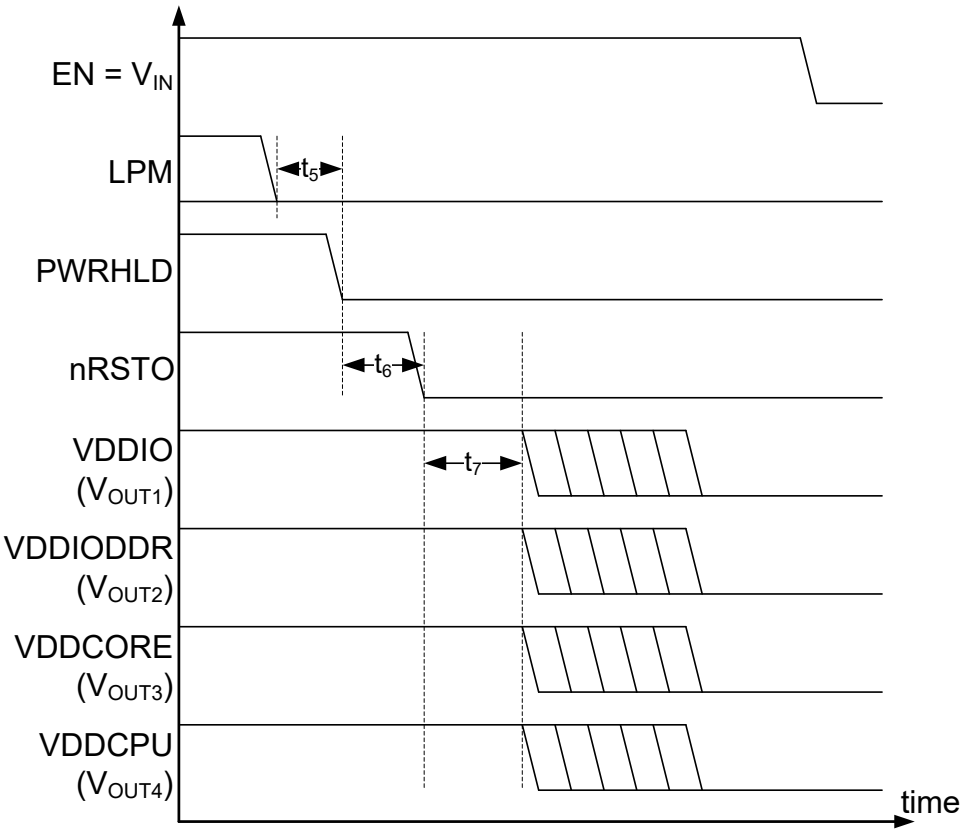
1. **Initiated by the MPU, by de-asserting PWRHLD** (LPM being already LOW or de-asserted simultaneously). This is the normal method, which assumes that the MCP16503 was in any operating state (i.e. was outside the start-up sequence).
2. **Initiated externally by pulling down EN**, after t_8 (enable timeout delay) + t_9 (enable interrupt assertion timeout delay, if no action is taken by the MPU within t_9).

After PWRHLD has been de-asserted or t_9 has reached EOC, nRSTO will immediately be asserted LOW by the MCP16503. After that, the turn-off of all Buck channels can take place with no delay, in any order.

The turn-off of each channel also activates the active discharge (if enabled) on the same channel.

The timing diagram shown in Figure 2-7 shows the typical sequence for the first case:

Figure 2-7. Power-Down (Shutdown) Sequence Timing Diagram

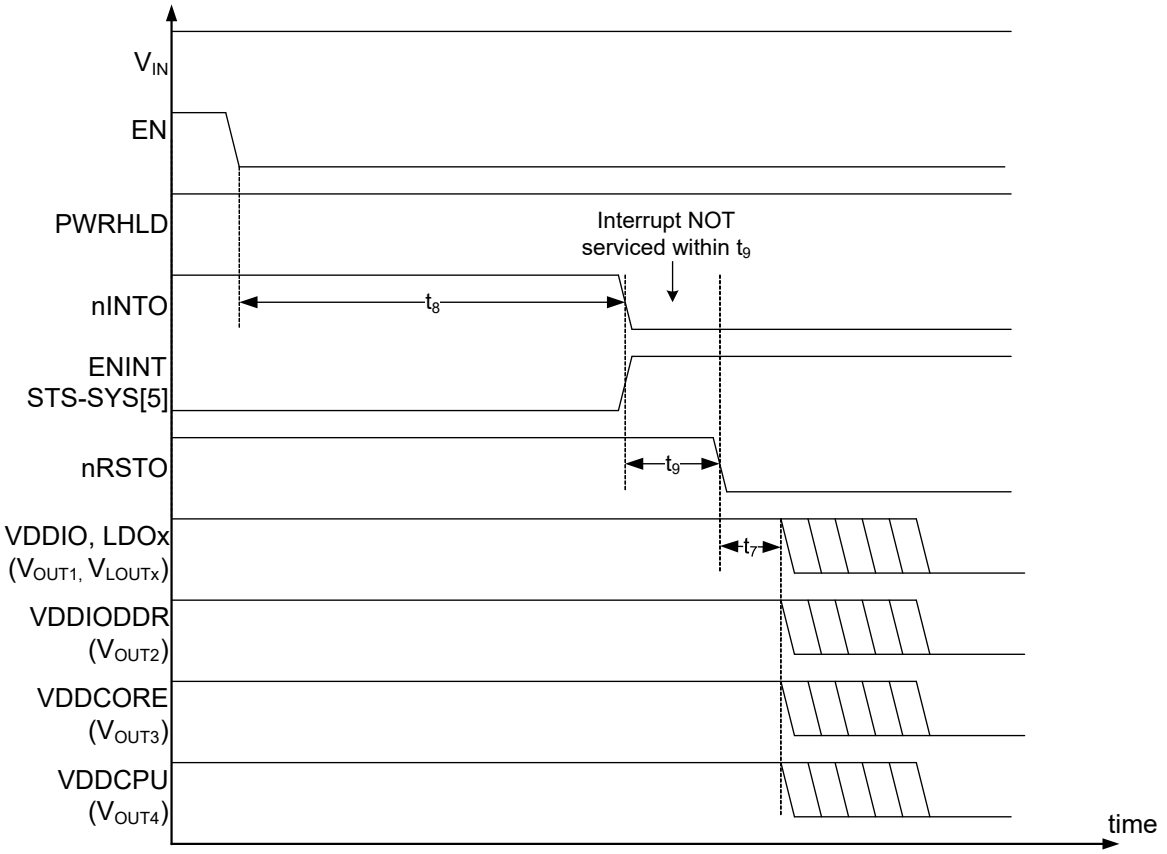


Where:

- t_5 = setup time, LPM = "0" to PWRHLD = "0": min. 0 ms (internal filtering applies)
- t_6 = delay from PWRHLD de-asserted to nRSTO asserted: min. 0 ms, max 10 ms (not a strict requirement)
- t_7 = dela
- y from nRSTO asserted to first V_{OUTX} turn-off: min. 0 ms, max 10 ms (not a strict requirement)

The following timing diagram in Figure 2-8 (shows the typical sequence for the second case):

Figure 2-8. EN Shutdown Sequence Timing Diagram



Where:

- t_8 = enable (EN = 0) timeout delay (default ENTO[1:0] = 01 i.e. 4s)
- t_9 = enable interrupt assertion timeout delay (default ENINTTO[1:0] = 01 i.e. 0.5s)
- t_7 = delay from nRSTO asserted to first V_{OUTX} turn-off: min. 0 ms, max 10 ms (not a strict requirement)

If EN is pulled down continuously for the entire t_8 duration, an interrupt will be asserted (nINTO goes LOW).

The interrupt assertion of this particular type of interrupt also set ENINT (Enable Interrupt) bit in register STS-SYS 0x04h (STS-SYS[5]). This interrupt is not maskable.

If the MPU reads register STS-SYS before t_9 expires, bit ENINT is acquired and Reset-on-Read. Then, the MPU can decide either to continue operating, or to initiate a shutdown by de-asserting PWRHLD.

Once the ENINT bit is cleared by the MPU upon reading register STS-SYS, MCP16503 de-asserts the interrupt, stops the t_9 counting, resets both t_8 (which reached EOC) and t_9, and if the condition (EN = 0) is no longer active, it does not take any countermeasure and continues operating.

If the MPU does NOT read STS-SYS register before t_9 expires, then MCP16503 will go into shutdown autonomously. A new EN = 1 start-up event will be needed to retrieve PMIC operation.

If t_9 expires when MCP16503 is in “Start-Up wait” mode, the 100 ms timer shall be terminated and MCP16503 shall move to “OFF” mode.

If the MPU reads register STS-SYS before the t_9 expires and decides to do nothing, but the enable condition is still present, the t_8 (and then t_9) counter will start again. This way, the long-press condition can be extended indefinitely by simply reading register STS-SYS each time nINTO is asserted.

The enable timeout delay t_8 is user programmable with bits ENTO[1:0] from 0s to 8s (0s – 2s – 4s – 8s).

The enable interrupt assertion timeout delay t_9 is user-programmable with bits ENINTTO[1:0] from 100 ms to 2s (100 ms – 500 ms –1s – 2s).

2.4.5. Enable Timeout Delay (t_8) and Enable Interrupt Assertion Timeout Delay (t_9) Programming Bits

Table 2-3. Enable Timeout Delay Bits ENTO[1:0] and Enable Interrupt Assertion Timeout Delay Bits ENINTTO[1:0]

ENTO[1:0]	Enable timeout delay t_8 (s)		ENINTTO[1:0]	Enable interrupt assertion timeout delay t_9 (s)
00	0		00	0.1
01	2		01	0.5
10	4		10	1
11	8		11	2

During runtime (when PWRHLD = 1), it is possible for the EN input to go LOW first, followed by the MPU setting PWRHLD to LOW before the expiration of t8 + t9. In this scenario, the steady EN = LOW condition does not trigger an automatic restart action.

If PWRHLD goes LOW during runtime, that means the MPU software has decided to go to OFF/HIBERNATE (by deasserting SHDN from the SHDWC Controller) regardless of the nSTRTO pin status (which is also monitored in the SHDWC controller).

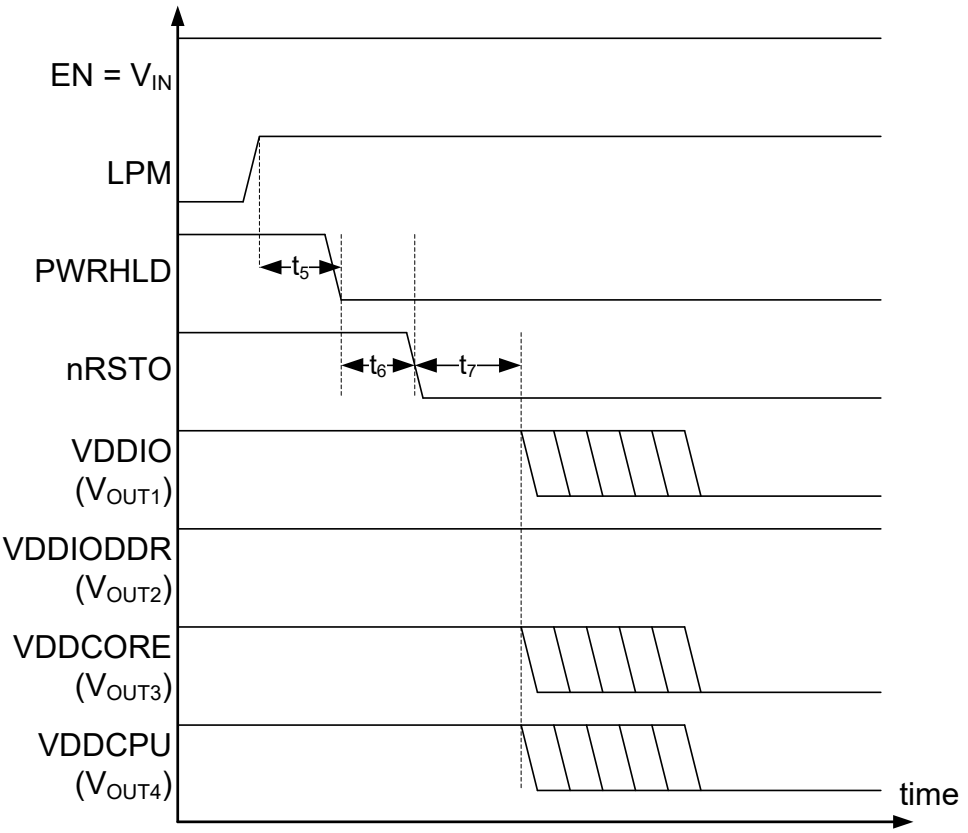
Therefore, the MCP16503 will attempt a new start-up only when PWRHLD transitions from Low to High, while also keeping the EN = High.

2.4.6. Typical HIBERNATE Sequences and Timing

The HIBERNATE mode entering sequence is similar to the Power-Down, with the only difference that LPM will be asserted HIGH by the MPU before de-assertion of PWRHLD, or at least at the same time PWRHLD is de-asserted (due to internal filtering, the setup time t_5 can be as low as 0 µs). The V_{OUT2} rail (and/or other rails which are defined ON in HIBERNATE mode) will remain active, while V_{OUT1}, V_{OUT3} and V_{OUT4} will be immediately disabled. In HIBERNATE mode, the DDRx/LPDDRx will typically be in backup self-refresh mode (BSR).

The following timing diagram of Figure 2-9 shows the typical HIBERNATE sequence for a device that keeps only V_{OUT2} ON during HIBERNATE mode:

Figure 2-9. Entering HIBERNATE Mode Timing Diagram



Where:

- t_5 = setup time, LPM = "1" to PWRHLD = "0": min. 0 µs (internal filtering applies)
- t_6 = delay from PWRHLD de-asserted to nRSTO asserted: min. 0 µs, max 10 µs (not a strict requirement)
- t_7 = delay from nRSTO asserted to first V_{OUTX} turn-off: min. 0 µs, max 10 µs (not a strict requirement)

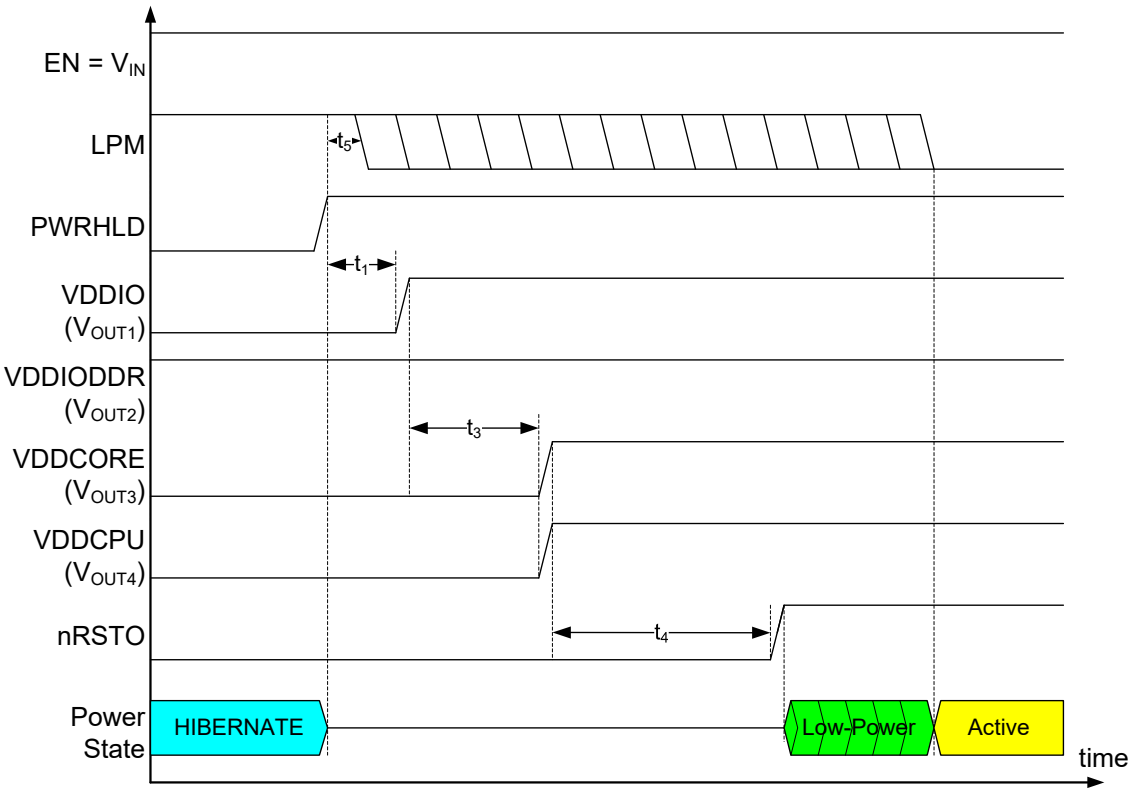
From the HIBERNATE state, the system can:

1. Move to OFF state (if also LPM goes LOW, the V_{OUT2} can be immediately turned OFF), or
2. initiate another start-up sequence (except for Buck2 which is already active and has its SEQEN = 1) by a low-to-high transition of PWRHLD.

The timing diagram of a start-up sequence from HIBERNATE mode is shown in Figure 2-10. After the assertion of PWRHLD, the MPU may de-assert LPM at any time. Due to internal filtering, simultaneous transition of LPM and PWRHLD is allowed (hold time t_5 can be 0 µs).

Depending on the time at which LPM is de-asserted, the MCP16503 may transition through the Low-Power state or not.

Figure 2-10. Start-Up Sequence exiting HIBERNATE Mode Timing Diagram



Where:

- t_1 = delay from PWRHLD asserted to first supply V_{OUT1} starting (SEQ[1:0] = 00, default DELAY[2:0] = 001 i.e. 0.5 ms)
- t_3 = time from V_{OUT1} established to V_{OUT3}, V_{OUT4} starting (SEQ[1:0] = 10, default DELAY[2:0] = 100 i.e. 4 ms)
- t_4 = time from V_{OUT3}, V_{OUT4} established to nRSTO de-assertion (default v[2:0] = 100 i.e. 16 ms)
- t_5 = minimum hold time, PWRHLD = ”1” to LPM = ”0”: min. 0 µs (internal filtering applies)

Note: Upon exiting HIBERNATE mode, Buck2 is not part of the sequence, because it is already ON (being in Auto PFM mode) and its SEQEN = 1.

However, also depending on the instant at which the MPU de-asserts LPM, it can toggle to FPWM mode at the time nRSTO is asserted HIGH.

Similar to Buck2, any other regulator which is defined ON in the HIBERNATE state, and has its bit SEQEN = 1, will NOT be turned OFF when exiting the HIBERNATE state for a new start-up sequence.

If the regulator is defined ON in the HIBERNATE state, but its bit SEQEN = 0, it will be turned OFF as soon as the new start-up sequence is initiated.

In conclusion, for a regulator to stay ON continuously from the HIBERNATE state throughout the new start-up sequence, two conditions must be satisfied:

1. The regulator is set ON in the HIBERNATE state;
2. The SEQEN bit is set to 1.

2.4.7. Restart Sequence After Fault and Automatic Wake-Up Pulse (AWKP) Generation

The power-up sequence is also automatically executed when reacting to severe fault conditions. Please see section Protections for information on which faults are triggering a new restart sequence. In the default configuration (i.e. HCPEN bit is 0 for the Buck channels), as soon as a fault is detected, the power delivery on all channels is terminated and the MCP16503 waits for 100 ms. After this wait time, a new start-up sequence is generated in the attempt to restart the system correctly.

A special feature is provided to enable system recovery if the restart sequence after fault occurs while in HIBERNATE mode. In HIBERNATE mode, the PWRHLD was previously asserted low by the MPU, and the MPU expects a wake-up event in order to set PWRHLD to high again. This must be a hardware event, which is flagged to some I/O inside the MPU Shutdown and Wake-Up Controller block (SHDWC), for example a logic transition on a WKUPx or PIOBUx pin.

On the other hand, if a fault (e.g. a short-circuit on a Buck channel having HCPEN = 0 and left ON during HIBERNATE) causes a restart sequence while in HIBERNATE, the restart sequence won't be successfully completed if no wake-up event is generated for the MPU SHDWC, because PWRHLD will stay low. It is necessary for the PWRHLD signal to be high just prior to the completion of the start-up sequence to have nRSTO asserted high.

This is solved by generating from the MCP16503 an automatic wake-up pulse (AWKP) on the nSTRTO output if the fault that generates a restart sequence has occurred while in HIBERNATE mode.

The automatic wake-up pulse generation can be optionally disabled by the user by setting bit AWKPDIS (bit4) in register SYS-CFG (0x03). The AWKP function is enabled by default.

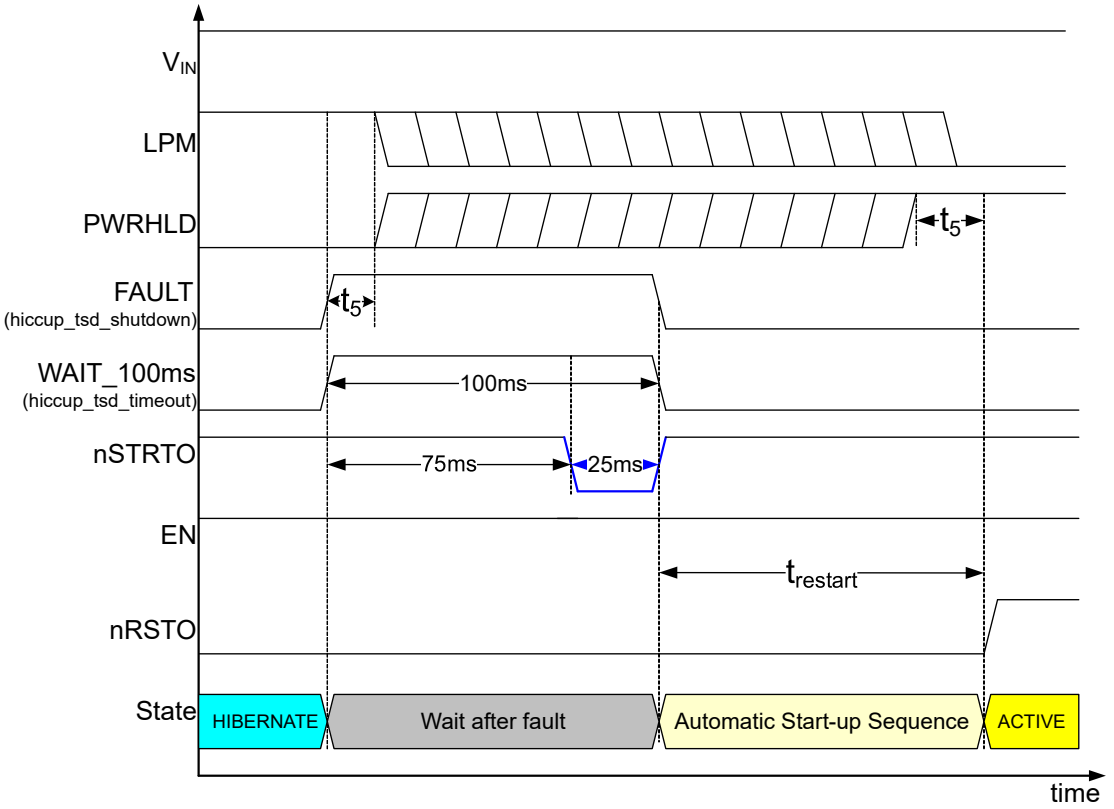
The timing diagram of a restart sequence caused by a fault while in HIBERNATE mode is shown below in Figure 2-11.

Just before initiating the restart sequence, the MCP16503 generates a 25 ms (nominal duration) Automatic Wake-Up Pulse on the nSTRTO output, even in lack of a low-level on the EN input. This is the only situation where the nSTRTO logic level does not reflect the EN input status. The duration of the AWK Pulse erodes into the 100 ms wait time that precedes the automatic restart sequence.

PWRHLD will typically return high as soon as the nSTRTO signal is detected to be low by the MPU SHDWC. If LPM stays high for any reason, the MCP16503 will go in Low-Power mode immediately after the automatic start-up sequence. This behavior is shown in Figure 4-15 in the Typical Performance Curves section.

If the restart sequence after a fault is executed in any other operational state but HIBERNATE, PWRHLD would either be already high (in applications with backup power) or it would return high as soon as the VDDIO rail is started, thus making the generation of the Automatic Wake-Up pulse not necessary.

Figure 2-11. Automatic Wake-Up Pulse Generation Timing Diagram (FAULT During HIBERNATE)



Where:

- $t_{restart}$ = duration of the automatic start-up (restart) sequence
- t_5 = minimum setup/hold time: min. 0 µs (internal filtering applies)

2.5. Configuration Words, Register Definitions and Maps

The position of the configuration words bits in the global register maps is described in section I²C Registers Maps and Bit Definitions.

2.5.1. VSET[5:0] Codes Definition

The user can set the default start-up voltage by connecting a resistor to ground on the VSETx and VSETLy pins. After the PMIC has started the user can change the output voltage via I²C. For Buck regulators (OUTx) and LDOs (LOUTx), the following Voltage Codes Definition Table applies:

Table 2-4. Voltage Codes Definition Bits VSET[5:0]

	Buck1, LDO1, 2	Buck2, 3, 4		Buck1, LDO1, 2	Buck2, 3, 4
VSET[5:0]	VOUT [V]	VOUT [V]	VSET[5:0]	VOUT [V]	VOUT [V]
111111	3.700	1.850	100101	2.400	1.200
111110	3.650	1.825	100100	2.350	1.175
111101	3.600	1.800	100011	2.300	1.150
111100	3.550	1.775	100010	2.250	1.125
111011	3.500	1.750	100001	2.200	1.100
111010	3.450	1.725	100000	2.150	1.075
111001	3.400	1.700	011111	2.100	1.050
111000	3.350	1.675	011110	2.050	1.025
110111	3.300	1.650	011101	2.000	1.000
110110	3.250	1.625	011100	1.950	0.975
110101	3.200	1.600	011011	1.900	0.950
110100	3.150	1.575	011010	1.850	0.925
110011	3.100	1.550	011001	1.800	0.900
110010	3.050	1.525	011000	1.750	0.875
110001	3.000	1.500	010111	1.700	0.850
110000	2.950	1.475	010110	1.650	0.825
101111	2.900	1.450	010101	1.600	0.800
101110	2.850	1.425	010100	1.550	0.775
101101	2.800	1.400	010011	1.500	0.750
101100	2.750	1.375	010010	1.450	0.725
101011	2.700	1.350	010001	1.400	0.700
101010	2.650	1.325	010000	1.350	0.675
101001	2.600	1.300	001111	1.300	0.650
101000	2.550	1.275	001110	1.250	0.625
100111	2.500	1.250	001101	1.200	0.600
100110	2.450	1.225	<001101	1.200	0.600

2.5.2. Switching (Oscillator) Frequency Displacement Programming Bits

Table 2-5. Switching Frequency Displacement Bits FSD[1:0]

FSD[1:0]	Frequency displacement
00	0%
01	0%
10	−16.5%
11	+16.5%

The frequency displacement acts on the main oscillator. The switching frequencies of all regulators and all timings are shifted accordingly.

2.5.3. Reset Assertion Delay (t_4) Programming Bits

Table 2-6. Reset Assertion Delay Bits RSTDLY[2:0]

RSTDLY[2:0]	Delay (ms)
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

2.5.4. Soft-Start, Start-Up Sequence Step Assignment and Sequence Step Delay (t_1, t_2, t_3) Programming Bits

For each regulator, the SSR[1:0] bits define the Soft-Start Rate in terms of time duration of each voltage step (t_{ramp}).

Table 2-7. Soft-Start Rate Bits SSR[1:0]

SSR[1:0]	2 MHz Clock Division	t_{ramp} (µs)	Buck2, 3, 4 25 mV Step - Average Ramp Rate (V/ms)	Buck1, LDO1,2 50 mV Step - Average Ramp Rate (V/ms)	C_{OUT} (µF)	Average C_{OUT} Capacitor Current (mA) - 25 mV step	Average C_{OUT} Capacitor Current (mA) - 50 mV step
00	16	8	3.125	6.250	22	69	138
01	32	16	1.563	3.125	22	34	69
10	48	24	1.042	2.083	22	23	46
11	64	32	0.781	1.563	22	17	34

The SEQ[1:0] bits assign each regulator at a determined step in the start-up sequence. Assignment SEQ[1:0] = 00 (first sequence step) means the regulator is started upon a valid start-up event.

However, each regulator is allowed to turn ON at its assigned start-up sequence step only if its SEQEN bit is set. If SEQEN = 0, the regulator will NOT turn on, and it will be disregarded in the sequence generation and nRSTO assertion algorithm.

Upon exit of HIBERNATE mode, all regulators (typically Buck2 and LDO2) which were already ON in HIBERNATE mode and have SEQEN = 1 will stay ON continuously throughout the execution of the start-up sequence.

Table 2-8. Start-Up Sequence Step Assignment Bits SEQ[1:0]

SEQ[1:0]	Start-Up Sequence Step
00	1
01	2
10	3
11	3

Table 2-9. Sequence Step Delay Bits DELAY[2:0]

DELAY[2:0]	Delay (ms)
000	0
001	0.5
010	1
011	2
100	4
101	8
110	12
111	16

For each regulator these bits program the delay (t_1 to t_3) from the completion of the previous sequence step to the beginning of its turn-on (beginning of Soft-Start, if SEQEN = 1).

For regulators assigned to the first sequence step (SEQ[1:0] = 00) i.e. starting at t_1, this is the additional delay after the device wake-up time since the start-up event (e.g. PWRHLD low-to-high).

This way, by setting a DELAY[2:0] = 001 or higher, it is possible to define a de-bouncing time of the EN event.

2.5.5. Dynamic Voltage Scaling Rate Programming Bits (t_{ramp})

The DVSR[1:0] bits define the Dynamic Voltage Scaling Rate in terms of time duration of each voltage step (t_{ramp}).

Due to the output capacitor voltage change rate, additional current is required at the output during DVS. The average current for 22 µF (recommended output capacitor value) is also given in the Table 2-9 below. In case the output capacitance is increased, see section PWM Mode Negative Current Limit Protection (Buck Channels).

The Buck channels of the MCP16503 also feature a negative inductor current limit protection when operating in Forced PWM mode. This prevents dangerous current levels in the power train. If the inductor current reaches the Low-Side Negative Peak Current Limit (I_{LIM_NEGx}) while the Low-Side MOSFET is conducting, the Low-Side MOSFET is turned off and the inductor current is pushed to the input voltage, either through the body diode of the High-Side MOSFET (if OFF) or its channel (when turned ON by the control loop). Since this feature is only intended to protect the device in some particular transient conditions (such as a large decresase of the ouput voltage setting associated with an extremely large capacitive load), it is only reported through I^2C, but it does not cause the assertion of the nRSTO (RESET) signal.

This protection should never be exercised continuously and/or without a very large bulk capacitor, because it may quickly destroy the device.

When this protection is engaged, energy is pumped back from the output into the input voltage. If the input supply has no sinking capability and/or the input bulk decoupling cap is not large enough, the input voltage will rise to the point where the device is permanently damaged.

Table 2-10. Dynamic Voltage Scaling Rate Bits DVSR[1:0]

DVSR[1:0]	2 MHz Clock Division	t_{ramp} (µs)	Buck2, 3, 4 25 mV Step - Average Ramp Rate (V/ms)	Buck1, LDO1,2 50 mV Step - Average Ramp Rate (V/ms)	C_{OUT} (µF)	Average C_{OUT} Capacitor Current (mA) - 25 mV step	Average C_{OUT} Capacitor Current (mA) - 50 mV step
00	16	8	3.125	6.250	22	69	138
01	32	16	1.563	3.125	22	34	69
10	48	24	1.042	2.083	22	23	46
11	64	32	0.781	1.563	22	17	34

2.6. I²C Registers Maps and Bit Definitions

For each Buck regulator, the user can program different voltages, ON/OFF status and mode of operation (FPWM or Auto PFM) for each of the four power states. For LDOs, mode of operation is not applicable.

The following Register Summary provides the registers mapping of all the bits available in the user registers space of **MCP16503**.

In Register Summary, each **BLACK** bit in the volatile (I^2C-accessible) register has a corresponding bit in the OTP bank. The default values of the **BLACK** bits in the volatile registers are loaded from the OTP bank.

It is possible to program the OTP at the factory to generate additional product variants with different default values for the **BLACK** bits. Please contact your nearest Microchip Sales Office for further assistance with the development of customized default configurations.

The default values of the **RED** bits are:

- Either hardwired in metal mask; or
- For the VSET[5:0] bits in RED, when the decoding process is complete, the detected start-up voltage settings are stored in the VSET[5:0] fields of the OUTx-A and LDOx-A registers. These values are then copied to the corresponding VSET[5:0] fields in OUTx-LPM, OUTx-HIB, OUTx-HPM, LDOx-LPM, LDOx-HIB, and LDOx-HPM.

The following topics, SYS-ADR to LDO2-CFG, provide the descriptions of the registers (bits/bit fields).

Default Registers Content shows the default value of each register.

Legend:

- R = READ access
- R/W = READ/WRITE access
- RoR = Reset-on-Read. After the value of the bit has been read, it will be cleared automatically.

2.6.1. Register Summary

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
System Registers										
0x00	SYS-ADR	7:0	Reserved	ADR[6:2]					ADR[1:0]	
0x01	SYS-ID	7:0	ID[3:0]				REV[3:0]			
0x02	SYS-TMG	7:0	ENTO[1:0]		ENINTTO[1:0]		Reserved	RSTDLY[2:0]		
0x03	SYS-CFG	7:0	TSDMSK	TWRMSK	HPMPEN	AWKPDIS	FSD [1:0]		B1HCEN	USER
System and Power Channels Status Registers										
0x04	STS-SYS	7:0	TSD	TWR	ENINT	STRTF	Reserved[3:0]			
0x05	STS-B1	7:0	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
0x06	STS-B2	7:0	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
0x07	STS-B3	7:0	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
0x08	STS-B4	7:0	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
0x09	STS-L1	7:0	FLT	Reserved[2:0]			ILIM	SSD	POK	ENS
0x0A	STS-L2	7:0	FLT	Reserved[2:0]			ILIM	SSD	POK	ENS
Buck1 Regulator Setup										
0x10	OUT1-A	7:0	EN	MODE	VSET[5:0]					
0x11	OUT1-LPM	7:0	EN	MODE	VSET[5:0]					
0x12	OUT1-HIB	7:0	EN	MODE	VSET[5:0]					
0x13	OUT1-HPM	7:0	EN	MODE	VSET[5:0]					
0x14	OUT1-SEQ	7:0	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
0x15	OUT1-CFG	7:0	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
Buck2 Regulator Setup										
0x20	OUT2-A	7:0	EN	MODE	VSET[5:0]					
0x21	OUT2-LPM	7:0	EN	MODE	VSET[5:0]					
0x22	OUT2-HIB	7:0	EN	MODE	VSET[5:0]					
0x23	OUT2-HPM	7:0	EN	MODE	VSET[5:0]					
0x24	OUT2-SEQ	7:0	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
0x25	OUT2-CFG	7:0	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
Buck3 Regulator Setup										
0x30	OUT3-A	7:0	EN	MODE	VSET[5:0]					
0x31	OUT3-LPM	7:0	EN	MODE	VSET[5:0]					
0x32	OUT3-HIB	7:0	EN	MODE	VSET[5:0]					
0x33	OUT3-HPM	7:0	EN	MODE	VSET[5:0]					
0x34	OUT3-SEQ	7:0	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
0x35	OUT3-CFG	7:0	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
Buck4 Regulator Setup										
0x40	OUT4-A	7:0	EN	MODE	VSET[5:0]					
0x41	OUT4-LPM	7:0	EN	MODE	VSET[5:0]					
0x42	OUT4-HIB	7:0	EN	MODE	VSET[5:0]					
0x43	OUT4-HPM	7:0	EN	MODE	VSET[5:0]					
0x44	OUT4-SEQ	7:0	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
0x45	OUT4-CFG	7:0	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
LDO1 Setup										
0x50	LDO1-A	7:0	EN	Reserved	VSET[5:0]					
0x51	LDO1-LPM	7:0	EN	Reserved	VSET[5:0]					
0x52	LDO1-HIB	7:0	EN	Reserved	VSET[5:0]					
0x53	LDO1-HPM	7:0	EN	Reserved	VSET[5:0]					
0x54	LDO1-SEQ	7:0	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
0x55	LDO1-CFG	7:0	FLTMSK	Reserved	DISCH	Reserved	DVSR[1:0]		REN	RCON
LDO2 Setup										
0x60	LDO2-A	7:0	EN	Reserved	VSET[5:0]					
0x61	LDO2-LPM	7:0	EN	Reserved	VSET[5:0]					
0x62	LDO2-HIB	7:0	EN	Reserved	VSET[5:0]					
0x63	LDO2-HPM	7:0	EN	Reserved	VSET[5:0]					
0x64	LDO2-SEQ	7:0	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
0x65	LDO2-CFG	7:0	FLTMSK	Reserved	DISCH	Reserved	DVSR[1:0]		REN	RCON

2.6.2. Device Address

Name: SYS-ADR
Address: 0x00
Default: 0xDA
Property: R

Bit	7	6	5	4	3	2	1	0
	Reserved	ADR[6:0]						
Access	R	R	R	R	R	R	R	R
Default	1	1	0	1	1	0	1	0

Bit 7 – Reserved
Default is always ‘1’ for factory-programmed units.

Bits 6:0 – ADR[6:0] I^2C address (7-bits)
Default is 0x5A.

2.6.3. PMIC Identification

Name: SYS-ID
Address: 0x01
Default: 0x60
Property: R

Bit	7	6	5	4	3	2	1	0
	ID[3:0]				REV[3:0]			
Access	R	R	R	R	R	R	R	R
Default	0	1	1	0	0	0	0	0

Bits 7:4 – ID[3:0] Device ID bits

Bits 3:0 – REV[3:0] Revision/version identification bits

2.6.4. System Timing Settings

Name: SYS-TMG
Address: 0x02
Default: 0x12
Property: R/W

Bit	7	6	5	4	3	2	1	0
	ENTO[1:0]		ENINTTO[1:0]		Reserved	RSTDLY[2:0]		
Access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Default	0	0	0	1	0	0	1	0

Bits 7:6 – ENTO[1:0] (EN) timeout delay programming bits
Default is 00 (0 seconds).

Bits 5:4 – ENINTTO[1:0] EN interrupt assertion timeout delay programming bits
Default is 01 (0.5 second).

Bit 3 – Reserved
Maintain as '0'

Bits 2:0 – RSTDLY[2:0] nRSTO assertion delay programming bits (t_4 in the start-up sequence)
Default is 010 (4 ms).

2.6.5. System Configuration

Name: SYS-CFG
Address: 0x03
Default: 0xC0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	TSDMSK	TWRMSK	HPMPEN	AWKPDIS	FSD [1:0]		B1HCEN	USER
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – TSDMSK Thermal Shutdown Masking Bit
If the bit is 1, it will prevent nINTO from being asserted LOW upon TSD = 1. Default is 1 (Thermal Shutdown TSD will not be flagged by nINTO).

Bit 6 – TWRMSK Thermal Warning Masking Bit
If the bit is 1, it will prevent nINTO from being asserted LOW upon a Thermal Warning event. Default is 1 (Thermal Warning will not be flagged by nINTO).

Bit 5 – HPMPEN High-Performance Mode Enable Pin Bit
This bit must be set to 1 through an I^2C command in order to enable the HPM pin. If the bit is 0, setting the HPM pin high will have no effect on the power status state machine.

Bit 4 – AWKPDIS Automatic Wake-Up Pulse DISable Bit
If the bit is set to 1, it disables the generation of a wake-up pulse on pin nSTRTO before an automatic start-up sequence after a fault (thermal shutdown or hiccup with HCPEN = 0) occurred in HIBERNATE mode.

Bits 3:2 – FSD [1:0] Switching (oscillator) frequency displacement bits, default is 00 (no displacement)

Bit 1 – B1HCEN Buck1 Hysteretic Control Mode Enable Bit
When set to 1, this bit enables the Hysteretic Control Mode for Buck1 in AutoPFM operation.

Bit 0 – USER User-accessible bit
User-accessible bit that can be used to store system information. This bit is volatile and it is cleared upon SVIN UVLO.

2.6.6. System Status

Name: STS-SYS
Address: 0x04
Default: 0x00
Property: R/RoR

Bit	7	6	5	4	3	2	1	0
	TSD	TWR	ENINT	STRTF	Reserved[3:0]			
Access	R/RoR	R/RoR	R/RoR	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 7 – TSD Thermal Shutdown Fault Flag (latched)
If a Thermal Shutdown occurs, TSD bit will be set to 1. It will not automatically return to 0 after the Thermal Shutdown condition has ceased. If the fault condition is no longer present, a READ operation will automatically also clear the flag (Reset-on-Read, RoR).
If the corresponding masking bit TSDMSK is 0, TSD = 1 will cause nINTO being asserted LOW.

Bit 6 – TWR Thermal Warning Fault Flag (latched)
If a Thermal Warning occurs, TWR bit will be set to 1. It will not automatically return to 0 after the Thermal Warning condition has ceased. If the fault condition is no longer present, a READ operation will automatically also clear the flag (Reset-on-Read, RoR).
If the corresponding masking bit TWRMSK is 0, TWR = 1 will cause nINTO being asserted LOW

Bit 5 – ENINT Interrupt flag
This bit is set as soon as the Enable timeout has expired. A read action will reset the ENINT flag and also reset the Enable timeout counter.

Bit 4 – STRTF Start-Up Fail Flag
If MCP16503 has counted 5 invalid Start-Up, this flag will be set. This flag will be automatically reset when EN = 0 has been detected when the IC is in OFF mode or at a power cycle or at any valid Start-Up. The IC will stay in OFF mode until the counter is reset.

Bits 3:0 – Reserved[3:0]
Maintain as '0'

2.6.7. Buck1 Status

Name: STS-B1
Address: 0x05
Default: 0x00
Property: R/RoR

Bit	7	6	5	4	3	2	1	0
	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
Access	R/RoR	R/RoR	R/RoR	R/RoR	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 7 – FLT Fault flag bit (latched) for Buck1
FLT is set to 1 if HICCUP = 1 or if (ENS = 1 and SSD = 1 and POK = 0).

Bit 6 – HICCUP Hiccup flag bit (latched)
If the HS OC Event counter reaches EOC and POK is low, the HICCUP flag is latched. The behavior of the system is determined by the HCPEN bit.

Bit 5 – ILIMNEG Negative current limit flag bit (latched)
If the negative current limit threshold is reached, the ILIMNEG flag is latched.

Bit 4 – ZCD Zero-Current crossing Detection flag (latched)
This bit is set every time the ZCD is enabled (in Auto-PFM mode) and the ZCD comparator trips.

Bit 3 – Reserved
Maintain as '0'

Bit 2 – SSD Soft-Start Done status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft-start ramp.

Bit 1 – POK Power OK status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

Bit 0 – ENS Enable status bit (not latched)
ENS = 1 means the regulator is currently enabled.

2.6.8. Buck2 Status

Name: STS-B2
Address: 0x06
Default: 0x00
Property: R/RoR

Bit	7	6	5	4	3	2	1	0
	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
Access	R/RoR	R/RoR	R/RoR	R/RoR	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 7 – FLT Fault flag bit (latched) for Buck2
FLT is set to 1 if HICCUP = 1 or if (ENS = 1 and SSD = 1 and POK = 0).

Bit 6 – HICCUP Hiccup flag bit (latched)
If the HS OC Event counter reaches EOC and POK is low, the HICCUP flag is latched. The behavior of the system is determined by the HCPEN bit.

Bit 5 – ILIMNEG Negative current limit flag bit (latched)
If the negative current limit threshold is reached, the ILIMNEG flag is latched.

Bit 4 – ZCD Zero-Current crossing Detection flag (latched)
This bit is set every time the ZCD is enabled (in Auto-PFM mode) and the ZCD comparator trips.

Bit 3 – Reserved
Maintain as '0'

Bit 2 – SSD Soft-Start Done status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft-start ramp.

Bit 1 – POK Power OK status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

Bit 0 – ENS Enable status bit (not latched)
ENS = 1 means the regulator is currently enabled.

2.6.9. Buck3 Status

Name: STS-B3
Address: 0x07
Default: 0x00
Property: R/RoR

Bit	7	6	5	4	3	2	1	0
	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
Access	R/RoR	R/RoR	R/RoR	R/RoR	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 7 – FLT Fault flag bit (latched) for Buck3
FLT is set to 1 if HICCUP = 1 or if (ENS = 1 and SSD = 1 and POK = 0).

Bit 6 – HICCUP Hiccup flag bit (latched)
If the HS OC Event counter reaches EOC and POK is low, the HICCUP flag is latched. The behavior of the system is determined by the HCPEN bit.

Bit 5 – ILIMNEG Negative current limit flag bit (latched)
If the negative current limit threshold is reached, the ILIMNEG flag is latched.

Bit 4 – ZCD Zero-Current crossing Detection flag (latched)
This bit is set every time the ZCD is enabled (in Auto-PFM mode) and the ZCD comparator trips.

Bit 3 – Reserved
Maintain as '0'

Bit 2 – SSD Soft-Start Done status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft-start ramp.

Bit 1 – POK Power OK status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

Bit 0 – ENS Enable status bit (not latched)
ENS = 1 means the regulator is currently enabled.

2.6.10. Buck4 Status

Name: STS-B4
Address: 0x08
Default: 0x00
Property: R/RoR

Bit	7	6	5	4	3	2	1	0
	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
Access	R/RoR	R/RoR	R/RoR	R/RoR	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 7 – FLT Fault flag bit (latched) for Buck4
FLT is set to 1 if HICCUP = 1 or if (ENS = 1 and SSD = 1 and POK = 0).

Bit 6 – HICCUP Hiccup flag bit (latched)
If the HS OC Event counter reaches EOC and POK is low, the HICCUP flag is latched. The behavior of the system is determined by the HCPEN bit.

Bit 5 – ILIMNEG Negative current limit flag bit (latched)
If the negative current limit threshold is reached, the ILIMNEG flag is latched.

Bit 4 – ZCD Zero-Current crossing Detection flag (latched)
This bit is set every time the ZCD is enabled (in Auto-PFM mode) and the ZCD comparator trips.

Bit 3 – Reserved
Maintain as '0'

Bit 2 – SSD Soft-Start Done status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft-start ramp.

Bit 1 – POK Power OK status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

Bit 0 – ENS Enable status bit (not latched)
ENS = 1 means the regulator is currently enabled.

2.6.11. LDO1 Status

Name: STS-L1
Address: 0x09
Default: 0x00
Property: R/RoR

Bit	7	6	5	4	3	2	1	0
	FLT	Reserved[2:0]			ILIM	SSD	POK	ENS
Access	R/RoR	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 7 – FLT Fault flag bit (latched) for LDO1
FLT is set if (ENS = 1 and SSD = 1 and POK = 0).

Bits 6:4 – Reserved[2:0]
Maintain as '0'

Bit 3 – ILIM Current Limit status bit (not latched)
ILIM = 1 means the regulator is within the current limit.

Bit 2 – SSD Soft-Start Done status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft-start ramp.

Bit 1 – POK Power OK status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

Bit 0 – ENS Enable status bit (not latched)
ENS = 1 means the regulator is currently enabled.

2.6.12. LDO2 Status

Name: STS-L2
Address: 0x0A
Default: 0x00
Property: R/RoR

Bit	7	6	5	4	3	2	1	0
	FLT	Reserved[2:0]			ILIM	SSD	POK	ENS
Access	R/RoR	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 7 – FLT Fault flag bit (latched) for LDO2
FLT is set if (ENS = 1 and SSD = 1 and POK = 0).

Bits 6:4 – Reserved[2:0]
Maintain as '0'

Bit 3 – ILIM Current Limit status bit (not latched)
ILIM = 1 means the regulator is within the current limit.

Bit 2 – SSD Soft-Start Done status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft-start ramp.

Bit 1 – POK Power OK status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

Bit 0 – ENS Enable status bit (not latched)
ENS = 1 means the regulator is currently enabled.

2.6.13. Buck1 Active Status

Name: OUT1-A
Address: 0x10
Default: 0b11 (VSET1 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Active Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the Active Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Active Status
Its default value is defined by the resistor at the VSET1 pin during power-on start.

2.6.14. Buck1 Low-Power Mode Status

Name: OUT1-LPM
Address: 0x11
Default: 0b10 (VSET1 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Low-Power Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the Low-Power Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Low-Power Mode Status
Its default value is defined by the resistor at the VSET1 pin during power-on start.

2.6.15. Buck1 HIBERNATE Mode Status

Name: OUT1-HIB
Address: 0x12
Default: 0b00 (VSET1 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the HIBERNATE Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the HIBERNATE Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the HIBERNATE Mode Status
Its default value is defined by the resistor at the VSET1 pin during power-on start.

2.6.16. Buck1 High-Performance Mode Status

Name: OUT1-HPM
Address: 0x13
Default: 0b11 (VSET1 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – EN Enable bit of the High-Performance Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the High-Performance Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the High-Performance Mode Status
Its default value is defined by the resistor at the VSET1 pin during power-on start.

2.6.17. Buck1 Start-up Sequence

Name: OUT1-SEQ
Address: 0x14
Default: 0x49
Property: R/W

Bit	7	6	5	4	3	2	1	0
	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	0	1	0	0	1

Bits 7:6 – SSR[1:0] Soft-Start Rate selection bits

Bits 5:4 – SEQ[1:0] Start-up Sequence Step assignment bits

Bit 3 – SEQEN Start-up Sequence Enable bit
The regulator will NOT start at the assigned step if SEQEN = 0. SSD and POK flags will be neglected during the Start-Up Sequence.

Bits 2:0 – DELAY[2:0] Start-up time delay
The time delay from the completion of the previous Start-Up Sequence Step or Start-Up Event to the turn-ON (beginning of Soft-Start).

2.6.18. Buck1 Configuration

Name: OUT1-CFG
Address: 0x15
Default: 0xB0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	1	1	0	0	0	0

Bit 7 – FLTMSK Fault Masking bit
If the bit is 1, it will prevent nINTO from being asserted LOW upon FLT = 1.

Bit 6 – HCPEN Short-Circuit Protection Hiccup Mode Enable
If HCPEN = 1, a short-circuit event will cause hiccup-mode response with unlimited Soft-Start retries, without shutting down the other channels. If HCPEN = 0, a short circuit event on the channel will cause immediate shutdown of ALL channels, and a new Start-Up Sequence will automatically be attempted after a 100 ms delay.

Bit 5 – DISCH Active Output Discharge Control
DISCH = 1 enables Active Output Discharge when a channel is turned OFF, DISCH = 0 disables it.

Bit 4 – PHASE Regulator Phase Control
Setting the bit to 1 will cause the regulator to operate 180° out of phase with the oscillator, and clearing the bit to 0 will cause the regulator to operate in phase with the oscillator.

Bits 3:2 – DVSR[1:0] Dynamic Voltage Scaling Rate programming bits

Bit 1 – REN Register Enable Bit
Used in combination with RCON:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

Bit 0 – RCON Register Enable Control Bit
Used in combination with REN:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

2.6.19. Buck2 Active Status

Name: OUT2-A
Address: 0x20
Default: 0b11 (VSET2 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Active Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the Active Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Active Status
Its default value is defined by the resistor at the VSET2 pin during power-on start.

2.6.20. Buck2 Low-Power Mode Status

Name: OUT2-LPM
Address: 0x21
Default: 0b10 (VSET2 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Low-Power Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the Low-Power Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Low-Power Mode Status
Its default value is defined by the resistor at the VSET2 pin during power-on start.

2.6.21. Buck2 HIBERNATE Mode Status

Name: OUT2-HIB
Address: 0x22
Default: 0b10 (VSET2 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the HIBERNATE Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the HIBERNATE Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the HIBERNATE Mode Status
Its default value is defined by the resistor at the VSET2 pin during power-on start.

2.6.22. Buck2 High-Performance Mode Status

Name: OUT2-HPM
Address: 0x23
Default: 0b11 (VSET2 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – EN Enable bit of the High-Performance Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the High-Performance Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the High-Performance Mode Status
Its default value is defined by the resistor at the VSET2 pin during power-on start.

2.6.23. Buck2 Start-up Sequence

Name: OUT2-SEQ
Address: 0x24
Default: 0x59
Property: R/W

Bit	7	6	5	4	3	2	1	0
	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	1	1	0	0	1

Bits 7:6 – SSR[1:0] Soft-Start Rate selection bits

Bits 5:4 – SEQ[1:0] Start-up Sequence Step assignment bits

Bit 3 – SEQEN Start-up Sequence Enable bit
The regulator will NOT start at the assigned step if SEQEN = 0. SSD and POK flags will be neglected during the Start-Up Sequence.

Bits 2:0 – DELAY[2:0] Start-up time delay
The time delay from the completion of the previous Start-Up Sequence Step or Start-Up Event to the turn-ON (beginning of Soft-Start).

2.6.24. Buck2 Configuration

Name: OUT2-CFG
Address: 0x25
Default: 0xA0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0

Bit 7 – FLTMSK Fault Masking bit
If the bit is 1, it will prevent nINTO from being asserted LOW upon FLT = 1.

Bit 6 – HCPEN Short-Circuit Protection Hiccup Mode Enable
If HCPEN = 1, a short-circuit event will cause hiccup-mode response with unlimited Soft-Start retries, without shutting down the other channels. If HCPEN = 0, a short circuit event on the channel will cause immediate shutdown of ALL channels, and a new Start-Up Sequence will automatically be attempted after a 100 ms delay.

Bit 5 – DISCH Active Output Discharge Control
DISCH = 1 enables Active Output Discharge when a channel is turned OFF, DISCH = 0 disables it.

Bit 4 – PHASE Regulator Phase Control
Setting the bit to 1 will cause the regulator to operate 180° out of phase with the oscillator, and clearing the bit to 0 will cause the regulator to operate in phase with the oscillator.

Bits 3:2 – DVSR[1:0] Dynamic Voltage Scaling Rate programming bits

Bit 1 – REN Register Enable Bit
Used in combination with RCON:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

Bit 0 – RCON Register Enable Control Bit
Used in combination with REN:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

2.6.25. Buck3 Active Status

Name: OUT3-A
Address: 0x30
Default: 0b11 (VSET3 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Active Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the Active Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Active Status
Its default value is defined by the resistor at the VSET3 pin during power-on start.

2.6.26. Buck3 Low-Power Mode Status

Name: OUT3-LPM
Address: 0x31
Default: 0b10 (VSET3 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Low-Power Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the Low-Power Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Low-Power Mode Status
Its default value is defined by the resistor at the VSET3 pin during power-on start.

2.6.27. Buck3 HIBERNATE Mode Status

Name: OUT3-HIB
Address: 0x32
Default: 0b00 (VSET3 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the HIBERNATE Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the HIBERNATE Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the HIBERNATE Mode Status
Its default value is defined by the resistor at the VSET3 pin during power-on start.

2.6.28. Buck3 High-Performance Mode Status

Name: OUT3-HPM
Address: 0x33
Default: 0b11 (VSET3 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – EN Enable bit of the High-Performance Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the High-Performance Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the High-Performance Mode Status
Its default value is defined by the resistor at the VSET3 pin during power-on start.

2.6.29. Buck3 Start-up Sequence

Name: OUT3-SEQ
Address: 0x34
Default: 0x69
Property: R/W

Bit	7	6	5	4	3	2	1	0
	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	1	0	1	0	0	1

Bits 7:6 – SSR[1:0] Soft-Start Rate selection bits

Bits 5:4 – SEQ[1:0] Start-up Sequence Step assignment bits

Bit 3 – SEQEN Start-up Sequence Enable bit
The regulator will NOT start at the assigned step if SEQEN = 0. SSD and POK flags will be neglected during the Start-Up Sequence.

Bits 2:0 – DELAY[2:0] Start-up time delay
The time delay from the completion of the previous Start-Up Sequence Step or Start-Up Event to the turn-ON (beginning of Soft-Start).

2.6.30. Buck3 Configuration

Name: OUT3-CFG
Address: 0x35
Default: 0xB0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	1	1	0	0	0	0

Bit 7 – FLTMSK Fault Masking bit
If the bit is 1, it will prevent nINTO from being asserted LOW upon FLT = 1.

Bit 6 – HCPEN Short-Circuit Protection Hiccup Mode Enable
If HCPEN = 1, a short-circuit event will cause hiccup-mode response with unlimited Soft-Start retries, without shutting down the other channels. If HCPEN = 0, a short circuit event on the channel will cause immediate shutdown of ALL channels, and a new Start-Up Sequence will automatically be attempted after a 100 ms delay.

Bit 5 – DISCH Active Output Discharge Control
DISCH = 1 enables Active Output Discharge when a channel is turned OFF, DISCH = 0 disables it.

Bit 4 – PHASE Regulator Phase Control
Setting the bit to 1 will cause the regulator to operate 180° out of phase with the oscillator, and clearing the bit to 0 will cause the regulator to operate in phase with the oscillator.

Bits 3:2 – DVSR[1:0] Dynamic Voltage Scaling Rate programming bits

Bit 1 – REN Register Enable Bit
Used in combination with RCON:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

Bit 0 – RCON Register Enable Control Bit
Used in combination with REN:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

2.6.31. Buck4 Active Status

Name: OUT4-A
Address: 0x40
Default: 0b11 (VSET4 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Active Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the Active Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Active Status
Its default value is defined by the resistor at the VSET4 pin during power-on start.

2.6.32. Buck4 Low-Power Mode Status

Name: OUT4-LPM
Address: 0x41
Default: 0b10 (VSET4 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Low-Power Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the Low-Power Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Low-Power Mode Status
Its default value is defined by the resistor at the VSET4 pin during power-on start.

2.6.33. Buck4 HIBERNATE Mode Status

Name: OUT4-HIB
Address: 0x42
Default: 0b00 (VSET4 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the HIBERNATE Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the HIBERNATE Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the HIBERNATE Mode Status
Its default value is defined by the resistor at the VSET4 pin during power-on start.

2.6.34. Buck4 High-Performance Mode Status

Name: OUT4-HPM
Address: 0x43
Default: 0b11 (VSET4 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	MODE	VSET[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit 7 – EN Enable bit of the High-Performance Mode Status
The regulator is enabled if EN = 1.

Bit 6 – MODE Mode bit of the High-Performance Mode Status
The FPWM Mode is selected if MODE = 1, otherwise (MODE = 0) Auto-PFM is selected.

Bits 5:0 – VSET[5:0] Output voltage selection bits for the High-Performance Mode Status
Its default value is defined by the resistor at the VSET4 pin during power-on start.

2.6.35. Buck4 Start-up Sequence

Name: OUT4-SEQ
Address: 0x44
Default: 0x7A
Property: R/W

Bit	7	6	5	4	3	2	1	0
	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	1	1	1	0	1	0

Bits 7:6 – SSR[1:0] Soft-Start Rate selection bits

Bits 5:4 – SEQ[1:0] Start-up Sequence Step assignment bits

Bit 3 – SEQEN Start-up Sequence Enable bit
The regulator will NOT start at the assigned step if SEQEN = 0. SSD and POK flags will be neglected during the Start-Up Sequence.

Bits 2:0 – DELAY[2:0] Start-up time delay
The time delay from the completion of the previous Start-Up Sequence Step or Start-Up Event to the turn-ON (beginning of Soft-Start).

2.6.36. Buck4 Configuration

Name: OUT4-CFG
Address: 0x45
Default: 0xA0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0

Bit 7 – FLTMSK Fault Masking bit
If the bit is 1, it will prevent nINTO from being asserted LOW upon FLT = 1.

Bit 6 – HCPEN Short-Circuit Protection Hiccup Mode Enable
If HCPEN = 1, a short-circuit event will cause hiccup-mode response with unlimited Soft-Start retries, without shutting down the other channels. If HCPEN = 0, a short circuit event on the channel will cause immediate shutdown of ALL channels, and a new Start-Up Sequence will automatically be attempted after a 100 ms delay.

Bit 5 – DISCH Active Output Discharge Control
DISCH = 1 enables Active Output Discharge when a channel is turned OFF, DISCH = 0 disables it.

Bit 4 – PHASE Regulator Phase Control
Setting the bit to 1 will cause the regulator to operate 180° out of phase with the oscillator, and clearing the bit to 0 will cause the regulator to operate in phase with the oscillator.

Bits 3:2 – DVSR[1:0] Dynamic Voltage Scaling Rate programming bits

Bit 1 – REN Register Enable Bit
Used in combination with RCON:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

Bit 0 – RCON Register Enable Control Bit
Used in combination with REN:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

2.6.37. LDO1 Active Status

Name: LDO1-A
Address: 0x50
Default: 0b10 (VSETL1 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	Reserved	VSET[5:0]					
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Active Status
The regulator is enabled if EN = 1.

Bit 6 – Reserved
Maintain as '0'

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Active Status
Its default value is defined by the resistor at the VSETL1 pin during power-on start.

2.6.38. LDO1 Low-Power Mode Status

Name: LDO1-LPM
Address: 0x51
Default: 0b10 (VSETL1 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	Reserved	VSET[5:0]					
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Low-Power Mode Status
The regulator is enabled if EN = 1.

Bit 6 – Reserved
Maintain as '0'

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Low-Power Mode Status
Its default value is defined by the resistor at the VSETL1 pin during power-on start.

2.6.39. LDO1 HIBERNATE Mode Status

Name: LDO1-HIB
Address: 0x52
Default: 0b00 (VSETL1 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	Reserved	VSET[5:0]					
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the HIBERNATE Mode Status
The regulator is enabled if EN = 1.

Bit 6 – Reserved
Maintain as '0'

Bits 5:0 – VSET[5:0] Output voltage selection bits for the HIBERNATE Mode Status
Its default value is defined by the resistor at the VSETL1 pin during power-on start.

2.6.40. LDO1 High-Performance Mode Status

Name: LDO1-HPM
Address: 0x53
Default: 0b10 (VSETL1 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	Reserved	VSET[5:0]					
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the High-Performance Mode Status
The regulator is enabled if EN = 1.

Bit 6 – Reserved
Maintain as '0'

Bits 5:0 – VSET[5:0] Output voltage selection bits for the High-Performance Mode Status
Its default value is defined by the resistor at the VSETL1 pin during power-on start.

2.6.41. LDO1 Start-up Sequence

Name: LDO1-SEQ
Address: 0x54
Default: 0x4A
Property: R/W

Bit	7	6	5	4	3	2	1	0
	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	0	1	0	1	0

Bits 7:6 – SSR[1:0] Soft-Start Rate selection bits

Bits 5:4 – SEQ[1:0] Start-up Sequence Step assignment bits

Bit 3 – SEQEN Start-up Sequence Enable bit
The regulator will NOT start at the assigned step if SEQEN = 0. SSD and POK flags will be neglected during the Start-Up Sequence.

Bits 2:0 – DELAY[2:0] Start-up time delay
The time delay from the completion of the previous Start-Up Sequence Step or Start-Up Event to the turn-ON of the LDO (beginning of Soft-Start).

2.6.42. LDO1 Configuration

Name: LDO1-CFG
Address: 0x55
Default: 0xA0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	FLTMSK	Reserved	DISCH	Reserved	DVSR[1:0]		REN	RCON
Access	R/W	R	R/W	R	R/W	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0

Bit 7 – FLTMSK Fault Masking bit
If the bit is 1, it will prevent nINTO from being asserted LOW upon FLT = 1.

Bit 6 – Reserved
Maintain as '0'

Bit 5 – DISCH Active Output Discharge Control
DISCH = 1 enables Active Output Discharge when a channel is turned OFF, DISCH = 0 disables it.

Bit 4 – Reserved
Maintain as '0'

Bits 3:2 – DVSR[1:0] Dynamic Voltage Scaling Rate programming bits.

Bit 1 – REN Register Enable Bit
Used in combination with RCON:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

Bit 0 – RCON Register Enable Control Bit
Used in combination with REN:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

2.6.43. LDO2 Active Status

Name: LDO2-A
Address: 0x60
Default: 0b10 (VSETL2 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	Reserved	VSET[5:0]					
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Active Status
The regulator is enabled if EN = 1.

Bit 6 – Reserved
Maintain as '0'

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Active Status
Its default value is defined by the resistor at the VSETL2 pin during power-on start.

2.6.44. LDO2 Low-Power Mode Status

Name: LDO2-LPM
Address: 0x61
Default: 0b10 (VSETL2 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	Reserved	VSET[5:0]					
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the Low-Power Mode Status
The regulator is enabled if EN = 1.

Bit 6 – Reserved
Maintain as '0'

Bits 5:0 – VSET[5:0] Output voltage selection bits for the Low-Power Mode Status
Its default value is defined by the resistor at the VSETL2 pin during power-on start.

2.6.45. LDO2 HIBERNATE Mode Status

Name: LDO2-HIB
Address: 0x62
Default: 0b00 (VSETL2 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	Reserved	VSET[5:0]					
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the HIBERNATE Mode Status
The regulator is enabled if EN = 1.

Bit 6 – Reserved
Maintain as '0'

Bits 5:0 – VSET[5:0] Output voltage selection bits for the HIBERNATE Mode Status
Its default value is defined by the resistor at the VSETL2 pin during power-on start.

2.6.46. LDO2 High-Performance Mode Status

Name: LDO2-HPM
Address: 0x63
Default: 0b10 (VSETL2 pin definition)
Property: R/W

Bit	7	6	5	4	3	2	1	0
	EN	Reserved	VSET[5:0]					
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit 7 – EN Enable bit of the High-Performance Mode Status
The regulator is enabled if EN = 1.

Bit 6 – Reserved
Maintain as '0'

Bits 5:0 – VSET[5:0] Output voltage selection bits for the High-Performance Mode Status
Its default value is defined by the resistor at the VSETL2 pin during power-on start.

2.6.47. LDO2 Start-up Sequence

Name: LDO2-SEQ
Address: 0x64
Default: 0x4B
Property: R/W

Bit	7	6	5	4	3	2	1	0
	SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	0	1	0	1	1

Bits 7:6 – SSR[1:0] Soft-Start Rate selection bits

Bits 5:4 – SEQ[1:0] Start-up Sequence Step assignment bits

Bit 3 – SEQEN Start-up Sequence Enable bit
The regulator will NOT start at the assigned step if SEQEN = 0. SSD and POK flags will be neglected during the Start-Up Sequence.

Bits 2:0 – DELAY[2:0] Start-up time delay
The time delay from the completion of the previous Start-Up Sequence Step or Start-Up Event to the turn-ON of the LDO (beginning of Soft-Start).

2.6.48. LDO2 Configuration

Name: LDO2-CFG
Address: 0x65
Default: 0xA0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	FLTMSK	Reserved	DISCH	Reserved	DVSR[1:0]		REN	RCON
Access	R/W	R	R/W	R	R/W	R/W	R/W	R/W
Default	1	0	1	0	0	0	0	0

Bit 7 – FLTMSK Fault Masking bit
If the bit is 1, it will prevent nINTO from being asserted LOW upon FLT = 1.

Bit 6 – Reserved
Maintain as '0'

Bit 5 – DISCH Active Output Discharge Control
DISCH = 1 enables Active Output Discharge when a channel is turned OFF, DISCH = 0 disables it.

Bit 4 – Reserved
Maintain as '0'

Bits 3:2 – DVSR[1:0] Dynamic Voltage Scaling Rate programming bits.

Bit 1 – REN Register Enable Bit
Used in combination with RCON:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

Bit 0 – RCON Register Enable Control Bit
Used in combination with REN:
If RCON = 0, the value of REN has no effect.
If RCON = 1, setting REN = 1 enables channel and setting REN = 0 disables it, regardless of the current Status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

2.6.49. Default Registers Content

MCP16503 has the following default registers content: (default means after initialization of the IC after power on reset):

Register Name	Register Address	MCP16503 Default Register Contents
SYS-ADR	**0x00**	0xDA
SYS-ID	**0x01**	0x60
SYS-TMG	**0x02**	0x12
SYS-CFG	**0x03**	0xC0
STS-SYS	**0x04**	0x00
STS-B1	**0x05**	0x00
STS-B2	**0x06**	0x00
STS-B3	**0x07**	0x00
STS-B4	**0x08**	0x00
STS-L1	**0x09**	0x00
STS-L2	**0x0A**	0x00
OUT1-A	**0x10**	0b11 (VSET1 pin definition)
OUT1-LPM	**0x11**	0b10 (VSET1 pin definition)
OUT1-HIB	**0x12**	0b00 (VSET1 pin definition)
OUT1-HPM	**0x13**	0b11 (VSET1 pin definition)
OUT1-SEQ	**0x14**	0x49
OUT1-CFG	**0x15**	0xB0
OUT2-A	**0x20**	0b11 (VSET2 pin definition)
OUT2-LPM	**0x21**	0b10 (VSET2 pin definition)
OUT2-HIB	**0x22**	0b10 (VSET2 pin definition)
OUT2-HPM	**0x23**	0b11 (VSET2 pin definition)
OUT2-SEQ	**0x24**	0x59
OUT2-CFG	**0x25**	0xA0
OUT3-A	**0x30**	0b11 (VSET3 pin definition)
OUT3-LPM	**0x31**	0b10 (VSET3 pin definition)
OUT3-HIB	**0x32**	0b00 (VSET3 pin definition)
OUT3-HPM	**0x33**	0b11 (VSET3 pin definition)
OUT3-SEQ	**0x34**	0x69
OUT3-CFG	**0x35**	0xB0
OUT4-A	**0x40**	0b11 (VSET4 pin definition)
OUT4-LPM	**0x41**	0b10 (VSET4 pin definition)
OUT4-HIB	**0x42**	0b00 (VSET4 pin definition)
OUT4-HPM	**0x43**	0b11 (VSET4 pin definition)
OUT4-SEQ	**0x44**	0x7A
OUT4-CFG	**0x45**	0xA0
LDO1-A	**0x50**	0b10 (VSETL1 pin definition)
LDO1-LPM	**0x51**	0b10 (VSETL1 pin definition)
LDO1-HIB	**0x52**	0b00 (VSETL1 pin definition)
LDO1-HPM	**0x53**	0b10 (VSETL1 pin definition)
LDO1-SEQ	**0x54**	0x4A
LDO1-CFG	**0x55**	0xA0
LDO2-A	**0x60**	0b10 (VSETL2 pin definition)
LDO2-LPM	**0x61**	0b10 (VSETL2 pin definition)

Default Registers Content (continued)		
Register Name	**Register Address**	**MCP16503 Default Register Contents**
LDO2-HIB	**0x62**	0b00 (VSETL2 pin definition)
LDO2-HPM	**0x63**	0b10 (VSETL2 pin definition)
LDO2-SEQ	**0x64**	0x4B
LDO2-CFG	**0x65**	0xA0

2.7. I²C Interface Description

The MCP16503 is a fast-plus mode device, supporting data transfers at up to 1 Mbit/s as described in the I²C Bus specification.

The MCP16503 is a target-only device without clock-stretching capability.

The MCP16503 assumes that the I²C logic levels on the bus are generated by a device operating from a nominal supply voltage of 3.3V (with ±10% tolerance). This is typically the I/O voltage generated by Buck1 (VDDIO). Therefore, V_{IH} and V_{IL} levels are not related to the SVIN voltage value. The SDA and SCL lines should not be pulled up to the MCP16503 SVIN voltage, but to the VDDIO voltage I²C host interface supply voltage (3.3V nominal).

The MCP16503 I²C interface is always accessible, even in the OFF state, as long as the SVIN pin is powered and above the UVLO threshold. Note that in the OFF state, the VDDIO voltage from Buck1 is turned off and therefore the I²C pull-up voltage rail must be provided externally.

2.7.1. Device Address

The MCP16503 uses 7-bit address (0x5A by default).

2.7.2. Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the host generates an extra acknowledge related clock pulse. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse; setup and hold times must be taken into account.

A target receiver which is addressed must generate an acknowledge after the reception of each byte.

Also, a host receiver must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter, except on the last received byte. A host receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target transmitter. In this event, the transmitter must leave the data line HIGH to enable the host to generate a STOP condition.

2.7.3. Bus Transactions

2.7.3.1. Single Write

The first seven bits of the first byte make up the target address. The eighth bit is the LSB (least significant bit). It determines the direction of the message (R/W). A ‘zero’ in the least significant position of the first byte means that the host will write information to a selected target. A ‘one’ in this position means that the host will read information from the target. When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the host as a target-receiver or target-transmitter, depending on the R/W bit.

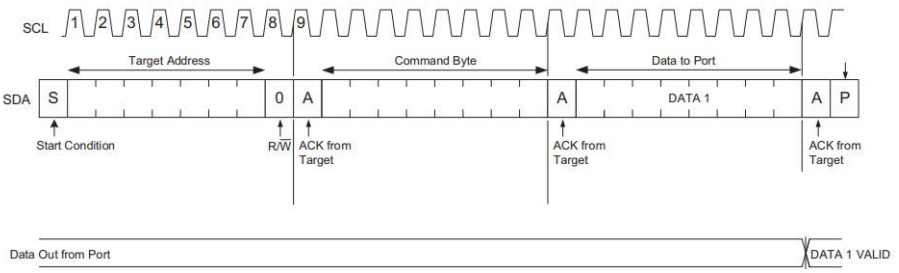
Command byte is a data byte which selects a register on the device (address of the register that needs to be written).

The data to port is the 8-bit data that needs to be written to the selected register. This is followed by the acknowledge from the target and then the STOP condition.

The write command is as follows, and it is illustrated in the timing diagram below.

1. Send START sequence
2. Send 7-bit target address
3. Send the R/W bit – 0 to indicate a write operation
4. Wait for Acknowledge from the target
5. Send the command byte - Address that needs to be written
6. Wait for acknowledge from the target
7. Receive the 8-bit data from the host and write it to the target register indicated in step 5 starting from MSB
8. Acknowledge from the target
9. Send STOP sequence

Figure 2-12. I²C Single Write



Note: Writing to a read-only register, a non-existing or not user-accessible register will still generate an ACK by the MCP16503 after the command byte, but it will have no effect.

2.7.3.2. Block Write (Auto Increment Mode)

The MCP16503 can receive multiple data bytes after a single address byte and automatically increments its register pointer to block fill internal volatile registers. This command writes the first data byte to register that is specified through the command byte and all the following data bytes to the subsequent registers.

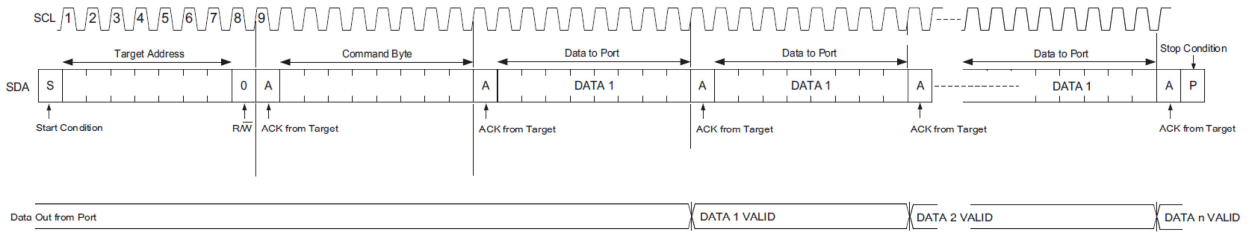
Byte data are latched after individual bytes are received, so multi-byte transfers could be corrupted if interrupted mid-stream.

The Block/Auto increment write command is as follows:

1. Send START sequence
2. Send 7-bit target address
3. Send the R/W bit – 0 to indicate a write operation
4. Wait for Acknowledge from the target
5. Send the command byte – First register address that needs to be written
6. Wait for acknowledge from the target.
7. Receive the 8-bit data from the host and write it to the target register indicated in step 5 starting from MSB.
8. Acknowledge from the target.
9. Receive the 8-bit data from the host and write it to the next target register address, starting from MSB.

10. Acknowledge from the target.
11. Repeat steps 9 and 10 until the entire data is sent.
12. Send STOP sequence.

Figure 2-13. I²C Block Write



In Block Write, the register order will be automatically incremented by one step, regardless of the register order. So, for example after writing to register location 0x15, the next register to be written will be 0x16, not 0x20.

Writing to non-existent or not accessible registers addresses will still generate an ACK by the MCP16503 after the command byte, but it will have no effect.

Note that if the host keeps writing data beyond the last register location, the MCP16503 will still generate an ACK on each received byte, but those data will not have any effect on the MCP16503 (i.e. disregarded). There is no register address wrap-around.

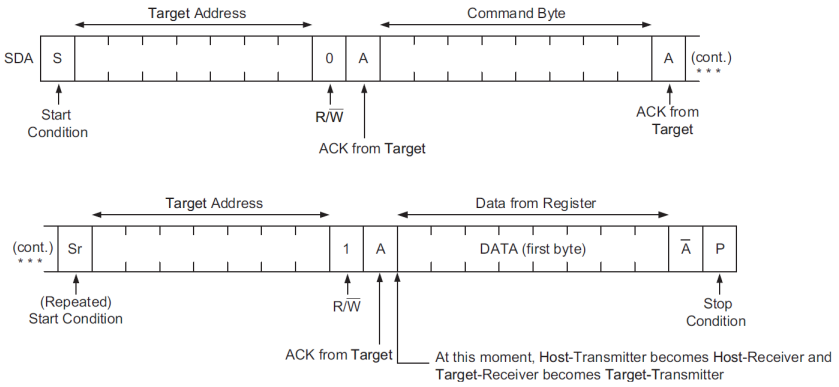
2.7.3.3. Single Read

This reads a single byte from a device, from a designated register. The register is specified through the Command byte.

The read command is as follows, and it is illustrated in the timing diagram below.

1. Send START sequence
2. Send 7-bit target address
3. Send the R/W bit – 0 to indicate a write operation
4. Wait for Acknowledge from the target
5. Send the register address that needs to be read
6. Wait for acknowledge from the target
7. Send START sequence again (Repeated Start condition)
8. Send the 7-bit target address
9. Send R/W bit – 1 to indicate a read operation
10. Wait for Acknowledge from the target
11. Receive the 8-bit data from the target starting from MSB
12. Acknowledge from the host
13. Send STOP sequence

Figure 2-14. I²C Single Read



If the Host attempts to read from an invalid register location, the MCP16503 will send out 0xFF data (all "1").

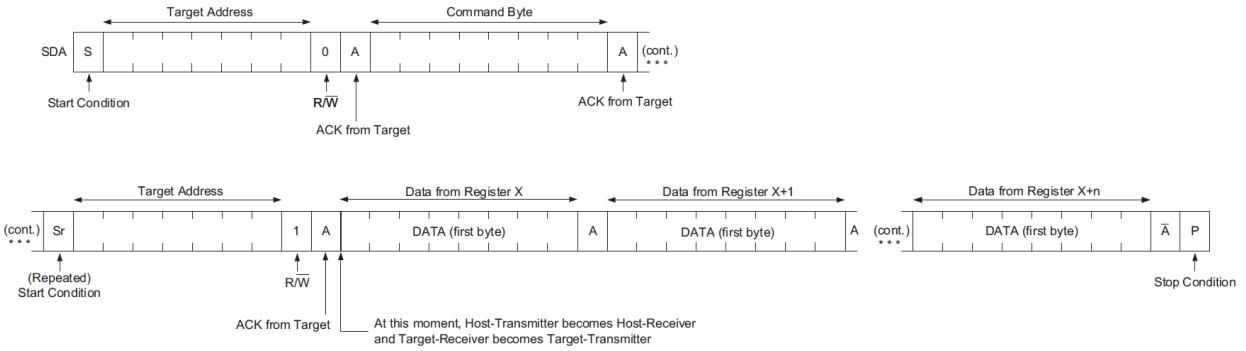
2.7.3.4. Block Read (Auto Increment Mode)

This command reads a block of bytes, starting from a designated register that is specified through the command byte. The address gets incremented by one automatically, and the registers are read in order starting from the address provided by the command byte.

The Block/Auto increment read command is as follows, and it is illustrated in the following timing diagram.

1. Send START sequence
2. Send 7-bit target address
3. Send the R/W bit – 0 to indicate a write operation
4. Wait for Acknowledge from the target
5. Send the command byte – Initial address that needs to be read.
6. Wait for acknowledge from the target
7. Send START sequence again (repeated START Sr)
8. Send the 7-bit target address
9. Send R/W bit – 1 to indicate a read operation
10. Wait for Acknowledge from the target
11. Receive the 8-bit data from the target register indicated in step 5 starting from MSB
12. Acknowledge from the host receiver.
13. Receive the 8-bit data from the next register starting from MSB
14. Acknowledge from the host receiver.
    Note: on the last byte, the host receiver issues a NACK in place of ACK to signal the end of the data transfer.
15. Repeat steps 13&14 until last byte.
16. STOP sequence is sent.

Figure 2-15. I²C Block Read



In Block Read, the register order will be automatically incremented by one step regardless of the register order. So, for example, after reading from register location 0x15, the next register address to be read will be 0x16, not 0x20.

Reading from non-existent or not accessible registers addresses will stream out 0xFF.

Also note that if the host keeps reading data beyond the last register location, the MCP16503 streams out 0xFF (all "1"s). There is no register address wrap-around.

In Block Read auto-increment mode, the host receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the host to generate a STOP condition.

2.7.3.5. I²C Interface Disable

While not necessary in a well-designed implementation, the MCP16503 also supports I²C interface disabling.

This is achieved by issuing three separated Single Write commands as follows (ADDRESS equals the device address in 7-bit format, default = 0x5A):

1. ADDRESS = 0x5A, COMMAND = 0xEA, DATA = 0xBD
2. ADDRESS = 0x5A, COMMAND = 0xE9, DATA = 0xBD
3. ADDRESS = 0x5A, COMMAND = 0xEC, DATA = 0xBD

Upon ACK of the last byte, the I²C interface will no longer respond to the device address or any other bus transaction.

To enable the I²C interface again, power (SVIN) must be cycled.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

SVIN to SGND	−0.3V to 6V
Power Supply Voltage Pins PVINx to EPGND	−0.3V to 6V
OUTx Sense Pins to SGND	−0.3V to 6V
LVIN to SGND	−0.3V to V_{SVIN}+0.3V
Output Switch Voltage SWx to EPGND	−0.3V to V_{PVINx}+0.3V
EPGND to SGND	−0.3V to +0.3V
VSET1, VSET2, VSET3, VSET4, VSETL1, VSETL2 to SGND	−0.3V to V_{SVIN}+0.3V
EN, SDA, SCL, LPM, HPM, PWRHLD, nRSTO, nSTRTO, nINTO to SGND	−0.3V to 6V
Maximum Junction Temperature	150°C
Storage Temperature	−65°C to 150°C
ESD Protection on all pins:	
HBM	2 kV
MM	200V
CDM	750V

⚠ WARNING Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2. DC/AC Characteristics

$T_A = T_J$ = +25°C; VIN = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 1.5 µH; COUT1 = COUT2 = COUT3 = COUT4 = 22 µF, unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
System Input Supply						
Supply Voltage Range	V_{IN}	**2.7**	—	**5.5**	V	—
Undervoltage Lockout Threshold	V_{UVLO_TH}	**2.4**	2.55	**2.7**	V	EN and PWRHLD tied to VIN
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	—	125	—	mV	—
Shutdown (OFF) Current	I_{SHDN}	—	—	**13**	µA	EN = PWRHLD = LPM = HPM = 0, nRSTO, nSTRTO, nINTO floating, VIN = 5.5V
	I_{SHDN_105}	—	—	10	µA	EN = PWRHLD = LPM = HPM = 0, nRSTO, nINTO floating, VIN = 4.5V, T_J = −40 to 105°C (Note 1)

Notes:

1. Maximum limit for T_J = −40°C to +125°C based on characterization data.
2. Not production tested.

DC/AC Characteristics (continued)

T_A = T_J = +25°C; VIN = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 1.5 µH; COUT1 = COUT2 = COUT3 = COUT4 = 22 µF, unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
HIBERNATE Mode Operational Quiescent Current (switching, buck2 ON, Note 2)	I_{QOP_HIB2}	—	165	—	µA	I_{OUT2} = 0mA, buck2 ON (V_{OUT2} = 1.2V), all other channels OFF, EN = LPM = 1, PWRHLD = HPM = 0
Low-Power Mode Operational Quiescent Current (switching, Note 2)	I_{QOP_LPM}	—	290	—	µA	IOUTx = 0mA, all channels ON, EN = PWRHLD = LPM = 1, HPM = 0
Active Mode Operational Quiescent Current (switching, Note 2)	I_{QOP_ACT}	—	16	—	mA	IOUTx = 0mA, all channels enabled, EN = PWRHLD = 1, LPM = HPM = 0
High-Performance Active Mode Operational Quiescent Current (switching, Note 2)	I_{QOP_HPM}	—	16	—	mA	IOUTx = 0mA, all channels enabled, EN = PWRHLD = HPM = 1, LPM = 0
Timebase						
Timebase Accuracy	ACC_TB	**–10**	—	**+10**	%	FSD[1:0] = 00, 01
Thermal Protection and Warning						
Overtemperature Shutdown Threshold (Note 2)	T_{TSD}	—	160	—	°C	Bit TSD to 1
Overtemperature Shutdown Hysteresis (Note 2)	T_{TSD_HYS}	—	20	—	°C	Bit TSD to 0
Overtemperature Warning Threshold (Note 2)	T_{TWR}	—	135	—	°C	Bit TWR to1
Overtemperature Warning Hysteresis (Note 2)	T_{TWR_HYS}	—	10	—	°C	Bit TWR to 0

Notes:

1. Maximum limit for T_J = −40°C to +125°C based on characterization data.
2. Not production tested.

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; V_{OUT1} = 3.3V, L1 = 1.5 µH; C_{OUT1} = 22 µF, unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Buck1						
Input Operating Voltage Range	V_{PVIN1}	**2.7**	—	**5.5**	V	—
Output Voltage Range	V_{OUT1}	1.2	—	3.7	V	—
Output Voltage Step	V_{step}	—	50	—	mV	—
PVIN1 Shutdown Current	I_{PVIN1_SHDN}	—	0.05	**2**	µA	Regulator disabled, PVIN1 = 5V

Note:

1. Not production tested.

DC/AC Characteristics (continued)

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; V_{OUT1} = 3.3V, L1 = 1.5 µH; C_{OUT1} = 22 µF, unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Operational Quiescent Current, AutoPFM, default setting (Note 1)	I_{QOP_PFM1}	—	45	—	µA	I_{OUT1} = 0mA, Auto PFM EN = PWRHLD = LPM = 1, HPM = 0 B1HCEN = 0 (default) ΔI_Q for buck1 activated
Operational Quiescent Current, AutoPFM + HCM (Note 1)	I_{QOP_HCM}	—	47	—	µA	I_{OUT1} = 0mA, Auto PFM PWRHLD = LPM = 1, HPM = 0, B1HCEN = 1 ΔI_Q for buck1 activated
Output Voltage Accuracy, FPWM	ACC_OUT_{PWM1}	**–2**	—	**+2**	%	I_{OUT1} = 0mA
Output Voltage Accuracy, Auto-PFM	ACC_OUT_{PFM1}	**–2**	—	**+2**	%	I_{OUT1} = 0mA B1HCEN = 0
Output Voltage Line Regulation (Note 1)	$LINE\_REG_{PWM1}$	—	0.03	—	%	I_{OUT1} = 0mA, FPWM, V_{IN} = PVIN1 = SVIN = 3.6V to 5.5V
	$LINE\_REG_{PFM1}$	—	0.07	—		I_{OUT1} = 0mA, Auto PFM, V_{IN} = PVIN1 = SVIN = 3.6V to 5.5V
Output Voltage Load Regulation (Note 1)	$LOAD\_REG_{PWM1}$	—	0.3	—	%	I_{OUT1} = 0A to 1A, FPWM
	$LOAD\_REG_{PFM1}$	—	0.5	—		I_{OUT1} = 0A to 1A, Auto PFM
Hysteretic Control Mode Upper Regulation Threshold, Auto-PFM	HCM_TH	**1.7**	2.9	**4.3**	%	I_{OUT1} = 0mA EN = PWRHLD = LPM = 1, HPM = 0 B1HCEN = 1 SVIN = PVIN1 = 1.06 V_{OUT1_NOM} OUT1 rising, % of V_{OUT1_NOM}
Hysteretic Control Mode Disable Threshold, Auto-PFM	HCM_DIS	—	11.1	—	%	I_{OUT1} = 0mA EN = PWRHLD = LPM = 1, HPM = 0 B1HCEN = 1 SVIN = PVIN1 rising, % of V_{OUT1_NOM}
Hysteretic Control Mode Enable Threshold, Auto-PFM	HCM_EN	**5**	9	**13**	%	I_{OUT1} = 0mA EN = PWRHLD = LPM = 1, HPM = 0 B1HCEN = 1 SVIN = PVIN1 falling, % of V_{OUT1_NOM}
Switching Frequency	f_{sw}	**1.8**	2	**2.2**	MHz	FPWM, FSD[1:0] = 00,01
Switching Frequency Displacement	FSD_10	—	−16.5	—	%	FPWM, FSD[1:0] = 10
	FSD_11	—	+16.5	—	%	FPWM, FSD[1:0] = 11
Maximum Duty Cycle	D_{MAX}	100	—	—	%	Functionality test
Minimum ON Time	T_{ON_MIN1}	—	35	—	ns	FPWM
High-Side Switch ON-Resistance	R_{DsonP1}	—	140	160	mΩ	PVIN1 = SVIN = 5V
Low-Side Switch ON-Resistance	R_{DsonN1}	—	120	140	mΩ	PVIN1 = SVIN = 5V

Note:

1. Not production tested.

DC/AC Characteristics (continued)

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; V_{OUT1} = 3.3V, L1 = 1.5 µH; C_{OUT1} = 22 µF, unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
POK (Power OK) Threshold	POK_TH1	**90**	92.5	**95**	%	OUT1 rising, % of V_{OUT1_NOM}
POK Hysteresis	POK_HYS1	—	4	—	%	OUT1 falling, % of V_{OUT1_NOM}
Start-up POK Bypass Threshold	$V_{POKB\_TH\_B1}$	**-**	615	**-**	mV	PVIN1-OUT1, OUT1 rising, PVIN1 = 3.0V, V_{OUT1_NOM} = 3.3V
Start-up POK Bypass Threshold Hysteresis	$V_{POKB\_HYS\_B1}$	—	50	—	mV	OUT1 falling, PVIN1 = 3.0V
Soft-start Rate (switching frequency clock cycles per DAC step)	SSR_00	—	16	—	cycles/ step	SSR[1:0] = 00 - default
	SSR_01	—	32	—		SSR[1:0] = 01
	SSR_10	—	48	—		SSR[1:0] = 10
	SSR_11	—	64	—		SSR[1:0] = 11
Dynamic Voltage Scaling Rate (switching frequency clock cycles per DAC step)	DVSR_00	—	16	—	cycles/ step	DVSR[1:0] = 00 - default
	DVSR_01	—	32	—		DVSR[1:0] = 01
	DVSR_10	—	48	—		DVSR[1:0] = 10
	DVSR_11	—	64	—		DVSR[1:0] = 11
High-Side Peak Current Limit (Cycle by Cycle)	I_{LIM_HS1}	**1.2**	1.8	**2.6**	A	—
Current Limit frequency foldback V_{OUT1} threshold	V_{TH_FFB1}	—	615	—	mV	—
Hiccup-Mode Short Circuit protection wait time	t_{HICCUP}	—	3x Soft-start Time	—		—
Low-side Negative Peak Current Limit (FPWM)	I_{LIM_NEG1}	−1.4	−1	−0.8	A	—
Zero Current Detection threshold	I_{ZCD1}	0	50	120	mA	—
Active Discharge Resistance	R_{DISCH_OUT1}	—	25	—	Ω	DISCH = 1, Enabled when regulator disabled

Note:

1. Not production tested.

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; V_{OUT2} = 1.8V, V_{OUT3} = 1.1V, V_{OUT4} = 1.1V; L2 = L3 = L4 = 1.5 µH; COUT2 = COUT3 = COUT4 = 22 µF, unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol (x = 2,3,4)	Min.	Typ.	Max.	Units	Conditions
Buck2, buck3, buck4						
Input Operating Voltage Range	V_{PVINx}	**2.7**	—	**5.5**	V	—
Output Voltage Range	V_{OUTx}	0.6	—	1.85	V	—
Output Voltage Step	V_{step}	—	25	—	mV	—
PVINx Shutdown Current	I_{PVINx_SHDN}	—	0.05	**2**	µA	Regulator disabled, PVINx = 5V
Operational Quiescent Current AutoPFM (Note 1)	I_{QOP_PFMx}	—	45	—	µA	I_{OUTx} = 0mA, Auto PFM EN = PWRHLD = LPM = 1, HPM = 0 ΔI_Q for one buck activated

Note:

1. Not production tested.

DC/AC Characteristics (continued)

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; V_{OUT2} = 1.8V, V_{OUT3} = 1.1V, V_{OUT4} = 1.1V; L2 = L3 = L4 = 1.5 µH; COUT2 = COUT3 = COUT4 = 22 µF, unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol (x = 2,3,4)	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy, FPWM	ACC_OUT_{PWMx}	**–1**	—	**+1**	%	I_{OUTx} = 0mA, 0.9V≤V_{OUTx} ≤1.3V
		–1.5	—	**+1.5**		I_{OUTx} = 0mA, V_{OUTx} <0.9V or V_{OUTx} >1.3V
Output Voltage Accuracy, Auto-PFM	ACC_OUT_{PFMx}	**–1**	—	**+1**	%	I_{OUTx} = 0mA, 0.9V≤V_{OUTx} ≤1.3V
		–1.5	—	**+1.5**		I_{OUTx} = 0mA, V_{OUTx} <0.9V or V_{OUTx} >1.3V
Output Voltage Line Regulation (Note 1)	$LINE\_REG_{PWMx}$	—	0.03	—	%	I_{OUT1} = 0mA, FPWM, V_{IN} = PVIN1 = SVIN = 3.6V to 5.5V
	$LINE\_REG_{PFMx}$	—	0.07	—		I_{OUT1} = 0 mA, Auto PFM, V_{IN} = PVIN1 = SVIN = 3.6V to 5.5V
Output Voltage Load Regulation (Note 1)	$LOAD\_REG_{PWMx}$	—	0.3	—	%	I_{OUTx} = 0A to 1A, FPWM
	$LOAD\_REG_{PFMx}$	—	0.5	—		I_{OUTx} = 0A to 1A, Auto PFM
Switching Frequency	f_{sw}	**1.8**	2	**2.2**	MHz	FPWM, FSD[1:0] = 00,01
Switching frequency displacement	FSD_10	—	–16.5	—	%	FPWM, FSD[1:0] = 10
	FSD_11	—	16.5	—	%	FPWM, FSD[1:0] = 11
Maximum Duty Cycle	D_{MAX}	100	—	—	%	Functionality test
Minimum ON Time	T_{ON_MINx}	—	35	—	ns	FPWM
High-Side Switch ON-Resistance	R_{DSonPx}	—	140	160	mΩ	PVINx = SVIN = 5V
Low-Side Switch ON-Resistance	R_{DSonNx}	—	120	140	mΩ	PVINx = SVIN = 5V
POK (Power OK) Threshold	POK_THx	**90**	92.5	**95**	%	OUTx rising, % of $V_{OUTx(NOM)}$
POK hysteresis	POK_HYSx	—	4	—	%	OUTx falling, % of $V_{OUTx(NOM)}$
Soft-start Rate (switching frequency clock cycles per DAC step)	SSR_00	—	16	—	cycles / step	SSR[1:0] = 00 - default
	SSR_01	—	32	—		SSR[1:0] = 01
	SSR_10	—	48	—		SSR[1:0] = 10
	SSR_11	—	64	—		SSR[1:0] = 11
Dynamic Voltage Scaling Rate (switching frequency clock cycles per DAC step)	DVSR_00	—	16	—	Cycles step	DVSR[1:0] = 00 - default
	DVSR_01	—	32	—		DVSR[1:0] = 01
	DVSR_10	—	48	—		DVSR[1:0] = 10
	DVSR_11	—	64	—		DVSR[1:0] = 11
High-Side Peak Current Limit (Cycle by Cycle)	I_{LIM_HSx}	**1.2**	1.8	**2.6**	A	—
Current Limit Frequency Fold-back V_{OUTx} Threshold	V_{TH_FFBx}	—	615	—	mV	—
Hiccup-mode Short Circuit Protection Wait Time	t_{HICCUP}	—	3 × Soft-start Time	—		—
Low-side Negative Peak Current Limit (FPWM)	I_{LIM_NEGx}	–1.4	–1	–0.8	A	—
Zero Current Detection Threshold	I_{ZCDx}	0	33	120	mA	—
Active Discharge Resistance	R_{DISCH_OUTx}	—	25	—	Ω	DISCH = 1, Enabled when regulator disabled

Note:

1. Not production tested.

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; $V_{LOUT1,2}$ = 3.3V; $C_{LOUT1,2}$ = 2.2 µF ($I_{LOUT1,2}$ ≤ 150 mA) or 4.7 µF ($I_{LOUT1,2}$ ≤ 300 mA), unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.						
Parameters	**Symbol (x = 1,2)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
LDO1, LDO2						
Input Operating Voltage Range	V_{LVIN}	**2.7**	—	**5.5**	V	—
Output Voltage Range	V_{LOUTx}	1.2	—	3.7	V	—
Output Voltage Step	V_{step}	—	50	—	mV	—
Stable Output Capacitor Range (Note 1)	C_{LOUTx}	2.2	—	20	µF	$I_{LOUT1,2}$ ≤ 150 mA – application requirement
		4.7	—	20	µF	$I_{LOUT1,2}$ ≤ 300 mA – application requirement
LVIN Shutdown Current	I_{LVIN_SHDN}	—	—	**2**	µA	LDOs disabled, LVIN = 5V
Operational Quiescent Current	I_{LVIN_Qx}	—	40	—	µA	$I_{LOUT1,2}$ = 0 mA, one LDO block
Output Voltage Accuracy	ACC_LOUTx	**–2**	—	**+2**	%	LVIN = SVIN = 3.6V $I_{LOUT1,2}$ = 0.1 mA
Dropout Voltage (Note 2)	V_{DOx}	—	170	**500**	mV	$I_{LOUT1,2}$ = 300 mA
Output Voltage Line Regulation	LINE_REGx	—	0.024	—	%	LVIN = SVIN = 3.6V to 5.5V $I_{LOUT1,2}$ = 0.1 mA
Output Voltage Load Regulation	LOAD_REGx	—	0.3	—	%	$I_{LOUT1,2}$ = 0.1 mA to 300 mA
PSRR	PSRRx	—	63	—	dB	f = 1kHz, I_{OUT} = 20 mA, $V_{LOUT1,2}$ = 1.8V, SVIN and LVIN modulated
		—	63	—	dB	f = 1kHz, I_{OUT} = 20 mA, $V_{LOUT1,2}$ = 1.8V, SVIN = 5V, LVIN modulated
		—	46	—	dB	f = 10kHz, I_{OUT} = 20 mA, $V_{LOUT1,2}$ = 1.8V, SVIN and LVIN modulated
		—	47	—	dB	f = 10kHz, I_{OUT} = 20 mA, $V_{LOUT1,2}$ = 1.8V, SVIN = 5V, LVIN modulated
POK (Power OK) Threshold	POK_THL	**90**	92.3	**95**	%	LOUT1,2 rising, % of $V_{LOUT1,2(NOM)}$
POK Hysteresis	POK_HYSL	—	4	—	%	LOUT1,2 falling, % of $V_{LOUT1,2(NOM)}$
Start-up POK Bypass Threshold	$V_{POKB\_TH\_Lx}$	—	—	**670**	mV	LVIN-LOUTx, LOUTx rising, LVIN = 3.0V, V_{LOUTx_NOM} = 3.3V
Start-up POK Bypass Threshold Hysteresis (Note 1)	$V_{POKB\_HYS\_Lx}$	—	50	—	mV	LOUTx falling, LVIN = 3.0V
Soft-start Rate (switching frequency clock cycles per DAC step)	SSR_00	—	16	—	cycles / step	SSR[1:0] = 00 – default
	SSR_01	—	32	—		SSR[1:0] = 01
	SSR_10	—	48	—		SSR[1:0] = 10
	SSR_11	—	64	—		SSR[1:0] = 11
Dynamic Voltage Scaling Rate (switching frequency clock cycles per DAC step) – rising only	DVSR_00	—	16	—	cycles / step	DVSR[1:0] = 00 – default
	DVSR_01	—	32	—		DVSR[1:0] = 01
	DVSR_10	—	48	—		DVSR[1:0] = 10
	DVSR_11	—	64	—		DVSR[1:0] = 11
Current Limit	I_{LIM_LOUTx}	**310**	400	**550**	mA	SVIN = LVIN = 4.5V, $V_{LOUT1,2}$ = 80% of nominal

Notes:

1. Not production tested.
2. Typical value from bench characterization. Maximum value production tested.

DC/AC Characteristics (continued)

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; $V_{LOUT1,2}$ = 3.3V; $C_{LOUT1,2}$ = 2.2 µF ($I_{LOUT1,2}$ ≤ 150 mA) or 4.7 µF ($I_{LOUT1,2}$ ≤ 300 mA), unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol (x = 1,2)	Min.	Typ.	Max.	Units	Conditions
Active Discharge Resistance	R_{DISCH_LOUTx}	—	25	—	Ω	DISCH = 1, Enabled when regulator disabled and during negative DVS

Notes:

1. Not production tested.
2. Typical value from bench characterization. Maximum value production tested.

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
EN Input						
Logic HIGH Input Voltage V_{IH}	V_{IH_EN}	**1.5**	—	—	V	SVIN = 3.6V-5.5V
Logic LOW Input Voltage V_{IL}	V_{IL_EN}	—	—	**0.4**	V	SVIN = 3.6V-5.5V
EN Deglitch Time	t_{DT_EN}	5	10	15	µs	SVIN = 2.7V-5.5V
VSET1, VSETL1, VSETL2 pins						
Output Voltage setting Resistor	R_{SEL}	—	Short to GND	—		VOUTx = OFF
		−1%	0.187	+1%	kΩ	VOUTx = 1.2V
			0.487			VOUTx = 1.25V
			0.976			VOUTx = 1.3V
			1.74			VOUTx = 1.35V
			2.94			VOUTx = 1.4V
			4.87			VOUTx = 1.5V
			8.06			VOUTx = 1.6V
			13			VOUTx = 1.8V
			21			VOUTx = 2.5V
			34			VOUTx = 2.8V
			54.9			VOUTx = 3.0V
			86.6			VOUTx = 3.15V
			140			VOUTx = 3.3V
			226			VOUTx = 3.4V
		—	Short to VIN	—		VOUTx = 3.6V
VSET2, VSET3, VSET4 pins						

Notes:

1. Not production tested.
2. Input filters on the SDA and SCL inputs suppress noise spikes of less than 5 ns.

DC/AC Characteristics (continued)

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage setting Resistor	R_{SEL}	—	Short to GND	—		VOUTx = OFF
		−1%	0.187	+1%	kΩ	VOUTx = 0.6V
			0.487			VOUTx = 0.8V
			0.976			VOUTx = 0.9V
			1.74			VOUTx = 1V
			2.94			VOUTx = 1.05V
			4.87			VOUTx = 1.1V
			8.06			VOUTx = 1.15V
			13			VOUTx = 1.2V
			21			VOUTx = 1.25V
			34			VOUTx = 1.275V
			54.9			VOUTx = 1.35V
			86.6			VOUTx = 1.375V
			140			VOUTx = 1.4V
			226			VOUTx = 1.5V
		—	Short to VIN	—		VOUTx = 1.8V
PWRHLD, LPM, HPM Logic Inputs (x = PWRHLD, LPM, HPM)						
Logic HIGH Input Voltage V_{IH}	V_{IH_x}	**1.5**	—	—	V	SVIN = 3.6V-5.5V
Logic LOW Input Voltage V_{IL}	V_{IL_x}	—	—	**0.4**	V	SVIN = 3.6V-5.5V
Input leakage current	I_{lkg_x}	**−1**	—	**1**	µA	—
Deglitch Time	t_{DT_x}	—	10	—	µs	—
nRSTO, nSTRTO, nINTO Logic Outputs (x = nRSTO, nSTRTO, nINTO)						
Output Voltage LOW V_{OL}	V_{OL_x}	—	—	**0.4**	V	SVIN = 3.6V-5.5V, I_{OL} = 2 mA
Leakage current	I_{lkg_x}	—	—	**1**	µA	5.5V applied, output driver OFF
SDA, SCL I^2C Interface Pins (x = SDA, SCL)						
SCL, SDA Logic HIGH Input Voltage V_{IH}	V_{IH_x}	**1.5**	—	—	V	SVIN = 3.6V-5.5V
SCL, SDA Logic LOW Input Voltage V_{IL}	V_{IL_x}	—	—	**0.4**	V	SVIN = 3.6V-5.5V
Hysteresis of Schmitt trigger inputs	V_{hys_x}	—	0.2	—	V	SVIN = 3.6V-5.5V
SDA, SCL leakage current	I_{lkg_x}	—	—	**1**	µA	SDA driver OFF, V_{SDA} = 5.5V, V_{SCL} = 5.5V
SDA output voltage LOW V_{OL}	V_{OL}	—	—	**0.4**	V	SVIN = 3.6V-5.5V, I_{OL} = 20 mA
Maximum SCL Clock Frequency	f_{SCL}	—	1	—	MHz	Functional Test Only
Maximum Pulse Width of input spikes that must be suppressed (Note 1, Note 2)	t_{SP}	—	50	—	ns	Functional Test Only

Notes:

1. Not production tested.
2. Input filters on the SDA and SCL inputs suppress noise spikes of less than 5 ns.

3.3. Temperature Specifications

Note: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

T_A = +25°C; VIN = SVIN = PVINx = LVIN = 5V; unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Junction Temperature	T_J	−40	—	+125	°C	Steady-state
Maximum Junction Temperature	T_{J_MAX}	—	—	+150	°C	Transient
Package Thermal Resistance	θ_{JA}	—	25.8	—	°C/W	

4. Typical Performance Curves

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Figure 4-1. V_{IN} Operating Current vs. Input Voltage and Temperature – HIBERNATE Mode (LPM = HIGH, PWRHLD = HPM = LOW)

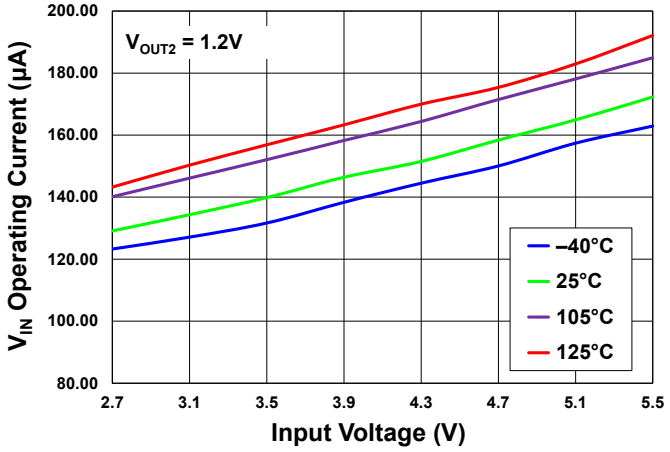


Figure 4-2. Buck1 Efficiency vs. Load Current (V_{OUT1} = 3.3V)

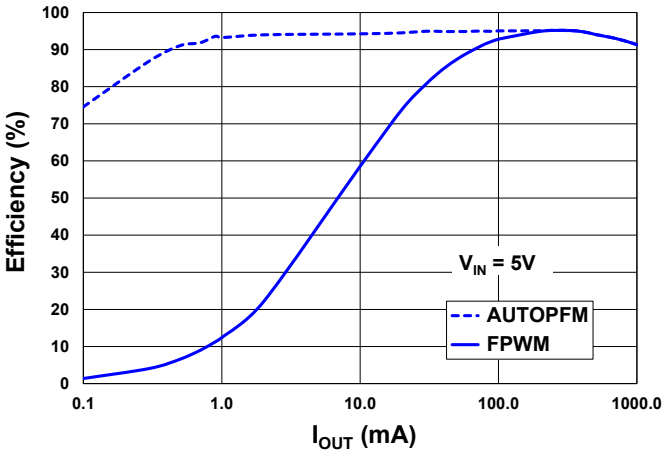


Figure 4-3. V_{IN} Operating Current vs. Input Voltage and Temperature – Low-Power Mode (LPM = PWRHLD = HIGH, HPM = LOW)

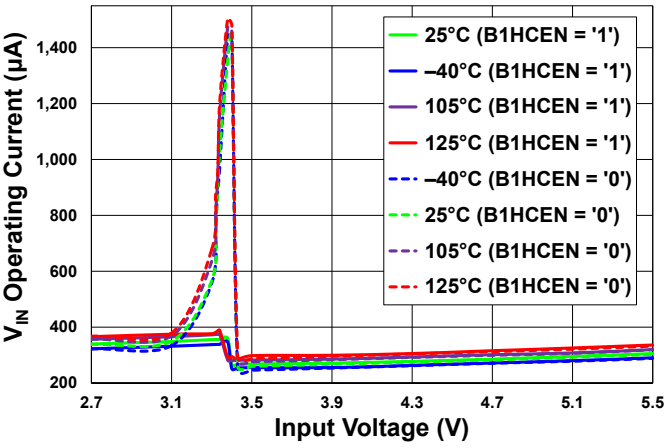


Figure 4-4. Buck2 Efficiency vs. Load Current (V_{OUT2} = 1.8V)

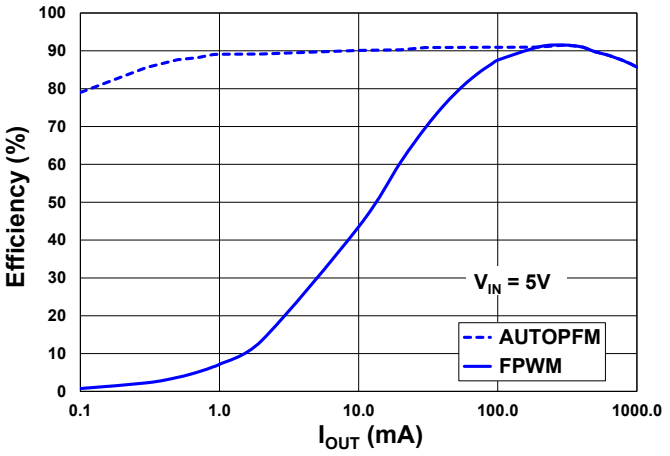


Figure 4-5. V_{IN} Operating Current vs. Input Voltage and Temperature – Active Mode (LPM = PWRHLD = HIGH, HPM = LOW).

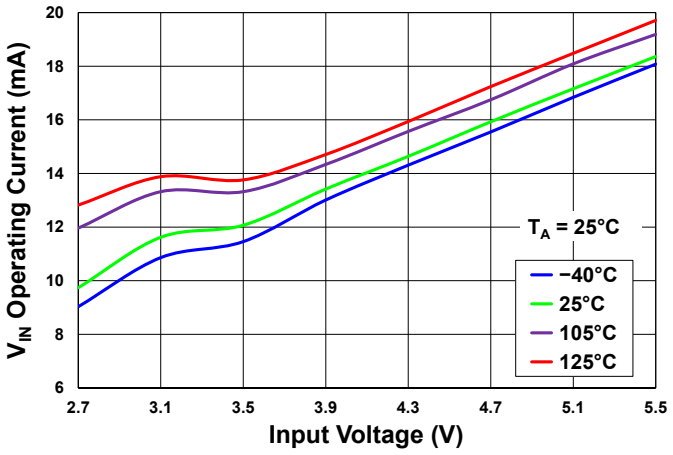


Figure 4-6. Buck3 Efficiency vs. Load Current (V_{OUT3} = 1.2V)

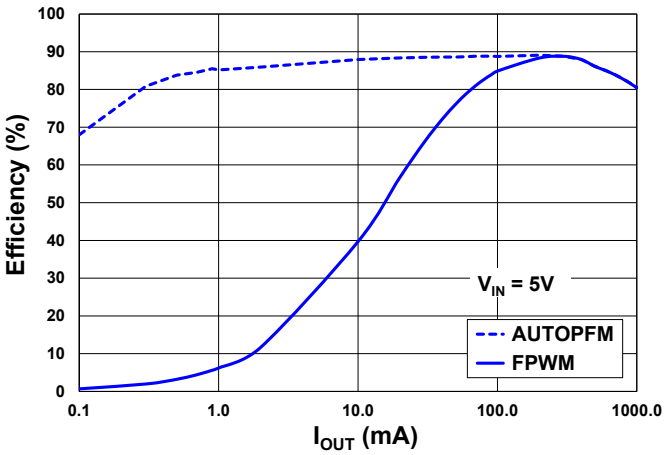


Figure 4-7. MOSFET $R_{DS(ON)}$ vs. Temperature

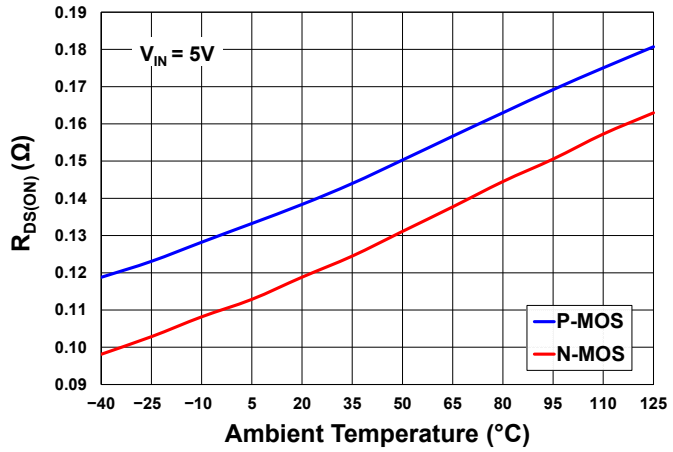


Figure 4-8. Buck4 Efficiency vs. Load Current (V_{OUT4} = 0.9V)

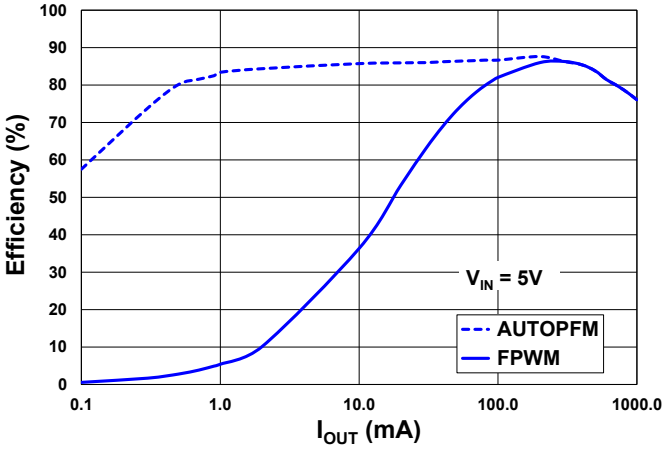


Figure 4-9. LDO1, LDO2 Dropout Voltage vs. Load Current

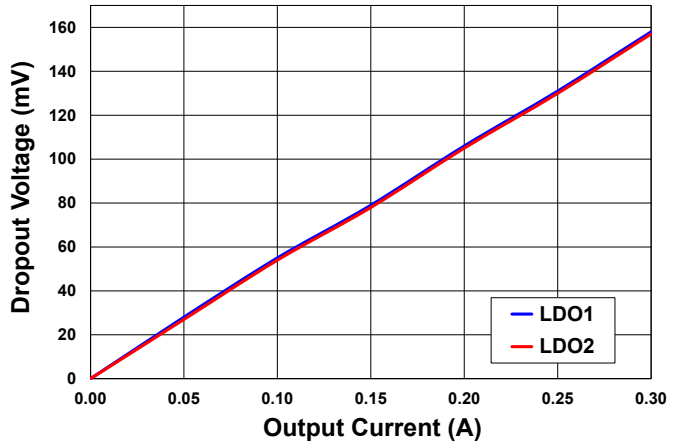


Figure 4-10. EN Start-up Sequence

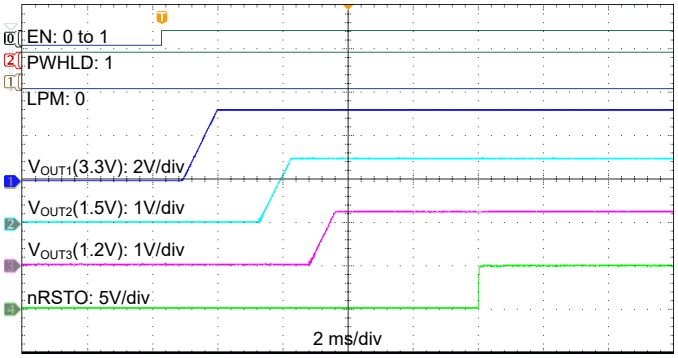


Figure 4-11. EN Shutdown

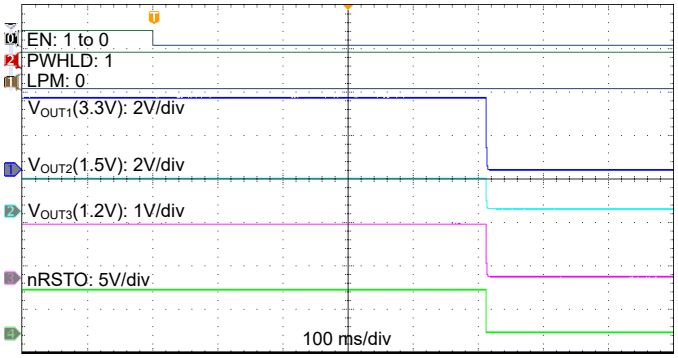


Figure 4-12. PWRHLD Start-up Sequence

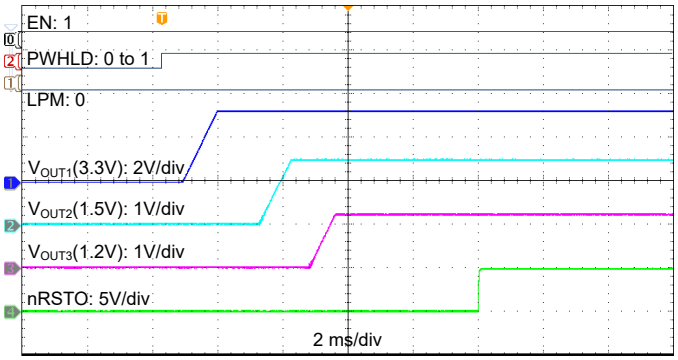


Figure 4-13. PWRHLD Shutdown Sequence

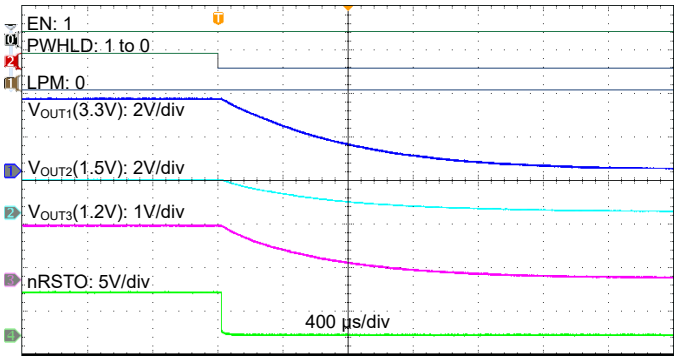


Figure 4-14. Entering HIBERNATE Mode

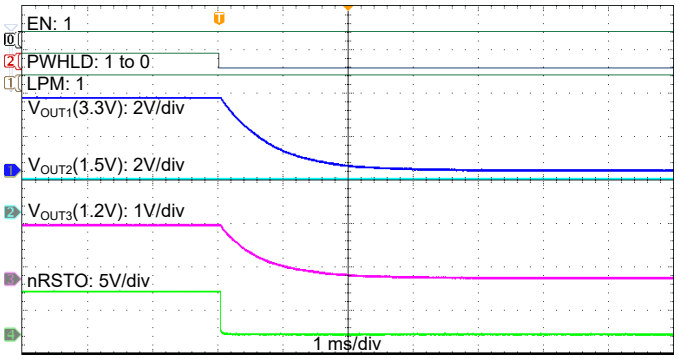


Figure 4-15. Automatic Wake-up Pulse, HIBERNATE Mode

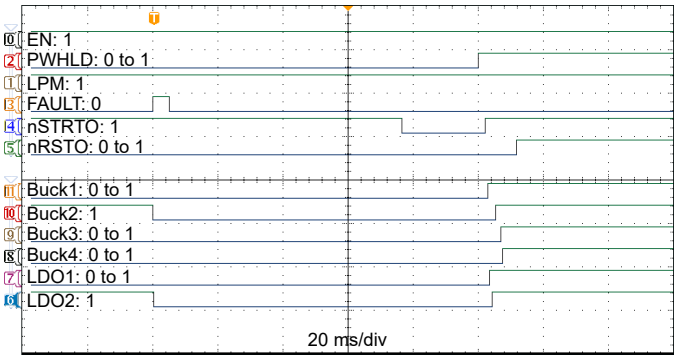


Figure 4-16. Buck4 DVS Transition

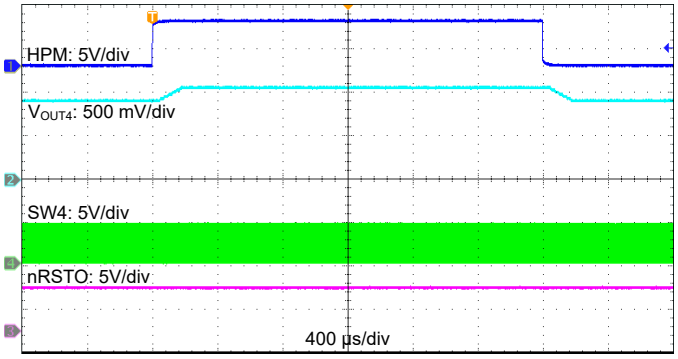


Figure 4-17. Buck3 Load Transient Response, Active (FPWM) Mode

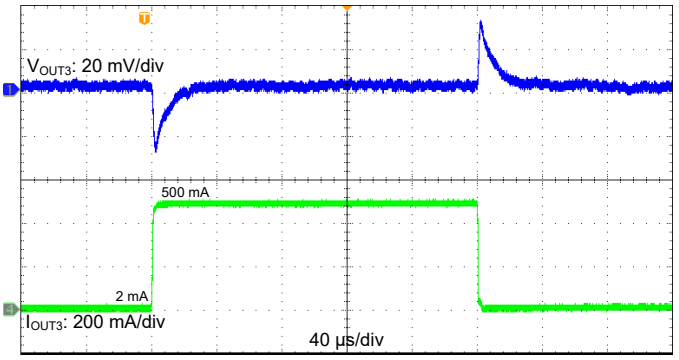


Figure 4-18. Buck Channels Output Voltage Ripple, Active (FPWM) Mode

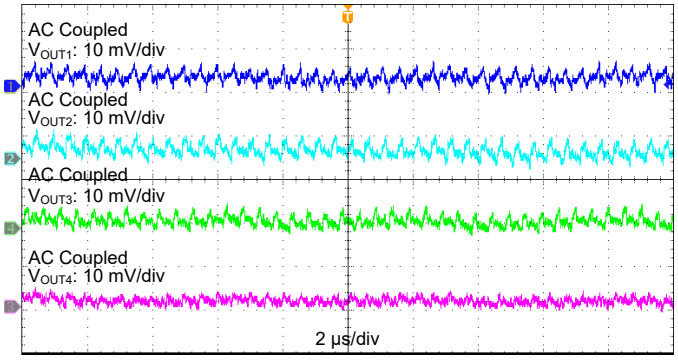


Figure 4-19. Buck Channels Output Voltage Ripple, Low-Power (Auto PFM) Mode

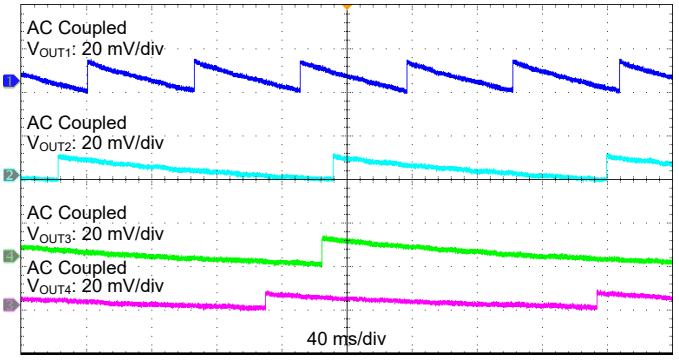


Figure 4-20. Output Short Circuit on Buck1 – HCPEN = 1

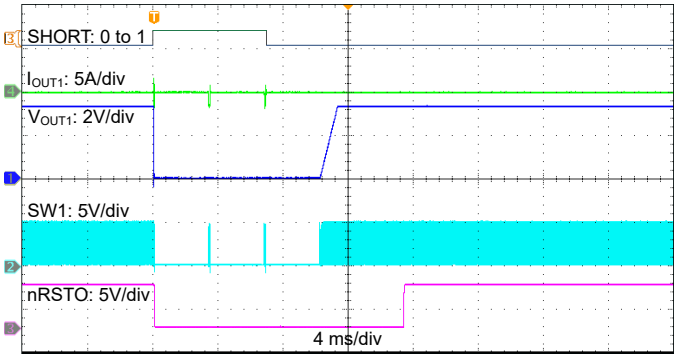
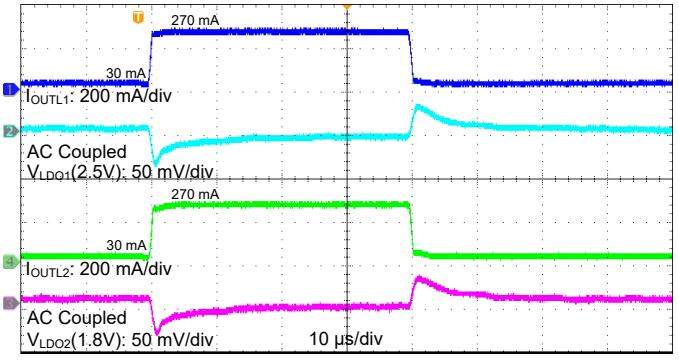


Figure 4-21. LDO1, LDO2 Load Transient Response



5. Application Information

5.1. Recommended External Components

The following table lists possible part numbers that can be used in the MCP16503 application. Please refer to the section Typical Application Circuit for component designators reference.

Table 5-1. Recommended External Components

Item	Part Number	Manufacturer	Description
C1-C4	C1608X5R1A226M080AC	TDK	Capacitor, 22 µF, 6.3V/10V, X5R, 20%, Size 0603
	GRM188R61A226ME15D	Murata	
	C1608X5R0J226M080AC	TDK	
	GRM188R60J226MEA0	Murata	
	JMK107BBJ226MA	Taiyo Yuden	
	CL10A226MQ8NRNC	Samsung Electro-Mechanics	
	06036D226MAT2A	AVX	
C5-C8, C10-C11 (for 300 mA max LDO current), C12	C1005X5R1A475K050BC	TDK	Capacitor, 4.7 µF, 10V, X5R, 10%/20%, Size 0402
	GRM155R61A475MEAA	Murata	
	LMK105BBJ475MV	Taiyo Yuden	
	CL05A475M(K)P5NRNC	Samsung Electro-Mechanics	
	0402ZD475MAT2A	AVX	
C9, C10-C11 (for 150 mA max LDO current)	C1005X5R1A225K050BC	TDK	Capacitor, 2.2 µF, 10V/16V, X5R, 10%, Size 0402
	GRM155R61C225KE11	Murata	
	LMK105BJ225KV	Taiyo Yuden	
	CL05A225KP5NSNC	Samsung Electro-Mechanics	
	0402ZD225KAT2A	AVX	
R1	RC0402KR-07100KL	Yageo	Resistor, 100 kΩ 5%, Size 0402
R2-R3	RC0402KR-0710K0L	Yageo	Resistor, 10 kΩ 5%, Size 0402
R4-R5	RC0402KR-072K20L	Yageo	Resistor, 2.2 kΩ 5%, Size 0402
L1, L2, L3, L4	MLP2520W1R5MT0S1	TDK	1.5 µH, 1.8A, 75 mΩ, Size 2520, Multilayer Ferrite
	LQM2HPN1R5MGH	Murata	1.5 µH, 1.6A, 65 mΩ, Size 2520, Multilayer Ferrite
	VLS252012CX-1R5M	TDK	1.5 µH, 2.3A, 62 mΩ, Size 2520, Wirewound Ferrite
	LQH2HPN1R5MGR	Murata	1.5 µH, 1.85A, 87 mΩ, Size 2520, Wirewound Ferrite
	CDPH28D11FNP-1R5MC	Sumida	1.5 µH, 1.74A, 69 mΩ, Size 3.0mm x 3.2mm, Wirewound Ferrite
	DFE252012P-1R5M=P2	Murata	1.5 µH, 2.6A, 60 mΩ MAX, Size 2520, Metal Alloy
	DFE252012P-2R2M=P2	Murata	2.2 µH, 2.2A, 84 mΩ MAX, Size 2520, Metal Alloy
	VLS252012HBX-1R5M-1	TDK	1.5 µH, 2.5A, 68 mΩ, Size 2520, Metal Alloy
	VLS252012HBX-2R2M-1	TDK	2.2 µH, 2.04A, 85 mΩ, Size 2520, Metal Alloy

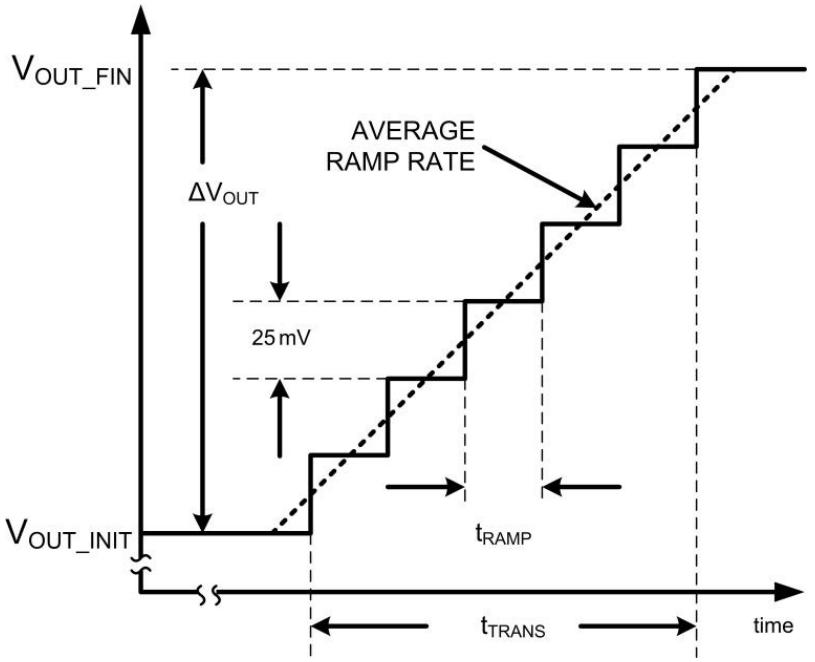
5.2. Dynamic Voltage Scaling (DVS) Operation

Dynamic Voltage Scaling is not a special mode of operation. When the state machine moves from one state to another, and the content of the regulator voltage in the new state is different from the previous one (assuming the regulator is ON in both the initial and final state), the output voltage of the regulator will be automatically updated in 25 mV (or 50 mV for Buck1 and LDOs) increments/decrements to reach the value which is defined for the final state.

This also happens if the regulator voltage is updated through I^2C, without any power mode state change.

The step rate is programmable, and it is derived from the switching frequency clock. The values are as described in section Dynamic Voltage Scaling Rate Programming Bits (t_{ramp}).

Figure 5-1. DVS Diagram and Parameters



Internal filtering time constants for the reference DAC steps and the finite response time of the control loop help in smoothing out the resulting ramp shape visible at the output of the regulator(s).

During DVS transitions:

- The Buck converters will operate in FPWM, to allow a predictable transition time in both the rising and falling DVS transitions.
- LDO: when the transition happens in the negative direction (i.e. decreasing voltage), the Active Discharge load will be activated during the transition, in order to speed up the transition time. This is to facilitate the support of dual-voltage SD Cards

The POK will not be de-asserted during rising DVS transitions because of change in reference (DAC) voltage.

During DVS transition, changes in POK logic value are inhibited until the transition is completed.

5.3. HPM Pin / HPMPEN Bit

The HPM pin is meant to be driven by a GPIO of the host MPU for the purpose of entering a software-defined high-performance mode. Its usage is optional, and it should be connected to ground if it is not used.

For example: SAMA7G MPUs will typically use the HPM pin to switch the VDDCPU rail voltage **(supplied by a buck channel)** to a higher voltage such that higher clock frequencies can be supported (DVS operation, see section Dynamic Voltage Scaling (DVS) Operation). The required overdrive voltage level in HPM mode needs to be defined by I^2C prior to entering DVS operation. If no action is taken, the HPM voltage value will default to the ACTIVE mode default value.

The HPM pin needs to be enabled (unmasked) through I^2C by setting bit HPMPEN in register SYS-CFG. If HPMPEN bit is not set, the internal logic will be insensitive to the HPM pin level, which will always appear internally as a logic “0”.

The HPMPEN bit is not automatically cleared due to a start-up or to a restart sequence after a fault. Also, the DVS voltage level definition stored in the HPM registers is not reset to the Active mode one.

Therefore, if for any reason the HPM pin remains high (or returns to high logic level) during the start-up/restart sequence while the HPMPEN bit has been previously set, the MCP16503 will move to the high-performance mode immediately after the start-up/restart sequence has successfully terminated. Thus, if the DVS voltage level defined in HPM mode is different than the voltage level defined in Active mode, the channel under consideration will immediately move to the HPM mode voltage level as soon as nRSTO is de-asserted.

While the DVS voltage level is not typically dangerous for the VDDCPU rail generated by a buck channel, if the behavior described above is not desirable, the following countermeasures can be considered:

- connect the HPM pin to a GPIO which is low by default at start-up;

- clear by software the relevant GPIO at the beginning of the software execution / configuration routine and/or clear the HPMPEN bit by I^2C command.

Also note that the channel (typically Buck1, VDDIO) powering the MPU voltage domain to which the GPIO driving the HPM pin belongs, should be always defined ON in HPM mode.

Failing to do so would set the HPM pin low again shortly after it has been set high, thereby generating a cyclic behavior where the relevant channel turns ON and OFF indefinitely.

If the LPM pin goes high (with PWRHLD = high) while HPM is low, the MCP16503 will move to Low-Power state. If HPM goes high after that, the MCP16503 will ignore it and it will stay in Low-Power state, as long as LPM = high.

On the other hand, if HPM goes high first (thus PWRHLD = HPM = 1, LPM = 0), the device remains in HPM state even if LPM is asserted high. To go to Low-Power State, HPM must be de-asserted first.

5.4. Buck1 Hysteretic Control Mode (HCM) / B1HCEN Bit

If Buck1 is set in AutoPFM mode while the input voltage (e.g. a discharging battery) is decreasing and eventually pushing Buck1 to 100% duty cycle (bypass mode), the operational no-load quiescent current of the MCP16503 shows some increase due to the augmented switching activity of Buck1.

This is intrinsic to the AutoPFM architecture. The peak in the quiescent current is in the 1 mA range, and it may or may not be detrimental to the overall system efficiency and/or battery life, depending mostly on the minimum loading of Buck1.

If the increase in quiescent current when approaching bypass mode on Buck1 is an important factor for the application, the user can optionally activate a different mode of light-load high-efficiency operation (called Hysteretic Control Mode, HCM) where the output voltage is controlled in a hysteretic fashion between the nominal output voltage and +2.9% of it. This is done by setting bit B1HCEN (Buck1 Hysteretic Control Enable) in register SYS-CFG through I^2C. This control method reduces significantly the average switching activity of Buck1, especially in proximity of the bypass operation, at the expense of an increase of the output ripple (typically 2.9% of the nominal output voltage).

The user should therefore carefully evaluate the need for activation of HCM for Buck1 and balance the increase in output ripple against the real benefit achieved in prolonging battery life. If the minimum loading on Buck1 is always significantly higher than 1 mA, activation of HCM is typically not needed.

The relevant EC Table parameter that defines the upper voltage regulation threshold (typically +3.45% of the nominal output voltage) is the Hysteretic Control Mode Upper Regulation Threshold.

Even if bit B1HCEN is set, HCM mode will only be activated when the input-to-output voltage differential decreases below a certain value. This is done to prevent fast inductor charging, which in turn may cause a poorer control of the effective upper regulation voltage.

The relevant EC Table parameter that defines the input voltage threshold (falling input voltage) below which HCM is enabled is the Hysteretic Control Mode Enable Threshold, and it is also expressed as a percentage of the nominal output voltage value (typically 2.9).

5.5. Protections

The MCP16503 offers the following:

- Thermal Shutdown
- Thermal Warning
- Overcurrent Protection

5.5.1. Thermal Warning and Protection

Thermal Shutdown protection will immediately terminate power delivery on all channels when the die temperature exceeds the upper Thermal Shutdown threshold. At the same time, nRSTO will be asserted low. If the corresponding masking bit is cleared, nINTO will also be asserted low.

After the die temperature has decreased below the lower Thermal Shutdown threshold (hysteresis = 20°C) and an additional 100 ms delay, the MCP16503 will automatically attempt a new start-up sequence, without the need of an external start condition (e.g. from PWRHLD).

Thermal Warning does not invoke any automatic action. If the die temperature exceeds the Thermal Warning upper threshold, and if the corresponding masking bit is cleared, it will only generate assertion (low) of the nINTO output. The host MPU can then interrogate the MCP16503 for diagnostic purposes.

5.5.2. LDO Current Limit Protection

LDOs are protected against short-circuits by a linear constant-voltage/constant-current (e.g., brick-wall) output characteristic. The output current under short-circuit conditions is not intermittent. Therefore, the internal power dissipation in the MCP16503 can reach high levels under LDO short-circuit conditions. The current limit condition of each LDO is also reported through I^2C. The intervention of the LDO current limit protection does not cause the assertion of the nRSTO (RESET) signal.

5.5.3. Overcurrent Protection (Buck Channels)

The overcurrent protection consists of a cycle-by-cycle, high-side current limit with digital filtering, followed by Hiccup for protection against short-circuits conditions.

The cycle-by-cycle, high-side current limit includes frequency fold-back. Because of Leading-Edge-Blanking in peak-current-mode control, frequency fold-back (with a factor = 4) is used to allow more time for inductor discharge and prevent current runaway in deep overload condition.

Frequency fold-back operation is entered when:

1. A high-side current limit event has been detected; and
2. The feedback voltage is less than 500 mV (typical).

Cycle-by-cycle overcurrent protection with frequency fold-back is always active and it is the first current limit protection mechanism.

The second current limit mechanism is Hiccup mode protection, which is by default always enabled, including during the Soft-Start ramp and DVS transitions.

Since the hiccup mode protection is also active during Soft-Start, there will be a limitation on the maximum simultaneous DC and capacitive loading to ensure that the hiccup mode protection will

not be engaged during the Soft-Start ramp. This is further explained in section PWM Mode Negative Current Limit Protection (Buck Channels).

Hiccup is invoked based on digital counting of high-side overcurrent (HS OC) events, regardless of the frequency at which they take place (full switching frequency or fold-back switching frequency).

Each time the overcurrent protection detects a high-side current limit event, the current ON time is terminated and a HS OC Event counter is incremented. The length of the counter is 4-bits.

If the counter reaches its EOC, while the instantaneous value of POK signal is still low, the buck converter is turned OFF (both High-side and Low-Side transistors are turned OFF) and Hiccup mode protection is triggered.

The intervention of Hiccup on any of the Buck channels can have two different behaviors, depending on the HCPEN bit value of the channel affected by overcurrent conditions. The HCPEN bit is user-accessible through I^2C.

If HCPEN = 0, the intervention of Hiccup will immediately terminate the power delivery on all channels, including LDOs. At the same time, nRSTO will be asserted low. If the corresponding masking bit is cleared, nINTO will also be asserted low.

After a 100 ms delay, the MCP16503 will automatically attempt a new start-up sequence, without the need of an external start condition (e.g.from PWRHLD).

If HCPEN = 1, the intervention of Hiccup only affects the responsible Buck channel. All other channels will continue to operate normally. If the affected channel is part of the Power-Up sequence, nRSTO will be asserted low, and if the corresponding masking bit is cleared, nINTO will also be asserted low.

The affected channel will be kept OFF for a certain hiccup time (t_{HICCUP}), which corresponds to 3x Soft-Start time on that channel, and after the hiccup time a new Soft-Start is attempted.

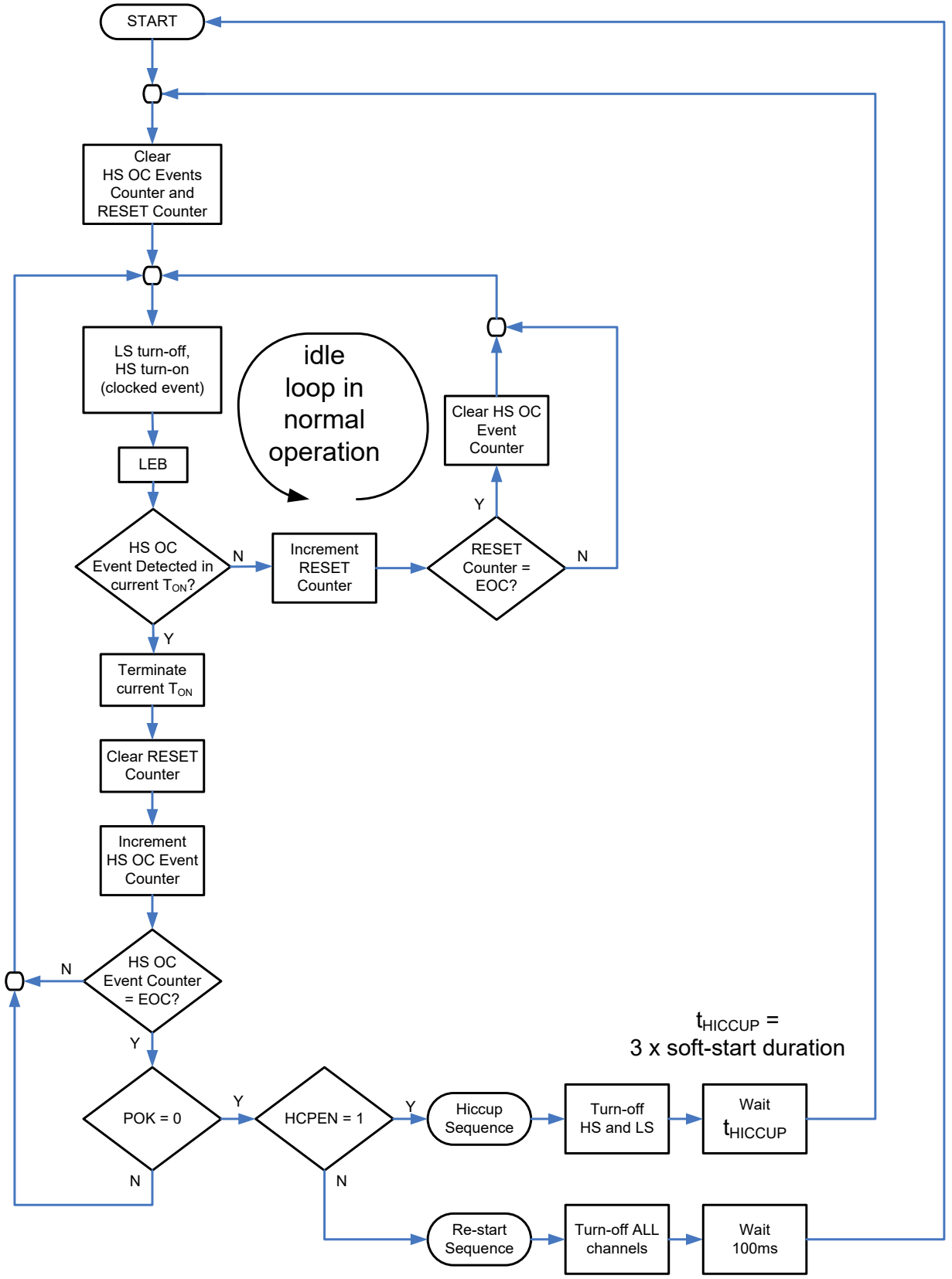
If the short-circuit condition is removed and the affected channel resumes normal operation (POK returns High), nRSTO will be asserted high after the programmed reset delay (t_4).

The HS OC event counter is reset only after 15 consecutive HS turn-on pulses without any overcurrent event. This counting is done by the RESET counter.

Note that all counting is switching-event based, so it is not relevant if the switching takes place at f_{sw} or at $f_{sw}/4$ (i.e. in frequency fold-back).

The hiccup flowchart is detailed below. The overcurrent condition of each Buck is also reported through I^2C.

Figure 5-2. Hiccup Protection Flowchart



5.5.4. PWM Mode Negative Current Limit Protection (Buck Channels)

The Buck channels of the MCP16503 also feature a negative inductor current limit protection when operating in Forced PWM mode. This prevents dangerous current levels in the power train. If the inductor current reaches the Low-Side Negative Peak Current Limit (I_{LIM_NEGx}) while the Low-Side MOSFET is conducting, the Low-Side MOSFET is turned off and the inductor current is pushed to the input voltage, either through the body diode of the High-Side MOSFET (if OFF) or its channel (when turned ON by the control loop). Since this feature is only intended to protect the device in some particular transient conditions (such as a large decrease of the output voltage setting associated with an extremely large capacitive load), it is only reported through I^2C, but it does not cause the assertion of the nRSTO (RESET) signal.

This protection should never be exercised continuously and/or without a very large bulk capacitor, because it may quickly destroy the device.

When this protection is engaged, energy is pumped back from the output into the input voltage. If the input supply has no sinking capability and/or the input bulk decoupling cap is not large enough, the input voltage will rise to the point where the device is permanently damaged.

5.6. Maximum Simultaneous Capacitive and DC Loading in Soft-Start and DVS

The Current-Mode architecture of the Buck channels in the MCP16503 make them tolerant to additional capacitive loads, from the stability point-of-view.

However, since the hiccup mode overcurrent protection is also enabled during Soft-Start and DVS ramping, the user needs to be aware that additional load capacitance distributed on the application board may cause the intervention of the hiccup mode protections under dynamic conditions (rising output voltage).

This is especially important for Buck1, since the I/O rail (typically 3.3V) can be used for a wide variety of loads and its total distributed capacitive load could significantly exceed the minimum recommended nominal capacitance value (i.e. 22 µF).

Using the symbols listed in the DC/AC Characteristics table, the following equation establishes the maximum allowable capacitive load C_{add_max} to prevent the cycle-by-cycle current limit from being engaged.

Complying with this condition will guarantee that hiccup mode overcurrent protection will not be activated during the Soft-Start ramp or DVS transitions in the positive direction.

$$C_{add\_max} = \left(\frac{I_{LIM\_HS}}{r} - I_{OUT}\right) \times \frac{SSR\_XX}{V_{step} \times f_{sw}} - C_{OUT}$$

Where:

- I_{LIM_HS}: High-Side MOSFET Current Limit
- r : ratio of the peak inductor current I_{Lpk} to average inductor current at the point where $I_{Lpk} = I_{LIM\_HS}$. For simplicity, assume r = 1 since the peak-to-peak inductor current ripple will be small in comparison to the average inductor current value when the high-side current limit is engaged.
- I_{OUT}: Output current of the Buck converter
- V_{step}: Output voltage step in SS (or DVS)
- SSR_XX: Soft-Start Rate (or DVS Rate), XX = 00, 01, 10, 11
- f_{sw}: switching frequency
- C_{OUT}: output capacitance already present on the Buck converter output (typically C_{OUT} = 22 µF)

Failing to comply with the conditions formulated above does not necessarily mean that hiccup mode protection will be engaged. The digital filtering provided in the hiccup mode overcurrent algorithm, as described in section Overcurrent Protection (Buck Channels), provides immunity to single and

even multiple cycle-by-cycle current limit events, and allows operation in proximity of the high-side current limit for significant amount of time during the Soft-Start or DVS ramping.

As a consequence, the maximum value of additional capacitance C_{add_max} that can be observed by experiments is significantly higher than the limit calculated with the formula.

5.7. VSETx and VSETLx resistor decoder

The default start-up voltage for each power channel is configured using the VSETx/VSETLx pins. The user can either connect a resistor from the pin to ground or short the pin to GND or SVIN. This provides 16 configuration options per channel:

- Pin shorted to GND: reserved to disable the corresponding power channel during the start-up sequence. The EN, SEQEN, and RCON and REN bits are internally masked when the corresponding VSET[5:0] value is set to 0. To enable a channel that was disabled during the start-up phase, the user must program the corresponding VSET[5:0] register to the required output voltage, according to the selected mode of operation. For example, if the user changes only the VSET[5:0] value for Active mode, the channel will be enabled exclusively during Active mode.
- All other 15 options: select 15 different start-up voltage levels (see the Configuring MCP16503 Default Start-up Voltage Table).

The resistor values connected to the VSETx/VSETLx pins are decoded only once during the initialization phase. Specifically, after power is applied and the Finite State Machine (FSM) enters the INIT (Initialization) state (see Finite State Machine (FSM) States Diagram), the device begins decoding the resistor configuration.

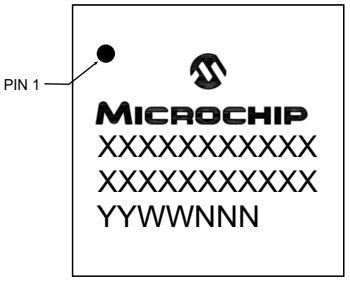
When the decoding process is complete, the detected start-up voltage settings are stored in the VSET[5:0] fields of the OUTx-A and LDOx-A registers. These values are then copied to the corresponding VSET[5:0] fields in OUTx-LPM, OUTx-HIB, OUTx-HPM, LDOx-LPM, LDOx-HIB, and LDOx-HPM.

After this point, each channel's output voltage can be changed only via I^2C (see Voltage Codes Definition Bits VSET[5:0]).

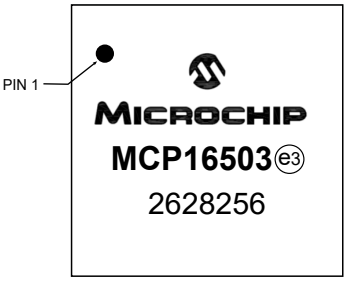
6. Package Information

Package Marking Information

32-Lead VQFN (5 × 5 × 1 mm)



Example:



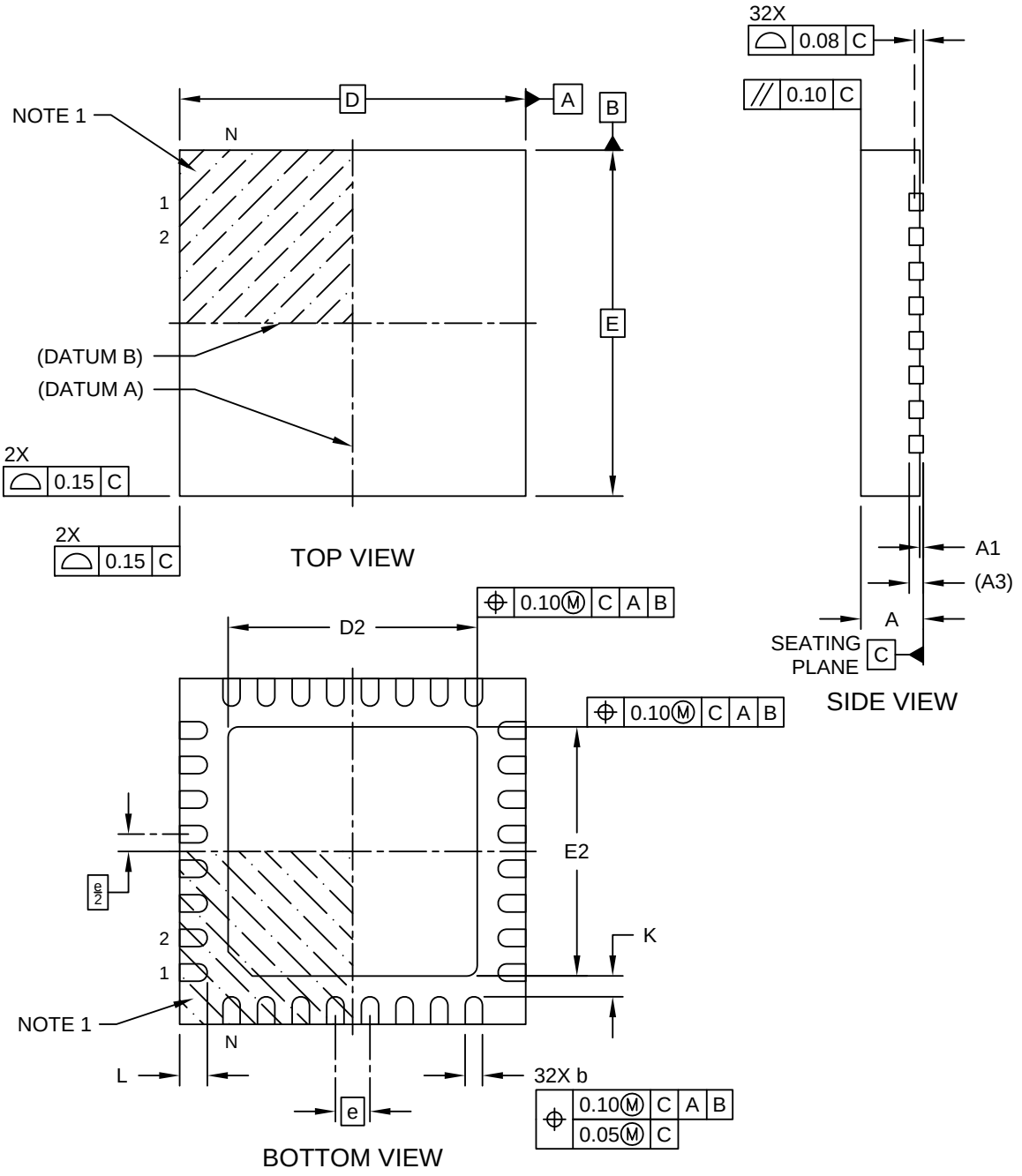
Legend:	XX...X	Product Code or Customer-specific information
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

Package Outline Drawing

32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

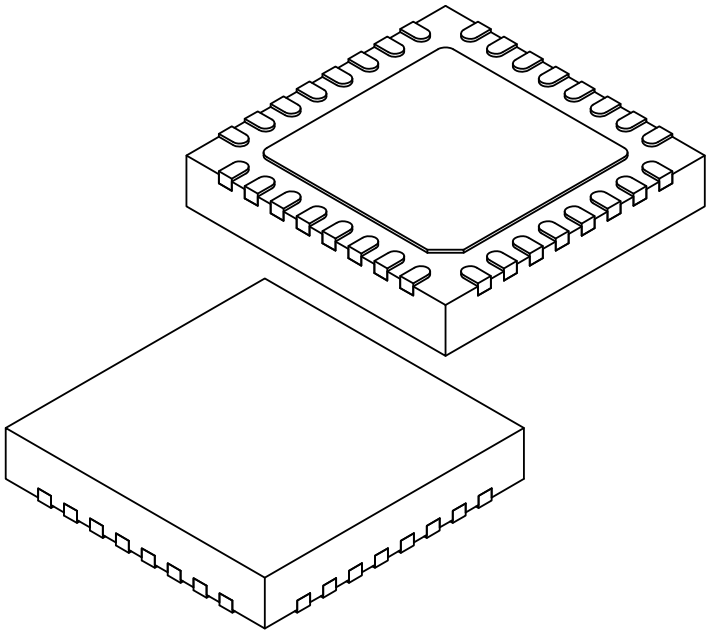
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21402 Rev A Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

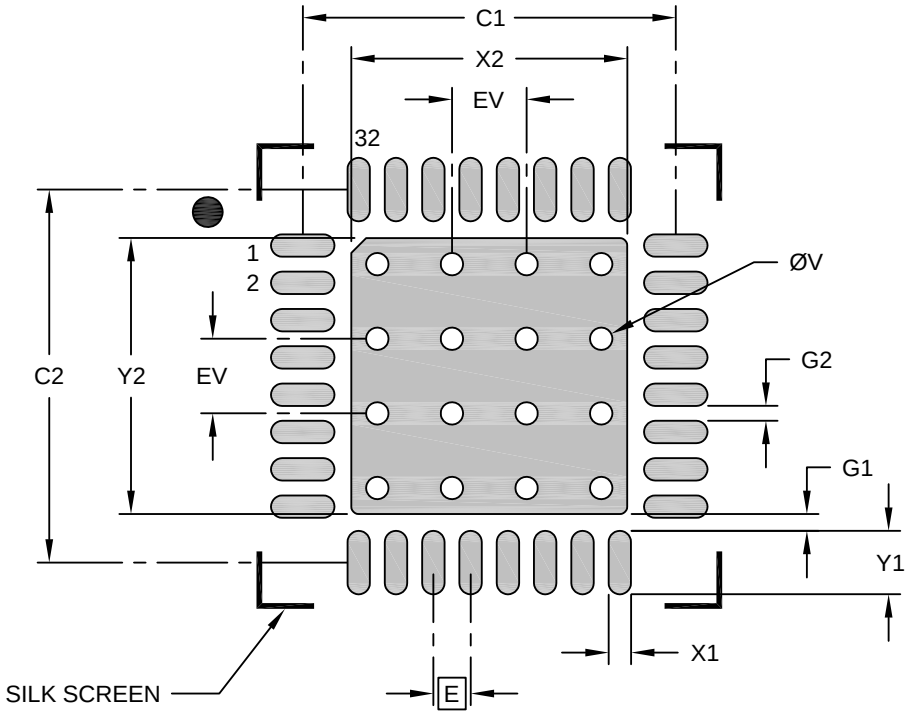
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21402 Rev A Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23402 Rev A

7. Revision History

Doc. Rev.	Date	Section	Comments
A	May 2026	—	Initial release of this document.

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.

Device:	MCP16503: High-Performance, General Purpose PMIC for MPUs	
Tape & Reel Option:	(Blank)	= Tube
	T	= Tape & Reel (3300/Reel)
Temperature Range:	E	= −40°C to +125°C (Extended)
Package:	S8B	= VQFN, Very Thin Quad Flatpack, No Leads, 32-Lead, 5 × 5 × 1 mm

Examples:

- MCP16503T-E/S8B: High-performance PMIC, Tape and Reel, Extended Temperature Range, VQFN Package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-3291-4

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.