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Mercury A2700 Accelerator Card

Next-Generation Platform for Accelerated Computing

User Manual

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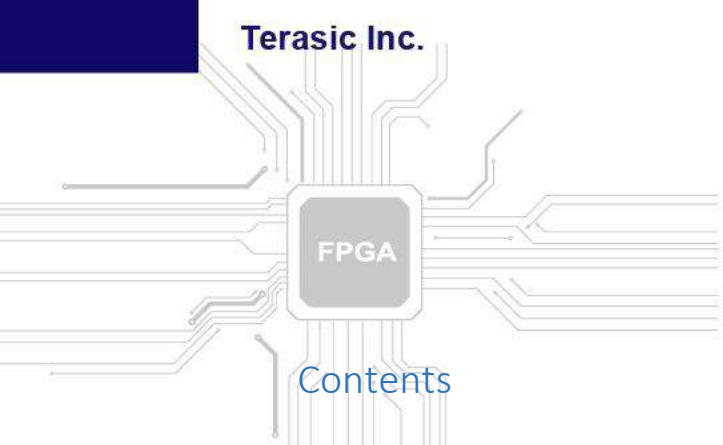

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Chapter 1

Overview

This chapter provides an overview of the **Terasic Mercury A2700 Accelerator Card (MA27)** and installation guide.

1.1 General Description

The Terasic Mercury A2700 accelerator card leverages the Intel industry's highest performance Agilex™ I-Series FPGA with 2700K logic elements to address the most compute and bandwidth-demanding applications in the data center, in the cloud, and in embedded devices.

As the first Terasic accelerator that provides PCIe 5.0 x16 and Compute Express Link (CXL) support, the Mercury A2700 accelerator card enables 2X higher bandwidth compared with PCIe 4.0 interface for higher data throughput, as well as high-speed, low-latency, and efficient performance between CPU and FPGA.

In addition, armed with two 200G QSFP-DD connectors, and four DDR4 SO-DIMM sockets, the Mercury A2700 accelerator card accelerates every workload across the data center and edge in computer vision, high performance computing, and other compute-intensive applications.

1.2 Key Features

The following hardware is implemented on the Mercury A2700 Accelerator Card:

- **Intel® Agilex™ I-Series**

- AG1B027R29A1E2V
  - 2.7M logic elements (LEs)
  - 287 Mb On-chip RAM (M20K and MLAB)
  - 17,056 18-bit x 19-bit multipliers
  - 4,510 Variable-precision DSP blocks

FPGA Configuration

- On-Board USB Blaster II (UB2) for FPGA programming and Debug
- AVSTx8 Configure with 2Gbit QSPI Flash.
- ASx4 Configure with 1Gbit QSPI Flash.

FPGA Fabric

- PCIe Gen5 x16 and CXL x16 **(*Note)**
- Four DDR4 SO-DIMM Socket, shared with HPS.
- Two QSFP-DD Port for 200/100/40/25/10 GbE network interface.
- Two MCIO 8x connectors to support PCIe and CXL **(*Note)**
- 2x5 Timing Expansion Header
- U.FL clock input / output
- 1x5 Bracket LED Expansion Header
- User LED x4, Button x2, DIP Switch x2

  ***Note: CXL feature only available for AGILEX AGIB027R29A1E2V (transceiver speed -1)**

HPS(Hard Processor System) Fabric

- MicroSD Socket
- One: DDR4 SO-DIMM Socket shared with FPGA
- Gigabit Ethernet PHY with RJ45 Port
- UART to USB Port
- USB OTG with MicroUSB Connector
- LED x1, Button x1, Cold Reset Button

Board Management System

- Power Monitor
- Temperature Monitor
- Auto fan Control

1.3. Block Diagram

Figure 1-1 shows the block diagram of the Mercury A2700 Accelerator Card. To provide maximum flexibility for the users, all key components are connected to the Agilex™ FPGA device. Thus, users can configure the FPGA to implement any system design.

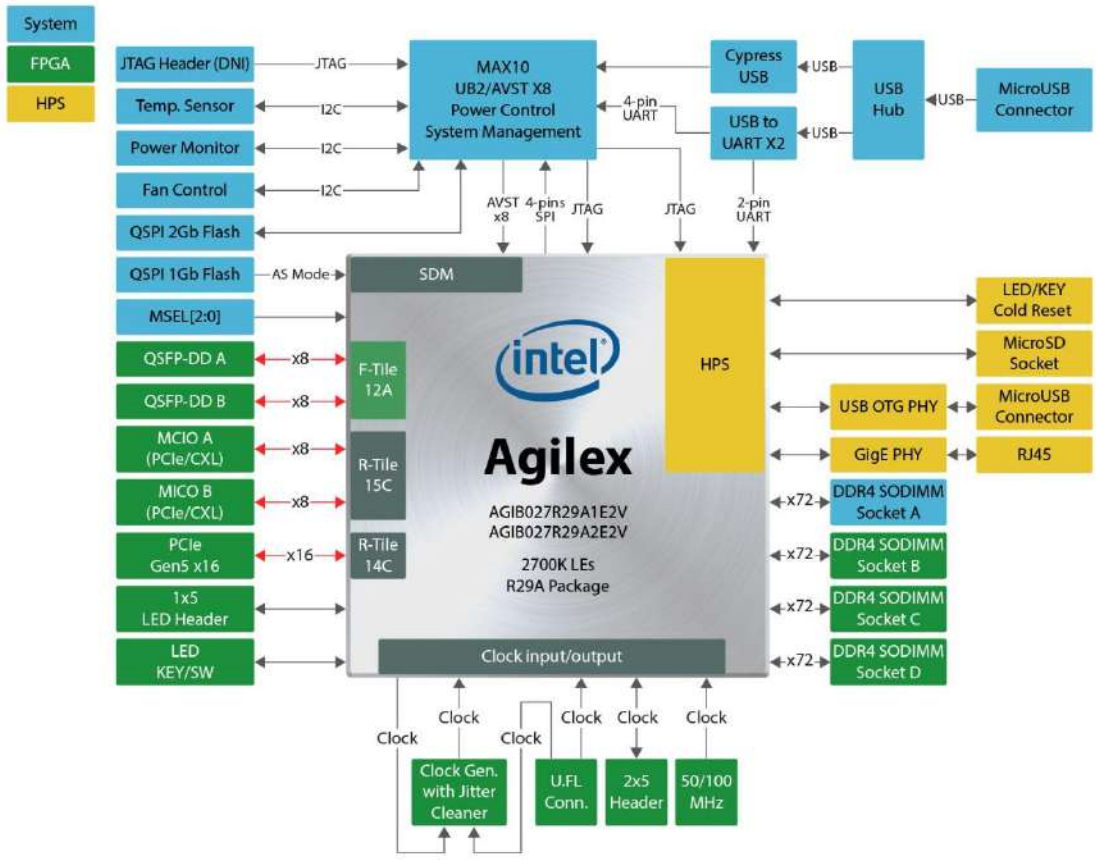


Figure 1-1 Block diagram of the Mercury A2700 Accelerator Card

1.4. Board Power On

The Mercury A2700 Accelerator Card can be used in stand-alone or be installed to the Host through PCIe slot. This section will introduce how to power on the board and the information that user should notice in these two modes.

■ Stand-alone Mode

When the Mercury A2700 Accelerator Card is used in stand-alone mode, users can use the 12V ATX power provided in the kit to connect to the 8-pin 12V ATX power connector (See **Figure 1-2**) of the Mercury A2700 Accelerator Card. To power up the board, user need to turn the power switch **SW2** to "ON" position.

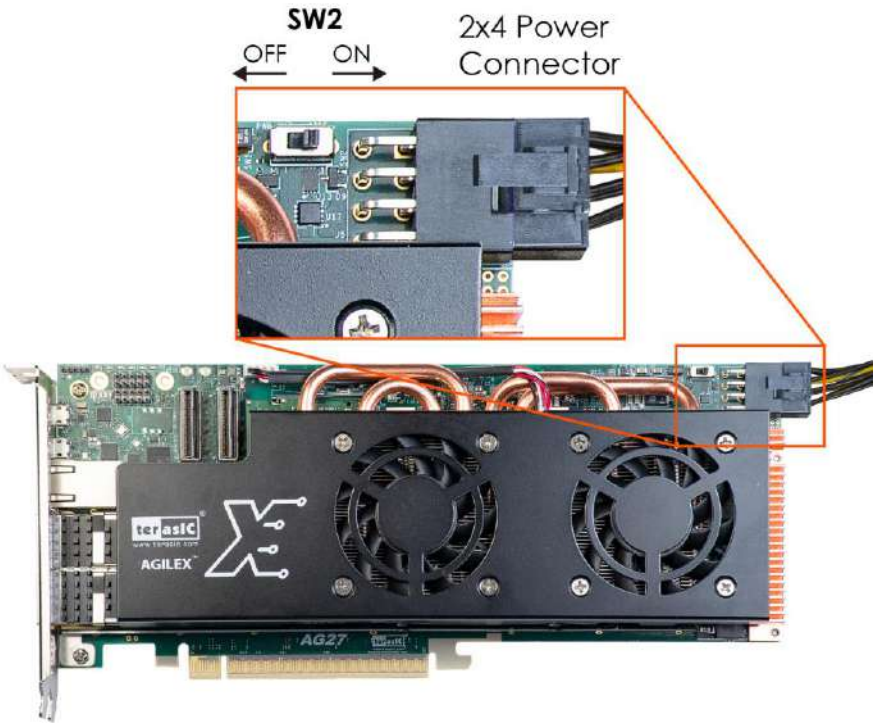


Figure 1-2 Board Power Control Switch

■ Install to Host

When the Mercury A2700 Accelerator Card is installed on the Host via PCIe slot. Although the Host can provide power to Mercury A2700 Accelerator Card via PCIe slot, but Terasic strongly recommends that users connect an external power (through

the 2x4 ATX power connector) to the board. This can prevent the power provided from Host unable to meet the power requirement of Mercury A2700 Accelerator Card. If the power supply to the board is insufficient, it may cause some components to be abnormal.

In order to avoid insufficient power supply to the board, there is a force external power switch (**SW1**) on the board (See **Figure 1-4**). The **SW1** is default set as **ON**. When install the board on the PCIe slot in the PC, users must connect the 2x4 pin 12V DC external power connector to the board, otherwise the board will not be power on. This restriction is designed to avoid FPGA damage due to insufficient power. Users can set it as **OFF** if the FPGA utilization rate is low and PCIe edge power source is sufficient.

Figure 1-3 Plug external power on the board

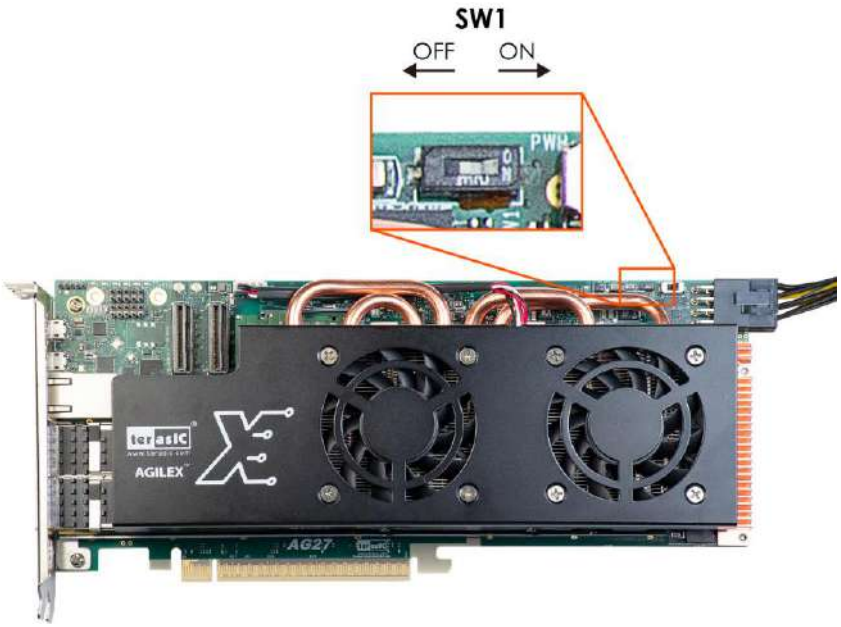


Figure 1-4 Force external power switch

1.5. Install Drivers for USB port

The Micro USB connector on the board provides 3 functions:

- USB blaster II circuit
- HPS USB to UART
- MAX10 USB to UART

The first one is **USB blaster II circuit**, which provides the JTAG interface between host and FPGA board.The second function is the serial communication function of HPS Fabric, which allows Host to communicate or debug with HPS Fabric. The last one is the UART function for board system monitoring. It allows user to monitor the staus on the board such as temperature and fan speed in real time.These three functions are all connected to the Micro USB connector through the USB hub. The user only needs to connect the host with a USB cable to the board to realize these three functions.

At the same time, some drivers need to be installed on the host to use these functions.

Users can refer to the following steps.

1. Please refer to this link to install USB Blaster II driver : Terasic Wiki

2. For the UART driver of HPS and system monitoring, please refer to section 4.1.

Figure 1-5 The Micro USB port

2.1. Board Protection

The temperature of Mercury A2700 Accelerator Card will have a lot to do with the user's design code, chassis, and ambient temperature. When using Mercury A2700 Accelerator Card in the server. Customers should pay attention to whether the temperature of Mercury A2700 Accelerator Card is too high to avoid abnormal work for user's design or even damage to the board.

The **Dashbaord_gui** software (see chapter 4 of this user manual) is provided in the system CD to allow users to monitor the temperature status of the board. A temperature monitor IP is also provided so that the user can directly monitor the temperature status in the Agilex FPGA.

If the board temperature is too high, it is recommended that customers can switch the PCIe slot position in the server chassis or increasing the fan strength in the chassis, or replace the chassis to a big space, or reduce the ambient temperature to improve

cooling system.

In addition, the efficiency of the Mercury A2700 Accelerator Card cooling system will decrease with the aging of dust and fans, so customers should re-evaluate the cooling efficiency regularly.

2.2. Mechanical Specifications

Figure 1-6 shows the Mechanical Layout of Mercury A2700 Accelerator Card. The unit of the Mechanical Layout is millimeter (mm).

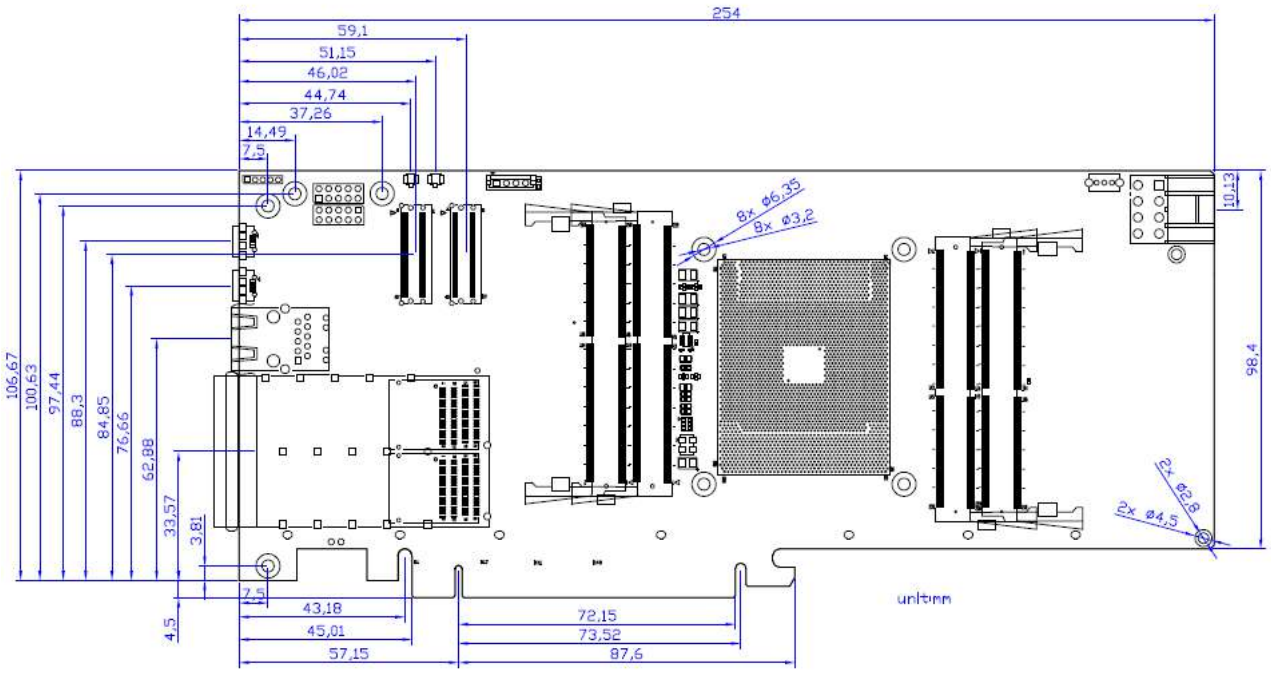


Figure 1-6 Mechanical layout

Chapter 2

Board Component

This chapter introduces all the important components on the Mercury A2700 Accelerator Card.

2.1 Board Overview

Figure 2-1 and **Figure 2-2** is the top and bottom view of the Mercury A2700 Accelerator Card development board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

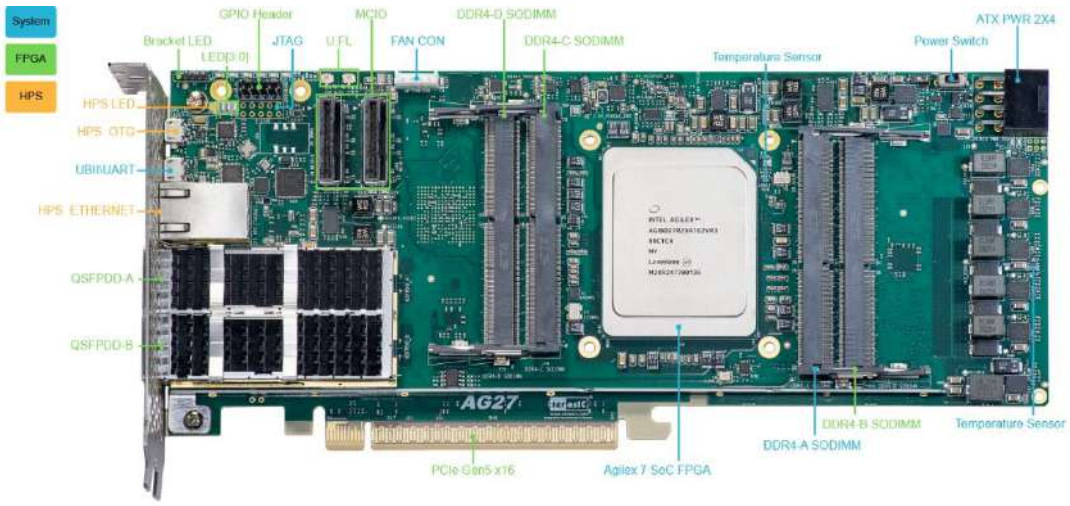


Figure 2-1 FPGA Board (Top)

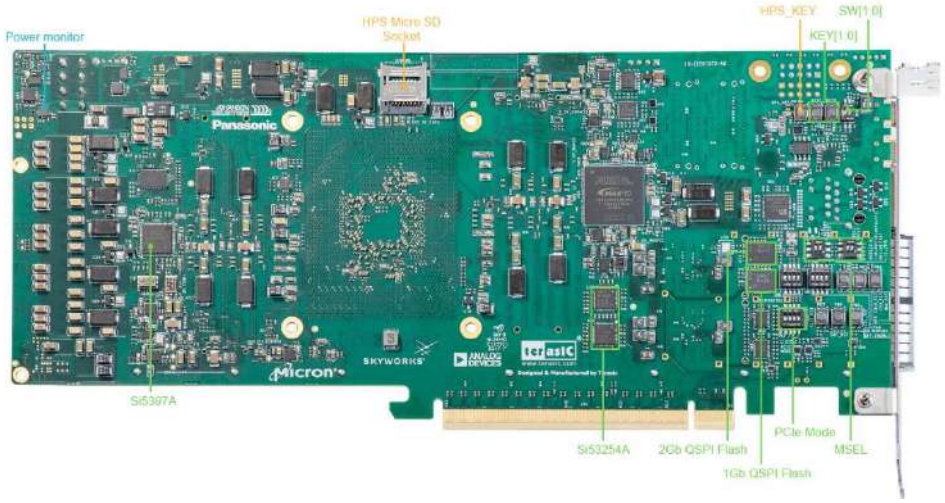


Figure 2-2 FPGA Board (Bottom)

2.2 Configuration

This section describes the configuration mode for intel Agilex® 7 device available on the board. The peripheral circuits and usage scenarios for each mode will be listed.

To switch these methods on the board, the user needs to switch the MSEL[2:0] pin of FPGA on SW4 and SW5 to change the configuration methods (See **Figure 2-3**). For details, please refer to Setup Configure Mode part of the section 2.3.

- Avalon-ST x8 (**MSEL[2:0] = 3'b110/Default Setting**)
- JTAG Mode (Configure the FPGA using the on-board USB Blaster II.
- Active Serial Fast mode (**MSEL[2:0] = 3'b001**)

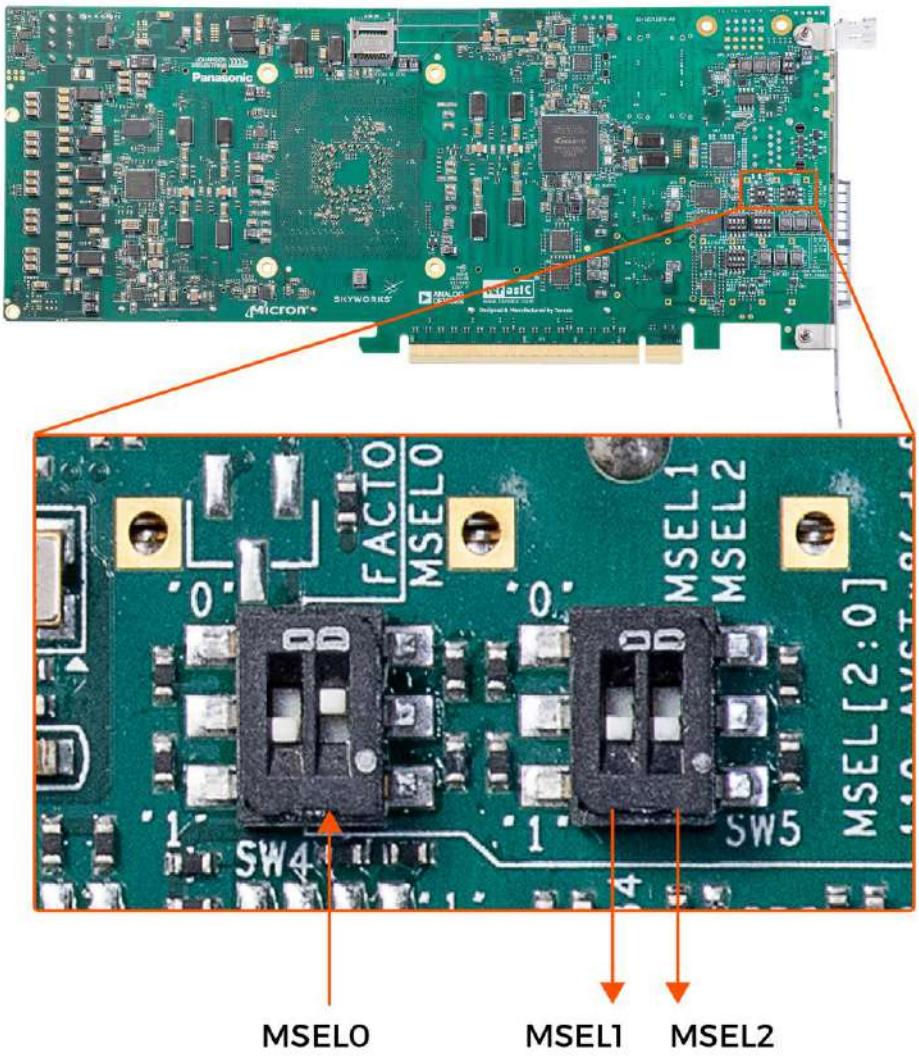


Figure 2-3 The MSEL pin setting

Detailed descriptions for each configuration methods are list in below.

■ Avalon-ST x8

Avalon-ST is the fastest configuration scheme for intel Agilex® 7 device. When using this mode, while power up the board, the System MAX10 FPGA on the board (used as an external host) will read the configuration file in the Flash, and then programming the data into the FPGA through the Avalon-ST protocol.

On DE10-Agilex board, the data bus width of Avalon-ST mode is 8-bit (Avalon-ST x 8 mode). To set board to Avalon-ST mode, users need to set MSEL[2:0] to "110" (See **Setup Configure Mode** part of the section 2.3). For how to program the configuration

file into the Flash, please refer to chapter 4.

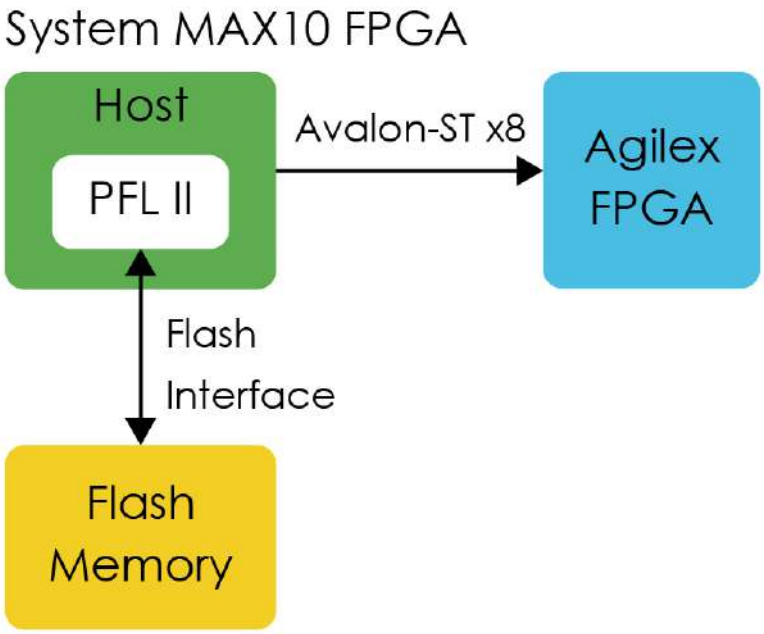


Figure 2-4 Block diagram of the Avalon-ST x 8 mode on the board

■ JTAG

JTAG-chain device programming is one of the most common and general methods. JTAG-chain device configuration uses the JTAG pins to configure the Intel® Agilex™ FPGA directly with the .sof file. Use this mode to configure FPGA, users do not need to modify MSEL specifically [2:0] pin, JTAG-chain device programming can be used under any setting. On board, users can use JTAG-chain device programming through the onboard USB blaster II circuit.

For JTAG programming by on-board USB-Blaster II, the following procedures show how to download a configuration bit stream into the Agilex FPGA:

- Make sure that power is provided to the FPGA board
- Connect your PC to the FPGA board using a Mini-USB cable and make sure the USB-Blaster II driver is installed on PC.
- Launch Quartus Prime programmer and make sure the USB-Blaster II is detected.
- In Quartus Prime Programmer, add the configuration bit stream file (.sof), check the associated “Program/Configure” item, and click “Start” to start

FPGA programming.

■ Active Serial (Fast) mode

Users can use these modes to configure the FPGA or HPS (Hardware Process System) fabric in the Intel Agilex® 7 device and make the FPGA to run the user's logic or boot the HPS to run the OS. In AS mode, the FPGA's configuration file is stored in the QSPI flash. The Secure Device Manager (SDM) in Intel Agilex® 7 device is responsible for the entire AS mode process and interface. The SDM will load the initial configuration firmware from the QSPI flash to configure the FPGA including FPGA I / O and core configuration. **Figure 2-5** shows the architecture of the AS mode of the Mercury A2700 Accelerator Card.

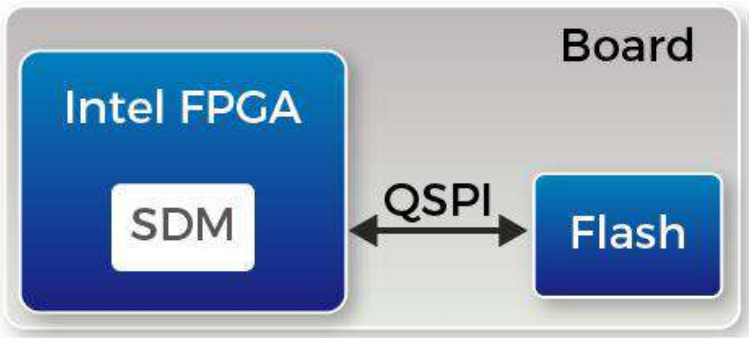


Figure 2-5 AS mode for the Mercury A2700 Accelerator Card

For more information on the configuration of Intel Agilex® 7 devices, please refer to the file: Intel Agilex Configuration User Guide

■ SoC FPGA boot

The boot process for Intel Agilex® 7 device can be divided into two different methods:

- FPGA Configuration First Mode
- HPS Boot First Mode

The difference between the two methods is the initial difference between HPS and FPGA fabric after powering on. More details can be found in the user documentation: Intel® Agilex™ SoC FPGA Boot User Guide.

The factory setting of the SoC boot of the Mercury A2700 Accelerator Card is the **FPGA Configuration First Mode**. The architecture is shown in the **Figure 2-6**. Two storage mediums are used. The system needs QSPI flash on Apollo Agilex as SDM flash for booting.

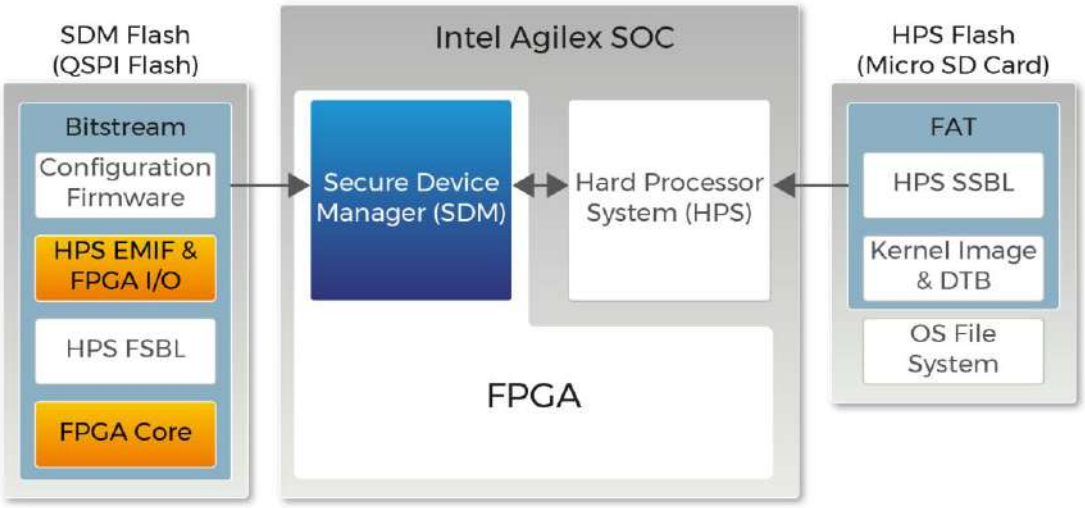


Figure 2-6 FPGA Configuration First Dual SDM and HPS Flash

The QSPI flash memory has the following boot data for the first part of the SoC FPGA configuration:

- Configuration firmware for the SDM
- FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
- FPGA core configuration data
- HPS First-Stage Boot Loader(FSBL) code and FSBL hardware handoff binary data

Meanwhile, Terasic provides the micro SD card with built-in image data as HPS flash, which is used for HPS boot in the later part. The micro SD card stores the following data:

- Second-Stage Boot Loader(SSBL)
- Kernel Image and Device Tree Blob(DTB)
- Operating System

The factory SoC boot process of Apollo Agilex is summarized as follows:

When the Mercury A2700 Accelerator Card is powered on, the SDM will read the configuration firmware and complete SDM initial form the QSPI flash according to the MSEL pin setting. Then, the SDM will configure the FPGA I/O and core (full configuration).

After the FPGA is first configured, SDM continues to load the FSBL(First-Stage Boot Loader) from the QSPI flash and transfer it to the HPS on-chip RAM, and releases the HPS reset to let the HPS start using the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals.

The FSBL then loads the SSBL(Second-Stage Boot Loader) from the Micro SD Card into HPS SDRAM and passes the control to the SSBL. The SSBL enables more advanced peripherals and loads OS into SDRAM.

Finally, the OS boots and applications are scheduled for runtime launch.

2.3 Status and Setup Components

■ Status LED

The FPGA Board development board includes board-specific status LEDs to indicate board status. Please refer to **Figure 2-7** and **Table 2-1** for the description of the LED indicator.

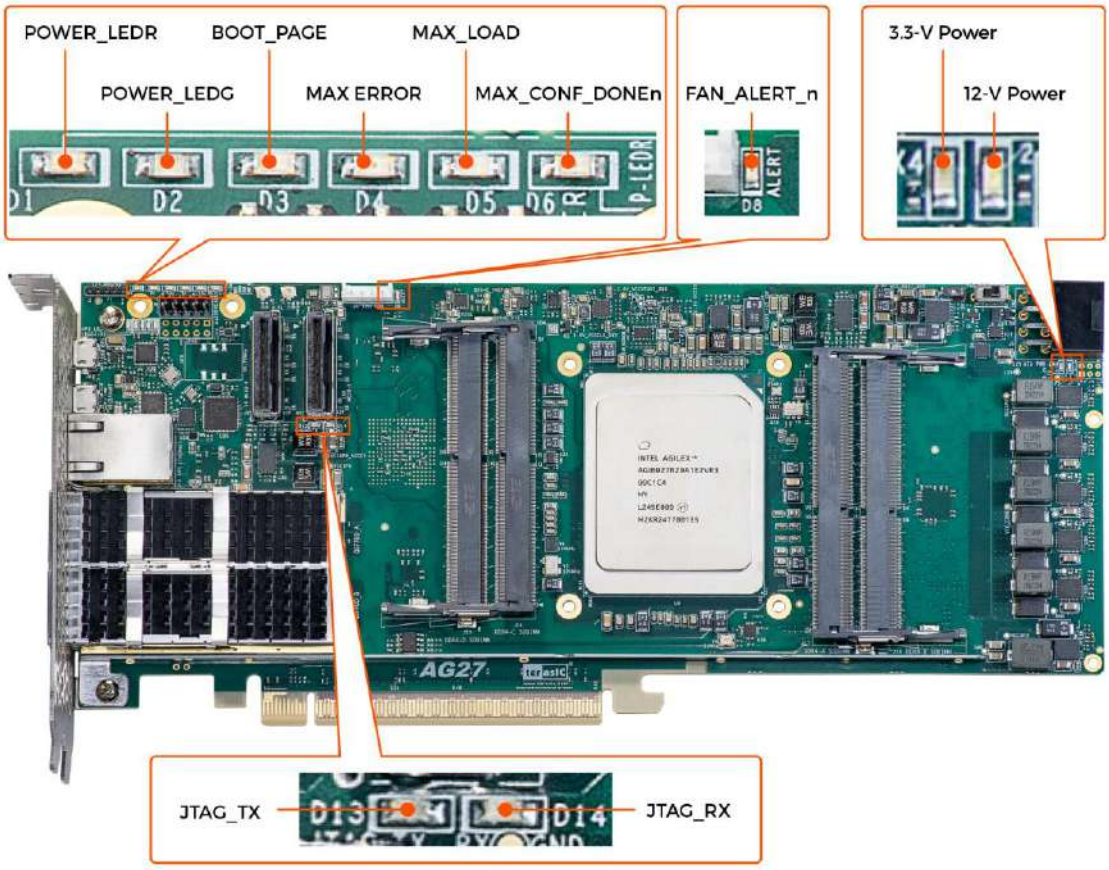


Figure 2-7 Position of the status LED

Table 2-1 Status LED

Board Reference	LED Name	Description
D11	12-V Power	Illuminates when 12-V power is active.
D10	3.3-V Power	Illuminates when 3.3-V power is active.
D8	FAN_ALERT_n	Illuminates when the fan is abnormal, such as when the fan speed is different from expected
D2	POWER_LEDG	Illuminates when the 3.3V power good and power sequence process finished. (*1)
D1	POWER_LEDR	Illuminates when the 3.3V power abnormal or power sequence process failed. (*1)

D6	MAX_CONF_DONEn	Illuminates when the FPGA is successfully configured.
D5	MAX_LOAD	Illuminates when the MAX 10 FPGA System Controller is actively configuring the FPGA.
D4	MAX_ERROR	Illuminates when the MAX 10 FPGA System Controller fails to configure the FPGA.
D3	BOOT_PAGE	Illuminates when FPGA is configured by the factory configuration bit stream.
D14	JTAG_RX	Illuminates when the USB Blaster II circuit is transmitting data
D13	JTAG_TX	Illuminates when the USB Blaster II circuit is receiving data

■ Setup PCI Express Control DIP switch

The PCI Express Control DIP switch (SW8) is provided to enable or disable different configurations of the PCIe Connector (See **Figure 2-8**). **Table 2-2** lists the switch controls and description.

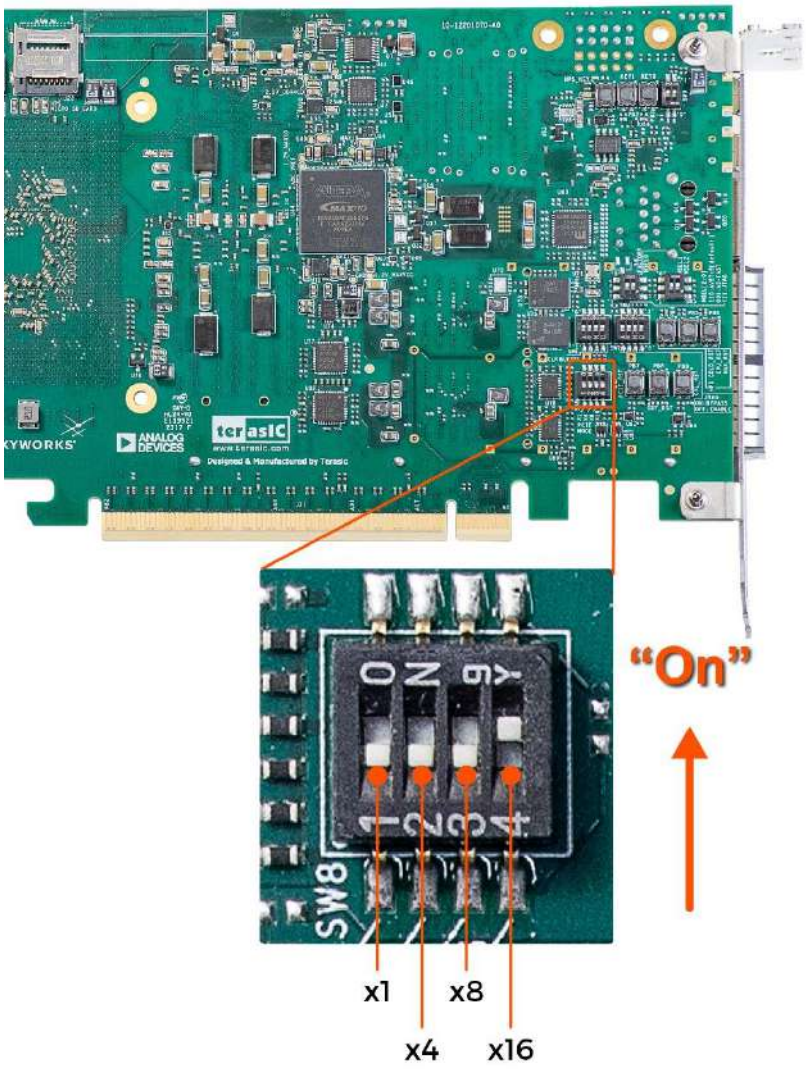


Figure 2-8 Position of the PCIe mode switch

Table 2-2 SW8 PCIe Control DIP Switch

Board Reference	Signal Name	Description	Default Setting
SW4.1	PCIE_PRSNT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	Off
SW4.2	PCIE_PRSNT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	Off
SW4.3	PCIE_PRSNT2n_x8	On : Enable x8 presence detect Off: Disable x8 presence detect	Off
SW4.4	PCIE_PRSNT2n_x16	On : Enable x16 presence detect Off: Disable x16 presence detect	**On**

■ Setup Configure Mode

The **SW5** and **SW4** slide switches are used to specify the configuration mode of the FPGA. The board supports **Avalon-ST x8** and **Fast AS** mode, please set MSEL[2:0] for your desired mode as shown in **Figure 2-9.** The default setting mode is **Avalon-ST x8** mode.

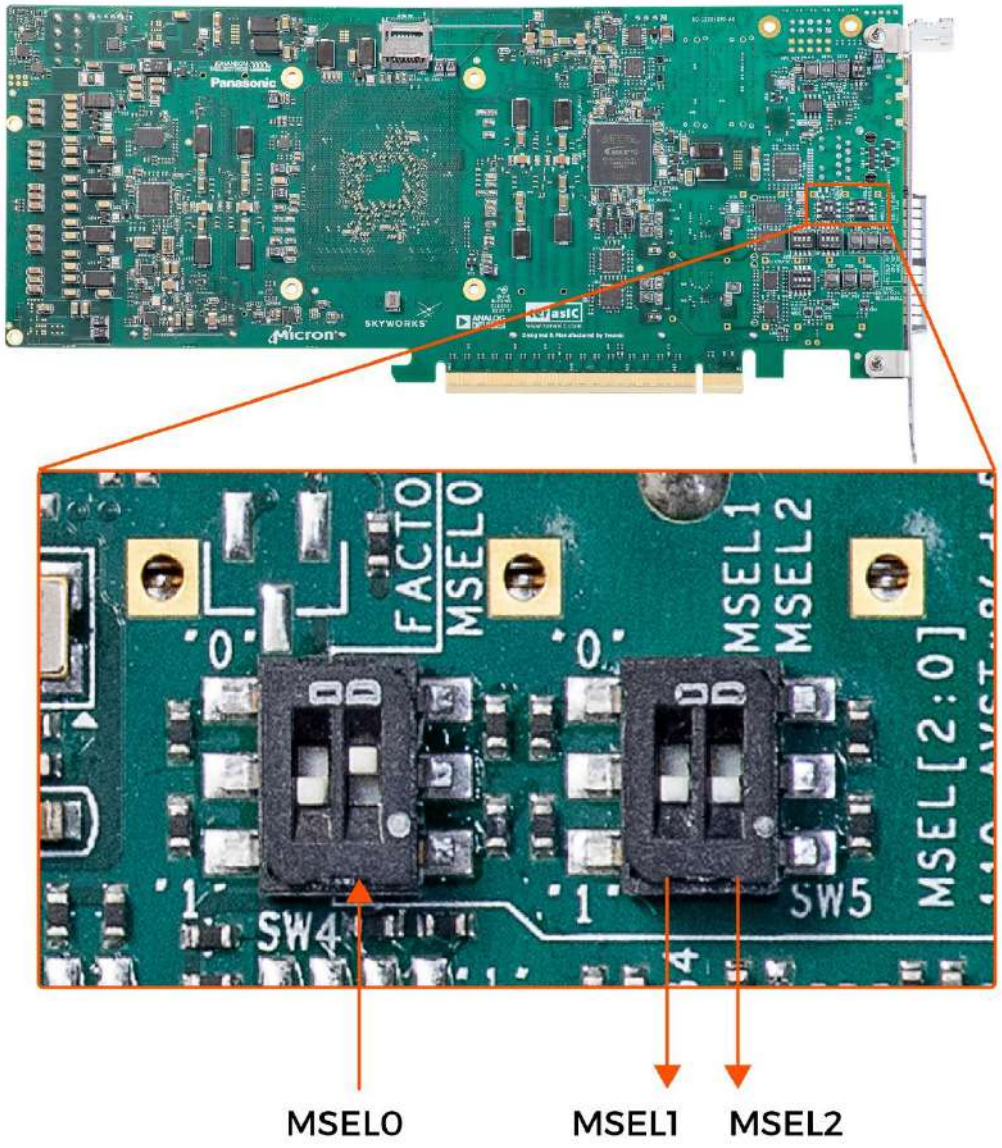


Figure 2-9 Position of slide switches SW5 and SW4 for Configuration Mode

Table 2-3 MSEL Settings for supported configuration Scheme of the board

FPGA Configuration Mode	MSEL2	MSEL1	MSEL0
Avalon-ST x8 (Default)	1	1	0
AS Fast	0	0	1
JTAG	1	1	1

■ Factory Image Switch

The factory switch can control the FPGA in AVSTx8 mode to select which page (**factory** or **user** page) of the QSPI Flash to read the configuration file from after the board is powered. When the user switches the factory switch to the "1" position, the FPGA will read the factory default code in the flash to boot the FPGA..

Table 2-4 Setting for Factory image switch

Board Reference	Signal Name	Description	Default
SW4	FACTORY_LOAD	**1** : Factory page image **0**: User page image	1

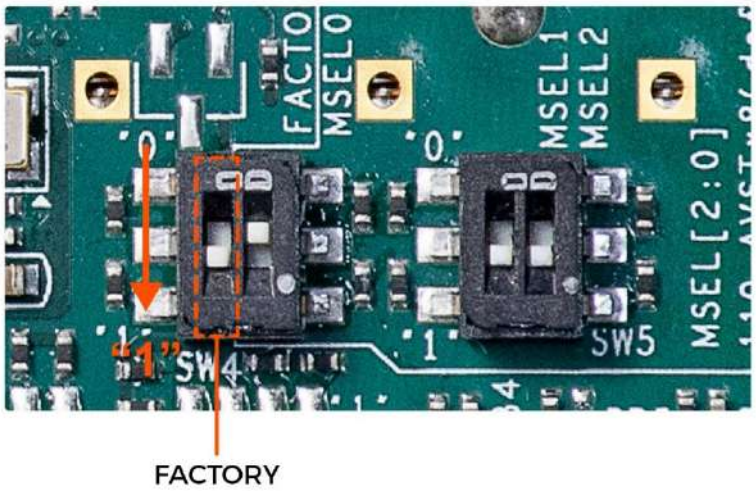


Figure 2-10 Factory Image Switch

■ JTAG Bypass Switch

The JTAG interface switch SW7 is to set whether the JTAG interface of the **HPS fabric** , **FPGA**, **System MAX10 FPGA** and **PCIe EP edge** is connected to the JTAG chain in the board. As long as the interface controlled by the switch is set to "**ON**" position, the interface will be included on the JTAG chain on the board. (See **Figure 2-11**).**Table 2-5** lists the setting of the SW3.

Note, if the user turns any of the position on SW3 to the "**OFF**" position, but does not connect the JTAG device on that interface. The JTAG chain on the board will not be able to form a closed loop and Quartus will not be able to detect the FPGA device.

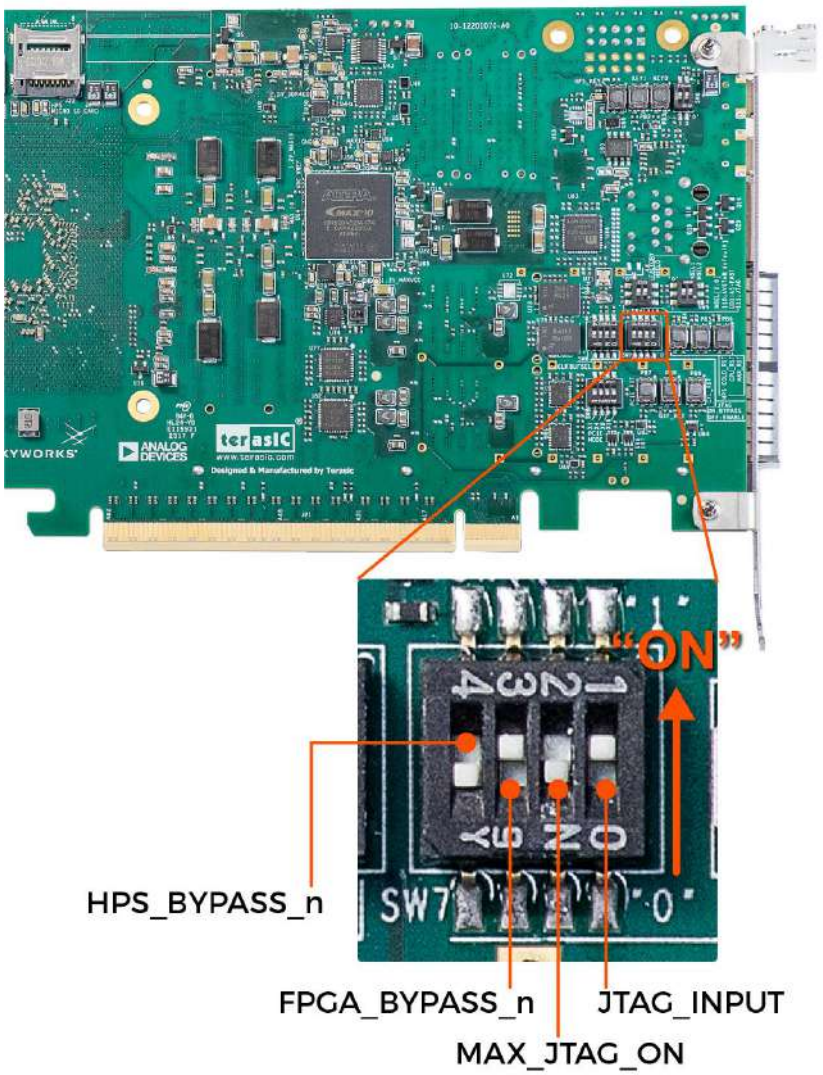


Figure 2-11 JTAG Bypass Switch

Table 2-5 JTAG Bypass Switch setting

Board Reference	Signal Name	Description	Default
SW7.1	JTAG_INPUT	**If no external blaster is connected to the External JTAG header (J7):** **ON** : The board's JTAG input interface is from the **on-board USB blaster II** **OFF**: The board's JTAG input interface is from the **PCIe EP Edge**	ON
SW7.2	MAX_JTAG_ON	**ON** : **Enable** the JTAG interface of the **System MAX10 FPGA** into the JTAG chain **OFF**: **Disable** the JTAG interface of the **System MAX10 FPGA** into the JTAG chain	OFF
SW7.3	FPGA_BYPASS_n	**ON** : **Enable** the JTAG interface of the **FPGA** into the JTAG chain **OFF**: **Disable** the JTAG interface of the **FPGA** into the JTAG chain	ON
SW7.4	HPS_BYPASS_n	**ON** : **Enable** the JTAG interface of the **HPS** connector into the JTAG chain **OFF**: **Disable** the JTAG interface of the **HPS** connector into the JTAG chain	OFF

■ PCIe Clock Select Switch

The **PCIe Clock Select Switch** is mainly used to control the reference clock source of PCIe applications sent to FPGA transceivers. **Figure 2-12** is the block diagram of the reference clocks distribution on the board for PCIe applications. As shown in the figure, there is an **PCIe Clock Generator**(SI52204) that can generate two sets of 100Mhz

clocks for the MCIO connector and two clocks to the **clock buffers**(SI53254).The board has two clock buffers, allowing the user to choose the source of the reference clock provided to the FPGA transceiver from the on-board PCIe Clock Generator or MCIO connector/PCIe golden finger. Users can set the clock source of clock buffers through the **PCIe Clock Select Switch** (**SW6**). Finally, if the user does not need to run MCIO RootPort mode or no need for the on-board PCIe Clock Generator to provide 100MHz clock to the FPGA transceiver. User can **turn off** the clock output of the PCIe clock generator through the switch on the **SW6**.

Figure 2-13 shows the position of SW6 on the board and the switch definition. For detailed settings of SW6, please refer to **Table 2-6**.

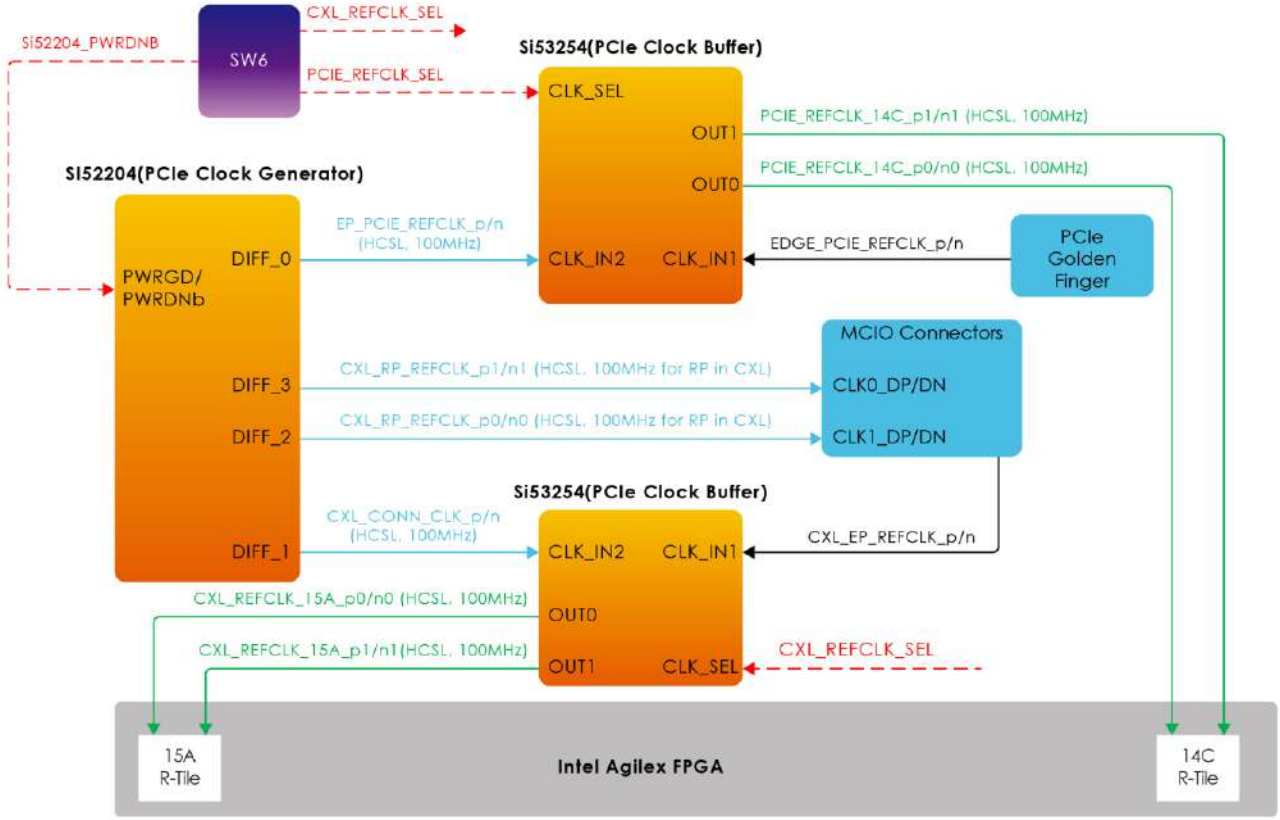


Figure 2-12 Block diagram of the PCIe clock application

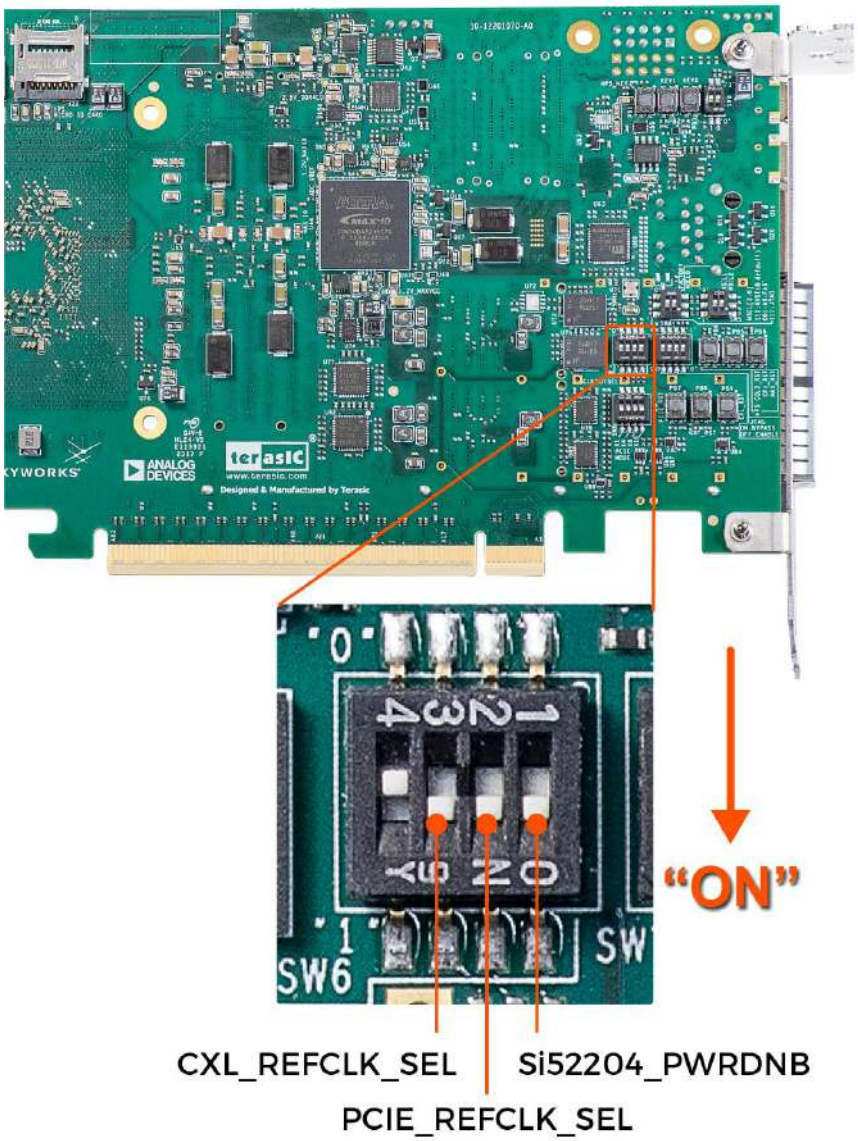


Figure 2-13 PCIe Clock Select Switch

Table 2-6 PCIe Clock Select Switch setting

Board Reference	Signal Name	Description	Default
SW6.1	Si52204_PWRDNB	**ON** : PCIe Clock Generator(SI52204) will output 100Mhz clock **OFF**: PCIe Clock Generator(SI52204) will **stop** output 100Mhz clock	ON
SW6.2	PCIE_REFCLK_SEL	**ON** : The reference clock for to FPGA (PCIE_REFCLK_14C_p/n[1:0]) will be	ON

		came from **PCIe golden finger**. **OFF**: The reference clock for to FPGA (PCIE_REFCLK_14C_p/n[1:0]) will be came from on-board **PCIe clock generator**.	
SW6.3	CXL_REFCLK_SEL	**ON** : The reference clock for to FPGA (CXL_REFCLK_15A_p/n[1:0]) will be came from **MCIO Connectors**. **OFF**: The reference clock for to FPGA (CXL_REFCLK_15A_p/n[1:0]) will be came from on-board **PCIe clock generator**.	ON

2.4 Reset Devices

The board provides 4 reset buttons for different system reset situations (see **Figure 2-14**). These buttons can reset FPGA, System MAX, HPS and FPGA respectively. Please refer to the following **Table 2-7** for details.

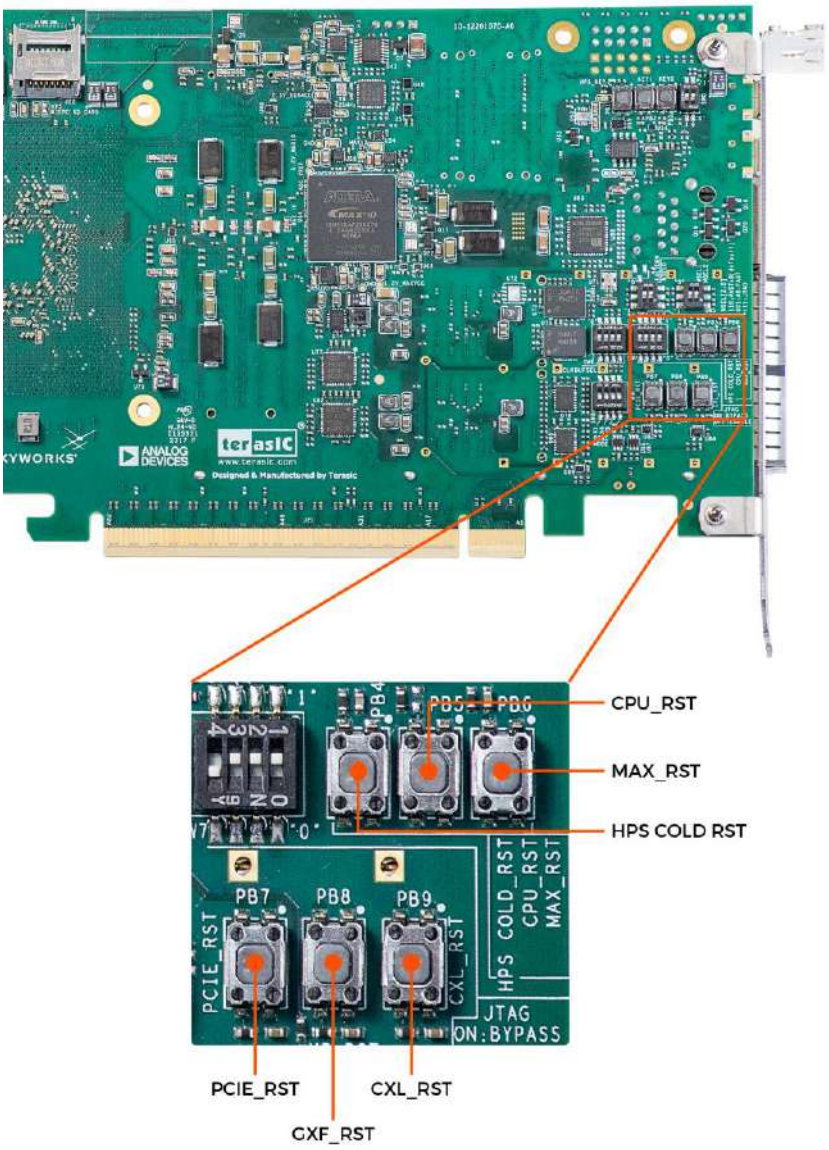


Figure 2-14 Rest devices of the board

Table 2-7 Reset Devices Pin Assignments, Schematic Signal Names, and Functions

Part Number	Schematic Signal Name	I/O Standard	Agilex Pin Number	Application
PB5	CPU_RST	1.2V	PIN_B47	This button can be used for rest FPGA

PB6	MAX_RST	--	--	For resetting System MAX10
PB4	HPS_COLD_RST	--	--	For resetting System HPS Fabric
PB7	PCIE_RST	1.2V	PIN_CD58	Push to reset PCIe bus
PB8	CXF_RST	1.2V	PIN_JL61	Push to reset CXF bus
PB9	CXL_RST	1.2V	PIN_HY33	Push to reset CXL bus on the MCIO connectors

2.5 General User Input/Output

This section describes the user I/O interface of the FPGA.

■ User Defined Push-buttons

As shown in **Figure 2-15**, the FPGA board includes three user defined push-buttons (one for HPS farbric) that allow users to interact with the Agilex device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-8** lists the board references, signal names and their corresponding Agilex device pin numbers.

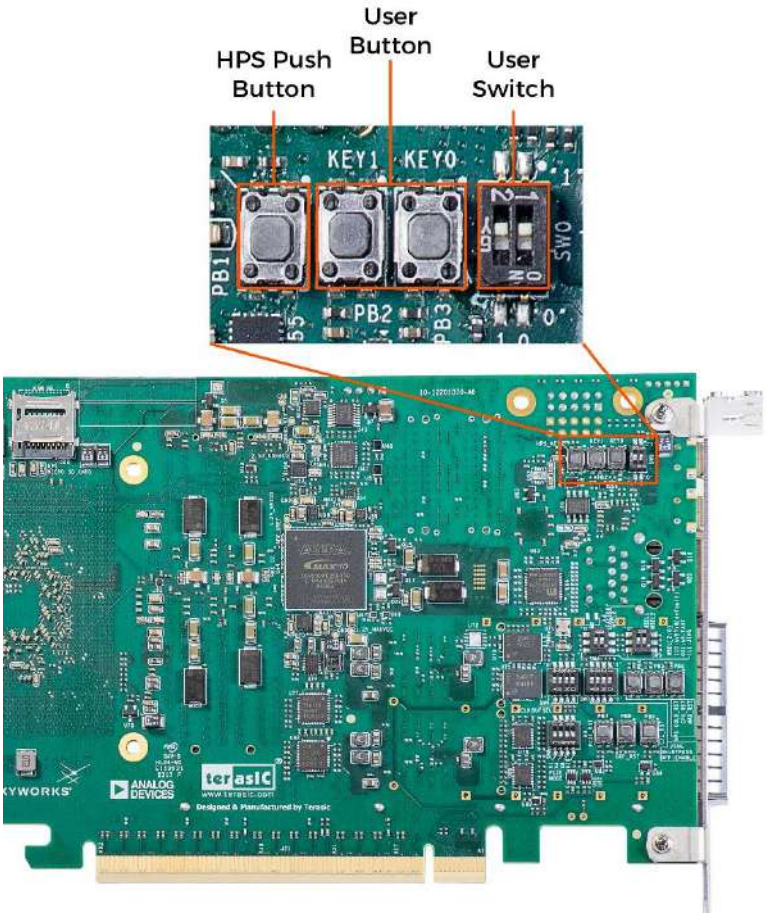


Figure 2-15 Position of user buttons and switch

Table 2-8 Push-button Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
KEY0	BUTTON0	High Logic Level when the button is not pressed	1.2V	PIN_U47
KEY1	BUTTON1		1.2V	PIN_N47
PB1	HPS Push Bitton		1.2V	PIN_N13

■ User-Defined Dip Switch

As shown in **Figure 2-15**,there are two positions dip switches (SW0) on the FPGA

board to provide additional FPGA input control. When a position of dip switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Agilex FPGA, respectively.

Table 2-9 lists the signal names and their corresponding Agilex device pin numbers.

Table 2-9 Push-button (FPGA) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
SW0.1	SW0	High logic level when SW in the UPPER position.	1.2 V	PIN_L48
SW0.2	SW1		1.2 V	PIN_W48

■ User-Defined LEDs

As shown in **Figure 2-16**, the FPGA board consists of 5 user-controllable LEDs(one for HPS fabric) and a 5-pin LED bracket connector. The user-controllable LEDs allow status and debugging signals to be driven to the LEDs from the designs loaded into the Agilex device. Each LED is driven directly by the Agilex FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in **Table 2-10**.

5-pin LED bracket connector is reserved for connecting expanded LEDs. **Figure 2-17** shows the circuit for the connectors and **TTable 2-11** list of the connector pin names on the FPGA that are connected to the LEDs.

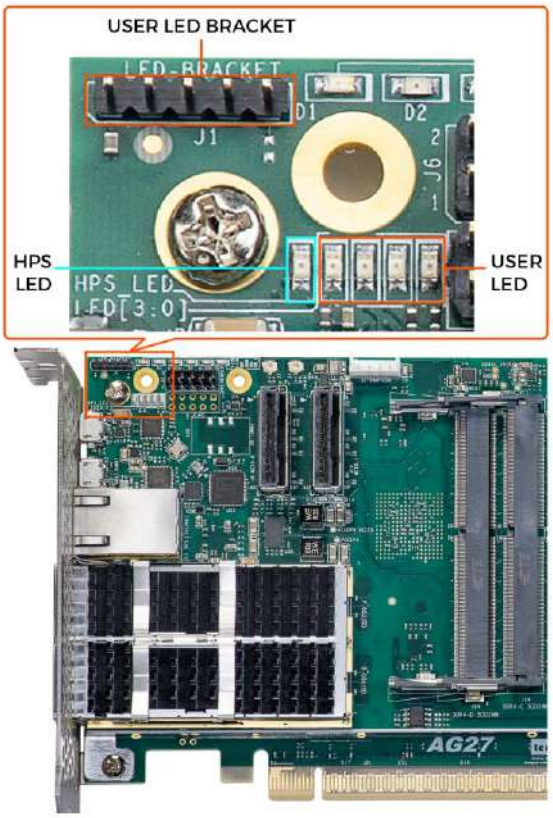


Figure 2-16 Position of all the user defined LEDs

Table 2-10 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
LED0	LED0	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	1.2V	PIN_H48
LED1	LED1		1.2V	PIN_J47
LED2	LED2		1.2V	PIN_W50
LED3	LED3		1.2V	PIN_N51
HPS_LED	HPS_LED		1.2V	PIN_BJ27

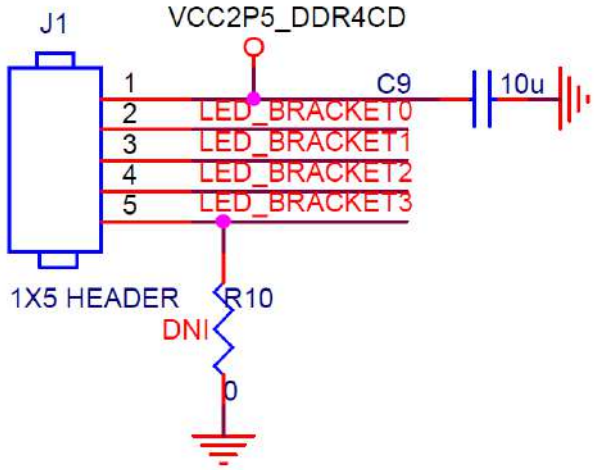


Figure 2-17 Circuit of the 5-pin LED bracket connector

Table 2-11 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
J1.1	LED_BRACKET0	--	1.2V	PIN_N49
J1.2	LED_BRACKET1		1.2V	PIN_L52
J1.3	LED_BRACKET 2		1.2V	PIN_L50
J1.4	LED_BRACKET 3		1.2V	PIN_U49

■ 2x5 GPIO Header (Timing Expansion Header)

The FPGA board has one 2x5 GPIO header J5 for expansion function as shown in **Figure 2-18.** The pin-out of J5 is shown in **Figure 2-19**. GPIO_P0 ~ GPIO_P3 are bi-direction 1.2V GPIO. GPIO_CLK0 and GPIO_CLK1 are connected to FPGA dedicated clock input and can be configured as two single-ended clock signals. **Table 2-12** shows the mapping of the FPGA pin assignments to the 2x5 GPIO header.

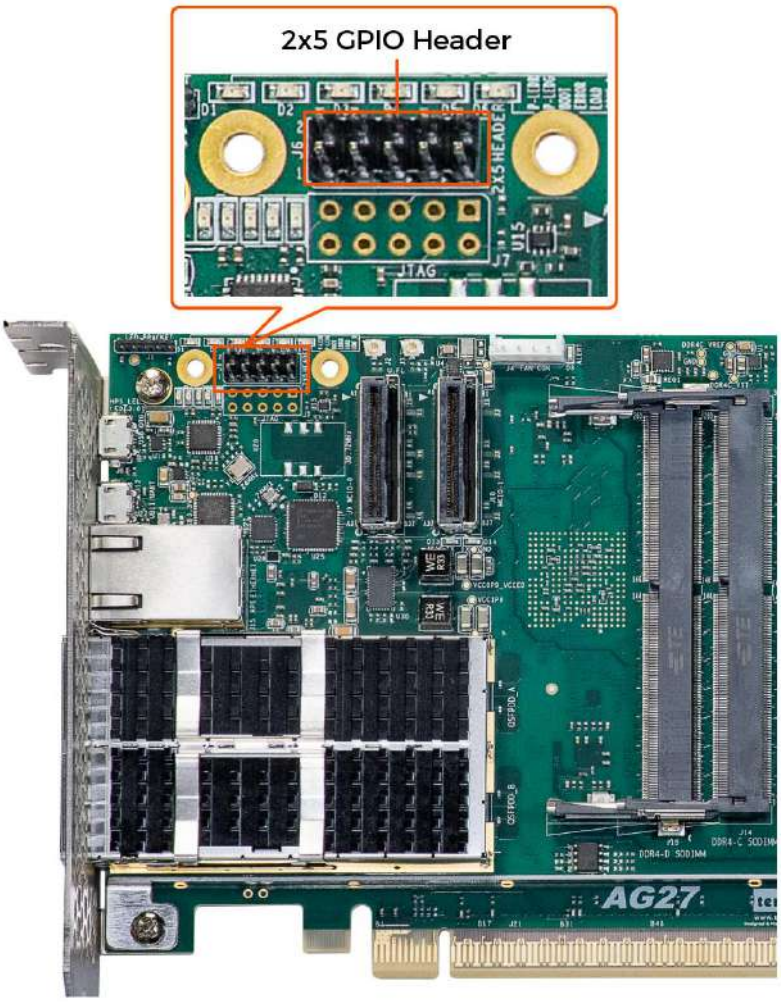


Figure 2-18 2x5 expansion header

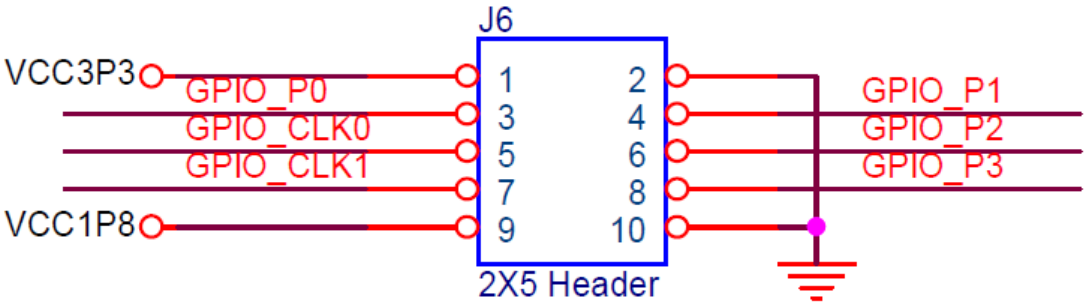


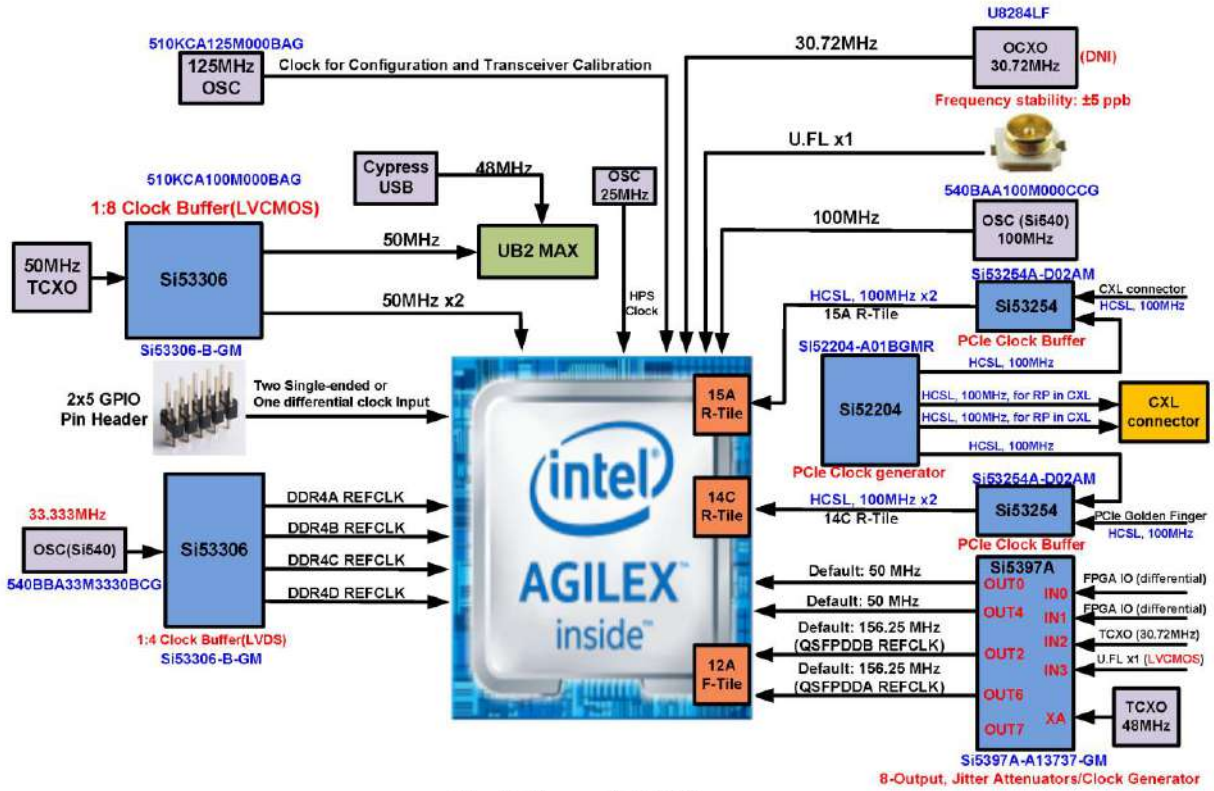
Figure 2-19 Pin-out of 2x5 expansion header

Table 2-12 2x5 GPIO Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
GPIO_P0	Bi-direction 1.2V GPIO	1.2V	PIN_KU28
GPIO_P1	Bi-direction 1.2V GPIO	1.2V	PIN_JY28
GPIO_P2	Bi-direction 1.2V GPIO	1.2V	PIN_KU26
GPIO_P3	Bi-direction 1.2V GPIO	1.2V	PIN_JP26
GPIO_CLK0	FPGA dedicated clock input or Bi-direction 1.2V GPIO	1.2V	PIN_KR29
GPIO_CLK1	FPGA dedicated clock input or Bi-direction 1.2V GPIO	1.2V	PIN_KF26

2.6 Clock Circuit

The development board includes several oscillator (25/50/33.33/100/125 MHz) and two programmable clock generators. **Figure 2-20** shows the default frequencies of on-board all external clocks going to the Agilex FPGA.



Clock Tree of AG27

Figure 2-20 Clock circuit of the FPGA Board

A clock buffer (Si53306) is used to duplicate the 50 MHz TCXO output clock, so there are two 50MHz clocks fed into different Agilex FPGA banks and one clock for USB blaster II circuit.

The programming clock generator (Si5397A) with low-jitter clock output which are used to provide special and high- quality clock signals for high-speed transceivers. Through I2C serial interface, the clock generator controllers in the Agilex FPGA can be used to program the Si5397As to generate many frequencies to each QSFP-DD port.

For memory interface, the board provide a 33.333Mhz clock and fan out it to four different clocks to the Agilex FPGA via clock buffer (Si53306). The four clocks are used for the reference clock of the four DDR4 SODIMMs.

Two UFL connectors provide two external single-ended clock inputs or one external differential clock inputs. One oscillator provides a 125 MHz clock used as configuration

clock or used as the clock for transceiver calibration. Besides, there is one 100 MHz clock source to use as the FPGA input clock.

Finally, for PCIe application, user can choose the clock output from the on-board PCIe clock generator (Si52204), or clock from the PCIe golden finger/MCIO connector to feed to Agilex FPGA as reference clock. For detailed information, please refer to section 2.3: *PCIe Clock Select Switch*.

Table 2-13 lists the clock source, signal names, default frequency and their corresponding Agilex device pin numbers.

Table 2-13 Clock Source, Signal Name, Default Frequency, Pin Assignments and Functions

Source	Schematic Signal Name	Default Frequency	I/O Standard	Agilex Pin Number	Application
U36	CLK_50_B3B	50.0 MHz	1.2V	PIN_U51	User application
	CLK_50_B3C		1.2V	PIN_N45	User application
Y6	CLK_100_B2B_p	100.0MHz	LVDS	PIN_LB60	User application
Y7	OSC_CLK_1	125MHz	LVDS	PIN_KU64	User-supplied configuration clock
J2	UFL_CLKIN	User Defined	*(1)	PIN_KU56	External Clock Input
U69	CLK_from_SI5397A_p0	50.0 MHz	LVDS	PIN_KC31	User application
	CLK_from_SI5397A_p1	50.0 MHz	LVDS	PIN_J41	User application
	QSFPDDA_REFCLK_p	156.25 MHz	LVDS	PIN_HJ68	QSFP-DD A port
	QSFPDDB_REFCLK_p	156.25 MHz	LVDS	PIN_JD74	QSFP-DD B port
	QSFPDDRSV_REFCLK_p	156.25 MHz	LVDS	PIN_HL74	Reserved for QSFP-DD port
U20	CLK_30M72	30.72MHz	1.2V	PIN_KJ27	Reserved
U62	DDR4A_REFCLK_p	33.333	LVDS	PIN_AA31	DDR4 reference

		MHz			clock for A port
	DDR4B_REFCLK_p	33.333 MHz	LVDS	PIN_AG63	DDR4 reference clock for B port
	DDR4C_REFCLK_p	33.333 MHz	LVDS	PIN_KU36	DDR4 reference clock for C port
	DDR4D_REFCLK_p	33.333 MHz	LVDS	PIN_MA44	DDR4 reference clock for D port

*(1): The I/O standard of the **UFL_CLKIN** clock input from J1 to the FPGA needs to be **1.2V**. If the input clock I/O standard from the J1 exceeds 1.2V, it should be divided to 1.2V by using two series resistors (R28 and R29). **Figure 2-21** shows that in the case of different input clock voltage level, the corresponding resistance value settings for R13 and R28 are required.

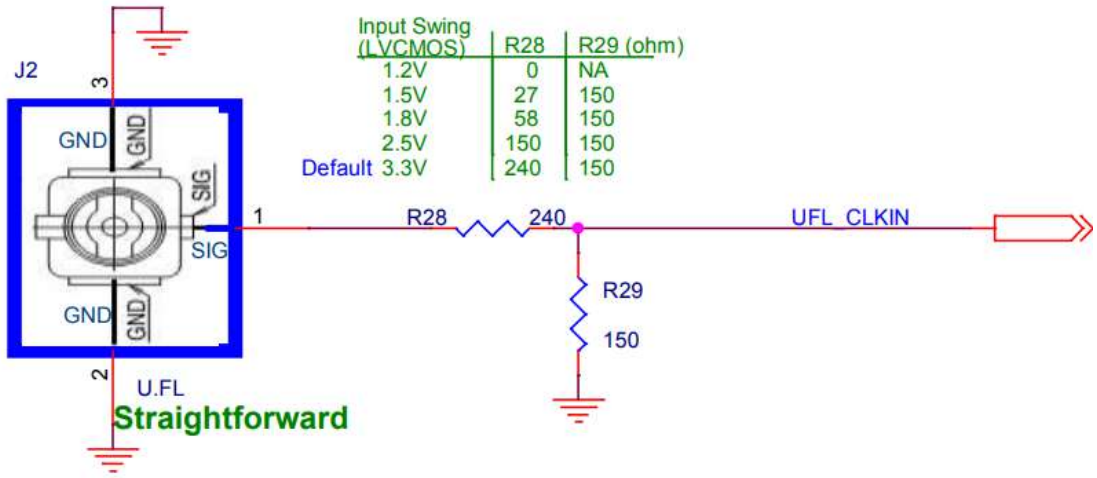


Figure 2-21 U.FL clock input signal level setting

Table 2-14 lists the programming clock generator (Si5397A and for QSFP-DD interface) control pin, signal names, I/O standard and their corresponding Agilex device pin numbers.

Table 2-14 Programmable clock generator control pin, Signal Name, I/O standard, Pin Assignments and Descriptions

Programmable clock generator	Schematic Signal Name	I/O Standard	Agilex Pin Number	Description
Si5397A (U69)	SI5397A_I2C_SCL	1.2V	PIN_B51	I2C bus, connected with Si5397A
	SI5397A_I2C_SDA	1.2V	PIN_D48	
	SI5397A_LOL_A	1.2V	PIN_J43	Loss Of Lock_A/B/C/D. These output pins indicate when DSPLL A, B, C, D is outof-lock (low) or locked (high). They can be left unconnected when not in use.
	SI5397A_LOL_B	1.2V	PIN_D42	
	SI5397A_LOL_C	1.2V	PIN_B41	
	SI5397A_LOL_D	1.2V	PIN_H44	
	SI5397A_LOS_XAXB	1.2V	PIN_D44	Si5397A loss of XA/XB signal
	SI5397A_RST_n	1.2V	PIN_J49	Si5397A reset signal
	SI5397A_OE_n	1.2V	PIN_D50	Si5397A output enable signal
	SI5397A_INTR_n	1.2V	PIN_U45	This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.

2.7 DDR4 SDRAM Interface

The development board supports four independent banks of DDR4 SDRAM SO-DIMM (DDR4 SO-DIMM **A/B/C/D**). DDR4 SO-DIMM **B**,**C** and **D** socket are used for the EMIF of the FPGA. The I/O bank where DDR4 SO-DIMM **A** socket is located can implement Intel Agilex FPGA EMIF IP with the Intel Agilex FPGA Hard Processor Subsystem (HPS). If HPS EMIF is not used in a system, the DDR4 SO-DIMM Socket A can be used for the EMIF of the FPGA. **Table 2-15** shows the maximum capacity and associated running speed for each DDR4 SO-DIMM socket. The maximum capacity of

DDR4 SO-DIMM socket A and DDR4 SO-DIMM socket B/C/D are 16GB and 32GB, respectively. The maximum running speed for each socket can be 1333Mhz.

Figure 2-22 shows the connections between the DDR4 interface and Intel Agilex® 7 device.

Table 2-15 DDR4 SO-DIMM sockets maximum capacity and associated running speed

Configuration	DDR4 SO-DIMM A	DDR4 SO-DIMM B/C/D	Maximum Capacity
Standard Configuration	8GB @ 2666MTS	8GB @ 2666MTS	32GB
Maximal Capacity	16GB @ 2666MTS	32GB @ 2400MTS	112GB
Maximal Capacity with 2666MTS	16GB @ 2666MTS	16GB @ 2666MTS	64GB

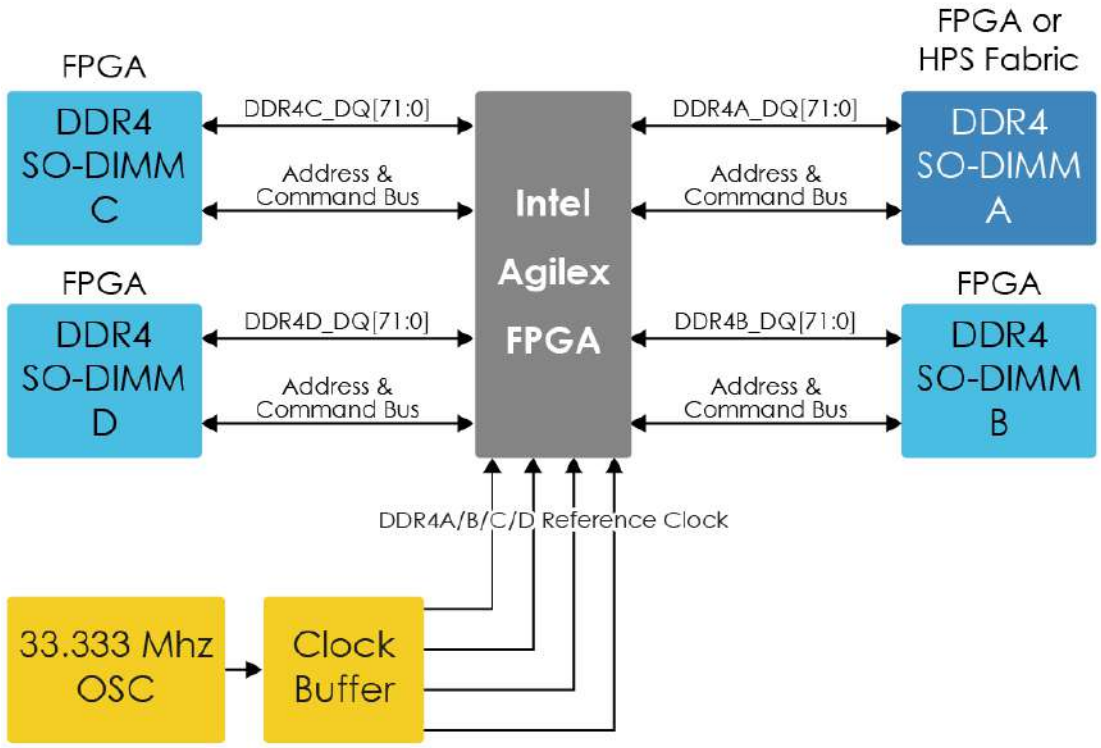


Figure 2-22 Connection between the DDR4 and Agilex FPGA

The pin assignments for DDR4 SDRAM SO-DIMM Bank A/B/C/D are listed in **Table 2-16** and **Table 2-17**.

Table 2-16 DDR4-A Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
DDR4A_REFCLK_p	DDR4 A port Reference Clock p	True Differential Signaling	PIN_AA31
DDR4A_A0	Address [0]	SSTL-12	PIN_N33
DDR4A_A1	Address [1]	SSTL-12	PIN_L34
DDR4A_A2	Address [2]	SSTL-12	PIN_U33
DDR4A_A3	Address [3]	SSTL-12	PIN_W34
DDR4A_A4	Address [4]	SSTL-12	PIN_N31
DDR4A_A5	Address [5]	SSTL-12	PIN_L32
DDR4A_A6	Address [6]	SSTL-12	PIN_U31
DDR4A_A7	Address [7]	SSTL-12	PIN_W32
DDR4A_A8	Address [8]	SSTL-12	PIN_N29
DDR4A_A9	Address [9]	SSTL-12	PIN_L30
DDR4A_A10	Address [10]	SSTL-12	PIN_U29
DDR4A_A11	Address [11]	SSTL-12	PIN_W30
DDR4A_A12	Address [12]	SSTL-12	PIN_AK32
DDR4A_A13	Address [13]	SSTL-12	PIN_AA29
DDR4A_A14	Address [14]/ WE_n	SSTL-12	PIN_AD30
DDR4A_A15	Address [15]/ CAS_n	SSTL-12	PIN_AN29
DDR4A_A16	Address [16]/ RAS_n	SSTL-12	PIN_AK30
DDR4A_BA0	Bank Select [0]	SSTL-12	PIN_AD28
DDR4A_BA1	Bank Select [1]	SSTL-12	PIN_AN27
DDR4A_BG0	Bank Group Select [0]	SSTL-12	PIN_AK28
DDR4A_BG1	Bank Group Select [1]	SSTL-12	PIN_AV37

DDR4A_CK	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_AV33
DDR4A_CK_n	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_AT34
DDR4A_CKE	Clock Enable pin	SSTL-12	PIN_BC35
DDR4A_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2V POD	PIN_N5
DDR4A_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2V POD	PIN_B13
DDR4A_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2V POD	PIN_B25
DDR4A_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2V POD	PIN_B31
DDR4A_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2V POD	PIN_N37
DDR4A_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2V POD	PIN_AA41
DDR4A_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2V POD	PIN_AV41
DDR4A_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2V POD	PIN_AA35
DDR4A_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2V POD	PIN_AV29
DDR4A_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2V POD	PIN_L7
DDR4A_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2V POD	PIN_D15
DDR4A_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2V POD	PIN_D26
DDR4A_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2V POD	PIN_D32
DDR4A_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2V POD	PIN_L38
DDR4A_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2V POD	PIN_AD42

DDR4A_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2V POD	PIN_AT42
DDR4A_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2V POD	PIN_AD36
DDR4A_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2V POD	PIN_AT30
DDR4A_DQ0	Data [0]	1.2V POD	PIN_W4
DDR4A_DQ1	Data [1]	1.2V POD	PIN_L4
DDR4A_DQ2	Data [2]	1.2V POD	PIN_U9
DDR4A_DQ3	Data [3]	1.2V POD	PIN_W11
DDR4A_DQ4	Data [4]	1.2V POD	PIN_U2
DDR4A_DQ5	Data [5]	1.2V POD	PIN_N2
DDR4A_DQ6	Data [6]	1.2V POD	PIN_N9
DDR4A_DQ7	Data [7]	1.2V POD	PIN_L11
DDR4A_DQ8	Data [8]	1.2V POD	PIN_H11
DDR4A_DQ9	Data [9]	1.2V POD	PIN_D11
DDR4A_DQ10	Data [10]	1.2V POD	PIN_B17
DDR4A_DQ11	Data [11]	1.2V POD	PIN_H19
DDR4A_DQ12	Data [12]	1.2V POD	PIN_H7
DDR4A_DQ13	Data [13]	1.2V POD	PIN_J9
DDR4A_DQ14	Data [14]	1.2V POD	PIN_D19
DDR4A_DQ15	Data [15]	1.2V POD	PIN_J17
DDR4A_DQ16	Data [16]	1.2V POD	PIN_B21
DDR4A_DQ17	Data [17]	1.2V POD	PIN_D23
DDR4A_DQ18	Data [18]	1.2V POD	PIN_D28
DDR4A_DQ19	Data [19]	1.2V POD	PIN_B27
DDR4A_DQ20	Data [20]	1.2V POD	PIN_J21
DDR4A_DQ21	Data [21]	1.2V POD	PIN_H23
DDR4A_DQ22	Data [22]	1.2V POD	PIN_H28
DDR4A_DQ23	Data [23]	1.2V POD	PIN_J27
DDR4A_DQ24	Data [24]	1.2V POD	PIN_B29
DDR4A_DQ25	Data [25]	1.2V POD	PIN_D30
DDR4A_DQ26	Data [26]	1.2V POD	PIN_J33
DDR4A_DQ27	Data [27]	1.2V POD	PIN_D34

DDR4A_DQ28	Data [28]	1.2V POD	PIN_H30
DDR4A_DQ29	Data [29]	1.2V POD	PIN_J29
DDR4A_DQ30	Data [30]	1.2V POD	PIN_B33
DDR4A_DQ31	Data [31]	1.2V POD	PIN_H34
DDR4A_DQ32	Data [32]	1.2V POD	PIN_N35
DDR4A_DQ33	Data [33]	1.2V POD	PIN_L40
DDR4A_DQ34	Data [34]	1.2V POD	PIN_U39
DDR4A_DQ35	Data [35]	1.2V POD	PIN_W40
DDR4A_DQ36	Data [36]	1.2V POD	PIN_U35
DDR4A_DQ37	Data [37]	1.2V POD	PIN_W36
DDR4A_DQ38	Data [38]	1.2V POD	PIN_N39
DDR4A_DQ39	Data [39]	1.2V POD	PIN_L36
DDR4A_DQ40	Data [40]	1.2V POD	PIN_AA43
DDR4A_DQ41	Data [41]	1.2V POD	PIN_AA39
DDR4A_DQ42	Data [42]	1.2V POD	PIN_AK40
DDR4A_DQ43	Data [43]	1.2V POD	PIN_AK44
DDR4A_DQ44	Data [44]	1.2V POD	PIN_AD40
DDR4A_DQ45	Data [45]	1.2V POD	PIN_AN39
DDR4A_DQ46	Data [46]	1.2V POD	PIN_AN43
DDR4A_DQ47	Data [47]	1.2V POD	PIN_AD44
DDR4A_DQ48	Data [48]	1.2V POD	PIN_AV43
DDR4A_DQ49	Data [49]	1.2V POD	PIN_AT44
DDR4A_DQ50	Data [50]	1.2V POD	PIN_BC39
DDR4A_DQ51	Data [51]	1.2V POD	PIN_BC43
DDR4A_DQ52	Data [52]	1.2V POD	PIN_AV39
DDR4A_DQ53	Data [53]	1.2V POD	PIN_AT40
DDR4A_DQ54	Data [54]	1.2V POD	PIN_BF40
DDR4A_DQ55	Data [55]	1.2V POD	PIN_BF44
DDR4A_DQ56	Data [56]	1.2V POD	PIN_AD34
DDR4A_DQ57	Data [57]	1.2V POD	PIN_AA37
DDR4A_DQ58	Data [58]	1.2V POD	PIN_AN33
DDR4A_DQ59	Data [59]	1.2V POD	PIN_AK34
DDR4A_DQ60	Data [60]	1.2V POD	PIN_AD38
DDR4A_DQ61	Data [61]	1.2V POD	PIN_AN37

DDR4A_DQ62	Data [62]	1.2V POD	PIN_AA33
DDR4A_DQ63	Data [63]	1.2V POD	PIN_AK38
DDR4A_DQ64	Data [64]	1.2V POD	PIN_BF28
DDR4A_DQ65	Data [65]	1.2V POD	PIN_BF32
DDR4A_DQ66	Data [66]	1.2V POD	PIN_AT32
DDR4A_DQ67	Data [67]	1.2V POD	PIN_AT28
DDR4A_DQ68	Data [68]	1.2V POD	PIN_BC31
DDR4A_DQ69	Data [69]	1.2V POD	PIN_AV31
DDR4A_DQ70	Data [70]	1.2V POD	PIN_BC27
DDR4A_DQ71	Data [71]	1.2V POD	PIN_AV27
DDR4A_DBI_n0	Data Bus Inversion [0]	1.2V POD	PIN_U5
DDR4A_DBI_n1	Data Bus Inversion [1]	1.2V POD	PIN_J13
DDR4A_DBI_n2	Data Bus Inversion [2]	1.2V POD	PIN_J25
DDR4A_DBI_n3	Data Bus Inversion [3]	1.2V POD	PIN_J31
DDR4A_DBI_n4	Data Bus Inversion [4]	1.2V POD	PIN_U37
DDR4A_DBI_n5	Data Bus Inversion [5]	1.2V POD	PIN_AN41
DDR4A_DBI_n6	Data Bus Inversion [6]	1.2V POD	PIN_BC41
DDR4A_DBI_n7	Data Bus Inversion [7]	1.2V POD	PIN_AN35
DDR4A_DBI_n8	Data Bus Inversion [8]	1.2V POD	PIN_BC29
DDR4A_CS_n	Chip Select	SSTL-12	PIN_BC37
DDR4A_RESET_n	Chip Reset	1.2 V	PIN_AT38
DDR4A_ODT	On Die Termination	SSTL-12	PIN_AV35
DDR4A_PAR	Command and Address Parity Input	SSTL-12	PIN_BF34

DDR4A_ALERT_n	Register ALERT_n output	1.2 V	PIN_AA27
DDR4A_ACT_n	Activation Command Input	SSTL-12	PIN_BF38
DDR4A_EVENT_n	Chip Temperature Event	1.2 V	PIN_N41
DDR4A_RZQ	Calibrated pins for OCT block	1.2 V	PIN_AN31

Table 2-17 DDR4-B Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
DDR4B_REFCLK_p	DDR4B port Reference Clock p	True Differential Signaling	PIN_AG63
DDR4B_A0	Address [0]	SSTL-12	PIN_N59
DDR4B_A1	Address [1]	SSTL-12	PIN_L60
DDR4B_A2	Address [2]	SSTL-12	PIN_U59
DDR4B_A3	Address [3]	SSTL-12	PIN_W60
DDR4B_A4	Address [4]	SSTL-12	PIN_N61
DDR4B_A5	Address [5]	SSTL-12	PIN_L62
DDR4B_A6	Address [6]	SSTL-12	PIN_U61
DDR4B_A7	Address [7]	SSTL-12	PIN_W62
DDR4B_A8	Address [8]	SSTL-12	PIN_N63
DDR4B_A9	Address [9]	SSTL-12	PIN_L64
DDR4B_A10	Address [10]	SSTL-12	PIN_U63
DDR4B_A11	Address [11]	SSTL-12	PIN_W64
DDR4B_A12	Address [12]	SSTL-12	PIN_AT64
DDR4B_A13	Address [13]	SSTL-12	PIN_AG65
DDR4B_A14	Address [14]	SSTL-12	PIN_AK66
DDR4B_A15	Address [15]	SSTL-12	PIN_AV65
DDR4B_A16	Address [16]	SSTL-12	PIN_AT66
DDR4B_BA0	Bank Select [0]	SSTL-12	PIN_AK70
DDR4B_BA1	Bank Select [1]	SSTL-12	PIN_AV68

DDR4B_BG0	Bank Group Select [0]	SSTL-12	PIN_AT70
DDR4B_BG1	Bank Group Select [1]	SSTL-12	PIN_B59
DDR4B_CK[0]	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_B63
DDR4B_CK[1]	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_BJ68
DDR4B_CK_n[0]	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_D64
DDR4B_CK_n[1]	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_BM70
DDR4B_CKE[0]	Clock Enable pin	SSTL-12	PIN_J61
DDR4B_CKE[1]	Clock Enable pin	SSTL-12	PIN_H62
DDR4B_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2V POD	PIN_AV47
DDR4B_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2V POD	PIN_AA53
DDR4B_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2V POD	PIN_AV53
DDR4B_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2V POD	PIN_AA47
DDR4B_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2V POD	PIN_N55
DDR4B_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2V POD	PIN_AA59
DDR4B_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2V POD	PIN_BJ59
DDR4B_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2V POD	PIN_AV59
DDR4B_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2V POD	PIN_B55
DDR4B_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2V POD	PIN_AT48
DDR4B_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2V	PIN_AD54

		POD	
DDR4B_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2V POD	PIN_AT54
DDR4B_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2V POD	PIN_AD48
DDR4B_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2V POD	PIN_L56
DDR4B_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2V POD	PIN_AD60
DDR4B_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2V POD	PIN_BM60
DDR4B_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2V POD	PIN_AT60
DDR4B_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2V POD	PIN_D56
DDR4B_DQ0	Data [0]	1.2V POD	PIN_BF50
DDR4B_DQ1	Data [1]	1.2V POD	PIN_BC49
DDR4B_DQ2	Data [2]	1.2V POD	PIN_AV45
DDR4B_DQ3	Data [3]	1.2V POD	PIN_AT46
DDR4B_DQ4	Data [4]	1.2V POD	PIN_AT50
DDR4B_DQ5	Data [5]	1.2V POD	PIN_AV49
DDR4B_DQ6	Data [6]	1.2V POD	PIN_BC45
DDR4B_DQ7	Data [7]	1.2V POD	PIN_BF46
DDR4B_DQ8	Data [8]	1.2V POD	PIN_AA51
DDR4B_DQ9	Data [9]	1.2V POD	PIN_AK52
DDR4B_DQ10	Data [10]	1.2V POD	PIN_AK56
DDR4B_DQ11	Data [11]	1.2V POD	PIN_AD56
DDR4B_DQ12	Data [12]	1.2V POD	PIN_AN51
DDR4B_DQ13	Data [13]	1.2V POD	PIN_AN55
DDR4B_DQ14	Data [14]	1.2V POD	PIN_AA55
DDR4B_DQ15	Data [15]	1.2V POD	PIN_AD52
DDR4B_DQ16	Data [16]	1.2V POD	PIN_BC51
DDR4B_DQ17	Data [17]	1.2V POD	PIN_AV51
DDR4B_DQ18	Data [18]	1.2V POD	PIN_AT56

DDR4B_DQ19	Data [19]	1.2V POD	PIN_AV55
DDR4B_DQ20	Data [20]	1.2V POD	PIN_BC55
DDR4B_DQ21	Data [21]	1.2V POD	PIN_BF52
DDR4B_DQ22	Data [22]	1.2V POD	PIN_BF56
DDR4B_DQ23	Data [23]	1.2V POD	PIN_AT52
DDR4B_DQ24	Data [24]	1.2V POD	PIN_AK50
DDR4B_DQ25	Data [25]	1.2V POD	PIN_AK46
DDR4B_DQ26	Data [26]	1.2V POD	PIN_AA45
DDR4B_DQ27	Data [27]	1.2V POD	PIN_AA49
DDR4B_DQ28	Data [28]	1.2V POD	PIN_AD46
DDR4B_DQ29	Data [29]	1.2V POD	PIN_AN45
DDR4B_DQ30	Data [30]	1.2V POD	PIN_AN49
DDR4B_DQ31	Data [31]	1.2V POD	PIN_AD50
DDR4B_DQ32	Data [32]	1.2V POD	PIN_N53
DDR4B_DQ33	Data [33]	1.2V POD	PIN_L54
DDR4B_DQ34	Data [34]	1.2V POD	PIN_U57
DDR4B_DQ35	Data [35]	1.2V POD	PIN_W58
DDR4B_DQ36	Data [36]	1.2V POD	PIN_U53
DDR4B_DQ37	Data [37]	1.2V POD	PIN_W54
DDR4B_DQ38	Data [38]	1.2V POD	PIN_N57
DDR4B_DQ39	Data [39]	1.2V POD	PIN_L58
DDR4B_DQ40	Data [40]	1.2V POD	PIN_AK58
DDR4B_DQ41	Data [41]	1.2V POD	PIN_AA57
DDR4B_DQ42	Data [42]	1.2V POD	PIN_AN61
DDR4B_DQ43	Data [43]	1.2V POD	PIN_AN57
DDR4B_DQ44	Data [44]	1.2V POD	PIN_AA61
DDR4B_DQ45	Data [45]	1.2V POD	PIN_AD58
DDR4B_DQ46	Data [46]	1.2V POD	PIN_AD62
DDR4B_DQ47	Data [47]	1.2V POD	PIN_AK62
DDR4B_DQ48	Data [48]	1.2V POD	PIN_BV62
DDR4B_DQ49	Data [49]	1.2V POD	PIN_CA61
DDR4B_DQ50	Data [50]	1.2V POD	PIN_CA57
DDR4B_DQ51	Data [51]	1.2V POD	PIN_BV58
DDR4B_DQ52	Data [52]	1.2V POD	PIN_BM62

DDR4B_DQ53	Data [53]	1.2V POD	PIN_BJ61
DDR4B_DQ54	Data [54]	1.2V POD	PIN_BJ57
DDR4B_DQ55	Data [55]	1.2V POD	PIN_BM58
DDR4B_DQ56	Data [56]	1.2V POD	PIN_BC61
DDR4B_DQ57	Data [57]	1.2V POD	PIN_AV61
DDR4B_DQ58	Data [58]	1.2V POD	PIN_BF58
DDR4B_DQ59	Data [59]	1.2V POD	PIN_AV57
DDR4B_DQ60	Data [60]	1.2V POD	PIN_BF62
DDR4B_DQ61	Data [61]	1.2V POD	PIN_AT62
DDR4B_DQ62	Data [62]	1.2V POD	PIN_BC57
DDR4B_DQ63	Data [63]	1.2V POD	PIN_AT58
DDR4B_DQ64	Data [64]	1.2V POD	PIN_B57
DDR4B_DQ65	Data [65]	1.2V POD	PIN_B53
DDR4B_DQ66	Data [66]	1.2V POD	PIN_D54
DDR4B_DQ67	Data [67]	1.2V POD	PIN_J57
DDR4B_DQ68	Data [68]	1.2V POD	PIN_H54
DDR4B_DQ69	Data [69]	1.2V POD	PIN_J53
DDR4B_DQ70	Data [70]	1.2V POD	PIN_H58
DDR4B_DQ71	Data [71]	1.2V POD	PIN_D58
DDR4B_DBI_n0	Data Bus Inversion [0]	1.2V POD	PIN_BC47
DDR4B_DBI_n1	Data Bus Inversion [1]	1.2V POD	PIN_AN53
DDR4B_DBI_n2	Data Bus Inversion [2]	1.2V POD	PIN_BC53
DDR4B_DBI_n3	Data Bus Inversion [3]	1.2V POD	PIN_AN47
DDR4B_DBI_n4	Data Bus Inversion [4]	1.2V POD	PIN_U55
DDR4B_DBI_n5	Data Bus Inversion [5]	1.2V POD	PIN_AN59
DDR4B_DBI_n6	Data Bus Inversion [6]	1.2V POD	PIN_CA59
DDR4B_DBI_n7	Data Bus Inversion	1.2V POD	PIN_BC59

	[7]		
DDR4B_DBI_n8	Data Bus Inversion [8]	1.2V POD	PIN_J55
DDR4B_CS_n[0]	Chip Select	SSTL-12	PIN_J59
DDR4B_CS_n[1]	Chip Select	SSTL-12	PIN_J63
DDR4B_RESET_n	Chip Reset	1.2 V	PIN_D60
DDR4B_ODT[0]	On Die Termination	SSTL-12	PIN_B61
DDR4B_ODT[1]	On Die Termination	SSTL-12	PIN_D62
DDR4B_PAR	Command and Address Parity Input	SSTL-12	PIN_H64
DDR4B_ALERT_n	Register ALERT_n output	1.2 V	PIN_AG68
DDR4B_ACT_n	Activation Command Input	SSTL-12	PIN_H60
DDR4B_EVENT_n	Chip Temperature Event	1.2 V	PIN_H52
DDR4B_C[0]	Chip ID	SSTL-12	PIN_BC63
DDR4B_C[1]	Chip ID	SSTL-12	PIN_AY64
DDR4B_RZQ	Calibrated pins for OCT block	1.2 V	PIN_AV63

Table 2-18 DDR4-C Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
DDR4C_REFCLK_p	DDR4C port Reference Clock p	True Differential Signaling	PIN_KU36
DDR4C_A0	Address [0]	SSTL-12	PIN_LH42
DDR4C_A1	Address [1]	SSTL-12	PIN_LL43
DDR4C_A2	Address [2]	SSTL-12	PIN_KW43
DDR4C_A3	Address [3]	SSTL-12	PIN_LB42
DDR4C_A4	Address [4]	SSTL-12	PIN_LH40

DDR4C_A5	Address [5]	SSTL-12	PIN_LL41
DDR4C_A6	Address [6]	SSTL-12	PIN_LB40
DDR4C_A7	Address [7]	SSTL-12	PIN_KW41
DDR4C_A8	Address [8]	SSTL-12	PIN_LH38
DDR4C_A9	Address [9]	SSTL-12	PIN_LL39
DDR4C_A10	Address [10]	SSTL-12	PIN_KW39
DDR4C_A11	Address [11]	SSTL-12	PIN_LB38
DDR4C_A12	Address [12]	SSTL-12	PIN_KF36
DDR4C_A13	Address [13]	SSTL-12	PIN_KU34
DDR4C_A14	Address [14]	SSTL-12	PIN_KR35
DDR4C_A15	Address [15]	SSTL-12	PIN_KF34
DDR4C_A16	Address [16]	SSTL-12	PIN_KJ35
DDR4C_BA0	Bank Select [0]	SSTL-12	PIN_KR33
DDR4C_BA1	Bank Select [1]	SSTL-12	PIN_KJ33
DDR4C_BG0	Bank Group Select [0]	SSTL-12	PIN_KF32
DDR4C_BG1	Bank Group Select [1]	SSTL-12	PIN_KR43
DDR4C_CK[0]	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_KR39
DDR4C_CK[1]	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_JP32
DDR4C_CK_n[0]	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_KU38
DDR4C_CK_n[1]	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_JL33
DDR4C_CKE[0]	Clock Enable pin	SSTL-12	PIN_KF40
DDR4C_CKE[1]	Clock Enable pin	SSTL-12	PIN_KJ41
DDR4C_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2V POD	PIN_LH34
DDR4C_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2V POD	PIN_MH30
DDR4C_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2V POD	PIN_MH11

DDR4C_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2V POD	PIN_LW17
DDR4C_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2V POD	PIN_LW33
DDR4C_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2V POD	PIN_MH23
DDR4C_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2V POD	PIN_LW5
DDR4C_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2V POD	PIN_LW27
DDR4C_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2V POD	PIN_LH28
DDR4C_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2V POD	PIN_LL35
DDR4C_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2V POD	PIN_MK31
DDR4C_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2V POD	PIN_MK13
DDR4C_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2V POD	PIN_MA19
DDR4C_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2V POD	PIN_MA34
DDR4C_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2V POD	PIN_MK25
DDR4C_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2V POD	PIN_MA7
DDR4C_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2V POD	PIN_MA28
DDR4C_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2V POD	PIN_LL29
DDR4C_DQ0	Data [0]	1.2V POD	PIN_LB32
DDR4C_DQ1	Data [1]	1.2V POD	PIN_LB36
DDR4C_DQ2	Data [2]	1.2V POD	PIN_LL33
DDR4C_DQ3	Data [3]	1.2V POD	PIN_LH32
DDR4C_DQ4	Data [4]	1.2V POD	PIN_KW33

DDR4C_DQ5	Data [5]	1.2V POD	PIN_KW37
DDR4C_DQ6	Data [6]	1.2V POD	PIN_LL37
DDR4C_DQ7	Data [7]	1.2V POD	PIN_LH36
DDR4C_DQ8	Data [8]	1.2V POD	PIN_MK29
DDR4C_DQ9	Data [9]	1.2V POD	PIN_MD32
DDR4C_DQ10	Data [10]	1.2V POD	PIN_MC33
DDR4C_DQ11	Data [11]	1.2V POD	PIN_MD28
DDR4C_DQ12	Data [12]	1.2V POD	PIN_MC29
DDR4C_DQ13	Data [13]	1.2V POD	PIN_MK33
DDR4C_DQ14	Data [14]	1.2V POD	PIN_MH28
DDR4C_DQ15	Data [15]	1.2V POD	PIN_MH32
DDR4C_DQ16	Data [16]	1.2V POD	PIN_MD7
DDR4C_DQ17	Data [17]	1.2V POD	PIN_MC17
DDR4C_DQ18	Data [18]	1.2V POD	PIN_MC9
DDR4C_DQ19	Data [19]	1.2V POD	PIN_MD15
DDR4C_DQ20	Data [20]	1.2V POD	PIN_MF5
DDR4C_DQ21	Data [21]	1.2V POD	PIN_MH15
DDR4C_DQ22	Data [22]	1.2V POD	PIN_MH7
DDR4C_DQ23	Data [23]	1.2V POD	PIN_MK17
DDR4C_DQ24	Data [24]	1.2V POD	PIN_MA15
DDR4C_DQ25	Data [25]	1.2V POD	PIN_MA23
DDR4C_DQ26	Data [26]	1.2V POD	PIN_LN15
DDR4C_DQ27	Data [27]	1.2V POD	PIN_LR21
DDR4C_DQ28	Data [28]	1.2V POD	PIN_LR13
DDR4C_DQ29	Data [29]	1.2V POD	PIN_LW13
DDR4C_DQ30	Data [30]	1.2V POD	PIN_LN23
DDR4C_DQ31	Data [31]	1.2V POD	PIN_LW21
DDR4C_DQ32	Data [32]	1.2V POD	PIN_MA36
DDR4C_DQ33	Data [33]	1.2V POD	PIN_LW35
DDR4C_DQ34	Data [34]	1.2V POD	PIN_LW31
DDR4C_DQ35	Data [35]	1.2V POD	PIN_LR31
DDR4C_DQ36	Data [36]	1.2V POD	PIN_LR35
DDR4C_DQ37	Data [37]	1.2V POD	PIN_LN36
DDR4C_DQ38	Data [38]	1.2V POD	PIN_MA32

DDR4C_DQ39	Data [39]	1.2V POD	PIN_LN32
DDR4C_DQ40	Data [40]	1.2V POD	PIN_MK21
DDR4C_DQ41	Data [41]	1.2V POD	PIN_MD26
DDR4C_DQ42	Data [42]	1.2V POD	PIN_MH19
DDR4C_DQ43	Data [43]	1.2V POD	PIN_MC21
DDR4C_DQ44	Data [44]	1.2V POD	PIN_MC27
DDR4C_DQ45	Data [45]	1.2V POD	PIN_MK27
DDR4C_DQ46	Data [46]	1.2V POD	PIN_MD19
DDR4C_DQ47	Data [47]	1.2V POD	PIN_MH26
DDR4C_DQ48	Data [48]	1.2V POD	PIN_LR9
DDR4C_DQ49	Data [49]	1.2V POD	PIN_LW9
DDR4C_DQ50	Data [50]	1.2V POD	PIN_MA4
DDR4C_DQ51	Data [51]	1.2V POD	PIN_LW2
DDR4C_DQ52	Data [52]	1.2V POD	PIN_MA11
DDR4C_DQ53	Data [53]	1.2V POD	PIN_LN11
DDR4C_DQ54	Data [54]	1.2V POD	PIN_MC5
DDR4C_DQ55	Data [55]	1.2V POD	PIN_LU4
DDR4C_DQ56	Data [56]	1.2V POD	PIN_LN26
DDR4C_DQ57	Data [57]	1.2V POD	PIN_MA26
DDR4C_DQ58	Data [58]	1.2V POD	PIN_LR29
DDR4C_DQ59	Data [59]	1.2V POD	PIN_LN30
DDR4C_DQ60	Data [60]	1.2V POD	PIN_LW25
DDR4C_DQ61	Data [61]	1.2V POD	PIN_LR25
DDR4C_DQ62	Data [62]	1.2V POD	PIN_LW29
DDR4C_DQ63	Data [63]	1.2V POD	PIN_MA30
DDR4C_DQ64	Data [64]	1.2V POD	PIN_KW27
DDR4C_DQ65	Data [65]	1.2V POD	PIN_LH30
DDR4C_DQ66	Data [66]	1.2V POD	PIN_LL31
DDR4C_DQ67	Data [67]	1.2V POD	PIN_LH26
DDR4C_DQ68	Data [68]	1.2V POD	PIN_LB26
DDR4C_DQ69	Data [69]	1.2V POD	PIN_LL27
DDR4C_DQ70	Data [70]	1.2V POD	PIN_LB30
DDR4C_DQ71	Data [71]	1.2V POD	PIN_KW31
DDR4C_DBI_n0	Data Bus Inversion	1.2V POD	PIN_LB34

	[0]		
DDR4C_DBI_n1	Data Bus Inversion [1]	1.2V POD	PIN_MD30
DDR4C_DBI_n2	Data Bus Inversion [2]	1.2V POD	PIN_MD11
DDR4C_DBI_n3	Data Bus Inversion [3]	1.2V POD	PIN_LR17
DDR4C_DBI_n4	Data Bus Inversion [4]	1.2V POD	PIN_LR33
DDR4C_DBI_n5	Data Bus Inversion [5]	1.2V POD	PIN_MD23
DDR4C_DBI_n6	Data Bus Inversion [6]	1.2V POD	PIN_LR5
DDR4C_DBI_n7	Data Bus Inversion [7]	1.2V POD	PIN_LR27
DDR4C_DBI_n8	Data Bus Inversion [8]	1.2V POD	PIN_LB28
DDR4C_CS_n[0]	Chip Select	SSTL-12	PIN_KF42
DDR4C_CS_n[1]	Chip Select	SSTL-12	PIN_KF38
DDR4C_RESET_n	Chip Reset	1.2 V	PIN_KU42
DDR4C_ODT[0]	On Die Termination	SSTL-12	PIN_KU40
DDR4C_ODT[1]	On Die Termination	SSTL-12	PIN_KR41
DDR4C_PAR	Command and Address Parity Input	SSTL-12	PIN_KJ39
DDR4C_ALERT_n	Register ALERT_n output	1.2 V	PIN_KU32
DDR4C_ACT_n	Activation Command Input	SSTL-12	PIN_KJ43
DDR4C_EVENT_n	Chip Temperature Event	1.2 V	PIN_JY26
DDR4C_C[0]	Chip ID	SSTL-12	PIN_KC37
DDR4C_C[1]	Chip ID	SSTL-12	PIN_JY36

DDR4C_RZQ	Calibrated pins for OCT block	1.2 V	PIN_KJ37

Table 2-19 DDR4-D Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
DDR4D_REFCLK_p	DDR4D port Reference Clock p	True Differential Signaling	PIN_MA44
DDR4D_A0	Address [0]	SSTL-12	PIN_KR45
DDR4D_A1	Address [1]	SSTL-12	PIN_KU44
DDR4D_A2	Address [2]	SSTL-12	PIN_KJ45
DDR4D_A3	Address [3]	SSTL-12	PIN_KF44
DDR4D_A4	Address [4]	SSTL-12	PIN_KU46
DDR4D_A5	Address [5]	SSTL-12	PIN_KR47
DDR4D_A6	Address [6]	SSTL-12	PIN_KF46
DDR4D_A7	Address [7]	SSTL-12	PIN_KJ47
DDR4D_A8	Address [8]	SSTL-12	PIN_KR49
DDR4D_A9	Address [9]	SSTL-12	PIN_KU48
DDR4D_A10	Address [10]	SSTL-12	PIN_KF48
DDR4D_A11	Address [11]	SSTL-12	PIN_KJ49
DDR4D_A12	Address [12]	SSTL-12	PIN_LR43
DDR4D_A13	Address [13]	SSTL-12	PIN_LW45
DDR4D_A14	Address [14]	SSTL-12	PIN_MA46
DDR4D_A15	Address [15]	SSTL-12	PIN_LR45
DDR4D_A16	Address [16]	SSTL-12	PIN_LN46
DDR4D_BA0	Bank Select [0]	SSTL-12	PIN_LW47
DDR4D_BA1	Bank Select [1]	SSTL-12	PIN_LN48
DDR4D_BG0	Bank Group Select [0]	SSTL-12	PIN_LR47
DDR4D_BG1	Bank Group Select [1]	SSTL-12	PIN_LH44
DDR4D_CK[0]	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_LH48

DDR4D_CK[1]	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_LR53
DDR4D_CK_n[0]	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_LL49
DDR4D_CK_n[1]	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_LN54
DDR4D_CKE[0]	Clock Enable pin	SSTL-12	PIN_LB46
DDR4D_CKE[1]	Clock Enable pin	SSTL-12	PIN_KW47
DDR4D_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2V POD	PIN_LH52
DDR4D_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2V POD	PIN_MH60
DDR4D_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2V POD	PIN_MH54
DDR4D_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2V POD	PIN_LW57
DDR4D_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2V POD	PIN_MH48
DDR4D_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2V POD	PIN_MH36
DDR4D_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2V POD	PIN_MH42
DDR4D_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2V POD	PIN_LW39
DDR4D_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2V POD	PIN_KU52
DDR4D_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2V POD	PIN_LL53
DDR4D_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2V POD	PIN_MK61
DDR4D_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2V POD	PIN_MK55
DDR4D_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2V POD	PIN_MA58
DDR4D_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2V	PIN_MK49

		POD	
DDR4D_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2V POD	PIN_MK37
DDR4D_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2V POD	PIN_MK43
DDR4D_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2V POD	PIN_MA40
DDR4D_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2V POD	PIN_KR53
DDR4D_DQ0	Data [0]	1.2V POD	PIN_LL55
DDR4D_DQ1	Data [1]	1.2V POD	PIN_LB54
DDR4D_DQ2	Data [2]	1.2V POD	PIN_LH50
DDR4D_DQ3	Data [3]	1.2V POD	PIN_LH54
DDR4D_DQ4	Data [4]	1.2V POD	PIN_KW51
DDR4D_DQ5	Data [5]	1.2V POD	PIN_LB50
DDR4D_DQ6	Data [6]	1.2V POD	PIN_LL51
DDR4D_DQ7	Data [7]	1.2V POD	PIN_KW55
DDR4D_DQ8	Data [8]	1.2V POD	PIN_MC63
DDR4D_DQ9	Data [9]	1.2V POD	PIN_MH62
DDR4D_DQ10	Data [10]	1.2V POD	PIN_MK59
DDR4D_DQ11	Data [11]	1.2V POD	PIN_MH58
DDR4D_DQ12	Data [12]	1.2V POD	PIN_MD62
DDR4D_DQ13	Data [13]	1.2V POD	PIN_MC59
DDR4D_DQ14	Data [14]	1.2V POD	PIN_MK63
DDR4D_DQ15	Data [15]	1.2V POD	PIN_MD58
DDR4D_DQ16	Data [16]	1.2V POD	PIN_MD56
DDR4D_DQ17	Data [17]	1.2V POD	PIN_MK57
DDR4D_DQ18	Data [18]	1.2V POD	PIN_MH52
DDR4D_DQ19	Data [19]	1.2V POD	PIN_MD52
DDR4D_DQ20	Data [20]	1.2V POD	PIN_MC57
DDR4D_DQ21	Data [21]	1.2V POD	PIN_MC53
DDR4D_DQ22	Data [22]	1.2V POD	PIN_MK53
DDR4D_DQ23	Data [23]	1.2V POD	PIN_MH56
DDR4D_DQ24	Data [24]	1.2V POD	PIN_LN60

DDR4D_DQ25	Data [25]	1.2V POD	PIN_MA60
DDR4D_DQ26	Data [26]	1.2V POD	PIN_LR55
DDR4D_DQ27	Data [27]	1.2V POD	PIN_LW55
DDR4D_DQ28	Data [28]	1.2V POD	PIN_LN56
DDR4D_DQ29	Data [29]	1.2V POD	PIN_LW59
DDR4D_DQ30	Data [30]	1.2V POD	PIN_MA56
DDR4D_DQ31	Data [31]	1.2V POD	PIN_LR59
DDR4D_DQ32	Data [32]	1.2V POD	PIN_MK51
DDR4D_DQ33	Data [33]	1.2V POD	PIN_MC47
DDR4D_DQ34	Data [34]	1.2V POD	PIN_MD46
DDR4D_DQ35	Data [35]	1.2V POD	PIN_MK47
DDR4D_DQ36	Data [36]	1.2V POD	PIN_MC51
DDR4D_DQ37	Data [37]	1.2V POD	PIN_MH50
DDR4D_DQ38	Data [38]	1.2V POD	PIN_MH46
DDR4D_DQ39	Data [39]	1.2V POD	PIN_MD50
DDR4D_DQ40	Data [40]	1.2V POD	PIN_MH34
DDR4D_DQ41	Data [41]	1.2V POD	PIN_MK39
DDR4D_DQ42	Data [42]	1.2V POD	PIN_MC35
DDR4D_DQ43	Data [43]	1.2V POD	PIN_MD38
DDR4D_DQ44	Data [44]	1.2V POD	PIN_MK35
DDR4D_DQ45	Data [45]	1.2V POD	PIN_MC39
DDR4D_DQ46	Data [46]	1.2V POD	PIN_MD34
DDR4D_DQ47	Data [47]	1.2V POD	PIN_MH38
DDR4D_DQ48	Data [48]	1.2V POD	PIN_MC45
DDR4D_DQ49	Data [49]	1.2V POD	PIN_MK41
DDR4D_DQ50	Data [50]	1.2V POD	PIN_MH40
DDR4D_DQ51	Data [51]	1.2V POD	PIN_MD40
DDR4D_DQ52	Data [52]	1.2V POD	PIN_MH44
DDR4D_DQ53	Data [53]	1.2V POD	PIN_MK45
DDR4D_DQ54	Data [54]	1.2V POD	PIN_MD44
DDR4D_DQ55	Data [55]	1.2V POD	PIN_MC41
DDR4D_DQ56	Data [56]	1.2V POD	PIN_LR37
DDR4D_DQ57	Data [57]	1.2V POD	PIN_LN42
DDR4D_DQ58	Data [58]	1.2V POD	PIN_LN38

DDR4D_DQ59	Data [59]	1.2V POD	PIN_LR41
DDR4D_DQ60	Data [60]	1.2V POD	PIN_LW37
DDR4D_DQ61	Data [61]	1.2V POD	PIN_MA38
DDR4D_DQ62	Data [62]	1.2V POD	PIN_LW41
DDR4D_DQ63	Data [63]	1.2V POD	PIN_MA42
DDR4D_DQ64	Data [64]	1.2V POD	PIN_KR55
DDR4D_DQ65	Data [65]	1.2V POD	PIN_KU54
DDR4D_DQ66	Data [66]	1.2V POD	PIN_KJ51
DDR4D_DQ67	Data [67]	1.2V POD	PIN_KF50
DDR4D_DQ68	Data [68]	1.2V POD	PIN_KJ55
DDR4D_DQ69	Data [69]	1.2V POD	PIN_KF54
DDR4D_DQ70	Data [70]	1.2V POD	PIN_KU50
DDR4D_DQ71	Data [71]	1.2V POD	PIN_KR51
DDR4D_DBI_n0	Data Bus Inversion [0]	1.2V POD	PIN_LB52
DDR4D_DBI_n1	Data Bus Inversion [1]	1.2V POD	PIN_MD60
DDR4D_DBI_n2	Data Bus Inversion [2]	1.2V POD	PIN_MD54
DDR4D_DBI_n3	Data Bus Inversion [3]	1.2V POD	PIN_LR57
DDR4D_DBI_n4	Data Bus Inversion [4]	1.2V POD	PIN_MD48
DDR4D_DBI_n5	Data Bus Inversion [5]	1.2V POD	PIN_MD36
DDR4D_DBI_n6	Data Bus Inversion [6]	1.2V POD	PIN_MD42
DDR4D_DBI_n7	Data Bus Inversion [7]	1.2V POD	PIN_LR39
DDR4D_DBI_n8	Data Bus Inversion [8]	1.2V POD	PIN_KF52
DDR4D_CS_n[0]	Chip Select	SSTL-12	PIN_LB44
DDR4D_CS_n[1]	Chip Select	SSTL-12	PIN_KW49
DDR4D_RESET_n	Chip Reset	1.2 V	PIN_LL45

DDR4D_ODT[0]	On Die Termination	SSTL-12	PIN_LH46
DDR4D_ODT[1]	On Die Termination	SSTL-12	PIN_LL47
DDR4D_PAR	Command and Address Parity Input	SSTL-12	PIN_LB48
DDR4D_ALERT_n	Register ALERT_n output	1.2 V	PIN_MA48
DDR4D_ACT_n	Activation Command Input	SSTL-12	PIN_KW45
DDR4D_EVENT_n	Chip Temperature Event	1.2 V	PIN_KJ61
DDR4D_C[0]	Chip ID	SSTL-12	PIN_MA50
DDR4D_C[1]	Chip ID	SSTL-12	PIN_LW49
DDR4D_RZQ	Calibrated pins for OCT block	1.2 V	PIN_LN44

2.8 QSPF-DD Ports

The board can support two standard QSFP-DD (Quad Small Form Factor Pluggable Double Density) optical modules. The QSFP-DD ports on the board will be able to support **8** pairs of **25 Gb/s NRZ** modulation or **4** pairs of **50 Gb/s PAM4** modulation with FPGA's high speed transceivers to achieve 200 Gbps bandwidth. Furthermore, the QSFP-DD modules also can backward compatible with QSFP28 and QSFP+ optical transceivers. **Figure 2-23** shows the connections between the QSFP-DD and Agilex FPGA.

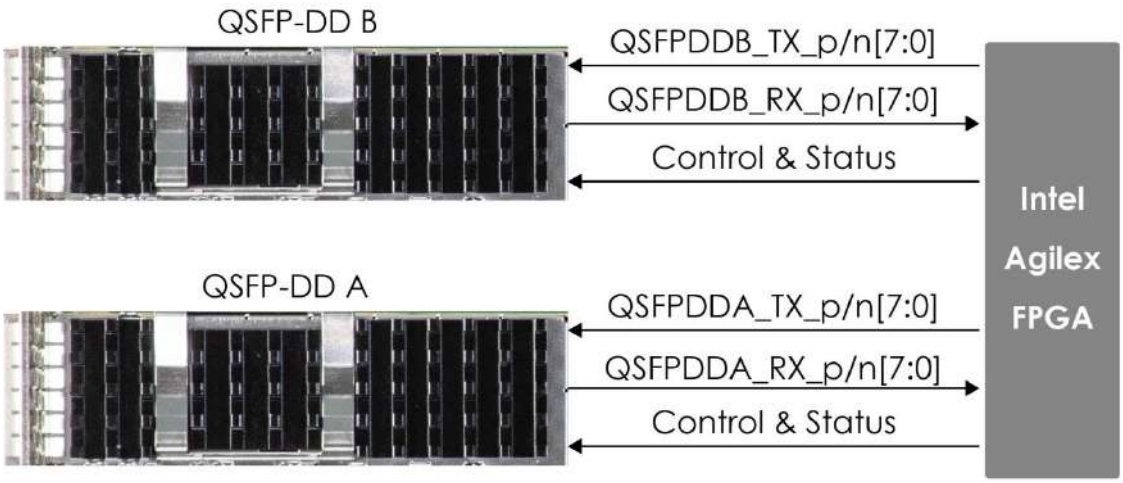


Figure 2-23 Connection between the QSFP28 and Agilex FPGA

Table 2-20, and **Table 2-21** list the QSFP-DD port A and B pin assignments and signal names relative to the Agilex device.

Table 2-20 QSFP-DD Port A Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
QSFPDDA_TX_p0	Transmitter non-inverted data of channel 0	High Speed Differential I/O	PIN_MB71
QSFPDDA_TX_p1	Transmitter non-inverted data of channel 1	High Speed Differential I/O	PIN_MJ74
QSFPDDA_TX_p2	Transmitter non-inverted data of channel 2	High Speed Differential I/O	PIN_LY74
QSFPDDA_TX_p3	Transmitter non-inverted data of channel 3	High Speed Differential I/O	PIN_LM74
QSFPDDA_TX_p4	Transmitter non-inverted data of channel 4	High Speed Differential I/O	PIN_LD77
QSFPDDA_TX_p5	Transmitter non-inverted data of channel 5	High Speed Differential I/O	PIN_LA74
QSFPDDA_TX_p6	Transmitter non-inverted data of channel 6	High Speed Differential I/O	PIN_KL77
QSFPDDA_TX_p7	Transmitter non-inverted data of channel 7	High Speed Differential I/O	PIN_KH74

QSFPDDA_TX_n0	Transmitter inverted data of channel 0	High Speed Differential I/O	PIN_ME69
QSFPDDA_TX_n1	Transmitter inverted data of channel 1	High Speed Differential I/O	PIN_MG73
QSFPDDA_TX_n2	Transmitter inverted data of channel 2	High Speed Differential I/O	PIN_LV73
QSFPDDA_TX_n3	Transmitter inverted data of channel 3	High Speed Differential I/O	PIN_LK73
QSFPDDA_TX_n4	Transmitter inverted data of channel 4	High Speed Differential I/O	PIN_LG76
QSFPDDA_TX_n5	Transmitter inverted data of channel 5	High Speed Differential I/O	PIN_KV73
QSFPDDA_TX_n6	Transmitter inverted data of channel 6	High Speed Differential I/O	PIN_KP76
QSFPDDA_TX_n7	Transmitter inverted data of channel 7	High Speed Differential I/O	PIN_KE73
QSFPDDA_RX_p0	Receiver non-inverted data of channel 0	High Speed Differential I/O	PIN_MB77
QSFPDDA_RX_p1	Receiver non-inverted data of channel 1	High Speed Differential I/O	PIN_LP77
QSFPDDA_RX_p2	Receiver non-inverted data of channel 2	High Speed Differential I/O	PIN_LY80
QSFPDDA_RX_p3	Receiver non-inverted data of channel 3	High Speed Differential I/O	PIN_LP83
QSFPDDA_RX_p4	Receiver non-inverted data of channel 4	High Speed Differential I/O	PIN_LM80
QSFPDDA_RX_p5	Receiver non-inverted data of channel 5	High Speed Differential I/O	PIN_LD83
QSFPDDA_RX_p6	Receiver non-inverted data of channel 6	High Speed Differential I/O	PIN_LA80
QSFPDDA_RX_p7	Receiver non-inverted data of channel 7	High Speed Differential I/O	PIN_KL83
QSFPDDA_RX_n0	Receiver inverted data of channel 0	High Speed Differential I/O	PIN_ME76
QSFPDDA_RX_n1	Receiver inverted data of	High Speed	PIN_LT76

	channel 1	Differential I/O	
QSFPDDA_RX_n2	Receiver inverted data of channel 2	High Speed Differential I/O	PIN_LV79
QSFPDDA_RX_n3	Receiver inverted data of channel 3	High Speed Differential I/O	PIN_LT82
QSFPDDA_RX_n4	Receiver inverted data of channel 4	High Speed Differential I/O	PIN_LK79
QSFPDDA_RX_n5	Receiver inverted data of channel 5	High Speed Differential I/O	PIN_LG82
QSFPDDA_RX_n6	Receiver inverted data of channel 6	High Speed Differential I/O	PIN_KV79
QSFPDDA_RX_n7	Receiver inverted data of channel 7	High Speed Differential I/O	PIN_KP82
QSFPDDA_REFCLK_p	QSFP-DD port A transceiver reference clock p	LVDS	PIN_HJ68
QSFPDDA_INITMODE	Initialization mode	1.2V	PIN_KR59
QSFPDDA_INTERRUPT_n	Interrupt	1.2V	PIN_KJ59
QSFPDDA_MOD_PRS_n	Module Present	1.2V	PIN_KF56
QSFPDDA_MOD_SEL_n	Module Select	1.2V	PIN_LH58
QSFPDDA_RST_n	Module Reset	1.2V	PIN_KU60
QSFPDDA_SCL	2-wire serial interface clock	1.2V	PIN_KR61
QSFPDDA_SDA	2-wire serial interface data	1.2V	PIN_KU58

Table 2-21 QSFP-DD Port B Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
QSFPDDB_TX_p0	Transmitter non-inverted data of channel 0	High Speed Differential I/O	PIN_JW77
QSFPDDB_TX_p1	Transmitter non-inverted data of channel 1	High Speed Differential I/O	PIN_JT74

QSFPDDB_TX_p2	Transmitter non-inverted data of channel 2	High Speed Differential I/O	PIN_JG77
QSFPDDB_TX_p3	Transmitter non-inverted data of channel 3	High Speed Differential I/O	PIN_HP77
QSFPDDB_TX_p4	Transmitter non-inverted data of channel 4	High Speed Differential I/O	PIN_HL80
QSFPDDB_TX_p5	Transmitter non-inverted data of channel 5	High Speed Differential I/O	PIN_HB77
QSFPDDB_TX_p6	Transmitter non-inverted data of channel 6	High Speed Differential I/O	PIN_GW80
QSFPDDB_TX_p7	Transmitter non-inverted data of channel 7	High Speed Differential I/O	PIN_GG78
QSFPDDB_TX_n0	Transmitter inverted data of channel 0	High Speed Differential I/O	PIN_KB76
QSFPDDB_TX_n1	Transmitter inverted data of channel 1	High Speed Differential I/O	PIN_JN73
QSFPDDB_TX_n2	Transmitter inverted data of channel 2	High Speed Differential I/O	PIN_JK76
QSFPDDB_TX_n3	Transmitter inverted data of channel 3	High Speed Differential I/O	PIN_HU76
QSFPDDB_TX_n4	Transmitter inverted data of channel 4	High Speed Differential I/O	PIN_HH79
QSFPDDB_TX_n5	Transmitter inverted data of channel 5	High Speed Differential I/O	PIN_HE76
QSFPDDB_TX_n6	Transmitter inverted data of channel 6	High Speed Differential I/O	PIN_GT79
QSFPDDB_TX_n7	Transmitter inverted data of channel 7	High Speed Differential I/O	PIN_GK77
QSFPDDB_RX_p0	Receiver non-inverted data of channel 0	High Speed Differential I/O	PIN_KH80
QSFPDDB_RX_p1	Receiver non-inverted data of channel 1	High Speed Differential I/O	PIN_JW83
QSFPDDB_RX_p2	Receiver non-inverted data of channel 2	High Speed Differential I/O	PIN_JT80
QSFPDDB_RX_p3	Receiver non-inverted data	High Speed	PIN_JG83

	of channel 3	Differential I/O	
QSFPDDB_RX_p4	Receiver non-inverted data of channel 4	High Speed Differential I/O	PIN_JD80
QSFPDDB_RX_p5	Receiver non-inverted data of channel 5	High Speed Differential I/O	PIN_HP83
QSFPDDB_RX_p6	Receiver non-inverted data of channel 6	High Speed Differential I/O	PIN_HB83
QSFPDDB_RX_p7	Receiver non-inverted data of channel 7	High Speed Differential I/O	PIN_GK83
QSFPDDB_RX_n0	Receiver inverted data of channel 0	High Speed Differential I/O	PIN_KE79
QSFPDDB_RX_n1	Receiver inverted data of channel 1	High Speed Differential I/O	PIN_KB82
QSFPDDB_RX_n2	Receiver inverted data of channel 2	High Speed Differential I/O	PIN_JN79
QSFPDDB_RX_n3	Receiver inverted data of channel 3	High Speed Differential I/O	PIN_JK82
QSFPDDB_RX_n4	Receiver inverted data of channel 4	High Speed Differential I/O	PIN_JA79
QSFPDDB_RX_n5	Receiver inverted data of channel 5	High Speed Differential I/O	PIN_HU82
QSFPDDB_RX_n6	Receiver inverted data of channel 6	High Speed Differential I/O	PIN_HE82
QSFPDDB_RX_n7	Receiver inverted data of channel 7	High Speed Differential I/O	PIN_GN82
QSFPDDB_REFCLK_p	QSFP-DD port B transceiver reference clock p	LVDS	PIN_JD74
QSFPDDB_INITMODE	Initialization mode	1.2V	PIN_LL59
QSFPDDB_INTERRUPT_n	Interrupt	1.2V	PIN_LL57
QSFPDDB_MOD_PRS_n	Module Present	1.2V	PIN_KW57
QSFPDDB_MOD_SEL_n	Module Select	1.2V	PIN_LH56
QSFPDDB_RST_n	Module Reset	1.2V	PIN_KJ57
QSFPDDB_SCL	2-wire serial interface clock	1.2V	PIN_LB58
QSFPDDB_SDA	2-wire serial interface data	1.2V	PIN_LB56

2.9 PCI Express

The FPGA development board is designed to fit entirely into a PC motherboard with x16 PCI Express slot. Utilizing built-in transceivers on an Agilex device, it is able to provide a fully integrated PCI Express-compliant solution for multi-lane (x1, x4, x8 and x16) applications. With the PCI Express hard IP block incorporated in the Agilex device, it will allow users to implement simple and fast protocol, as well as saving logic resources for logic application. **Figure 2-24** presents the pin connection established between the Agilex FPGA and PCI Express.

The PCI Express interface supports complete PCI Express Gen1 at 2.5Gbps/lane, Gen2 at 5.0Gbps/lane, Gen3 at 8.0Gbps/lane, Gen4 at 16.0Gbps/lane and Gen5 protocol stack solution compliant to PCI Express base specification 5.0 that includes PHY-MAC, Data Link, and transaction layer circuitry embedded in PCI Express hard IP blocks.

Please note that it is a requirement that you connect the PCIe external power connector 8-pin 12V DC power connector in the FPGA to avoid FPGA damage due to insufficient power.

The PCIE_REFCLK_p[1:0] signal are driven from the PC motherboard on this board through the PCIe edge connector or on-board PCIe clock generator. User can use switch to choose wich clock soure are used as reference clock. Please see the section 2.3 : *PCIe Clock Select Switch* for detailed.

A DIP switch (SW4) is connected to the PCI Express to allow different configurations to enable x1, x4, x8 or x16 PCIe lane. Please see the section 2.3 : *Setup PCI Express Control DIP switch* for detailed.

Table 2-22 summarizes the PCI Express pin assignments of the signal names relative to the Agilex FPGA.

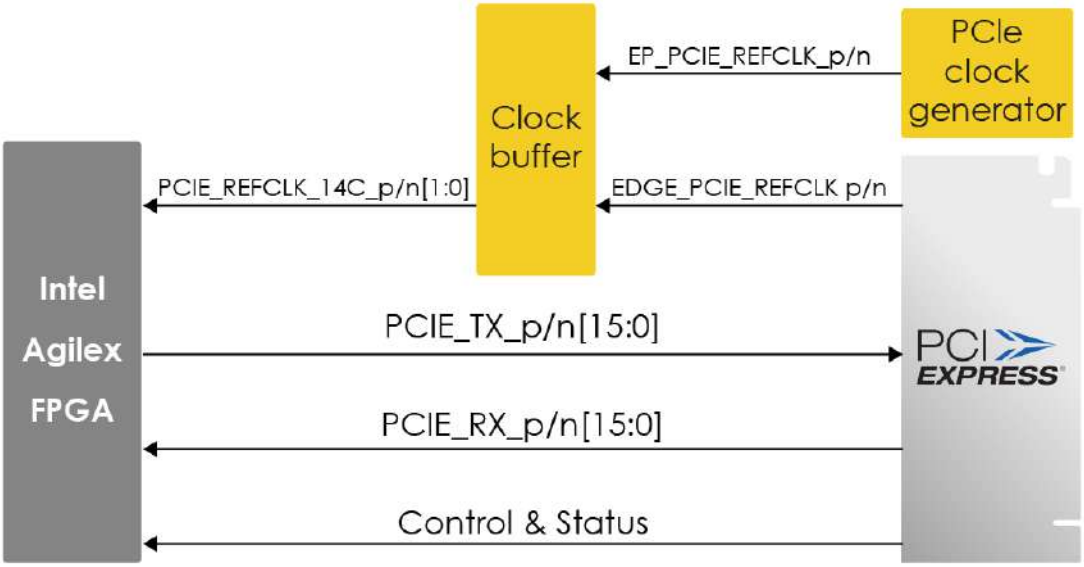


Figure 2-24 PCI Express pin connection

Table 2-22 PCI Express Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
PCIE_TX_p0	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_DL74
PCIE_TX_p1	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_DB77
PCIE_TX_p2	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_CW74
PCIE_TX_p3	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_CJ77
PCIE_TX_p4	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_CF74
PCIE_TX_p5	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BU77
PCIE_TX_p6	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BP74
PCIE_TX_p7	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BE77
PCIE_TX_p8	Add-in card transmit bus	HIGH Speed	PIN_BB74

		Differential I/O	
PCIE_TX_p9	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_AM77
PCIE_TX_p10	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_AJ74
PCIE_TX_p11	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_Y77
PCIE_TX_p12	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_V74
PCIE_TX_p13	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_K74
PCIE_TX_p14	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_C71
PCIE_TX_p15	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_M71
PCIE_TX_n0	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_DH73
PCIE_TX_n1	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_DE76
PCIE_TX_n2	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_CT73
PCIE_TX_n3	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_CM76
PCIE_TX_n4	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_CC73
PCIE_TX_n5	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BY76
PCIE_TX_n6	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BL73
PCIE_TX_n7	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BH76
PCIE_TX_n8	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_AW73
PCIE_TX_n9	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_AR76

PCIE_TX_n10	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_AF73
PCIE_TX_n11	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_AC76
PCIE_TX_n12	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_T73
PCIE_TX_n13	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_G73
PCIE_TX_n14	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_E69
PCIE_TX_n15	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_P69
PCIE_RX_p0	Add-in card receive bus	HIGH Speed Differential I/O	PIN_DE82
PCIE_RX_p1	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CW80
PCIE_RX_p2	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CM82
PCIE_RX_p3	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CF80
PCIE_RX_p4	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BY82
PCIE_RX_p5	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BP80
PCIE_RX_p6	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BH82
PCIE_RX_p7	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BB80
PCIE_RX_p8	Add-in card receive bus	HIGH Speed Differential I/O	PIN_AR82
PCIE_RX_p9	Add-in card receive bus	HIGH Speed Differential I/O	PIN_AJ80
PCIE_RX_p10	Add-in card receive bus	HIGH Speed Differential I/O	PIN_AC82
PCIE_RX_p11	Add-in card receive bus	HIGH Speed	PIN_V80

		Differential I/O	
PCIE_RX_p12	Add-in card receive bus	HIGH Speed Differential I/O	PIN_P82
PCIE_RX_p13	Add-in card receive bus	HIGH Speed Differential I/O	PIN_K80
PCIE_RX_p14	Add-in card receive bus	HIGH Speed Differential I/O	PIN_M77
PCIE_RX_p15	Add-in card receive bus	HIGH Speed Differential I/O	PIN_C77
PCIE_RX_n0	Add-in card receive bus	HIGH Speed Differential I/O	PIN_DB83
PCIE_RX_n1	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CT79
PCIE_RX_n2	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CJ83
PCIE_RX_n3	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CC79
PCIE_RX_n4	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BU83
PCIE_RX_n5	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BL79
PCIE_RX_n6	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BE83
PCIE_RX_n7	Add-in card receive bus	HIGH Speed Differential I/O	PIN_AW79
PCIE_RX_n8	Add-in card receive bus	HIGH Speed Differential I/O	PIN_AM83
PCIE_RX_n9	Add-in card receive bus	HIGH Speed Differential I/O	PIN_AF79
PCIE_RX_n10	Add-in card receive bus	HIGH Speed Differential I/O	PIN_Y83
PCIE_RX_n11	Add-in card receive bus	HIGH Speed Differential I/O	PIN_T79
PCIE_RX_n12	Add-in card receive bus	HIGH Speed Differential I/O	PIN_M83

PCIE_RX_n13	Add-in card receive bus	HIGH Speed Differential I/O	PIN_G79
PCIE_RX_n14	Add-in card receive bus	HIGH Speed Differential I/O	PIN_P76
PCIE_RX_n15	Add-in card receive bus	HIGH Speed Differential I/O	PIN_E76
PCIE_CLKREQ_n	Request the reference clock	1.2V	PIN_B49
PCIE_REFCLK_14C_p[0]	Motherboard reference clock	HCSL	PIN_DR68
PCIE_REFCLK_14C_p[1]	Motherboard reference clock	HCSL	PIN_CU68
PCIE_PERST_n	Reset	1.8V	PIN_CD58
PCIE_WAKE_n	Active-low signal that is used to return the PCIe interafce to an active state when in a low-power state	1.2V	PIN_W52

2.10 MCIO Connector

This board provides two 74-pin MCIO connectors (See **Figure 2-25** and **Figure 2-26**) that can be used to connect to Agilex FPGA's 16 R-tile transceiver channels for CXL or PCIe* interface applications.Users can use cable to connect the board to the host and establish CXL or PCIe* link.

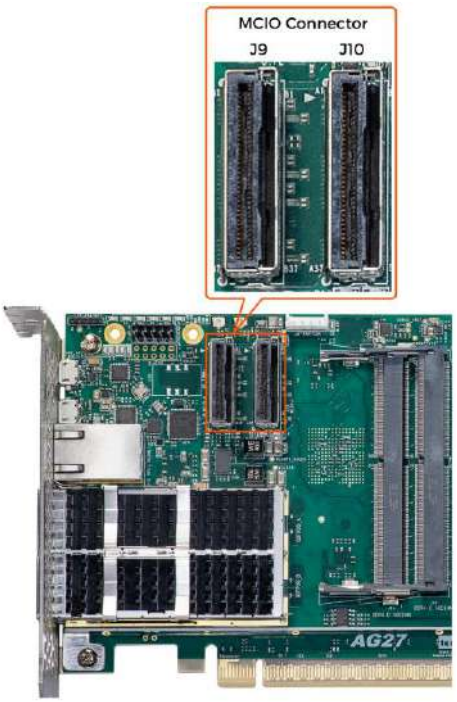


Figure 2-25 MCIO connectors on Mercury A2700 Accelerator Card

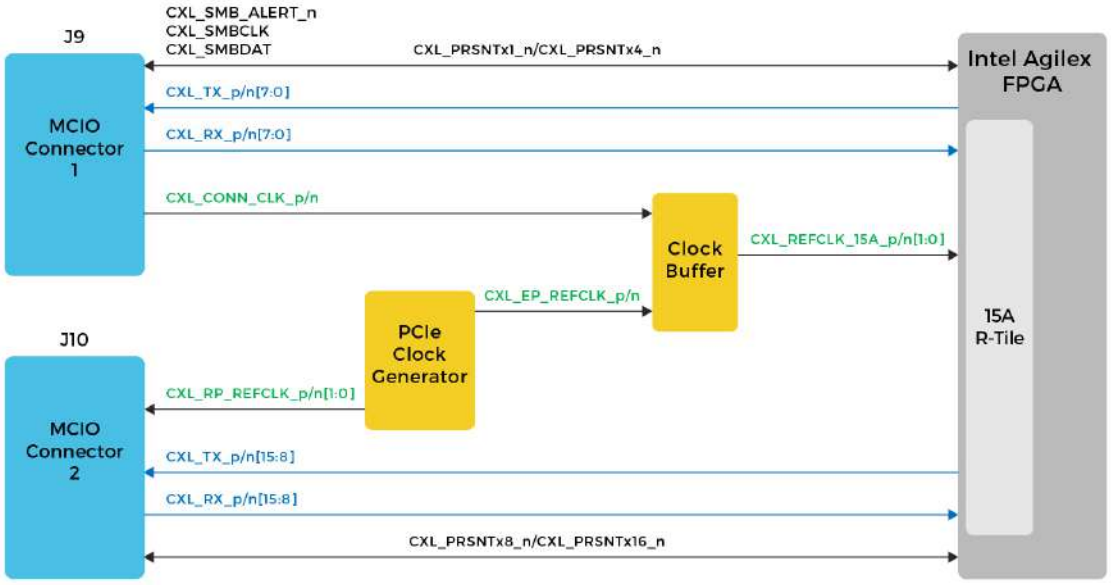


Figure 2-26 MCIO connectors connection to FPGA

Table 2-23 shows the FPGA dedicated clock input pin placement on the MCIO connectors.

Table 2-23 MCIO Connectors Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin Number	Description	I/O Standard
CXL_SMBCLK	PIN_JL31	SMB clock	1.2 V
CXL_SMBDAT	PIN_JP30	SMB data	1.2 V
CXL_TX_p[0]	PIN_FK20	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[1]	PIN_FN14	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[2]	PIN_GB20	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[3]	PIN_GE14	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[4]	PIN_GR20	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[5]	PIN_GV14	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[6]	PIN_HG20	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[7]	PIN_HK14	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[8]	PIN_HW20	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[9]	PIN_JC14	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[10]	PIN_JM20	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[11]	PIN_JR14	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[12]	PIN_KD20	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[13]	PIN_KG14	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[14]	PIN_KT20	CXL transmit bus	High Speed Differential I/O
CXL_TX_p[15]	PIN_KY14	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[0]	PIN_FG22	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[1]	PIN_FT16	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[2]	PIN_FW22	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[3]	PIN_GJ16	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[4]	PIN_GM22	CXL transmit bus	High Speed Differential I/O

CXL_TX_n[5]	PIN_HA16	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[6]	PIN_HD22	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[7]	PIN_HN16	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[8]	PIN_HT22	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[9]	PIN_JF16	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[10]	PIN_JJ22	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[11]	PIN_JV16	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[12]	PIN_KA22	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[13]	PIN_KK16	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[14]	PIN_KN22	CXL transmit bus	High Speed Differential I/O
CXL_TX_n[15]	PIN_LC16	CXL transmit bus	High Speed Differential I/O
CXL_RX_p[0]	PIN_FK8	CXL receive bus	High Speed Differential I/O
CXL_RX_p[1]	PIN_FN1	CXL receive bus	High Speed Differential I/O
CXL_RX_p[2]	PIN_GB8	CXL receive bus	High Speed Differential I/O
CXL_RX_p[3]	PIN_GE1	CXL receive bus	High Speed Differential I/O
CXL_RX_p[4]	PIN_GR8	CXL receive bus	High Speed Differential I/O
CXL_RX_p[5]	PIN_GV1	CXL receive bus	High Speed Differential I/O
CXL_RX_p[6]	PIN_HG8	CXL receive bus	High Speed Differential I/O
CXL_RX_p[7]	PIN_HK1	CXL receive bus	High Speed Differential I/O
CXL_RX_p[8]	PIN_HW8	CXL receive bus	High Speed Differential I/O
CXL_RX_p[9]	PIN_JC1	CXL receive bus	High Speed Differential I/O
CXL_RX_p[10]	PIN_JM8	CXL receive bus	High Speed Differential I/O
CXL_RX_p[11]	PIN_JR1	CXL receive bus	High Speed Differential I/O
CXL_RX_p[12]	PIN_KD8	CXL receive bus	High Speed Differential I/O
CXL_RX_p[13]	PIN_KG1	CXL receive bus	High Speed Differential I/O
CXL_RX_p[14]	PIN_KT8	CXL receive bus	High Speed Differential I/O
CXL_RX_p[15]	PIN_KY1	CXL receive bus	High Speed Differential I/O

CXL_RX_n[0]	PIN_FG10	CXL receive bus	High Speed Differential I/O
CXL_RX_n[1]	PIN_FT3	CXL receive bus	High Speed Differential I/O
CXL_RX_n[2]	PIN_FW10	CXL receive bus	High Speed Differential I/O
CXL_RX_n[3]	PIN_GJ3	CXL receive bus	High Speed Differential I/O
CXL_RX_n[4]	PIN_GM10	CXL receive bus	High Speed Differential I/O
CXL_RX_n[5]	PIN_HA3	CXL receive bus	High Speed Differential I/O
CXL_RX_n[6]	PIN_HD10	CXL receive bus	High Speed Differential I/O
CXL_RX_n[7]	PIN_HN3	CXL receive bus	High Speed Differential I/O
CXL_RX_n[8]	PIN_HT10	CXL receive bus	High Speed Differential I/O
CXL_RX_n[9]	PIN_JF3	CXL receive bus	High Speed Differential I/O
CXL_RX_n[10]	PIN_JJ10	CXL receive bus	High Speed Differential I/O
CXL_RX_n[11]	PIN_JV3	CXL receive bus	High Speed Differential I/O
CXL_RX_n[12]	PIN_KA10	CXL receive bus	High Speed Differential I/O
CXL_RX_n[13]	PIN_KK3	CXL receive bus	High Speed Differential I/O
CXL_RX_n[14]	PIN_KN10	CXL receive bus	High Speed Differential I/O
CXL_RX_n[15]	PIN_LC3	CXL receive bus	High Speed Differential I/O
CXL_REFCLK_15A_p[0]	PIN_GA27	Clock for RootPort mode	HCSL
CXL_REFCLK_15A_p[1]	PIN_GY26	Clock for RootPort mode	HCSL
CXL_PERST_n	PIN_HY33	PCIe interface reset	1.2 V
CXL_RST_n	PIN_J51	CXL bus reset	1.2 V
CXL_SMB_ALERT_n	PIN_KF30	an interrupt line for devices that want to trade their ability to master for	1.2 V

2.11 USB to UART

The board provides two UART functions (See **Figure 2-27**). One of them is connected to HPS fabric in the Agilex FPGA, allowing host to communicate and debug with the

HPS fabric through the UART interface. The other one is to connect to the system MAX10 device. It allows users to monitor various status of the board such as temperature and voltage value from the Host.

The board uses a USB hub to allow two USB to UART interface (HPS fabric and system MAX10) and a USB Blaster II circuit to share a Micro USB connector to connect to the host. Users only need one Micro USB cable to establish several UART and JTAG connections with the Host to transmit data.

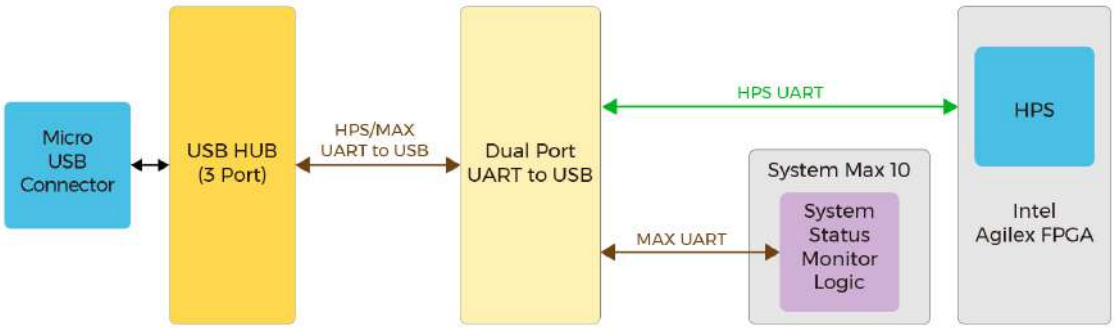


Figure 2-27 The UART interface on the board

■ USB to UART for HPS Fabric

The board provides a UART interface for users to communicate and transfer data with HPS through the host. This interface is mainly implemented via a dual UART to USB (CP2105). For detailed chip information, please refer to \Datasheets\UART_TO_USB\ of the system CD. It can convert commands and data from the host via USB protocol to the UART interface and send it to HPS. **Figure 2-28** shows the connections between the HPS, CP2105 chip, and the Micro USB connector.

Table 2-24 lists the pin assignment of UART interface connected to the HPS.

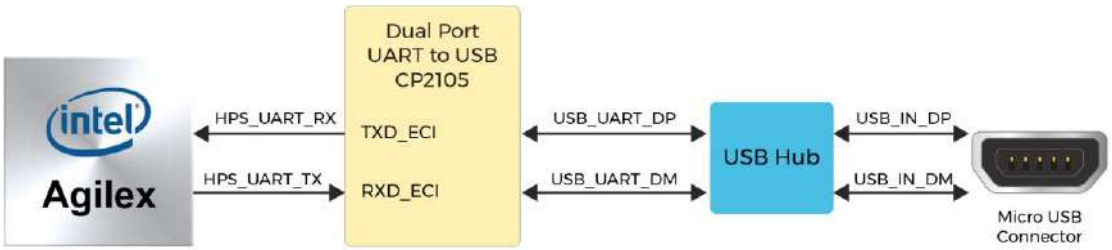


Figure 2-28 Connections between the HPS of Apollo Agilex and FT232R Chip

Table 2-24 Pin Assignment of UART Interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_UART_RX	PIN_L15	HPS UART Receiver	1.8V
HPS_UART_TX	PIN_BF26	HPS UART Transmitter	1.8V

■ USB to UART for System MAX10

The other USB to UART interface is connected with the System MAX10. It allows users to monitor the status of the board from the host through the UART interface. As shown in **Figure 2-29**, the board provides several sensors to monitor the status of the board, such as FPGA temperature, board power monitor, and fan speed status. These interfaces are connected to the System MAX10 FPGA on the board. The board management logic (**Dashboard**) in the system MAX10 FPGA will monitor these status and perform corresponding control according to the status. For example, when the temperature of the FPGA increases, the system will automatically increase the fan speed to reduce the temperature. When the temperature of the FPGA continues to exceed the working range (such as a fan failure condition), the FPGA power will be cut to protect the board.

See **chapter 3** for details. Terasic also provide a “board information IP” that allow user can place it in the Agilex FPGA to read these board status. Please refer to the section 2.5 of the demonstration manual.

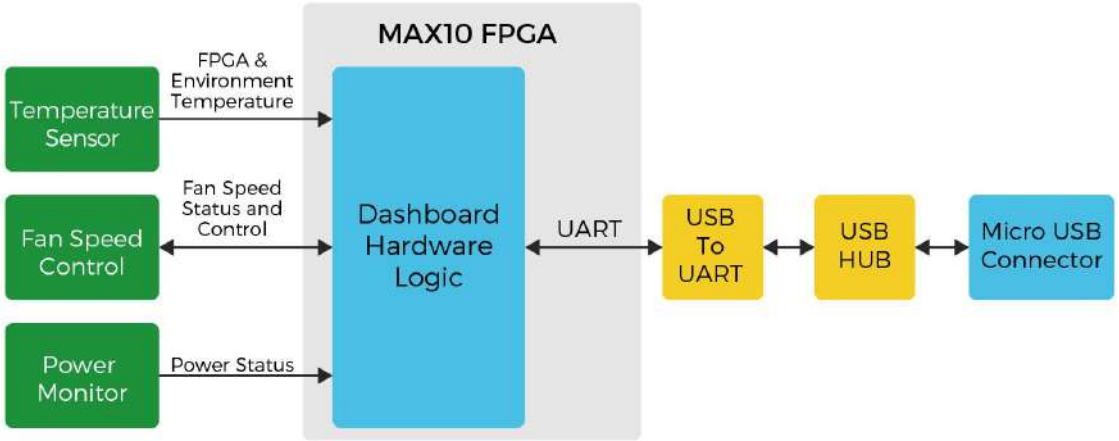


Figure 2-29 Block diagram of the system status interface

2.12 USB 2.0 OTG PHY

The board provides USB interfaces using the SMSC USB3320 controller. A Microchip USB3320 device is used to interface to a single Type AB Micro-USB connector. This device supports UTMI+ Low Pin Interface (ULPI) to communicate to USB 2.0 controller in HPS. As defined by OTG mode, the PHY can operate in Host or Device modes. When operating in Host mode, the interface will supply the power to the device through the Micro-USB interface. **Figure 2-30** shows the connections of USB PTG PHY to the HPS.

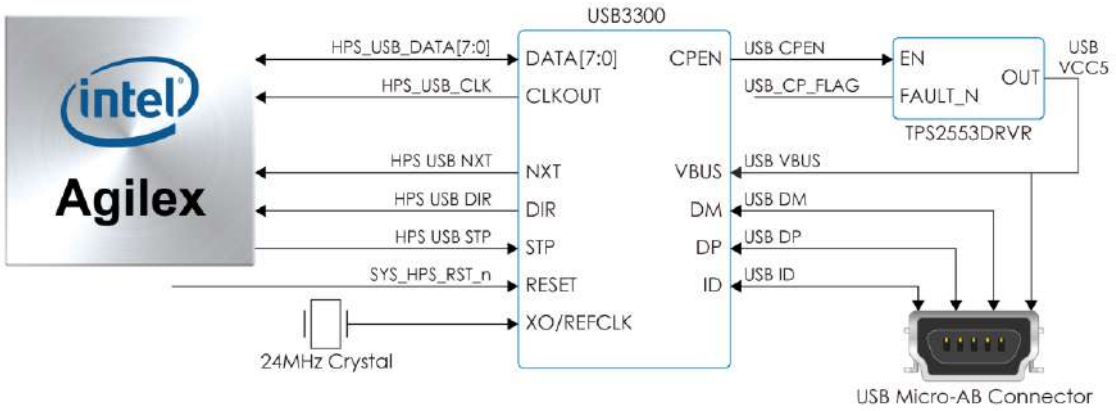


Figure 2-30 Connections between the HPS of Apollo Agilex and USB controller

Table 2-25 Pin Assignment of USB OTG PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_USB_CLK	PIN_BM34	60MHz Reference Clock Output	1.8V
HPS_USB_DATA[0]	PIN_AE16	HPS USB_DATA[0]	1.8V
HPS_USB_DATA[1]	PIN_BM26	HPS USB_DATA[1]	1.8V
HPS_USB_DATA[2]	PIN_CD28	HPS USB_DATA[2]	1.8V
HPS_USB_DATA[3]	PIN_AB6	HPS USB_DATA[3]	1.8V
HPS_USB_DATA[4]	PIN_CA27	HPS USB_DATA[4]	1.8V
HPS_USB_DATA[5]	PIN_AE3	HPS USB_DATA[5]	1.8V
HPS_USB_DATA[6]	PIN_BV28	HPS USB_DATA[6]	1.8V
HPS_USB_DATA[7]	PIN_AB1	HPS USB_DATA[7]	1.8V
HPS_USB_DIR	PIN_BJ33	Direction of the Data Bus	1.8V
HPS_USB_NXT	PIN_AB14	Throttle the Data	1.8V

HPS_USB_STP	PIN_AB18	Stop Data Stream on the Bus	1.8V

2.13 Micro SD Card Socket

The board supports Micro SD card interface with x4 data lines. It serves for an external storage for the **HPS fabric**. Figure 2-31 shows signals connected between the HPS and Micro SD card socket. **Table 2-26** lists the pin assignment of Micro SD card socket to the HPS.

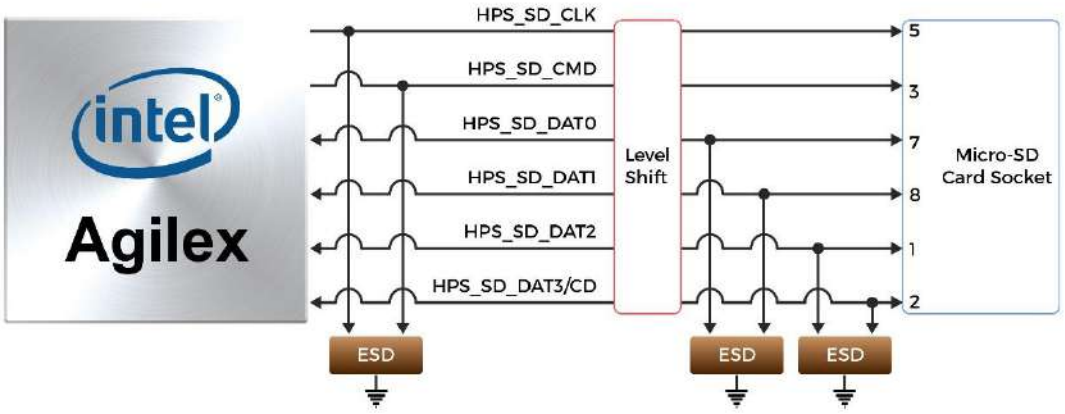


Figure 2-31 Pin-out of Micro SD Card socket

Table 2-26 Micro SD Card Socket Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_SD_CLK	HPS SD Clock	1.8-V	PIN_N27
HPS_SD_CMD	HPS SD Command Line	1.8-V	PIN_N21
HPS_SD_DATA[0]	HPS SD Data[0]	1.8-V	PIN_L28
HPS_SD_DATA[1]	HPS SD Data[1]	1.8-V	PIN_L23
HPS_SD_DATA[2]	HPS SD Data[2]	1.8-V	PIN_U27
HPS_SD_DATA[3]	HPS SD Data[3]	1.8-V	PIN_W26

2.14 Gigabit Ethernet

The board supports Gigabit Ethernet transfer by an external Micrel KSZ9031RN PHY chip and **HPS** Ethernet MAC function. The KSZ9031RN chip with integrated

10/100/1000 Mbps Gigabit Ethernet transceiver also supports RGMII MAC interface. **Figure 2-32** shows the connections between the HPS, Gigabit Ethernet PHY, and RJ-45 connector.

For more information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, which are available on the manufacturer's website.

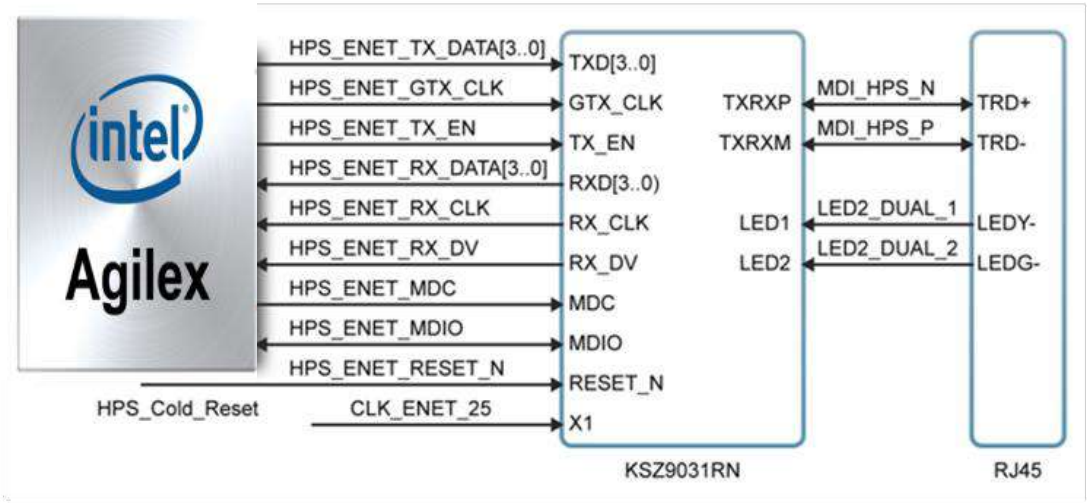


Figure 2-32 Connections between the HPS of Apollo Agilex and RGMII MAC

There are two LEDs, a green LED (LEDG) and a yellow LED (LEDY), which represent the status of the Ethernet PHY (KSZ9031RN). The LED control signals are connected to the LEDs on the RJ45 connector. The state and the definition of LEDG and LEDY are listed in **Table 2-27**. For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-27 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity

Toggle	Toggle	Blinking	Blinking	Link / Activity (RX, TX)

Table 2-28 Pin Assignment of Gigabit Ethernet PHY

Signal Name	FPGA Pin No	Description	I/O Standard
HPS_ENET_MDC	PIN_L26	Management Data Clock Reference	1.8V
HPS_ENET_MDIO	PIN_BJ31	Management Data	1.8V
HPS_ENET_RX_CLK	PIN_BV30	GMII and MII receive clock	1.8V
HPS_ENET_RX_CTL	PIN_CG27	GMII and MII receive data valid	1.8V
HPS_ENET_RX_DATA[0]	PIN_BV32	GMII and MII receive data[0]	1.8V
HPS_ENET_RX_DATA[1]	PIN_CD26	GMII and MII receive data[1]	1.8V
HPS_ENET_RX_DATA[2]	PIN_BM28	GMII and MII receive data[2]	1.8V
HPS_ENET_RX_DATA[3]	PIN_U13	GMII and MII receive data[3]	1.8V
HPS_ENET_TX_CLK	PIN_CA29	GMII Transmit Clock	1.8V
HPS_ENET_TX_CTL	PIN_CN27	GMII and MII transmit enable	1.8V
HPS_ENET_TX_DATA[0]	PIN_CA31	MII transmit data[0]	1.8V
HPS_ENET_TX_DATA[1]	PIN_J5	MII transmit data[1]	1.8V
HPS_ENET_TX_DATA[2]	PIN_BV26	MII transmit data[2]	1.8V
HPS_ENET_TX_DATA[3]	PIN_D7	MII transmit data[3]	1.8V

2.15 System Status Interface

As shown in **Figure 2-33**, the Mercury A2700 Accelerator Card provides several sensors to monitor the status of the board, such as FPGA temperature, board power monitor, and fan speed status. These interfaces are connected to the System MAX10 FPGA on the board. The board management logic (Dashboard) in the System MAX10 FPGA will monitor those status and perform corresponding control according to the status. For example, when the temperature of the FPGA increases, the system will automatically increase the fan speed to reduce the temperature. When the temperature of the FPGA continues to exceed the working range (such as a fan failure condition), the FPGA power will be cut to protect the board.

The board also provides USB to UART interface to connect with the System MAX10

FPGA, so that users can monitor the status of the board from the host through the UART interface. See chapter 8 for details.

Finally, the board status also can be read on the Agilex FPGA side via the SPI interface connected to the System MAX10 FPGA. Terasic had provided a “board information IP” that allow user can place it in the FPGA to read these board status. **Table 2-29** shows the pin assignments of the SPI interface on the Agilex FPGA.

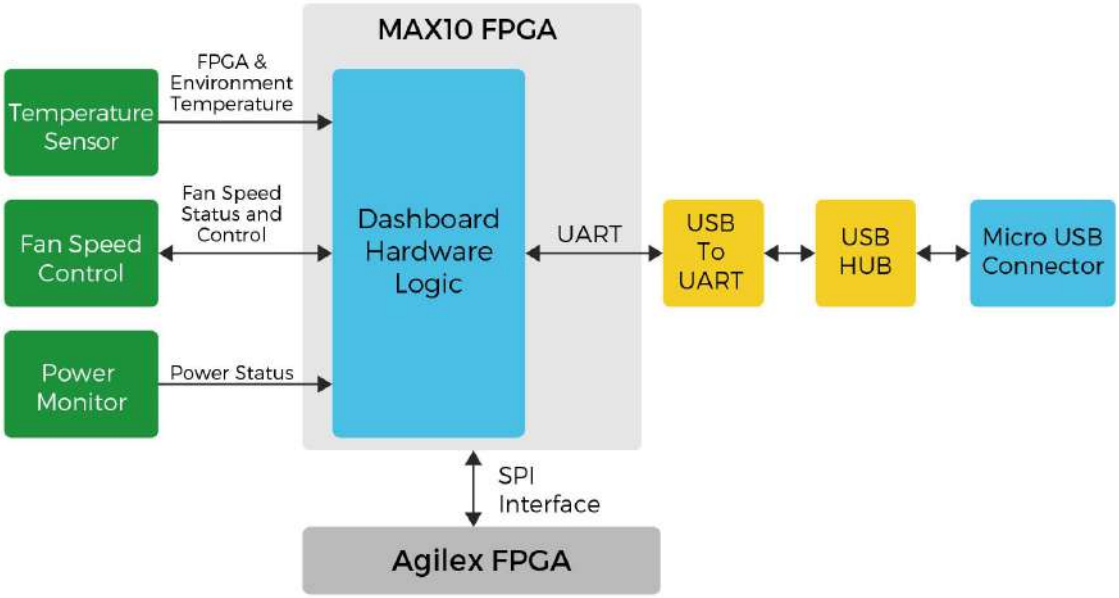


Figure 2-33 Block diagram of the system status interface

Table 2-29 Pin Assignments, Schematic Signal Names, and Functions for SPI interface of the board status

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
INFO_SPI_SCLK	Serial Clock, SPI master output to salve.	1.2V	PIN_B45
INFO_SPI_MISO	Master input.	1.2V	PIN_H46
INFO_SPI_MOSI	Master output.	1.2V	PIN_J45
INFO_SPI_CS_n	Slave Select, Master output.	1.2V	PIN_D46

Chapter 3

QSPI-Flash Programming

In this chapter, we will introduce how to use the AVSTx8 configuration method to load their design file from the flash memory device to the FPGA after the board power on. As shown in **Figure 3-1**, the System MAX 10 FPGA is the core component of this configuration system. A Parallel Flash Loader II (PFL II) IP is implemented in the System MAX 10 FPGA, allowing users to send bit stream files of user's project from host to the System MAX 10 FPGA through the JTAG interface. Then, the bit stream files will be written into the QSPI Flash connected to the System MAX 10 FPGA via the PFL II IP. Batch file sof_2_pof.bat is designed to merge factory.sof, user.sof, and option bit into a AVSTx8.pof file. Batch file program_pof.bat is designed to program the AVSTx8.pof file into QSPI Flash.

After the user's bit stream files are stored into the QSPI Flash device, when the MA27 board is powered on, the PFL II IP in the System MAX 10 FPGA will automatically load the bit stream file from the QSPI Flash first, and then configure the FPGA through the Avalon-ST x8 interface.

In this chapter, we will introduce how to correctly set the FPGA to work in AVSTx8 mode, how to program bit stream files into the QSPI Flash, and how to switch the image file to be loaded.

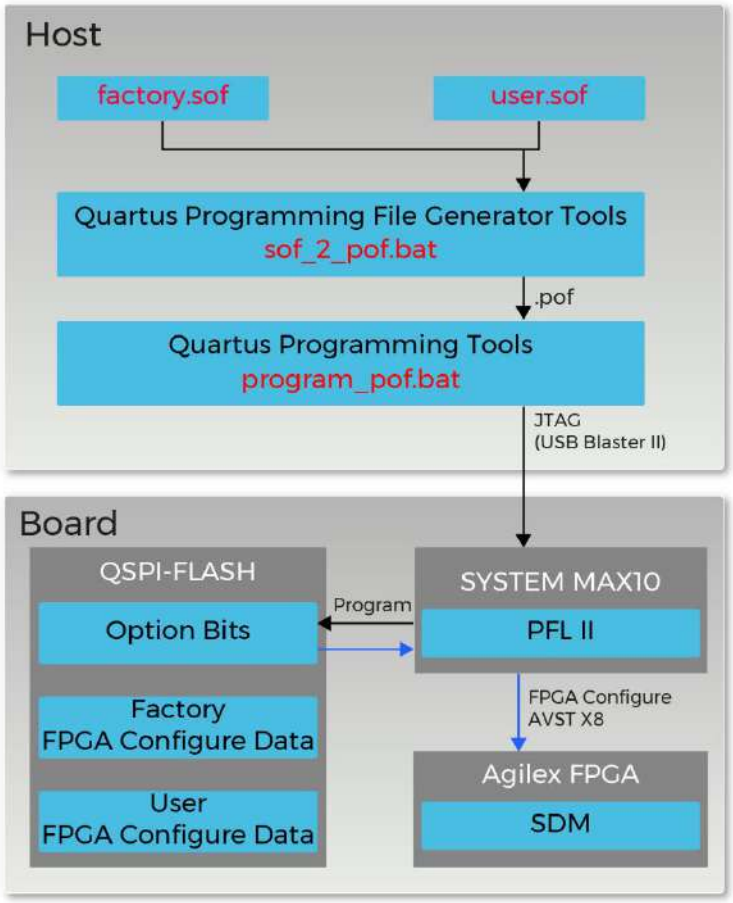


Figure 3-1 Block diagram of the Avalon-ST x 8 mode on the board

Note that the MA27 board ships with the QSPI flash device preprogrammed with two FPGA configurations. The two configuration images are called: **factory** image and **user** image, respectively.

3.1 FPGA Configure Operation

This section will show the procedure for how to enable the FPGA configuration from QSPI Flash (Set FPGA to AVSTx8 mode). Also, it will show how to select one boot image between factory image and user image.

1. Make sure the two default FPGA configurations data has been stored in the QSPI flash (The board ships with two images in the 2Gbit QSPI flash).
2. Set the FPGA configuration mode to AVSTx8 mode by setting **SW4** and **SW5** MSEL[2:0] as **110** as shown in **Figure 3-2**.

3. Specify the configuration of the FPGA using the default Factory Configuration Image or User Configuration Image by setting SW4 according to Figure 3-3. When the switch is in position “1”, the factory image is used when the system boots. When the switch is in position “0”, user image is used when the system boots.
4. Power on the FPGA board or press the MAX_RST button if board is already powered on,
5. When the configuration is completed, the green Configure Done LED will light. If there is an error, the red Configure Error LED will light (See **Figure 3-4**).

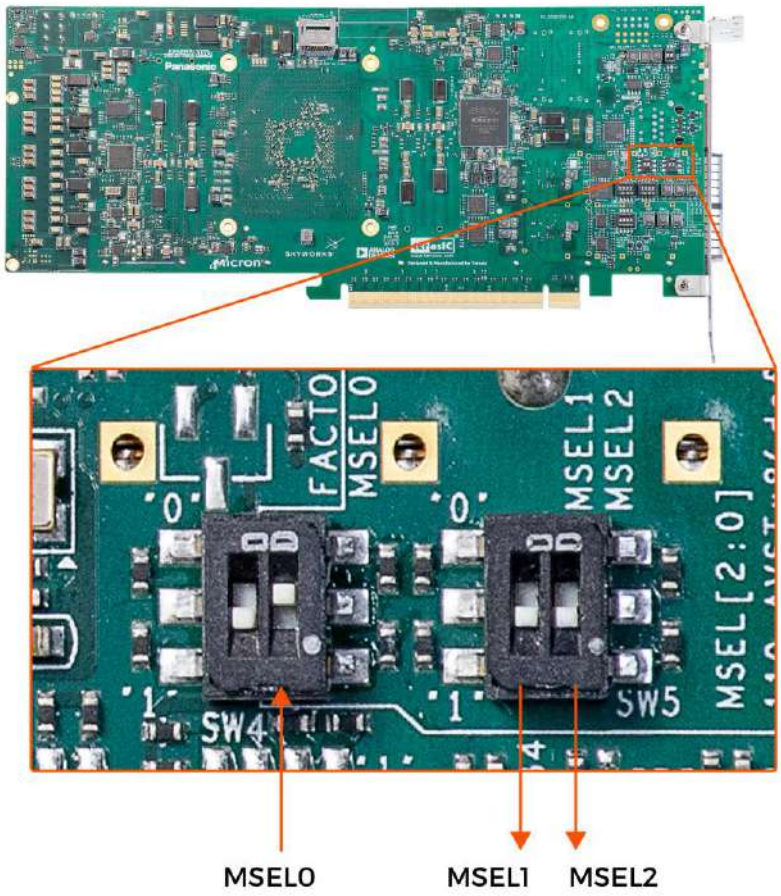


Figure 3-2 Position of the MSEL[2:0] switch

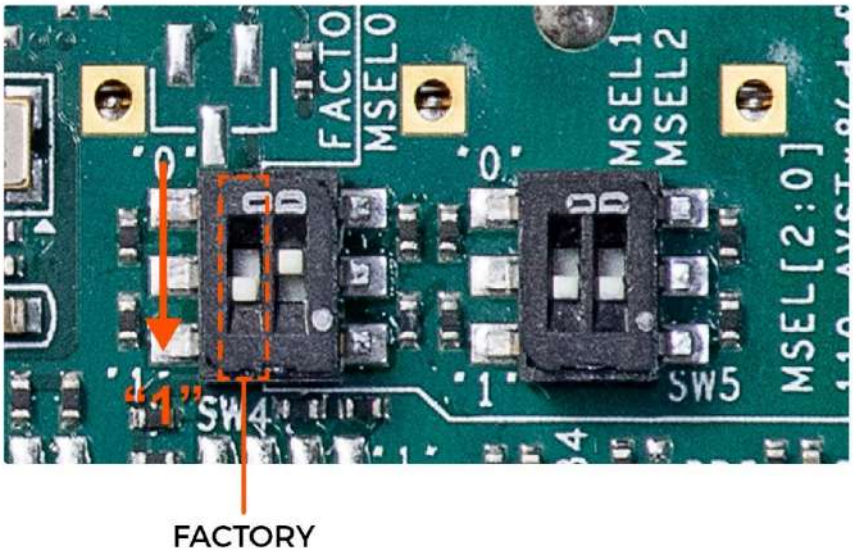


Figure 3-3 Configuration Image Selection

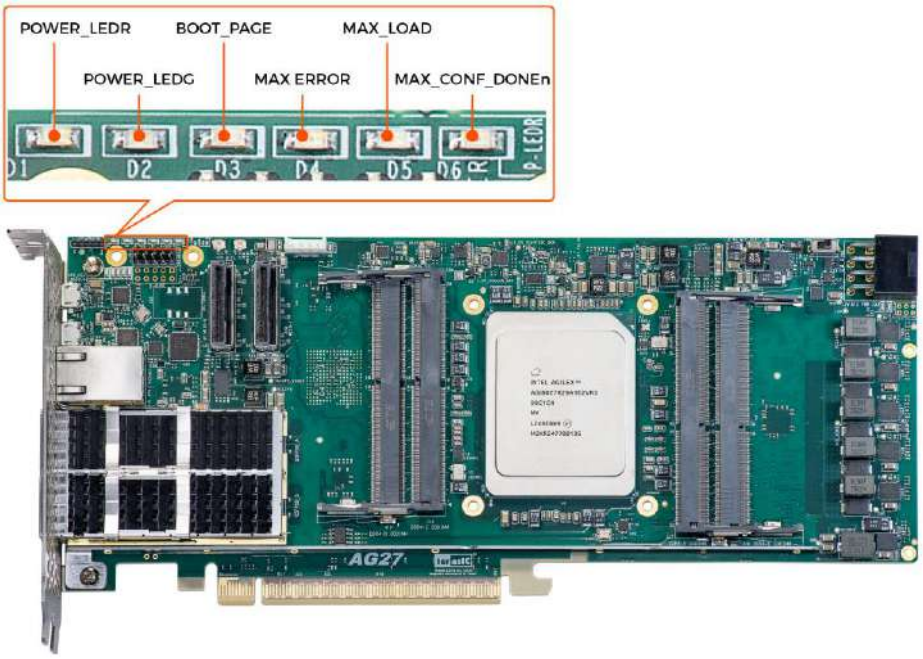


Figure 3-4 Position of the Configuration status LED

3.2 QSPI Flash Memory Map

The MA27 has one 2-Gbit QSPI flash device for non-volatile storage of the FPGA configuration data for AVTSx8 Mode. Only the System MAX10 FPGA can access this Flash device.

Table 4-1 shows the memory map for the on-board flash. This memory provides non-volatile storage space for two FPGA bit-streams, and FPL option bits for PFL II configuration bits and board information. For the factory and user code to run correctly and update designs in the user memory, this FPL option bit address (0x00002000) must not be altered.

Table 4-1 Flash Memory Map (Byte Address)

Block Description	Size(MB)	Address Range
PFL option bits	-	0x00002000 – 0x00003FFF
Factory image	~128	0x00004000 – 0x07FFFFF
User image	128	0x08000000 – 0x0FFFFFFF

The **PFL option bits** contain the image location of the **Factory image** and **User image**, so the PLF II IP in the System MAX10 FPGA can know where to find the FPGA configuration data. If developers erase all flash content, please ensure that the PFL option is reprogrammed with the FPGA configuration data.

For user's application, the **User image** is stored with start address **0x08000000**. Users also can overwrite the Factory hardware on their application. **Factory image** is stored with start address **0x00004000**. We strongly recommend users to use the batch file in the **AVSTx8_Restored** folder to write the FPGA configuration bit stream and option bit data into the QSPI Flash.

3.3 Programming Bit Stream File Into QSPI Flash

This section will introduce how to allow users to program the bit stream file generated by their own project into the QSPI Flash on the MA27 board, so that the design file can be automatically loaded into the FPGA and executed after the board power on.

The QSPI Flash of the MA27 board can only be programmed from the Host PC through the JTAG interface. The QSPI Flash is connected to the system MAX10 FPGA on the board. Before program the QSPI flash, users must set MSEL[2:0]=110 for AVSTx4

mode, so MAX10(VTAP10) is visible on the JTAG bus.

Figure 3-5 shows the standard QSPI Flash programming steps. Users first need to convert the bit stream file (.sof) generated by their Quartus project into a Programmer Object File (.pof) file through the Programming File Generator tool. Then use the Quartus Programmer tool to connect with the System MAX10 FPGA on the MA27 board through the JTAG interface and program the .pof file into QSPI Flash. In order to help users easily and quickly program the QSPI Flash on the board, Terasic provides some batch files so that users can quickly complete the operations for the QSPI Flash such as erasing and programming. Users can find these batch files under the path: *\System CD\Demonstrations\AVSTx8_Restore*.
Users can copy this "**AVSTx8_Restore**" folder to Host for further use.

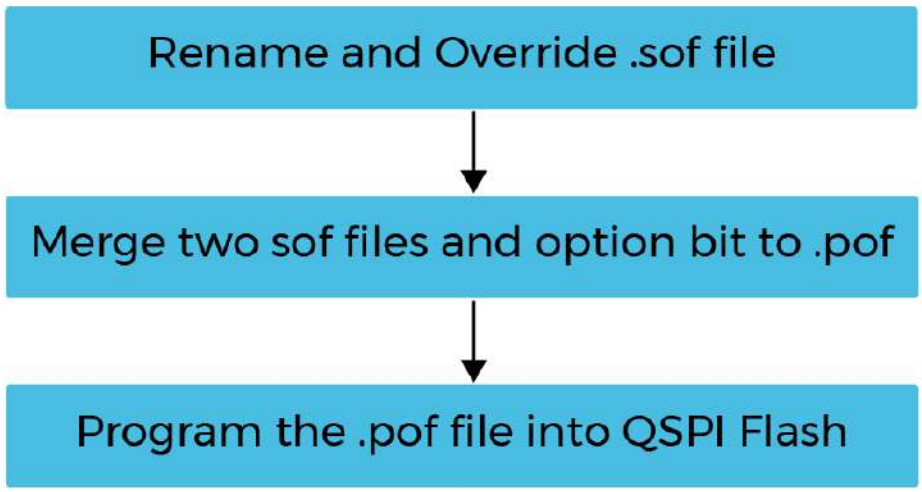


Figure 3-5 Program Flash flow

Table 4-2 is the file list and descriptions in the AVSTx8_Restore folder.

Table 4-2 File list and descriptions of the batch file folder

Example Folder	Description
factory.sof	The bit stream file to be programmed into the factory image area of the QSPI Flash.
user.sof	The bit stream file to be programmed into the user image area of the QSPI Flash.
sof_2_pof.bat	sof_2_pof.bat merges factory.sof, user.sof, and option bit to AVTSx8.pof file.

AVSTx8.pof	This Programmer Object File (.pof) file will be programmed into the QSPI Flash.
program_pof.bat	program_pof.bat programs the AVSTx8.pof into QSPI Flash.
erase_flash.bat	This batch file erases the QSPI Flash.
AVSTx8_pof.map	A text file containing the byte addresses information about option bits and factory/user images.
AVSTx8_program.cdf	This Chain Description File (.cdf) is used by Program_pof.bat to program the .pof file into Flash.
erace_flash.cdf	This Chain Description File (.cdf) is used by erase_flash.bat to erase the Flash.
AVSTx8.pfg	This PFG setting file (.pfg) is used by sof_2_pof.bat to generate AVSTx8.pof.

The detailed description about the usage flow of these batch files is as follows:

■ Override sof

After users complete their owned project design and generate the .sof file, if they want to use the batch file tools to program the .sof into the QSPI Flash on the MA27 board. The user must first modify the file name of his own .sof file to **factory.sof** or **user.sof**. Then overwrite the .sof file in the "AVSTx8_Restore" folder. If users want to program their .sof file into the Factory image area, they need to rename their .sof file to **factory.sof** and copy it into the "**AVSTx8_Restore**" folder (overwrite the original factory.sof). Similarly, if users want to program into the User image area, rename their .sof file to **user.sof** and copy it into the "**AVSTx8_Restore**" folder.

■ Merger sof and option bit to pof

After the user's own project's .sof file has been overwritten into the "AVSTx8_Restore" folder, the next step is to merger the .sof files and option bit to a .pof file. Please execute the **sof_2_pof.bat** in the **"AVSTx8_Restore"** folder to automatically merge the **factory.sof, user.sof** and option bit to **AVSTx8.pof**. The **AVSTx8.pof** is the file will be programmed into the QSPI Flash.

■ Program .pof inot QSPI Flash

Executing the **AVSTx8_pogram.bat** will program the **AVSTx8.pof** file from Host to QSPI Flash via System MAX10 FPGA on MA27 board (please make sure the

MSEL[2:0] on the board is set to 3'b110 and the USB connection is setup from Host to the USB blaster II port on the MA27 board). Before program the Flash, the system will erase Flash contents first. After the programming step is completed, the users only need to power cycle the board, and the user's design file will be automatically loaded into the FPGA for execution.

■ Erase Flash

When the users want to clear the design in QSPI Flash, they can execute **Erase_flash.bat** to complete this action.

3.4 Restore Factory Settings

This section describes how to restore the original **Factory** image and **User** image into the flash memory device on the FPGA development board. A programming batch file located in the **AVSTx8_Restored** folder is used to restore the flash content. Performing the following instructions can restore the flash content:

1. Make sure the Quartus II EDS (Quartus 23.1 Pro edition or later) and USB-Blaster II driver are installed.
2. Set FPGA configuration mode as AVSTx8 Mode by setting SW4/5 MSEL[2:0] to **110**.
3. Make sure the FPGA board and PC are connected with an USB Cable.
4. Power on the FPGA board.
5. Copy the “Demonstrations/AVSTx8_Restored” folder under the CD to your PC’s local drive.
6. Execute the batch file AVSTx8_program.bat to start flash programming.

After restoring the flash, perform the following procedures to test the restored boot code.

1. Power off the FPGA Board.
2. Set FPGA configuration mode as AVSTx8 Mode by setting SW4/5 MSEL[2:0] to **110**.
3. Specify configuration of the FPGA to Factory Hardware by setting the FACTORY_LOAD dip in SW4 to the ‘1’ position.
4. Power on the FPGA Board, and the Configure Done LED should light up.

Batch file sof_2_pof.bat merges the **Factory** and **User** .sof and PFL option bit into a

AVTSx8.pof file. Batch file AVSTx8_program.bat calls Quartus Programmer to program the QSPI-Flash with the generated AVST8x.pof. The factory.sof files generated by **LED_BLINK** project, and the user.sof files generated by **PCIe_DDR4** project.

Chapter 4

Dashboard GUI

The Mercury A2700 Accelerator Card Dashboard GUI is a board status monitor system. This system is connected from the Host to the System MAX10 FPGA on the Mercury A2700 Accelerator Card through the UART interface, and reads various status on the board (See section 2.14 for detailed). The reported status includes FPGA/Board temperature, fan speed, FPGA core power and 12V input power. **Figure 4-1** shows the block diagram of the Mercury A2700 Accelerator Card Dashboard. Note that, the Dashboard GUI software only support windows OS.

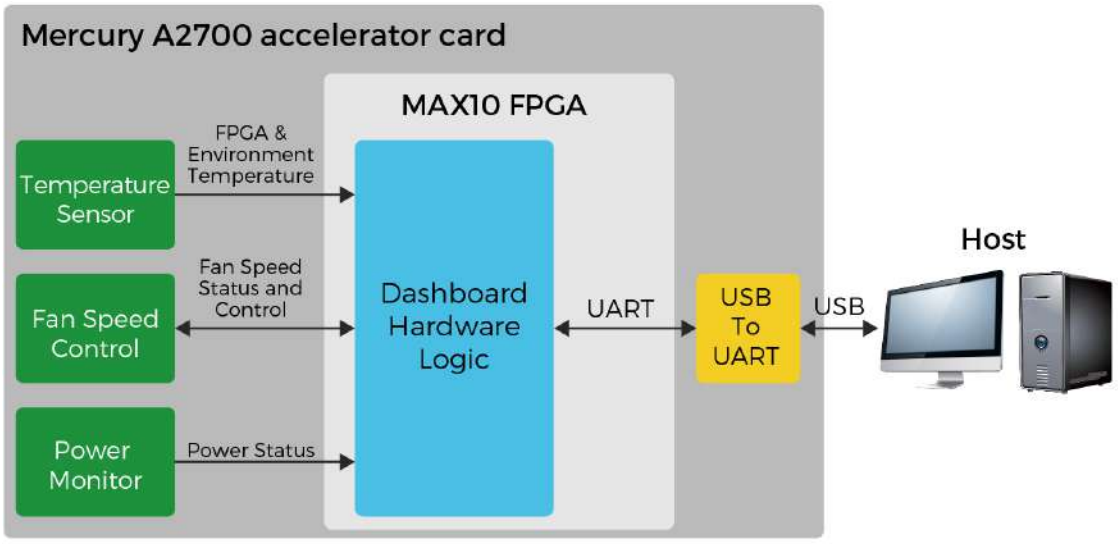


Figure 4-1 Block Diagram of the Mercury A2700 Accelerator Card Dashboard

4.1 Driver Installed on Host

To use the dashboard system, users need to install the USB to UART driver on the host first, so that user can establish a connection with the Mercury A2700 Accelerator Card. This section will describe how to install USB to UART driver on the windows OS host.

■ USB to UART driver location

Users can find it from the path: Tool\dashboard_gui\Driver in the Mercury A2700 Accelerator Card system CD and copy it to the Host.

■ Connection Setting

1. Connect the Micro USB connector of the Mercury A2700 Accelerator Card to the Host USB port through Micro USB cable.

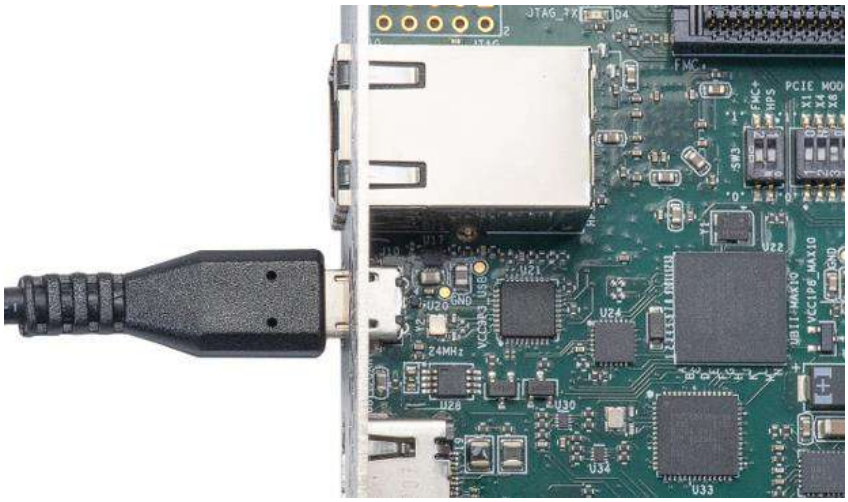


Figure 4-2 Connection setup for using dashboard system

2. Connect power to the Mercury A2700 Accelerator Card.
3. Power on the Mercury A2700 Accelerator Card.

■ Install Driver

When connect the Mercury A2700 Accelerator Card to the Host. As shown in **Figure 4-3**, two USB to UART Com Port device is shown in “Device Manager” of Host.

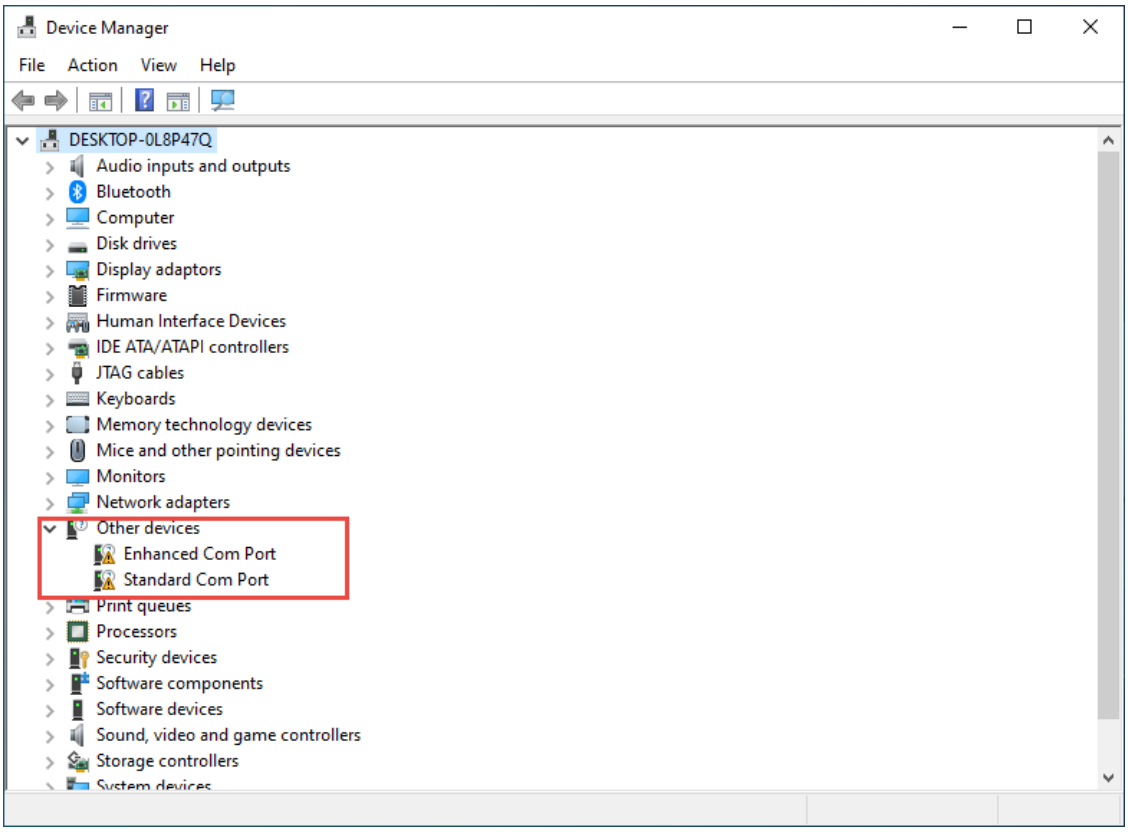


Figure 4-3 Uninstalled USB to UART device

Copy the device driver (System CD\Tool\dashboard_gui\Driver) to the Host and install it, as shown in **Figure 4-4.** Please note that the COM Port number is different in different Host.

Figure 4-4 Install USB to UART driver

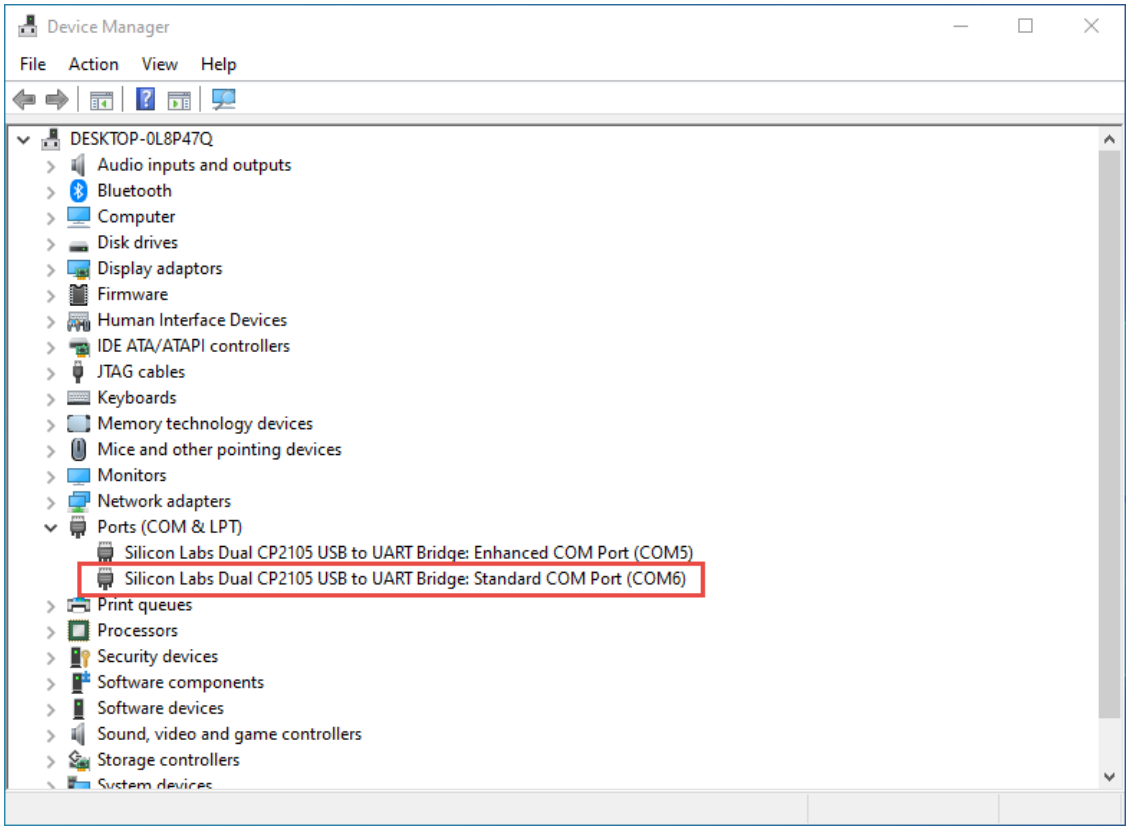


Figure 4-5 The USB to UART device after driver is installed successfully

4.2 Run Dashboard GUI

■ Dashboard GUI software location

Users can find it from the path: Tool\dashboard_gui\Dashboard.exe in the Mercury A2700 Accelerator Card system CD and copy it to the Host.

Execute the **Dashboard.exe**, a window will show as **Figure 4-6**. It will describe the detail functions as below.

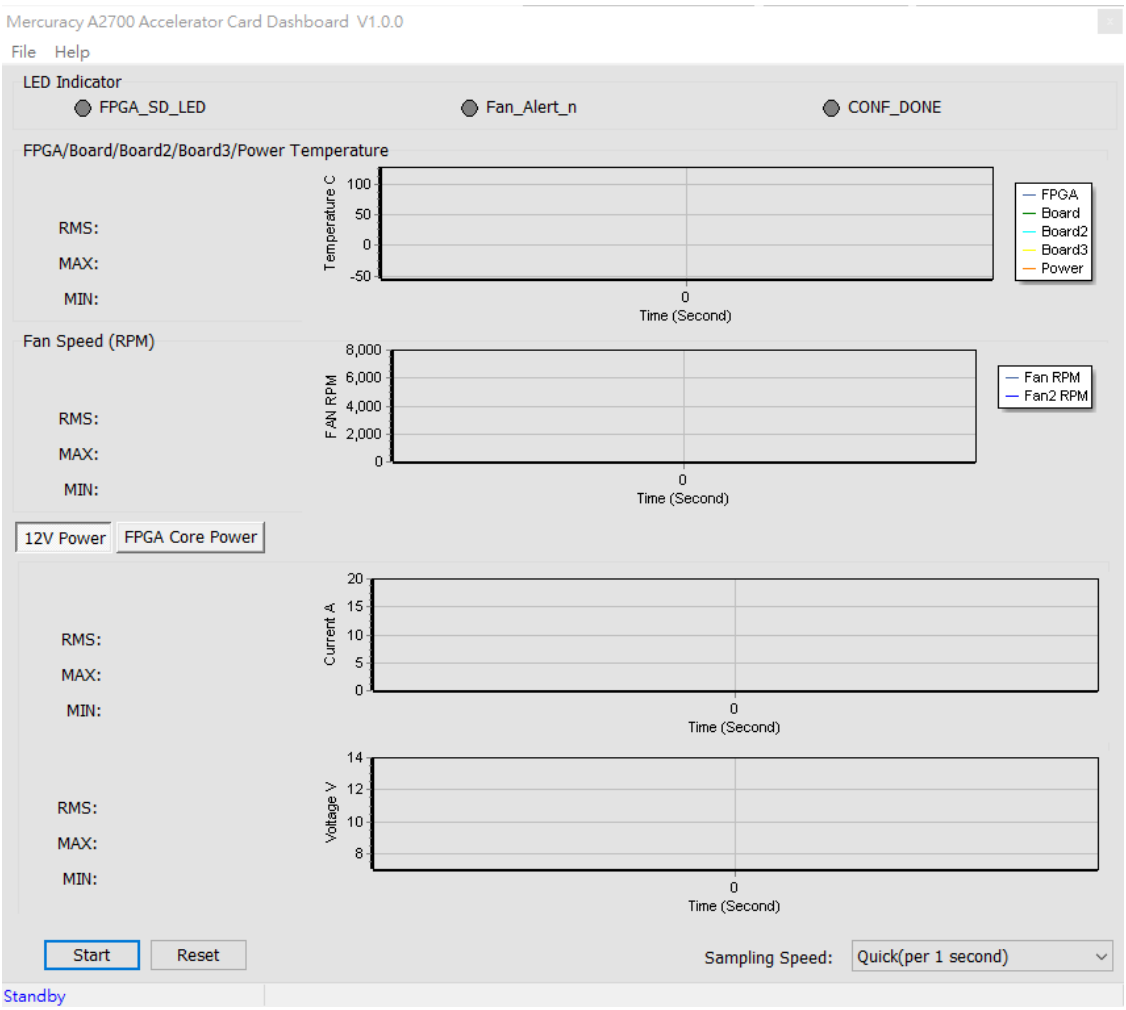


Figure 4-6 Dashboard GUI

■ Dashboard GUI function introduction

- **Start/Stop**: As shown in **Figure 4-7**, there is a Start button at the bottom-left of the GUI window. Click it to run the program (Start will change to Stop), it will show the Mercury A2700 Accelerator Card status. Users can press Stop button to stop the status data transmission and display.
- **Reset Button**: Press this button to clear the historical data shown in GUI, and record the data again.

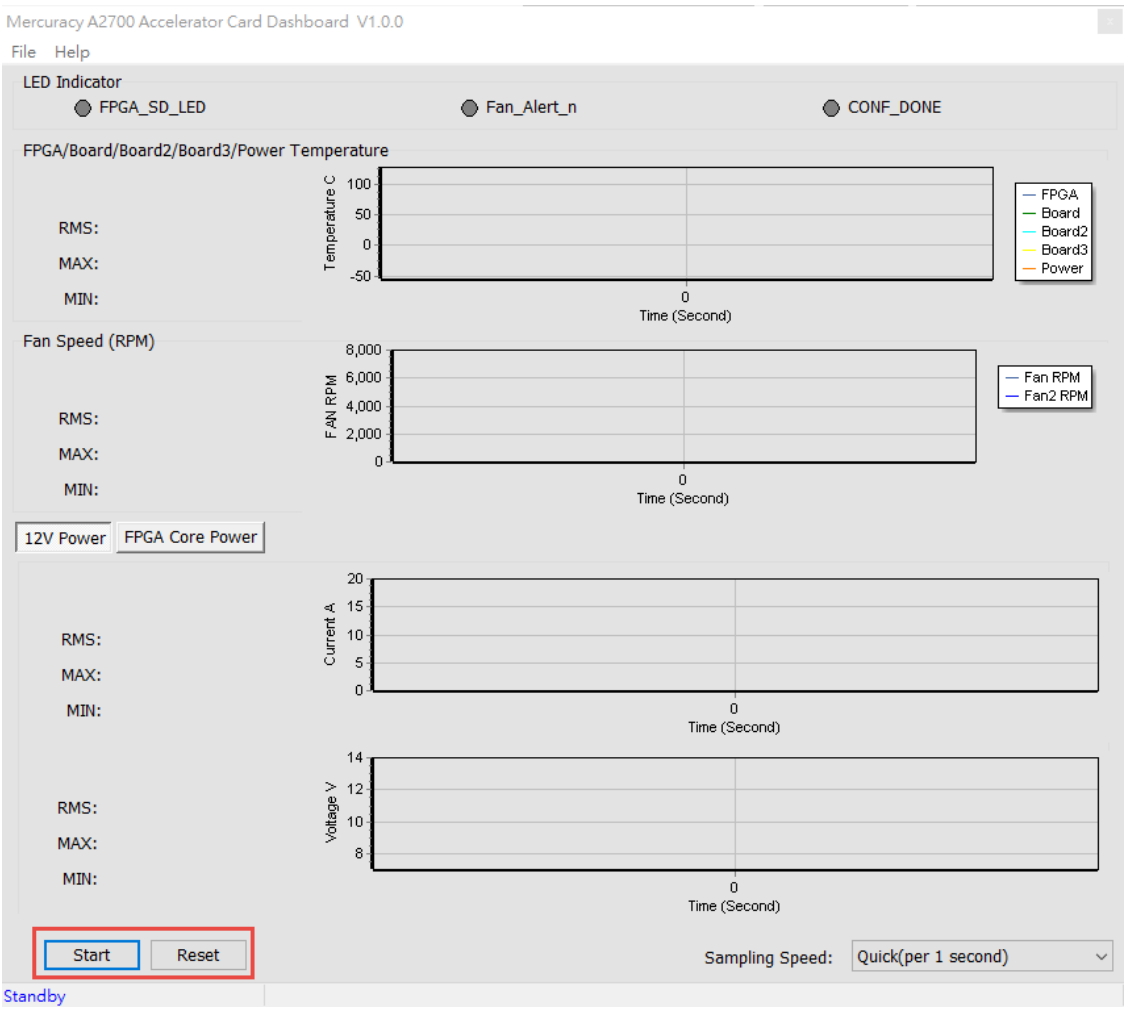


Figure 4-7 Start and Reset button

- **FPGA Status**: As shown in **Figure 4-8**, it will show the status LED number on the Mercury A2700 Accelerator Card. The definitions of these indicator LEDs are as follows:

  - **FPGA_SD_LED**

    When this status is shown in green on the GUI, it means that the FPGA temperature or the board temperature exceeds 95 degrees or the power consumption exceeds 180W. All the power of the FPGA will be cut off.

  - **FPGA_Altert_n**

    When this status is shown in green on the GUI, it means that the fan is abnormal, such as when the fan speed is different from expected

- **CONF_DONE**

  Stands for FPGA configure done status. When this status is shown in green on the GUI, it means that FPGA configuration has been completed.

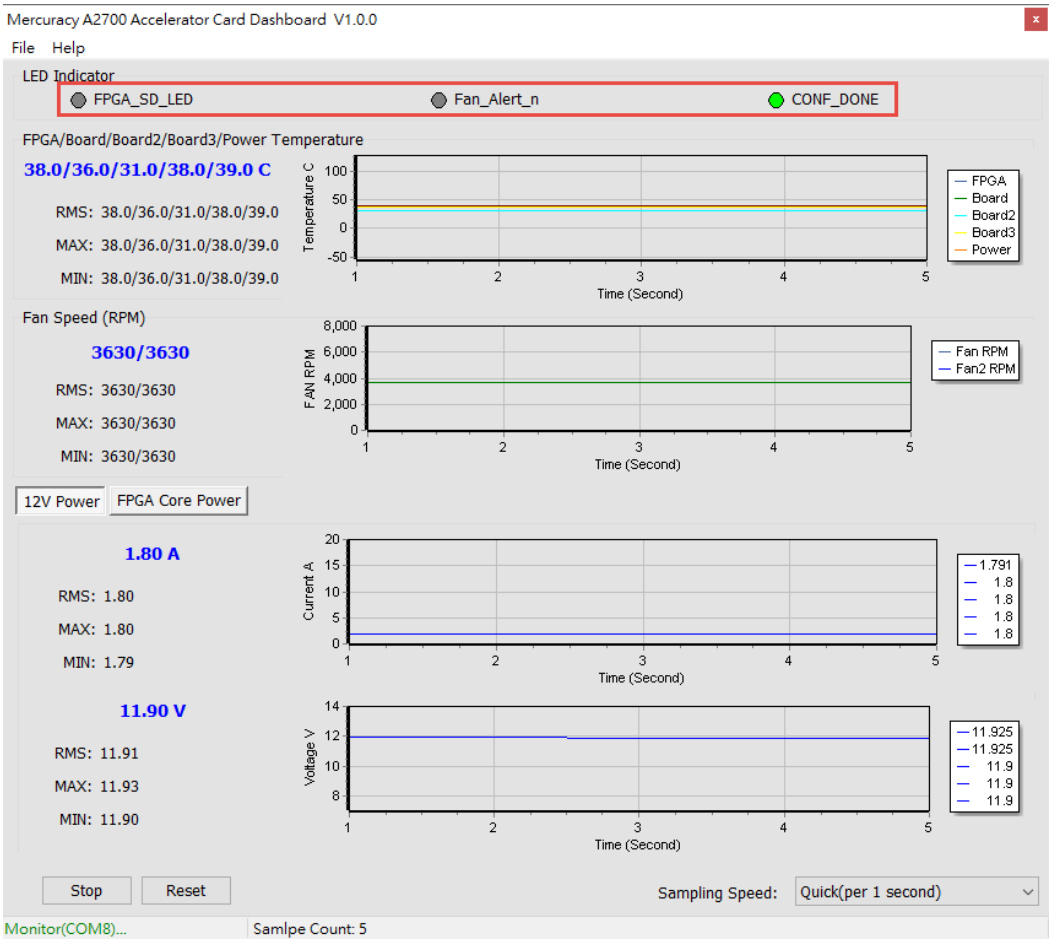


Figure 4-8 FPGA Status section

- **FPGA/Board/Transceiver Temperature**: The Dashboard GUI will real-time show the Mercury A2700 Accelerator Card's ambient temperature (**Board**,**Board2 and Board3** data in the GUI) and FPGA and Power transceiver temperature. Users can get the board's temperature status in time. The information will be refreshed per 1 second, and displays through diagram and number, as shown in **Figure 4-9**. **Figure 4-10** shows the location of the two temperature sensors of **Board** and **Board2** on the GUI.

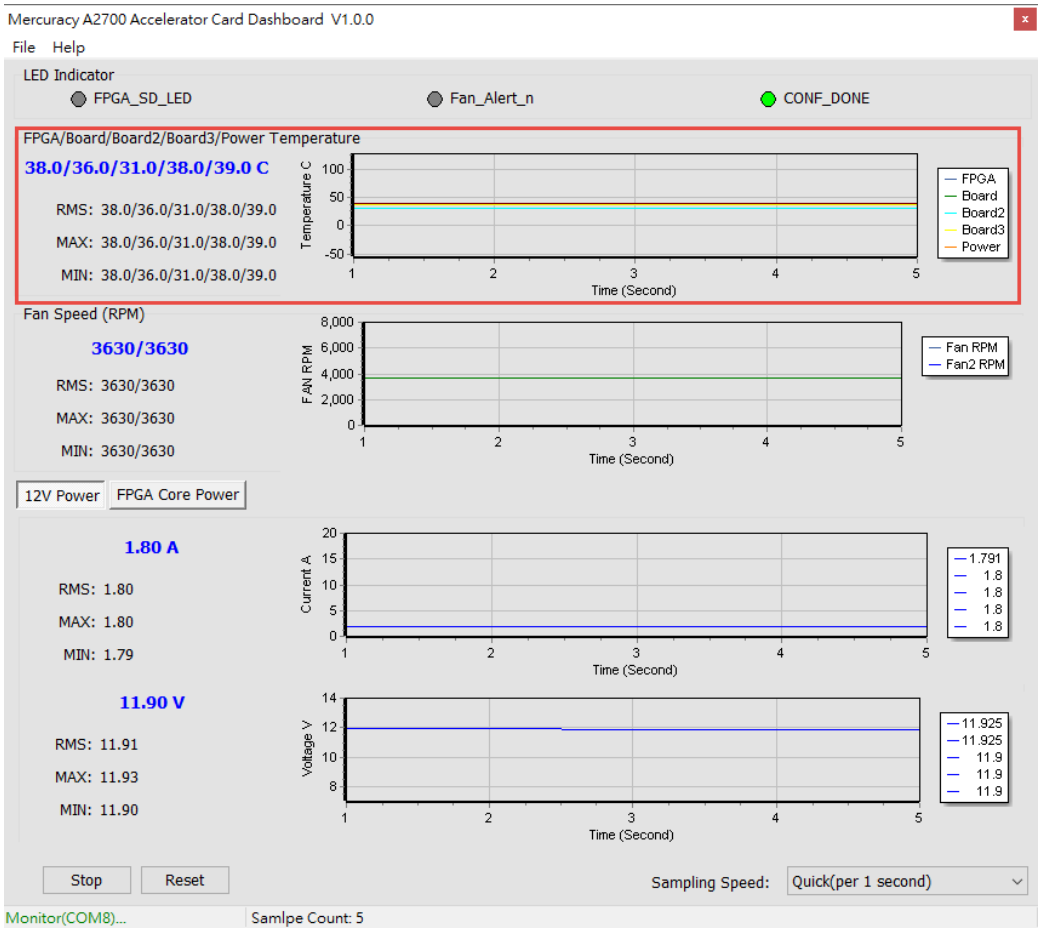


Figure 4-9 Temperature section

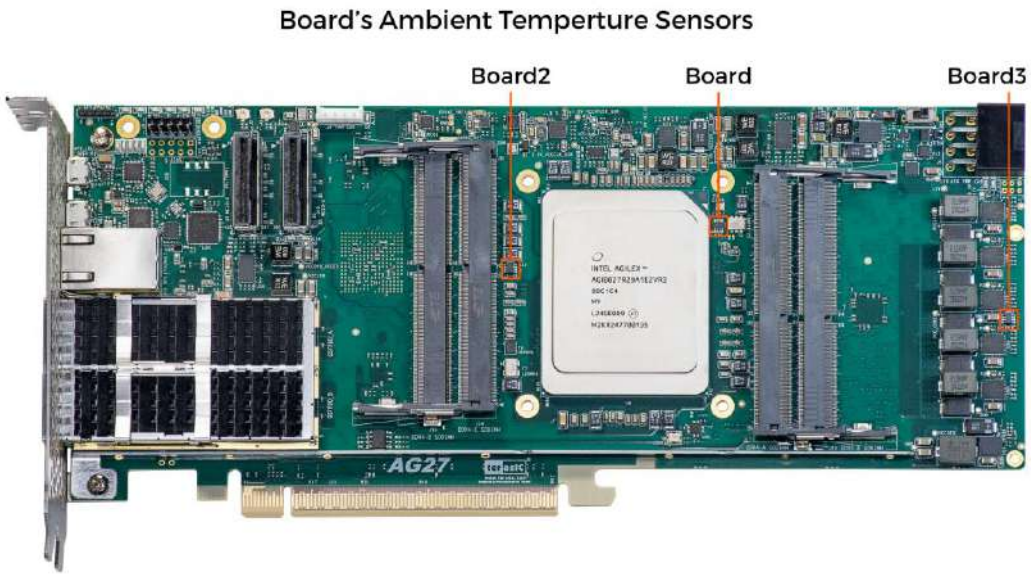


Figure 4-10 Location of the board's ambient temperature

- **Fan RPM**: It displays the real-time speed of the **two** fans (Fan and Fan2 in the GUI) on the Mercury A2700 Accelerator Card, as shown in **Figure 4-11**.

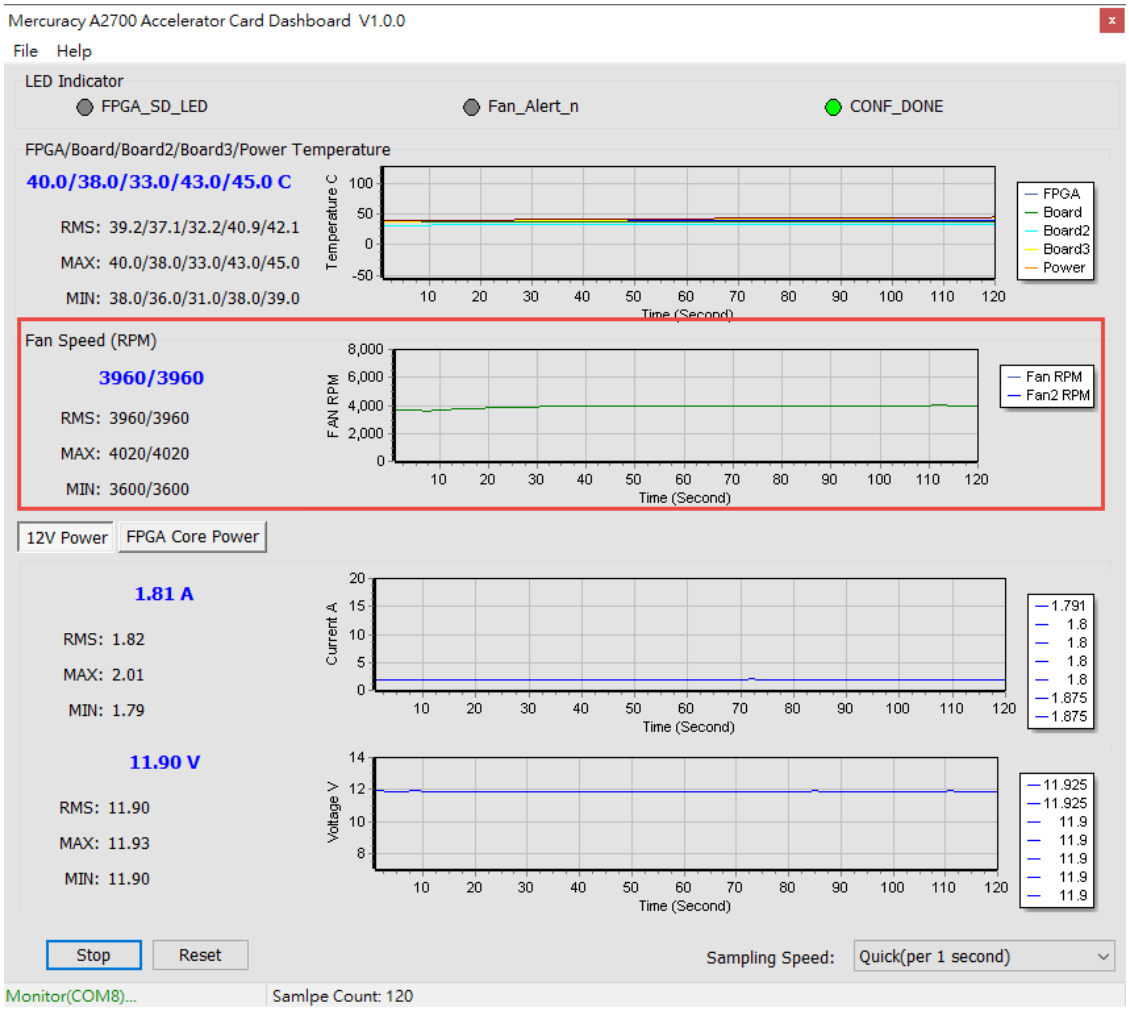


Figure 4-11 FAN RPM section

- **12V/Core Power monitor**: It displays the real-time 12V/Core Power (0.8V~0.85V) voltage and consumption current on the Mercury A2700 Accelerator Card.

  When the user clicks the "**12V Power**" button (See **Figure 4-12**), the GUI will display the voltage level and current number of 12V Power on the board.

  While user clicking the "**FPGA Core Power**" button (See **Figure 4-13**), the GUI will show the voltage level and current value of the FPGA core power on the board.

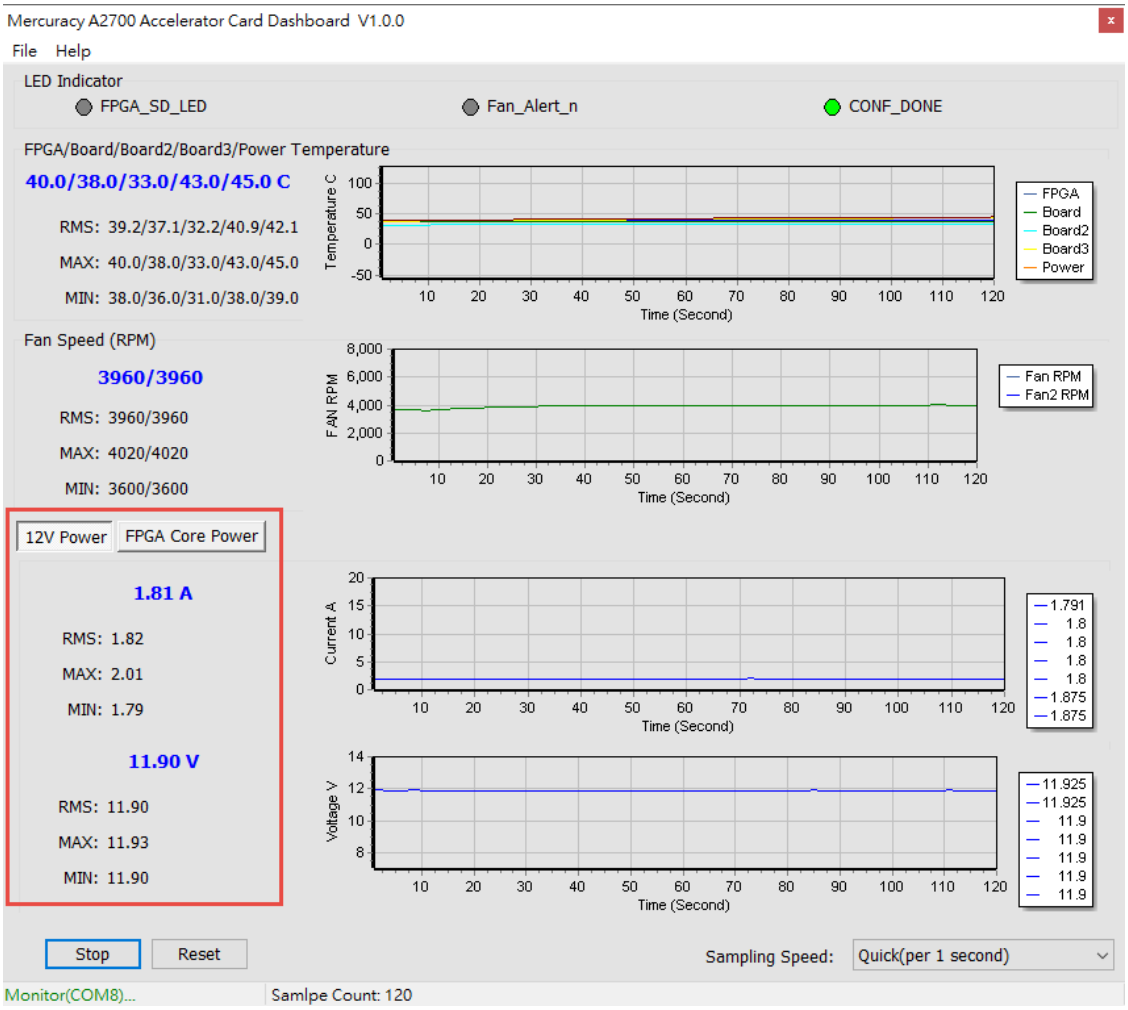


Figure 4-12 Select "12V Power"

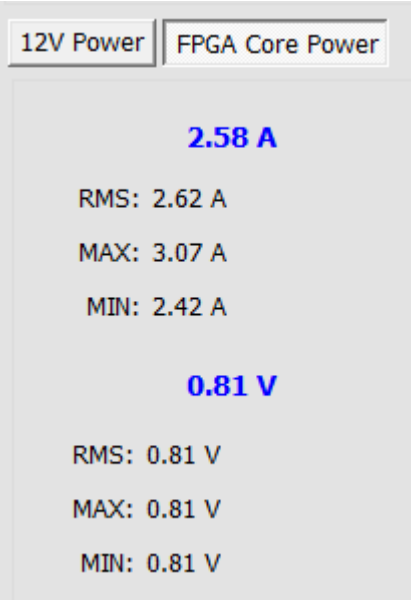


Figure 4-13 Select "FPGA Monitor Section"

- **Sampling Speed**: It can change interval time that the Dashboard GUI sample the board status. Users can adjust it to 1s/10s/1min/Full Speed (0.1s) to sample the board status, as shown in **Figure 4-14** and **Figure 4-15**.

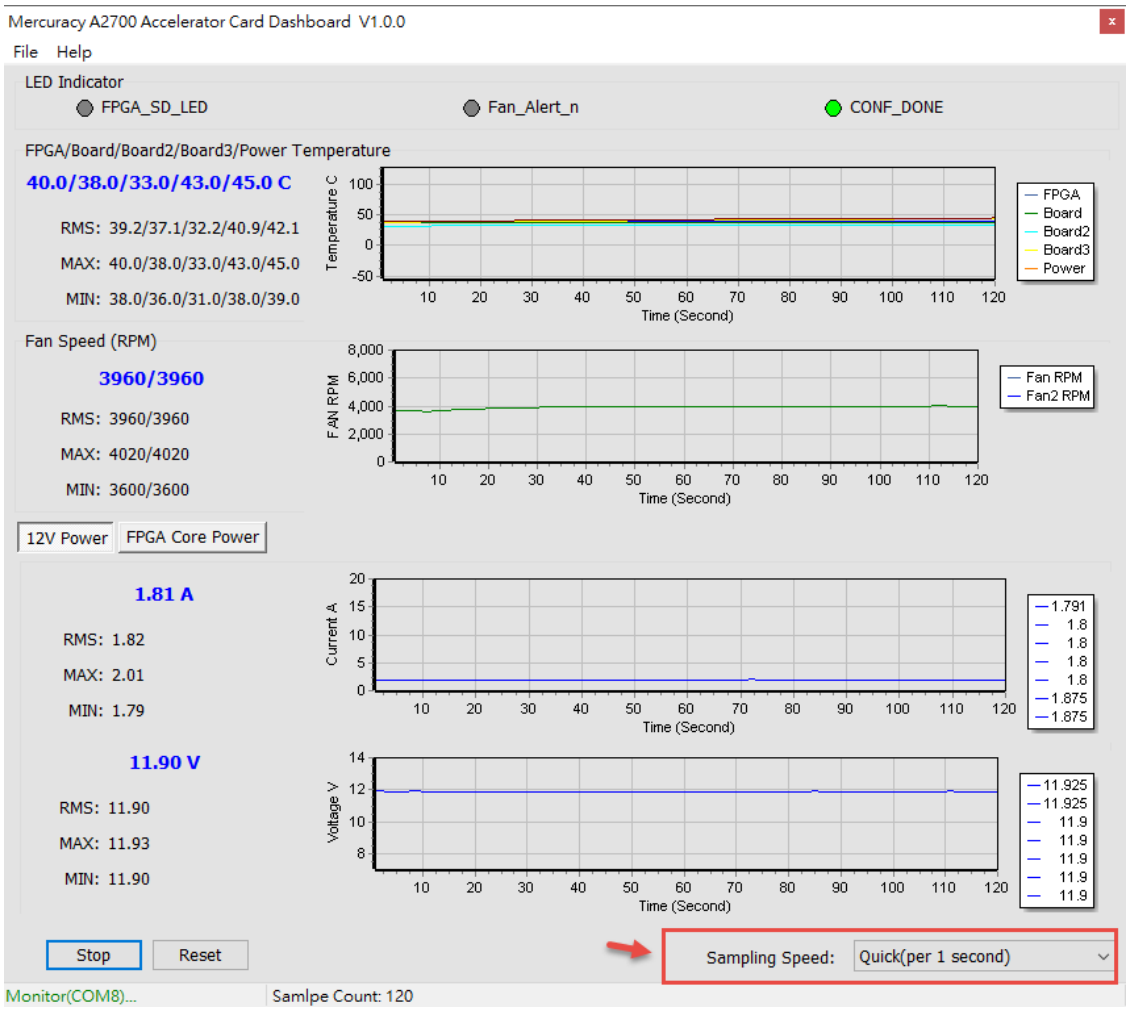


Figure 4-14 Sampling Speed section

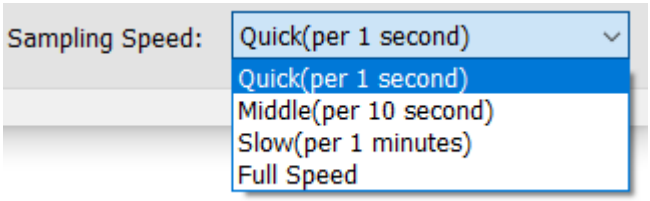


Figure 4-15 Options of Sampling Speed

- **File Manu:** The user can click "**File**" menu at the top left of the GUI (See **Figure 4-16**) and some options such as board information and status export will appear. Note that to active these functions, you will need to **stop** obtaining the board status (i.e. Don't Press "**Start**" button or Press "**Stop**" button) in the GUI. Detailed introductions of these functions are described in below.

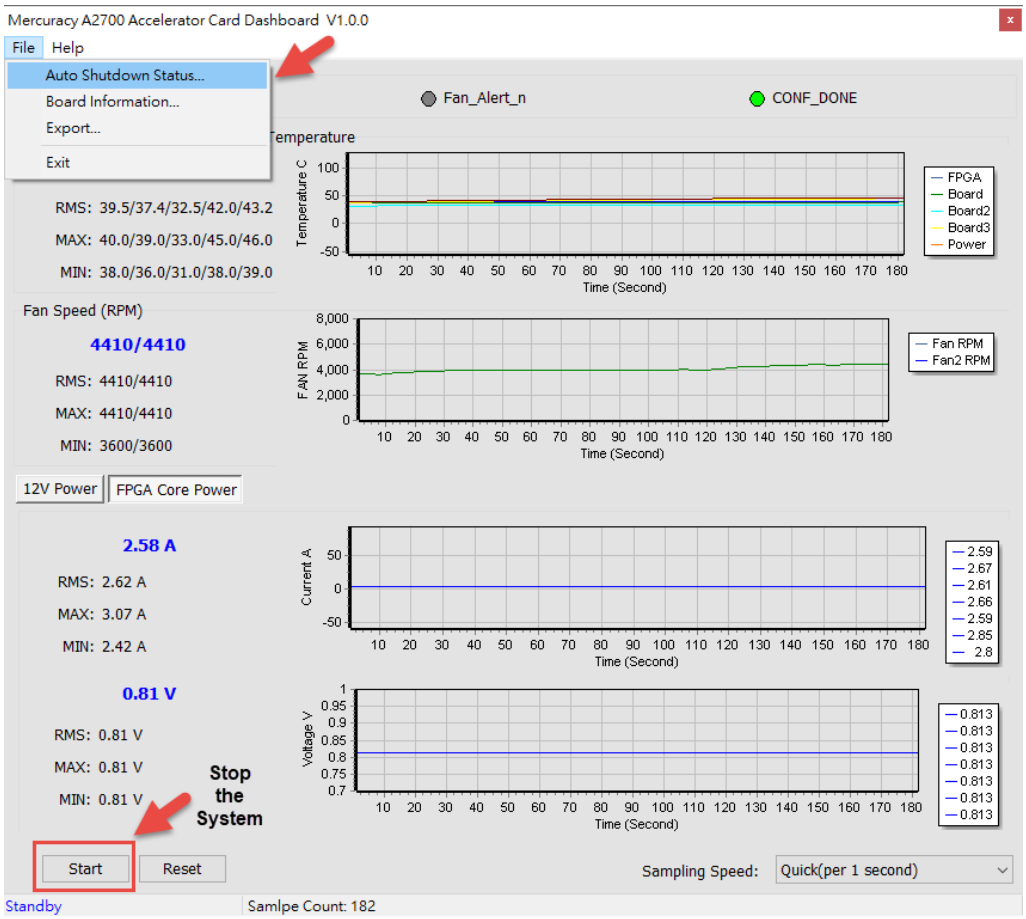


Figure 4-16 File Menu Options

- **Auto Shutdown Status**: This option will report whether the board entered "Auto shutdown status" because the FPGA temperature is too high or the fan speed is abnormal.
- **Board Information**: Click the "Board Information" to get the current MAX 10 FPGA software version and the Mercury A2700 Accelerator Card version, as shown in **Figure 4-17**.

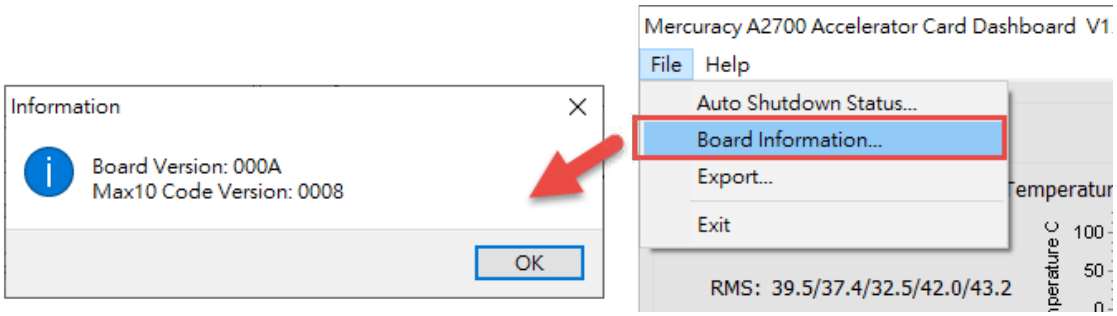


Figure 4-17 Board Information

- **Log File**: Click the Export in the File page to save the board temperature, fan speed and voltage data in .csv format document, as shown in **Figure 4-18** and Figure 4-19.

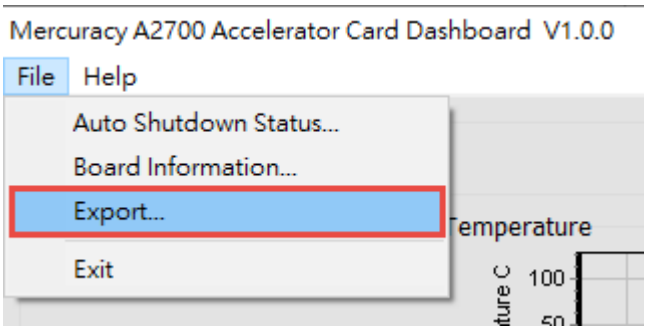


Figure 4-18 Export the log file

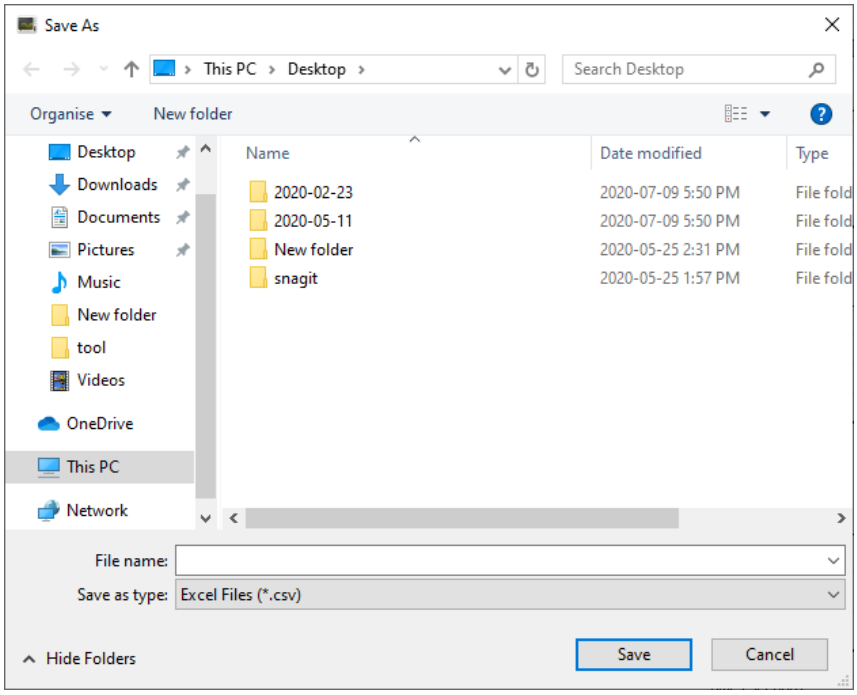


Figure 4-19 Export the log file in .csv format

Chapter 5

Additional Information

5.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

Mercury A2700 Accelerator Card Web: A7SK.terasic.com

■ Revision History

Date	Version	Changes
2023.08	First publication	

■