Low-Power, Low-Jitter, Six-Output Clock Generator for Space Applications

DSA504RT

Introduction

The DSA504RT device is a six-output programmable clock generator engineered for space applications. It features a low-jitter fractional-divide APLL, two downstream fractional dividers with spread-spectrum capability, and two integer dividers. The generated frequencies can be routed to any of the six outputs through an integrated crosspoint switch. In addition, each output buffer includes an internal divider, enabling the finer frequency resolution.

Its triple fractional-divider architecture eliminates traditional integer-N limitations and delivers exceptional flexibility across a wide range of applications, especially those requiring multi-standard operation.

The device uses an external differential or single-ended clock as its reference, allowing all outputs to synchronize with the system's primary clock. Each of the six outputs can be independently configured either as a differential output, such as LPHCSL, LVPECL or LVDS, or as two single-ended CMOS outputs operating at the same frequency. As a result, the DSA504RT device can support up to twelve CMOS outputs at six different frequencies or any combination of differential and single-ended outputs.

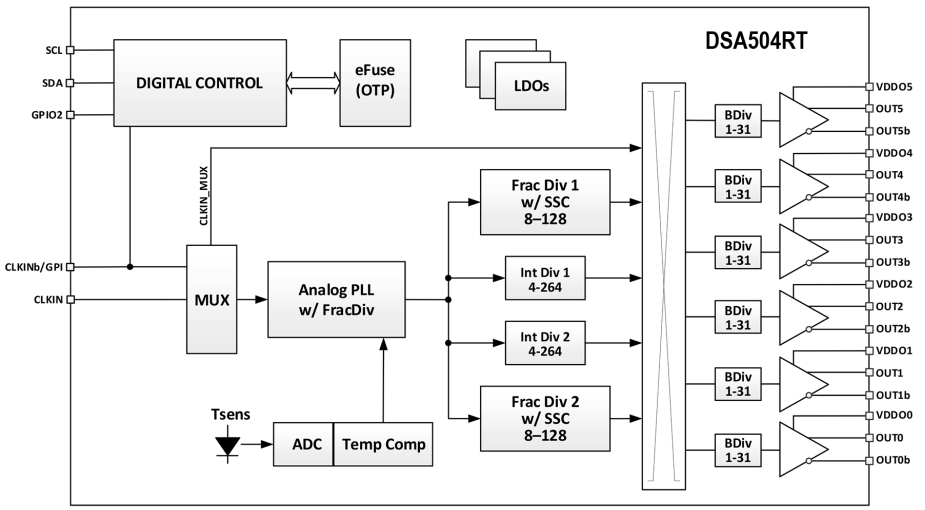
Features

- Six-Output Any Frequency Clock Generators
- Up to 6 Differential Outputs or 12 CMOS Outputs
- External Clock Reference
- External Reference Frequency Range:
  - External Differential Clock: 10 MHz to 250 MHz
  - External LVCMOS Clock: 10 MHz to 200 MHz
- Highly Configurable Outputs with Separate Supply and Independent Format Selection: LPHCSL, LVDS, LVPECL and LVCMOS
- Output Frequency Range:
  - Differential Output:
    - LPHCSL: 0.35 MHz to 250 MHz
    - LVDS, LVPECL: 0.35 MHz to 662 MHz
  - LVCMOS Output: 0.35 MHz to 200 MHz
- Standby Mode for Low Power Consumption when Not in Use
- I^2C Interface
- PCIe Gen1 - Gen 7 Compliant Outputs
- Extended Temperature Range: −55 °C to +125 °C
- Operating Voltage: 1.71V to 3.63V
  - Operating voltage must not exceed 3.30V on VDDOx supply pins (See *Radiation Report* for details)
- Packages
  - VQFN28, 28-lead Very Thin Quad Flat No-Lead, 4 mm × 4 mm body size
  - CQFP32, 32-lead Ceramic Quad Flat Package, 16 mm × 16 mm body size

- ESD
  - HBM: 2000V for VQFN28; TDB for CQFP32
  - CDM: 1000V for VQFN28; TDB for CQFP32
- Radiation performances
  - No Single Event Latch-up below a LET of 78 MeV.cm exposant to set (78 MeV.cm²)/mg at 125 °C
  - TID immunity targeted up to 50 krad (Si) according to ESCC-22900 test method
- Mass
  - VQFN28: 0.043g
  - CQFP32: 5.516g with ceramic tie-bars

Functional Block Diagram

Figure 1. DSA504RT Functional Block Diagram



Notes:

1. IntDiv1 and IntDiv2 can divide the APLL frequency by an integer between 4 and 33, followed by a post-divider of 1, 2, 4, 6 or 8.
2. FracDiv1 and FracDiv2 can divide the APLL frequency by a value between 8 and 128, which contains a programmable fractional part with resolution of up to 36 bits.

Table of Contents

1. Space Quality Grade

For more details about Screening and qualification flows, see Packaged Part for Aerospace and Defense Applications: Screening and Qualification Monitoring.

The hermetic DSA504RT is available in several quality grades, SV is our most stringent grade, compliant with class V/ESCC9000 in terms of screening testing, qualification testing and TCI/QCI specification requirements.

The plastic DSA504RT is also available for HiRel applications.

2. Pin Description

The following figure shows the pin diagram and the table lists the pin names and its functional description.

Figure 2-1. Pin Diagram

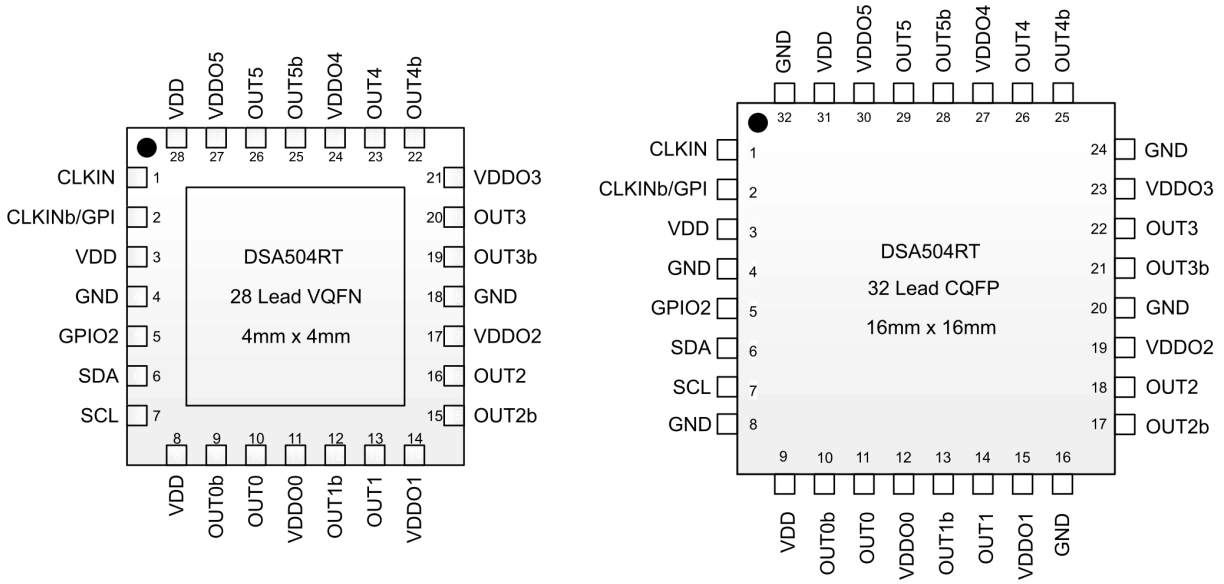


Table 2-1. DSA504RT Pin Description

Pin Number for VQFN Package	Pin Number for CQFP Package	Pin Names	Description
1	1	CLKIN	Differential Clock input/Single-Ended LVCMOS Clock Input.
2	2	CLKINb/GPI	Differential Clock input/General Purpose input. If not used, pull down to GND.
3	3	VDD	VDD pins (3, 8 and 28 for VQFN and 3, 9 and 31 for CQFP) should be connected to the same power supply.
4	4	GND	Ground
5	5	GPIO2	General Purpose Input/Output. This pin has an programmable internal (~100 kΩ) pull-up.
6	6	SDA	I^2C Data. This pin has a programmable internal (~100 kΩ) pull-up.
7	7	SCL	I^2C Clock. This pin has a programmable internal (~100 kΩ) pull-up.
—	8	GND	Ground
8	9	VDD	VDD for the digital block. VDD pins (3, 8 and 28 for VQFN and 3, 9 and 31 for CQFP) should be connected to the same power supply.
9	10	OUT0b	Complementary Output 0. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
10	11	OUT0	True Output 0. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.

Table 2-1. DSA504RT Pin Description (continued)

Pin Number for VQFN Package	Pin Number for CQFP Package	Pin Names	Description
11	12	VDDO0	VDD for OUT0/OUT0b
12	13	OUT1b	Complementary Output 1. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
13	14	OUT1	True Output 1. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
14	15	VDDO1	VDD for OUT1/OUT1b
—	16	GND	Ground
15	17	OUT2b	Complementary Output 2. Output logic can be selected to be differential (LHCSL, LVDS and LVPECL) or single-ended LVCMOS.
16	18	OUT2	True Output 1. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
17	19	VDDO2	VDD for OUT2/OUT2b
18	20	GND	Ground
19	21	OUT3b	Complementary Output 3. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
20	22	OUT3	True Output 3. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
21	23	VDDO3	VDD for OUT3/OUT3b
—	24	GND	Ground
22	25	OUT4b	Complementary Output 4. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
23	26	OUT4	True Output 4. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
24	27	VDDO4	VDD for OUT4/OUT4b
25	28	OUT5b	Complementary Output 5. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
26	29	OUT5	True Output 5. Output logic can be selected to be differential (LPHCSL, LVDS and LVPECL) or single-ended LVCMOS.
27	30	VDDO5	VDD for OUT5/OUT5b
28	31	VDD	VDD for the core. VDD pins (3, 8 and 28 for VQFN and 3, 9 and 31 for CQFP) should be connected to the same power supply.
—	32	GND	Ground
29	—	EPAD/Tie-bar	Ground

3. Functional Description

DSA504RT is high performance, low jitter, six-output programmable clock generators that make each device a good oscillator-clock-generator-fanout-buffer combination replacement in many applications.

The internal high-performance PLL locks to an external reference clock signal. While using the external reference clock, this device can simultaneously be used as a fanout buffer for the external reference clock. Thus, it offers clock generator and clock buffer function combinations. In the buffer configuration, the external clock is routed directly from the input to the crossbar at the output.

DSA504RT can accept an external differential clock up to 250 MHz and a single-ended LVCMOS up to 200 MHz. It combines excellent jitter and stability performance with very low power consumption over a wide range of supply voltages and temperatures.

With its high performance PLL and wide range VCO, followed by two integer dividers, two fractional dividers, and a crossbar, each device can synthesize frequencies up to 662 MHz (LVPECL and LVDS outputs), up to 250 MHz (LPHCSL output), up to 200 MHz (LVCMOS output), and provide any frequency in the specified range on any output. Furthermore, each output buffer integrates a back-end integer divider for more frequency flexibility. Each output buffer has a dedicated power pin with an internal LDO to provide separate output level selection and minimize crosstalk between outputs.

DSA504RT includes functional safety features required by some applications and have spread spectrum capability for better EMI control. They also feature GPIO pins and an I^2C serial interface. Each GPIO pin can be configured to perform a specific function according to Table 3-1. The I^2C interface can be used to read back or modify user registers, reboot the part to reset it to its factory settings, and clear any functional safety flags.

Custom configurations can be created using Microchip's Timing GUI software available on the corresponding products' web pages.

Microchip can program the device OTP memory with the required configuration and provide the user with custom-programmed parts (see the Product Identification System section). Such custom-programmed parts will come up with the required settings on every power-up. Additionally, the device's OTP memory can be programmed using the OTP programmer tools provided in the DSA504RT evaluation kits.

3.1. Startup

Once core VDD (Pins 3, 8, and 28) supply voltages are applied, the device starts the initialization phase which ends by uploading the content of the OTP non-volatile memory into shadow registers. The chip will typically start 3ms after the power supply is applied. For minimal start delay, apply core VDD and VDDOx at the same time. If VDDOx are applied before the core VDD, the outputs are kept disabled until a stable clock is available at the crossbar output. The off state of the outputs can be selected to be Hi-Z or Low-High. VDDOx should not be delayed for more than 1.5ms than the core VDD to ensure the buffers are synchronized.

3.2. Input Reference Selection

The PLL reference clock of DSA504RT always uses an external clock source. This configuration is set by default in OTP during the factory programming. The sel_refclk field is set in the configuration register at address 86.

3.3. Input Reference Interface

By default, clock inputs (CLKIN/CLKINb) accept differential HCSL signals and can be programmed to accept single-ended LVCMOS at CLKIN (Pin 1) while CLKINb (Pin 2) becomes a GPI (General Purpose Input). The diagrams in Figure 3-1 through Figure 3-5 show how to interface the device input to LPHCSL, HCSL, LVCMOS, LVDS and LVPECL outputs respectively.

Figure 3-1. Interfacing Clock Input with LPHCSL Driver

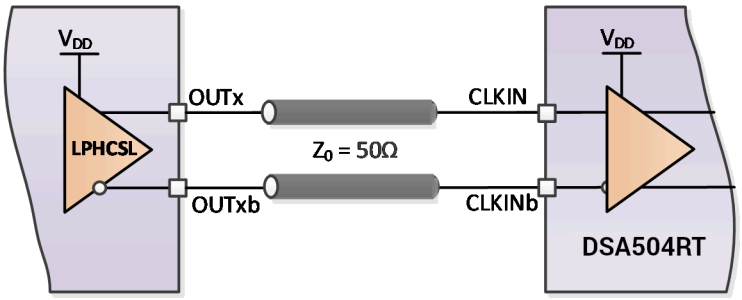


Figure 3-2. Interfacing Clock Input with HCSL Driver

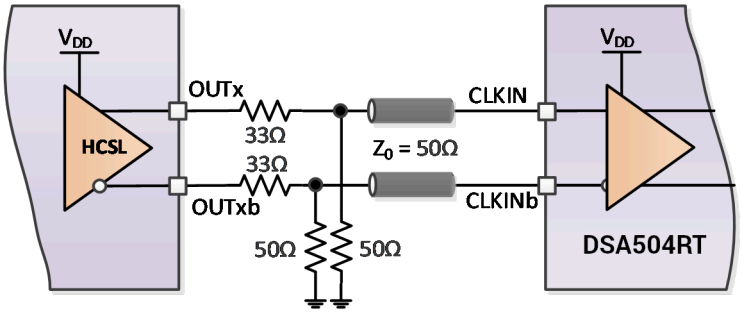


Figure 3-3. Interfacing Clock Input with LVCMOS Driver

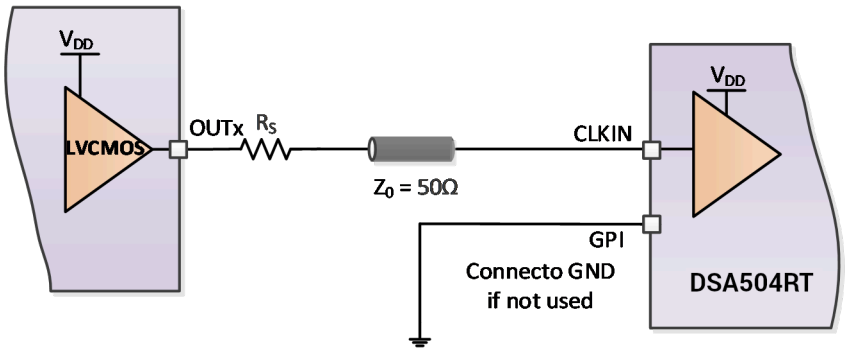


Figure 3-4. Interfacing Clock Input with LVDS Driver

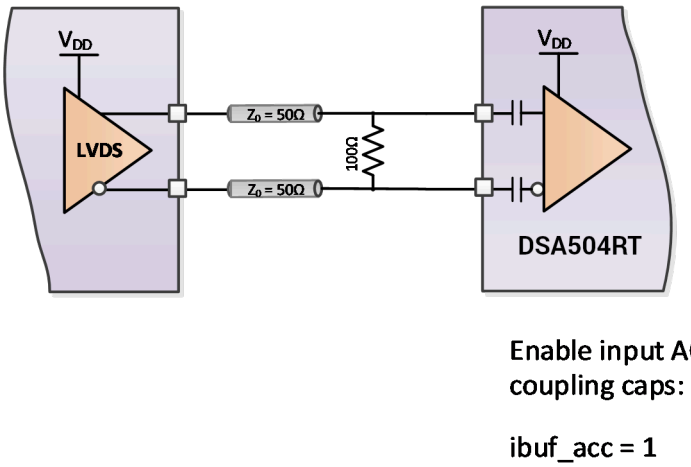
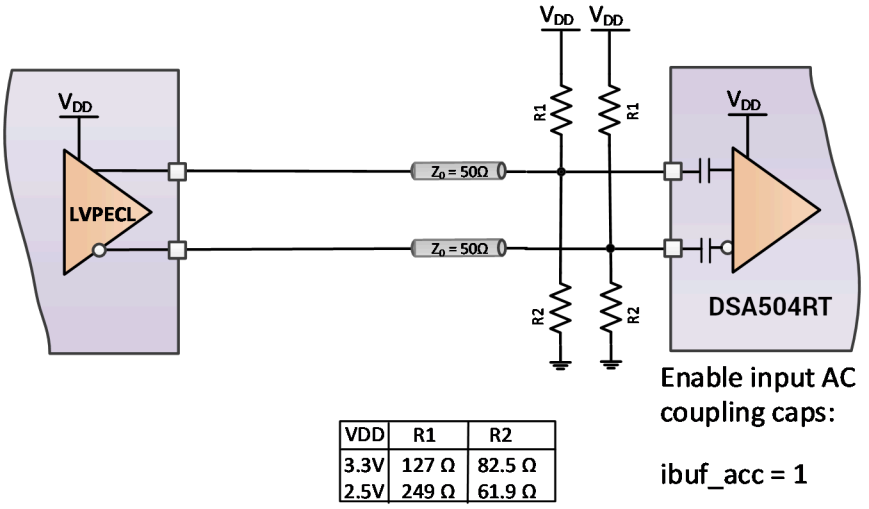


Figure 3-5. Interfacing Clock Input with LVPECL Driver



VDD	R1	R2
3.3V	127 Ω	82.5 Ω
2.5V	249 Ω	61.9 Ω

3.4. Outputs Enable Control

In addition to output control via I²C, each GPIO pin can be programmed to be OEx (Output Enable) for one or for a group of outputs (see Table 3-1). OEx is active high and the output is enabled/disabled synchronously to offer glitch-free transitions. As shown in the figures below, after the change in the logic level of the OEx, the output enable/disable will occur after two to four output clock cycles. The user can enable (default) or disable any output independently through the I²C interface by setting the corresponding **obufx_en** register or using dedicated GPIO (see Table 3-1).

Figure 3-6. OEx Assertion (Output Enable) Timing Diagram

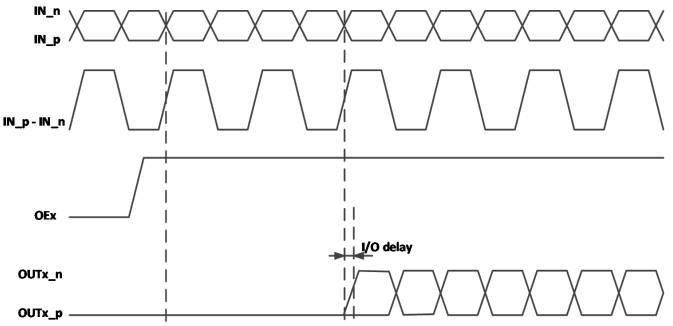
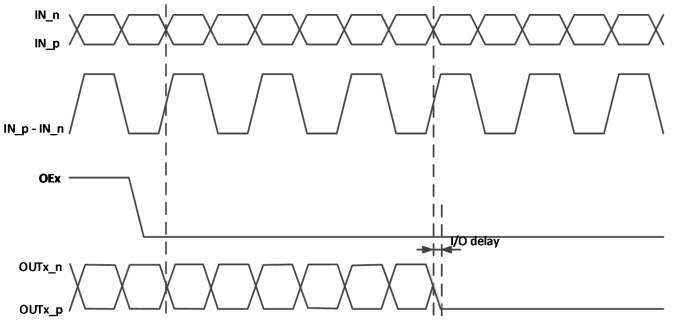


Figure 3-7. OEx Deassertion (Output Disable) Timing Diagram



3.5. Outputs Type Control

Each of the six output buffers is powered through a dedicated pin and an internal LDO. Separate output buffers' voltage supplies provide less crosstalk between outputs and, therefore, offer better jitter performance and more flexibility in interfacing the outputs. The output format is set independently for each output to be differential (LVPECL, LVDS, or LPHCSL) or single-ended LVCMOS to offer up to six differential outputs or up to 12 LVCMOS outputs.

3.6. Output LVCMOS Polarity

When LVCMOS format is selected, each pair of CMOS signals generated from the same output buffer can be programmed to be in phase or be complementary. The polarity of each of the two outputs can be independently modified through the I^2C serial interface, and each of the outputs can be independently turned off to save power in case that particular one is not used.

3.7. Output Frequency Selection

The desired output frequencies must be entered in the GUI software during part creation and then the algorithm calculates the appropriate parameters (PLL feedback ratio, VCO frequency, and dividers ratios). The output frequencies can also be selected from pre-stored frequency plan A, frequency plan B, or from both (combination).

3.8. Output Termination

Figure 3-8. LVDS Output Termination

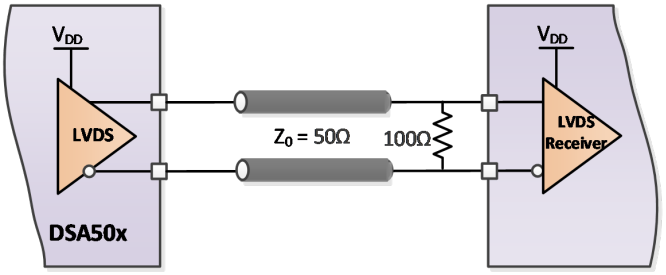


Figure 3-9. LPHCSL Output Termination

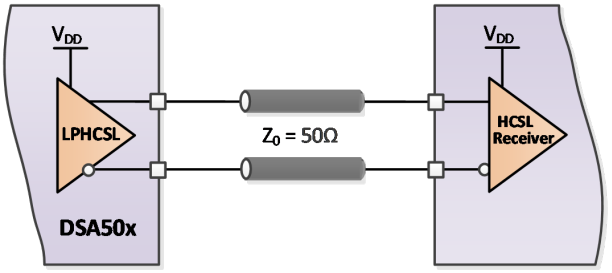
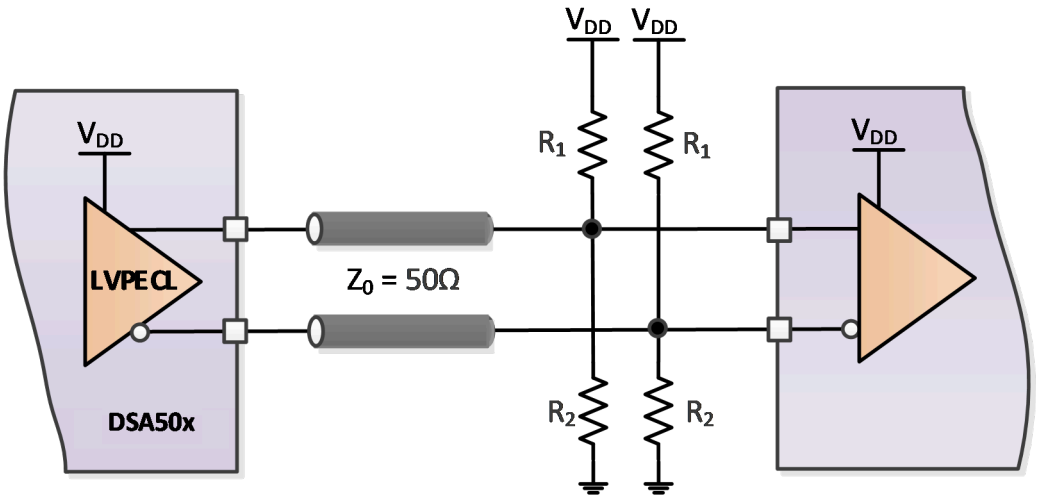
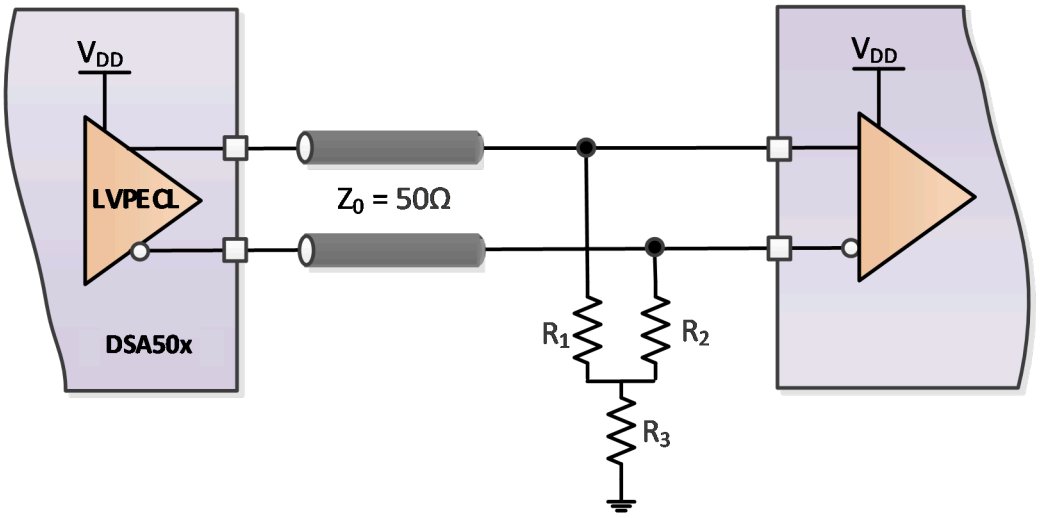


Figure 3-10. LVPECL Output Termination (Option 1)



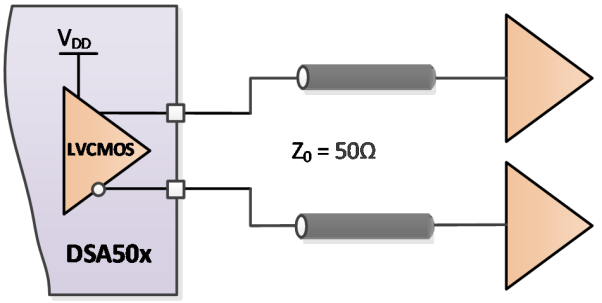
VDD	R1	R2
3.3V	127 Ω	82.5 Ω
2.5V	249 Ω	61.9 Ω

Figure 3-11. LVPECL Output Termination (Option 2)



VDD	R1, R2	R3
3.3V	50 Ω	50 Ω
2.5V	50 Ω	0 Ω

Figure 3-12. LVCMOS Output Termination



3.9. Spread Spectrum Clocking

To offer flexibility in controlling EMI interference, a Spread Spectrum Clocking (SSC) feature is incorporated in the two fractional dividers by modulating their output clock. The spread level range is ±2.5% for center spread and 0% to –2.5% for down spread with 0.1% resolution. The level of spread for each fractional divider can be set during production or post-production by using dedicated GPIO (see Table 3-1) or through I^2C serial interface by setting register fields **enss** and **dwnen** for the fractional dividers.

3.10. Low Power Standby Mode

The device features a standby mode that lowers power consumption. The standby mode can be activated by using a dedicated GPIO.

3.11. General Purpose IO

Depending on the external clock input configuration, either differential or single-ended, DSA504RT supports up to 2 pins that can be configured as GPIOs (General Purpose Input/Output) and be

programmed at register field **sel_gpiox_func** to perform a specific function as described in the following table.

Table 3-1. GPIO Pin Function

Selection 0-31 (5 bits)	Function	Direction	Function Description	Comment
0	OFF	Input	No GPIO Function	GPIO function OFF
1	OE0	Input	OE OUT0	L=OFF, H=ON (default) (Note 3)
2	OE1	Input	OE OUT1	L=OFF, H=ON (default) (Note 3)
3	OE2	Input	OE OUT2	L=OFF, H=ON (default) (Note 3)
4	OE3	Input	OE OUT3	L=OFF, H=ON (default) (Note 3)
5	OE4	Input	OE OUT4	L=OFF, H=ON (default) (Note 3)
6	OE5	Input	OE OUT5	L=OFF, H=ON (default) (Note 3)
7	OE0-5	Input	OE OUT0-5	L=OFF, H=ON (default) (Note 3)
8	OE0-2	Input	OE OUT0-2	L=OFF, H=ON (default) (Note 3)
9	OE3-5	Input	OUT3-5	L=OFF, H=ON (default) (Note 3)
10	FS0 (Note 1)	Input	Frequency Select using back-end dividers (BEDx).	6-bit register SEL_GPIO_FS0_BED with LSB (bit 0) associated with BED0 and MSB (bit 5) associated with BED5: If bit = 0: associated frequency plan A BED selected (default) If bit = 1: associated frequency plan B BED selected Example: SEL_BANK_BED = 010110 corresponds to: OUT0 = A0, OUT1 = B1, OUT2 = A2, OUT3 = B3, OUT4 = B4, OUT5 = A5
11	FS1 (Note 1)	Input	Frequency Select Frequency Plan A or B: APLL LC-VCO, APLL FB, FracDiv1-2, IntDiv1-2, MUX0-5, BEDiv0-5	L=Frequency Plan A at OUT0-5 H=Frequency Plan B at OUT0-5
12	SS0	Input	Spread Spectrum FD1	SS0=L=OFF (default) SS0=H=ON (Note 4)
13	SS1	Input	Spread Spectrum FD2	SS1=L=OFF (default) SS1=H=ON (Note 4)
14	SS2	Input	Spread Spectrum FD1 & FD2	SS2=L=OFF (default) SS2=H=ON (Note 4)
15	SS3	Input	Spread Spectrum Multiplier FD1 & FD2	SS3=L=1x (default) SS3=H=2x (Note 4)

Table 3-1. GPIO Pin Function (continued)

Selection 0-31 (5 bits)	Function	Direction	Function Description	Comment
16	SEL (Note 1)	Input	Reference Clock Select	Not available on DSA504RT, as it does not include an internal MO.
17	FAULT0	Output	PLL_LOL (PLL Loss of Lock)	FAULT0=L=PLL locked FAULT0=H=PLL out of lock 1 OTP bit is reserved to select if PLL_LOL and PLL_LOS will squelch the buffer's outputs or no.
18	FAULT1	Output	PLL_LOS (PLL Loss of Source)	FAULT1=L External clock present and monitored. FAULT1=H LOS of external clock 1 OTP bit is reserved to select if PLL_LOL and PLL_LOS will squelch the buffer's outputs or no.
19	FAULT2	Output	Temperature Sensor is out of range. Programmed ADC range –55 °C to +115 °C	FAULT2=L=Temperature within range FAULT2=H=Temperature out of range
20	FAULT5	Output	OTP Checksum failure (not part of Poly, custom RTL code needed)	FAULT5=L=No failure FAULT5=H=Failure Applies to the customer configuration. This fault generates a flag, but does not stop the part.
...				
28	SYNC (Note 1)	Input	Synchronize BED in same Frequency Plan	Synchronizes BED on 0->1 edge trigger
...				
30	STDBY_b (Note 1)	Input	Low power standby mode	L: OPERATE to STDBY H: Go to OPERATE, Stay in OPERATE
31	CHIPID (Note 2)	Input	Controlling LSB in I^2C Client Address	L={CHIPID[6:1],0} or {CHIPID[9:1],0} H={CHIPID[6:1],1} or {CHIPID[9:1],1}

Notes:

1. These GPIOs have to be toggled one at a time with at least 10ms in between.
2. Should not be toggled after power-up.
3. The device only supports one GPIO controlling output enable for each of OUT0-OUT5. This makes, for example, decode 7 mutually exclusive with decodes 1-6 and decode 8 mutually exclusive with decodes 1-3 and 7.
4. The device only supports one GPIO controlling spread spectrum for each fractional divider. This makes, for example, decode 14 mutually exclusive with decodes 12, 13, and 15.

4. Host Interface

This section describes about I²C interface available for DSA504RT device.

4.1. I²C Serial Interface

DSA504RT has I²C interface. The I²C interface is compatible with NXP UM10204 specifications for standard (100kHz) and fast (400kHz) modes. During part creation in the GUI software, the customer can select the default device I²C address provided by the GUI or can choose another client address that's not reserved according to Table 4-1. DSA504RT supports 7-bit addressing and 10-bit addressing.

To solve the issue of conflict of address between two devices placed on the same I²C bus, a GPIO can be used as the LSB (least significant bit) in the device I²C client address so the user can use that bit to distinguish between the two devices addresses by setting it to Low (0) or High (1).

Table 4-1. Reserved Addresses

Client Address	R/W Bit	Description
0000_000	0	General call address (Note 1)
0000_000	1	Start byte (Note 2)
0000_001	X	CBUS address (Note 3)
0000_010	X	Reserved for different bus format (Note 4)
0000_011	X	Reserved for future purposes
0000_1XX	X	HS-mode host code
1111_1XX	X	Reserved for future purposes
1111_0XX	X	10-bit client addressing

Notes:

1. DSA504RT does not support general calls.
2. No device is allowed to acknowledge at the reception of START byte.
3. Reserved to enable inter-mixing of CBUS compatible and I²C-compatible devices in the same system.
4. Reserved to enable I²C compatible buses with different format to be mixed with I²C.

4.2. I²C Byte Format

The 7-bit and 10-bit Chip ID and address structures are shown in Table 4-2 and Table 4-3. The data byte that follows is sent MSB first, multi-byte transmissions are sent from lower byte to upper byte. CHIPID is a 10-bit OTP register field and acts as *Client Address* (Call Address and CBUS Address are not supported).

Table 4-2. I²C 7-bit CHIPID First 3 Byte Call Structure

Byte	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	CHIPID[6]	CHIPID[5]	CHIPID[4]	CHIPID[3]	CHIPID[2]	CHIPID[1]	CHIPID[0]	0 or 1
2	ADDR[9]	ADDR[8]	ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]
3	ADDR[1]	ADDR[0]	0	0	0	0	0	0

Table 4-3. I²C 10-bit CHIPID First 4 Byte Call Structure

Byte	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	1	1	1	1	0	CHIPID[9]	CHIPID[8]	0 or 1
2	CHIPID[7]	CHIPID[6]	CHIPID[5]	CHIPID[4]	CHIPID[3]	CHIPID[2]	CHIPID[1]	CHIPID[0]
3	ADDR[9]	ADDR[8]	ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]
4	ADDR[1]	ADDR[0]	0	0	0	0	0	0

4.3. I²C Read Write Protocol

This section describes 7-bit and 10-bit operation protocols. The legend is shown below:

- S = Start Condition
- P = Stop Condition
- Sr = Repeated Start Condition
- 0 = Write Condition
- 1 = Read Condition
- A = Acknowledge
- N = Not Acknowledge

7-bit I²C Single Read

S	Clt Addr [6:0]	0	A	Reg Addr #1	A	Reg Addr #2	A	Sr	Clt Addr [6:0]	1	A	Data	N	P

7-bit I²C Burst Read

S	Clt Addr [6:0]	0	A	Reg Addr #1	A	Reg Addr #2	A	Sr	Clt Addr [6:0]	1	A	Data	A	Data	N	P

7-bit I²C Single Write

S	Clt Addr [6:0]	0	A	Reg Addr #1	A	Reg Addr #2	A	Data	A	P

7-bit I²C Burst Write

S	Clt Addr [6:0]	0	A	Reg Addr #1	A	Reg Addr #2	A	Data	A	Data	A	P

10-bit I²C Single Read

S	Clt Addr #1 [9:0]	0	A	Clt Addr #2 [9:0]	A	Reg Addr #1	A	Reg Addr #2	A	Sr	Clt Addr #1 [9:0]	1	A	Data	A	P

10-bit I²C Burst Read

S	Clt Addr #1 [9:0]	0	A	Clt Addr #2 [9:0]	A	Reg Addr #1	A	Reg Addr #2	A	Sr	Clt Addr #1 [9:0]	1	A	Data	A	Data	A	P

10-bit I²C Single Write

S	Clt Addr #1 [9:0]	0	A	Clt Addr #2 [9:0]	A	Reg Addr #1	A	Reg Addr #2	A	Data	A	P

10-bit I²C Burst Write

S	Clt Addr #1 [9:0]	0	A	Clt Addr #2 [9:0]	A	Reg Addr #1	A	Reg Addr #2	A	Data	A	Data	A	P

5. Register Map

Addresses labeled "Reserved" should not be written by the user.

When using the Microchip Timing GUI software to configure the device, registers that are not changed by user inputs will take the default values listed in the following tables.

Address	Name	Default	Type
0x0000:0x004A	Reserved	—	—
0x004F:0x0050	config_0x4F_50	0x0000	R/W
0x0051	config_0x51	0x00	R/W
0x0052	config_0x52	0x00	R/W
0x0053	config_0x53	0x00	R/W
0x0054	config_0x54	0x00	R/W
0x0055	config_0x55	0x00	R/W
0x0056	config_0x56	0x0C	R/W
0x0057	lpflt_ctl_b	0x3F	R/W
0x0058	config_0x58	0x81	R/W
0x0059	config_0x59	0x5D	R/W
0x005A	config_0x5A	0x4A	R/W
0x005B	config_0x5B	0x20	R/W
0x005C	config_0x5C	0xAA	R/W
0x005D:0x005E	output0_config0	0x0200	R/W
0x005F:0x0060	output0_config1	0xDA00	R/W
0x0061	output0_config2	0x03	R/W
0x0062	output0_config3	0x00	R/W
0x0063:0x0064	output1_config0	0x0200	R/W
0x0065:0x0066	output1_config1	0xDA00	R/W
0x0067	output1_config2	0x03	R/W
0x0068	output1_config3	0x00	R/W
0x0069:0x006A	output2_config0	0x0200	R/W
0x006B:0x006C	output2_config1	0xDA00	R/W
0x006D	output2_config2	0x03	R/W
0x006E	output2_config3	0x00	R/W
0x006F:0x0070	output3_config0	0x0200	R/W
0x0071:0x0072	output3_config1	0xDA00	R/W
0x0073	output3_config2	0x03	R/W
0x0074	output3_config3	0x00	R/W
0x0075:0x0076	output4_config0	0x0200	R/W
0x0077:0x0078	output4_config1	0xDA00	R/W
0x0079	output4_config2	0x03	R/W
0x007A	output4_config3	0x00	R/W
0x007B:0x007C	output5_config0	0x0200	R/W

Register Map (continued)

Address	Name	Default	Type
0x007D:0x007E	output5_config1	0xDA00	R/W
0x007F	output5_config2	0x03	R/W
0x0080	output5_config3	0x00	R/W
0x0081	lpflt_ctl	0x3F	R/W
0x0082	apll_config0	0x01	R/W
0x0083	apll_config1	0xE8	R/W
0x0084:0x0085	afbden	0x0000	R/W
0x0086:0x0087	afbrem	0x0000	R/W
0x0088	afbbp	0x00	R/W
0x0089:0x008E	afbdiv	0x001E613716AE	R/W
0x008F:0x0094	afbdiv_b	0x001E613716AE	R/W
0x0095	xbar_sel01	0x3F	R/W
0x0096	xbar_sel23	0x3F	R/W
0x0097	xbar_sel45	0x3F	R/W
0x0098	xbar_sel01_b	0x3F	R/W
0x0099	xbar_sel23_b	0x3F	R/W
0x009A	xbar_sel45_b	0x3F	R/W
0x009B	oc1_divn	0x00	R/W
0x009C	oc1_divn_pdn	0xF	R/W
0x009D	oc1_divn_b	0x00	R/W
0x009E	oc2_divn	0x00	R/W
0x009F	oc2_divn_pdn	0xF	R/W
0x00A0	oc2_divn_b	0x00	R/W
0x00A1:0x00A5	fd1_div	0x0000000000	R/W
0x00A6:0x00A7	fd1_den	0x0000	R/W
0x00A8:0x00A9	fd1_rem	0x0000	R/W
0x00AA:0x00AB	fd1_ss_cnt	0x0000	R/W
0x00AC:0x00AF	fd1_ss_id	0x00000000	R/W
0x00B0	fd1_config0	0x30	R/W
0x00B1	fd1_config1	0x80	R/W
0x00B2	fd1_config2	0x00	R/W
0x00B3	fd1_config3	0x00	R/W
0x00B4:0x00B8	fd1_div_b	0x0000000000	R/W
0x00B9:0x00BC	fd1_ss_id_b	0x00000000	R/W
0x00BD:0x00BE	fd1_ss_cnt_b	0x0000	R/W
0x00BF	fd1_config4	0x00	R/W
0x00C0	fd1_config5	0x60	R/W
0x00C1	fd1_config6	0x00	R/W
0x00C2:0x00C6	fd2_div	0x0000000000	R/W

Register Map (continued)

Address	Name	Default	Type
0x00C7:0x00C8	fd2_den	0x0000	R/W
0x00C9:0x00CA	fd2_rem	0x0000	R/W
0x00CB:0x00CC	fd2_ss_cnt	0x0000	R/W
0x00CD:0x00D0	fd2_ss_id	0x00000000	R/W
0x00D1	fd2_config0	0x30	R/W
0x00D2	fd2_config1	0x80	R/W
0x00D3	fd2_config2	0x00	R/W
0x00D4	fd2_config3	0x00	R/W
0x00D5:0x00D9	fd2_div_b	0x0000000000	R/W
0x00DA:0x00DD	fd2_ss_id_b	0x00000000	R/W
0x00DE:0x00DF	fd2_ss_cnt_b	0x0000	R/W
0x00E0	fd2_config4	0x00	R/W
0x00E1	fd2_config5	0x60	R/W
0x00E2	fd2_config6	0x00	R/W
0x00E3:0x00FF	Reserved	—	—
0x0100:0x01FF	Reserved	—	—
0x0200:0x02FF	Reserved	—	—

Register List, Page0 Registers

Address: Name: Default: Type:	0x004F:0x0050 config_0x4F_50 0x0000 R/W	
Bit Field	Function Name	Description
15	sel_bank_bed5	OUT5 back end divider frequency plan select. 0 = Frequency plan A 1 = Frequency plan B
14	sel_bank_bed4	OUT4 back end divider frequency plan select. 0 = Frequency plan A 1 = Frequency plan B
13	sel_bank_bed3	OUT3 back end divider frequency plan select. 0 = Frequency plan A 1 = Frequency plan B
12	sel_bank_bed2	OUT2 back end divider frequency plan select. 0 = Frequency plan A 1 = Frequency plan B
11	sel_bank_bed1	OUT1 back end divider frequency plan select. 0 = Frequency plan A 1 = Frequency plan B
10	sel_bank_bed0	OUT0 back end divider frequency plan select. 0 = Frequency plan A 1 = Frequency plan B

9:0	reserved	—

Address:	0x0051	
Name:	config_0x51	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	sel_x_xck	CLKIN to output XBAR enable. 0 = disable 1 = enable
6:5	fusa_cnt_ts	FUSA FAULT2 Temperature Sensor consecutive hits before setting the flag. 0 = 4 (default) 1 = 8 2 = 16 3 = 32
4:0	sel_gpio0_func	GPIO0 pin function select. All decodes make GPIO0 an input that controls something except 17-21. 0 = None 1 = OUT0 output enable (GPIO0 = 1 for output enabled, same for enables below) 2 = OUT1 output enable 3 = OUT2 output enable 4 = OUT3 output enable 5 = OUT4 output enable 6 = OUT5 output enable 7 = OUT0-OUT5 output enable 8 = OUT0-OUT2 output enable 9 = OUT3-OUT5 output enable 10 = FS0 (frequency select 0) for back-end (i.e. output) dividers with A vs B frequency plan indicated by sel_bank_bed[5:0] register bits. 11 = FS1 (frequency select 1) (GPIO0 = 0 for A frequency plan, GPIO0 = 1 for B frequency plan for entire device) 12 = Spread spectrum enable for FDIV1 (GPIO0 = 1 for enabled) 13 = Spread spectrum enable for FDIV2 14 = Spread spectrum enable for FDIV1 and FDIV2 15 = Spread spectrum modulation frequency multiple for FDIV1 and FDIV2 (GPIO0 = 0 for 1x, GPIO0 = 1 for 2x) 16 = Reference select (This option is not available on DSA504RT) 17 = PLL loss of lock output 18 = PLL loss of source output 19 = Temperature sensor out of range output 20 = OTP checksum failure output 28 = Synchronize back end dividers in same frequency plan (A or B) on 0-to-1 transition 30 = Low-power standby mode 31 = I^2C client address least-significant bit Only one GPIO can be configured for each input control function. Only one GPIO can be configured to have output enable control for each of OUT0-OUT5. Only one GPIO can be configured to have spread spectrum enable control for each of FDIV1 and FDIV2. OTP failure sets GPIO0=1 but does not stop the device.

Address:	0x0052	
Name:	config_0x52	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	fusa_clr_lol	FUSA FAULT0 PLL_LOL clear trigger signal. 0 = normal operation 0->1 transition clears flag
6:5	reserved	—
4:0	sel_gpio1_func	GPIO1 pin function select. See the sel_gpio0_func description at address 0x51.

Address:	0x0053	
Name:	config_0x53	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	fusa_en_lol	FUSA FAULT0 PLL_LOL enable. 0 = disable 1 = enable
6:5	sel_bank_fs0	Register bit for FS0 frequency select. Ignored if any GPIO is configured for FS0 in its sel_gpioX_func register field. FS0 selects frequency plan A or B for the back-end dividers (i.e. the output dividers). 0 = disabled 1 = disabled 2 = frequency plan A (if FS1=0) or frequency plan B (if FS1=1) 3 = frequency plan for each output set by corresponding sel_bank_bed bit (if FS1=0) or !sel_bank_bed (if FS1=1) For decodes 0 and 1, FS0 is disabled and FS1 selects the frequency plan for the output dividers along with the rest of the device. In decode 3 above 'sel_bank_bed' means the frequency plan for each output divider is specified by its sel_bank_bed bit in register config_0x4F_50.
4:0	sel_gpio2_func	GPIO2 pin function select. See the sel_gpio0_func description at address 0x51.

Address:	0x0054	
Name:	config_0x54	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	fusa_clr_ts	FUSA FAULT2 Temperature Sensor clear trigger signal. 0 = normal operation 0->1 transition clears flag
6	fusa_en_los	FUSA FAULT1 PLL_LOS enable. 0 = disable 1 = enable

5	fusa_clr_los	FUSA FAULT1 PLL_LOS clear trigger signal. 0 = normal operation 0->1 transition clears flag
4:0	sel_gpio3_func	GPIO3 pin function select. See the sel_gpio0_func description at address 0x51.

Address: Name: Default: Type:	0x0055 config_0x55 0x00 R/W	
Bit Field	Function Name	Description
7	reserved	—
6	reserved	—
5	fusa_en_ts	FUSA FAULT2 Temperature Sensor enable. 0 = disable 1 = enable
4:0	sel_gpio4_func	GPIO4 pin function select. See the sel_gpio0_func description at address 0x51.

Address: Name: Default: Type:	0x0056 config_0x56 0x0C R/W	
Bit Field	Function Name	Description
7	sel_sync_bed	BED (i.e. output divider) synchronization trigger bit. Ignored if any GPIO is configured for sync in its sel_gpioX_func register field. 0 = normal operation 0->1 transition triggers BED synchronization
6	sel_bank_fs1	Frequency plan select bit. Ignored if any GPIO is configured for FS1 in its sel_gpioX_func register field. 0 = frequency plan A 1 = frequency plan B
5	sel_both_moxclk	This option is not available on DSA504RT. This field must always be 0.
4	sel_refclk	APLL reference clock select. Ignored if any GPIO is configured for reference select in its sel_gpioX_func register field. Always 1 : CLKIN (external CLK) clock selected.
3	sel_pad_pe567	Pull Enable (pull-up) pins 5, 6, and 7. 0 = disable 1 = enable
2	sel_pad_pe12	Pull Enable (pull-down) pins 1 and 2. 0 = disable 1 = enable
1	sel_pad_ds	GPIO Drive Strength. 0 = 4mA 1 = 8mA
0	reserved	—

Address:	0x0057	
Name:	lpflt_ctl_b	
Default:	0x3F	
Type:	R/W	
Bit Field	Function Name	Description
7:4	lpflt_rprop	APLL frequency plan B proportional path resistor. 0 = 12.5kΩ 1 = 10.0kΩ 2 = 8.0kΩ 3 = 6.0kΩ 4 = 4.5kΩ 5 = 3.0kΩ 6 = 2.0kΩ 7 = 1.25kΩ other = insert +3kΩ post (higher-order pole)
3:0	lpflt_cprop	APLL frequency plan B proportional path capacitor. 0 = 1pF 1 = 5pF 2 = 9pF 3 = 13pF 4 = 17pF 5 = 21pF 6 = 25pF 7 = 29pF other = +4pf post (higher-order pole)

Address:	0x0058	
Name:	config_0x58	
Default:	0x81	
Type:	R/W	
Bit Field	Function Name	Description
7:6	fusa_en_buf	Enable outputs stop (squelch) on FUSA LOL/LOS flags. 0 = no squelch (test mode), 1 = no squelch (test mode), 2 = release squelch in operate state 3 = release squelch in operate state but squelch if fusa lol/los flag raised
5:4	chp_scaling_b	APLL frequency plan B charge pump scaling. 0 = normal 1 = lower iprop by 30% 2 = lower iint by 30% 3 = lower iprop & iintg by 30%

3:0	chp_iprop_iint_b	APLL frequency plan B charge pump iprop (proportional current) / iint (integral current). 0 = 100µA/25µA 1 = 200µA/25µA 2 = 300µA/25µA 3 = 400µA/25µA 4 = 500µA/50µA 5 = 600µA/50µA 6 = 700µA/50µA 7 = 800µA/50µA 8 = 1000µA/50µA 9 = 1000µA/100µA 10 = 1200µA/50µA 11 = 1200µA/100µA 12 = 1400µA/50µA 13 = 1400µA/100µA 14 = 1600µA/50µA 15 = 1600µA/100µA

Address: Name: Default: Type:	0x0059 config_0x59 0x5D R/W	
Bit Field	Function Name	Description
7	reserved	
6	ref_clk_mwidth_b	Frequency plan B REF clock minimum width selector when rfdivn is doubling. 0 = disable (minimum width) 1 = enable (minimum width when APLL REF > 90MHz and rfdivn_b=1)
5	afb_en_rem_den_b	APLL frequency plan B remainder and denominator selector 0 = Disabled, internal rem=0, den=1 1 = Enable, use registers afbrem and afbden
4:3	js_order_b	APLL frequency plan B feedback divider sigma-delta modulation order. 0 = no sigma delta (fractional bits ignored) 1 = js1. no shaping (integer mode) 2 = js2. 20dB/decade — do not use 3 = js3. 40dB/decade (fractional mode)
2:0	pfd_ctl_432_b	Frequency plan B APLL PFD. Anti-backlash width setting and PFD boost. 0=250ps, mode 1x plateau width=0ps, 1=700ps, mode 1x plateau width=0ps, 2=250ps (boost mode 2x) plateau width=±80ps, 3=350ps (boost mode 2x) plateau width=±80ps, 4=1000ps, mode 1x plateau width=0ps, 5=1200ps, mode 1x plateau width=0ps, 6=1400ps, mode 1x plateau width=0ps, 7=1600ps, mode 1x plateau width=0ps

Address: Name: Default: Type:	0x005A config_0x5A 0x4A R/W	
Bit Field	Function Name	Description
7	autotune	APLL captune algorithm control. 0 = only controlled by retune (internal state machine) 1 = PLL will re-captune if OOL is tripped
6	ibufc_hyst_en	Clock/GPIO01 input select: CMOS buffer hysteresis selector. 0 = disable 1 = enable
5	ibuf_pd	Clock/GPIO01 input select: VDDMI12 LDO power down. 0 = enable (normal) 1 = disable (power down)
4	ibuf_acc	Clock/GPIO01 input select: HCSL buffer coupling mode selector. 0 = DC 1 = AC
3:0	ibuf_ctrl	Clock/GPIO01 input select: HCSL buffer power mode selector. 0 = 51µA 1 = 67µA 2 = 84µA 3 = 101µA (lpwr) 4 = 120µA 5 = 139µA 6 = 158µA 7 = 179µA (poly rho fast) 8 = 199µA 9 = 221µA 10 = 243µA (poly rho nom) (default) 11 = 265µA 12 = 288µA 13 = 311µA (poly rho slow) 14 = 335µA

Address:	0x005B	
Name:	config_0x5B	
Default:	0x20	
Type:	R/W	
Bit Field	Function Name	Description
7	afb_en_rem_den	APLL frequency plan A remainder and denominator selector. 0 = Disabled, internal rem=0, den=1 1 = Enable, use registers afbrem and afbden
6:5	rfdivn	Frequency plan A reference clock doubler/divider selector. 0 = 1x (pass refclk) 1 = 2x (refclk*2) 2 = 0.5x (refclk/2) 3 = 0.25x (refclk/4)
4:0	tc_ndiv	Frequency plan A system clock divider between 2 to 16. tc_ndiv=fbclk_MHz/16 (openloop=4).

Address:	0x005C	
Name:	config_0x5C	
Default:	0xAA	
Type:	R/W	
Bit Field	Function Name	Description
7	ref_clk_mwidth	Frequency plan A REF clock minimum width selector when rfdivn is doubling. 0 = disable (minimum width) 1 = enable (minimum width when APLL REF > 90MHz and rfdivn=1)
6:5	rfdivn_b	Frequency plan B reference clock doubler/divider selector. 0 = 1x (pass refclk) 1 = 2x (refclk*2) 2 = 0.5x (refclk/2) 3 = 0.25x (refclk/4)
4:0	tc_ndiv_b	Frequency plan B system clock divider between 2 to 16. tc_ndiv=fbclk_MHz/16 (openloop=4).

Address: Name: Default: Type:	0x005D:0x005E output0_config0 0x0200 R/W	
Bit Field	Function Name	Description
15	reserved	—
14:11	mode	OUT0 output buffer mode selector 0 = LVPECL, high-impedance when disabled 1 = LVDS, high-impedance when disabled 2 = LVDS 1.8V, high-impedance when disabled 3 = LPHCSL, high-impedance when disabled 4 = 2 CMOS in phase, high-impedance when disabled, start at low 5 = 2 CMOS, OUT0b inverted, high-impedance when disabled, start at OUT0 low 6 = 2 CMOS, OUT0b inverted, high-impedance when disabled, start at OUT0 high 7 = 2 CMOS in phase, high-impedance when disabled, start at high 8 = LVPECL, low/high when disabled 9 = LVDS, low/high when disabled 10 = LVDS 1.8V, low/high when disabled 11 = LP-HCSL, low/high when disabled 12 = 2 CMOS in phase, low when disabled, start at low when enabled 13 = 2 CMOS, OUT0b inverted, OUT0 low when disabled, start at OUT0 low 14 = 2 CMOS, OUT0b inverted, OUT0 high when disabled, start at OUT0 high 15 = 2 CMOS in phase, high when disabled, start at high

10:0	bdiv_val_b	OUT0 buffer divider ratio frequency plan B. 0x200 = div 1 0x400 = div 2 0x622 = div 3 0x000 = div 4 0x003 = div 5 0x022 = div 6 0x025 = div 7 0x044 = div 8 0x047 = div 9 0x066 = div 10 0x069 = div 11 0x088 = div 12 0x08B = div 13 0x0AA = div 14 0x0AD = div 15 0x0CC = div 16 0x0CF = div 17 0x0EE = div 18 0x0F1 = div 19 0x110 = div 20 0x113 = div 21 0x132 = div 22 0x135 = div 23 0x154 = div 24 0x157 = div 25 0x176 = div 26 0x179 = div 27 0x198 = div 28 0x19B = div 29 0x1BA = div 30 0x1BD = div 31

Address: Name: Default: Type:	0x005F:0x0060 output0_config1 0xDA00 R/W	
Bit Field	Function Name	Description
15:14	cmos_edge_n	OUT0b CMOS edge rate selector. These two bits are concatenated with bit 3 of byte 0x61 to have 3 bits edge control of OUT0b. The latter being the MSB. 000 = minimum edge rate 001 = second smallest edge rate ... 111 = maximum edge rate
13	cmos_n_disable	OUT0b disable 0 = Enabled 1 = Disabled

12:11	en_pass_res	OUT0 reference voltage bias adjustment for ldo_variable (PECL, LVDS, HCSL) : 00 = 20.58kΩ (@ 1.235V): LVCMOS x1 = 12.35kΩ (@1.235V): LVPECL, LVDS 1.8V 10 = 14.41kΩ (@ 1.235V): LVDS xx = 14.41kΩ/0.98kΩ (@ 1.235V/0.75V): LPHCSL
10:0	bdiv_val	OUT0 buffer divider ratio, frequency plan A. 0x200 = div 1 0x400 = div 2 0x622 = div 3 0x000 = div 4 0x003 = div 5 0x022 = div 6 0x025 = div 7 0x044 = div 8 0x047 = div 9 0x066 = div 10 0x069 = div 11 0x088 = div 12 0x03B = div 13 0x0AA = div 14 0x0AD = div 15 0x0CC = div 16 0x0CF = div 17 0x0EE = div 18 0x0F1 = div 19 0x110 = div 20 0x113 = div 21 0x132 = div 22 0x135 = div 23 0x154 = div 24 0x157 = div 25 0x176 = div 26 0x179 = div 27 0x198 = div 28 0x19B = div 29 0x1BA = div 30 0x1BD = div 31

Address: Name: Default: Type:	0x0061 output0_config2 0x03 R/W	
Bit Field	Function Name	Description
7	en	OUT0 driver enable 0 = Disabled 1 = Enabled
6	reserved	—

5	cmos_drvp	OUT0 CMOS drive strength 0 = 1x (drive strength 0) 1 = 2x (drive strength 1) See Table 6-7 and its notes for V_{OH}, V_{OL}, I_{OH}, and I_{OL} values.
4	cmos_drvn	OUT0b CMOS drive strength 0 = 1x (drive strength 0) 1 = 2x (drive strength 1) See Table 6-7 and its notes for V_{OH}, V_{OL}, I_{OH}, and I_{OL} values.
3	cmos_edge_n[2]	Concatenated with cmos_edge_n[1:0] in the output0_config1 register at 0x5F:0x60.
2:0	cmos_edge_p	OUT0 CMOS edge p control 000 = minimum edge rate 001 = second smallest edge rate ... 111 = maximum edge rate

Address:	0x0062	
Name:	output0_config3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	—
4	pecl_lvds_res	Output buffer LVPECL and LVDS signal swing control 0 = Normal 1 = 100mV smaller
3	hcsl_en42ohm	Output buffer LPHCSL output impedance selector 0 = 50Ω 1 = 42Ω
2	ldo_en	OUT0 buffer enable LDO selector 0 = Disable 1 = Enable
1	en_mod18	OUT0 LVCMOS bias selector for duty cycle enhancement at 1.8V 0 = Normal duty cycle 1 = Enhancement for 1.8V
0	cmos_p_disable	OUT0 disable 0 = Enabled 1 = Disabled (high-impedance)

Address:	0x0063:0x0064	
Name:	output1_config0	
Default:	0x0200	
Type:	R/W	
Bit Field	Function Name	Description
15	reserved	—
14:11	mode	OUT1 output buffer mode selector. See output0_config0::mode at 0x5D:0x5E.
10:0	bdiv_val_b	OUT1 buffer divider ratio, frequency plan B. See output0_config0::bdiv_val_b at 0x5D:0x5E.

Address:	0x0065:0x0066	
Name:	output1_config1	
Default:	0xDA00	
Type:	R/W	
Bit Field	Function Name	Description
15:14	cmos_edge_n	OUT1b CMOS edge rate selector. See output0_config1::cmos_edge_n at 0x5F:0x60.
13	cmos_n_disable	OUT1b disable. See output0_config1::cmos_n_disable at 0x5F:0x60.
12:11	en_pass_res	OUT1 reference voltage bias adjustment for ldo_variable (PECL, LVDS, HCSL). See output0_config1::en_pass_res at 0x5F:0x60.
10:0	bdiv_val	OUT1 buffer divider ratio, frequency plan A. See output0_config1::bdiv_val at 0x5F:0x60.

Address:	0x0067	
Name:	output1_config2	
Default:	0x03	
Type:	R/W	
Bit Field	Function Name	Description
7	en	OUT1 driver enable. See output0_config2::en at 0x61.
6	reserved	—
5	cmos_drvp	OUT1 drive strength. See output0_config2::cmos_drvp at 0x61.
4	cmos_drvn	OUT1b drive strength. See output0_config2::cmos_drvn at 0x61.
3	cmos_edge_n[2]	Concatenated with cmos_edge_n[1:0] in the output1_config1 register at 0x65:0x66.
2:0	cmos_edge_p	OUT1 CMOS edge p control. See output0_config2::cmos_edge_p at 0x61.

Address:	0x0068	
Name:	output1_config3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	—
4	pecl_lvds_res	Output buffer LVPECL and LVDS signal swing control. See output0_config3::pecl_lvds_res at 0x62.
3	hcsl_en42ohm	Output buffer LPHCSL output impedance selector. See output0_config3::hcsl_en42ohm at 0x62.
2	ldo_en	OUT0 buffer enable LDO selector. See output0_config3::ldo_en at 0x62.
1	en_mod18	OUT0 LVCMOS bias selector for duty cycle enhancement at 1.8V. See output0_config3::en_mod18 at 0x62.
0	cmos_p_disable	OUT0 disable. See output0_config3::cmos_p_disable at 0x62.

Address:	0x0069:0x006A	
Name:	output2_config0	
Default:	0x0200	
Type:	R/W	
Bit Field	Function Name	Description
15	reserved	—
14:11	mode	OUT2 output buffer mode selector. See output0_config0::mode at 0x5D:0x5E.
10:0	bdiv_val_b	OUT2 buffer divider ratio, frequency plan B. See output0_config0::bdiv_val_b at 0x5D:0x5E.

Address:	0x006B:0x006C	
Name:	output2_config1	
Default:	0xDA00	
Type:	R/W	
Bit Field	Function Name	Description
15:14	cmos_edge_n	OUT2b CMOS edge rate selector. See output0_config1::cmos_edge_n at 0x5F:0x60.
13	cmos_n_disable	OUT2b disable. See output0_config1::cmos_n_disable at 0x5F:0x60.
12:11	en_pass_res	OUT2 reference voltage bias adjustment for ldo_variable (PECL, LVDS, HCSL). See output0_config1::en_pass_res at 0x5F:0x60.
10:0	bdiv_val	OUT2 buffer divider ratio, frequency plan A. See output0_config1::bdiv_val at 0x5F:0x60.

Address:	0x006D	
Name:	output2_config2	
Default:	0x03	
Type:	R/W	
Bit Field	Function Name	Description
7	en	OUT2 driver enable. See output0_config2::en at 0x61. 0 = Disabled 1 = Enabled
6	reserved	—
5	cmos_drvp	OUT2 drive strength. See output0_config2::cmos_drvp at 0x61.
4	cmos_drvn	OUT2b drive strength. See output0_config2::cmos_drvn at 0x61.
3	cmos_edge_n[2]	Concatenated with cmos_edge_n[1:0] in the output2_config1 register at 0x6B:0x6C.
2:0	cmos_edge_p	OUT2 CMOS edge p control. See output0_config2::cmos_edge_p at 0x61.

Address:	0x006E	
Name:	output2_config3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	—

4	pecl_lvds_res	Output buffer LVPECL and LVDS signal swing control. See output0_config3::pecl_lvds_res at 0x62.
3	hcsl_en42ohm	Output buffer LPHCSL output impedance selector. See output0_config3::hcsl_en42ohm at 0x62.
2	ldo_en	OUT0 buffer enable LDO selector. See output0_config3::ldo_en at 0x62.
1	en_mod18	OUT0 LVCMOS bias selector for duty cycle enhancement at 1.8V. See output0_config3::en_mod18 at 0x62.
0	cmos_p_disable	OUT0 disable. See output0_config3::cmos_p_disable at 0x62.

Address: Name: Default: Type:	0x006F:0x0070 output3_config0 0x0200 R/W	
Bit Field	Function Name	Description
15	reserved	—
14:11	mode	OUT3 output buffer mode selector. See output0_config0::mode at 0x5D:0x5E.
10:0	bdiv_val_b	OUT3 buffer divider ratio, frequency plan B. See output0_config0::bdiv_val_b at 0x5D:0x5E.

Address: Name: Default: Type:	0x0071:0x0072 output3_config1 0xDA00 R/W	
Bit Field	Function Name	Description
15:14	cmos_edge_n	OUT3b CMOS edge rate selector. See output0_config1::cmos_edge_n at 0x5F:0x60.
13	cmos_n_disable	OUT3b disable. See output0_config1::cmos_n_disable at 0x5F:0x60.
12:11	en_pass_res	OUT3 reference voltage bias adjustment for ldo_variable (PECL, LVDS, HCSL). See output0_config1::en_pass_res at 0x5F:0x60.
10:0	bdiv_val	OUT3 buffer divider ratio, frequency plan A. See output0_config1::bdiv_val at 0x5F:0x60.

Address: Name: Default: Type:	0x0073 output3_config2 0x03 R/W	
Bit Field	Function Name	Description
7	en	OUT3 driver enable. See output0_config2::en at 0x61. 0 = Disabled 1 = Enabled
6	reserved	—
5	cmos_drvp	OUT3 drive strength. See output0_config2::cmos_drvp at 0x61.
4	cmos_drvn	OUT3b drive strength. See output0_config2::cmos_drvn at 0x61.
3	cmos_edge_n[2]	Concatenated with cmos_edge_n[1:0] in the output3_config1 register at 0x71:0x72.
2:0	cmos_edge_p	OUT3 CMOS edge p control. See output0_config2::cmos_edge_p at 0x61.

Address:	0x0074	
Name:	output3_config3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	—
4	pecl_lvds_res	Output buffer LVPECL and LVDS signal swing control. See output0_config3::pecl_lvds_res at 0x62.
3	hcsl_en42ohm	Output buffer LPHCSL output impedance selector. See output0_config3::hcsl_en42ohm at 0x62.
2	ldo_en	OUT0 buffer enable LDO selector. See output0_config3::ldo_en at 0x62.
1	en_mod18	OUT0 LVCMOS bias selector for duty cycle enhancement at 1.8V. See output0_config3::en_mod18 at 0x62.
0	cmos_p_disable	OUT0 disable. See output0_config3::cmos_p_disable at 0x62.

Address:	0x0075:0x0076	
Name:	output4_config0	
Default:	0x0200	
Type:	R/W	
Bit Field	Function Name	Description
15	reserved	—
14:11	mode	OUT4 output buffer mode selector. See output0_config0::mode at 0x5D:0x5E.
10:0	bdiv_val_b	OUT4 buffer divider ratio, frequency plan B. See output0_config0::bdiv_val_b at 0x5D:0x5E.

Address:	0x0077:0x0078	
Name:	output4_config1	
Default:	0xDA00	
Type:	R/W	
Bit Field	Function Name	Description
15:14	cmos_edge_n	OUT4b CMOS edge rate selector. See output0_config1::cmos_edge_n at 0x5F:0x60.
13	cmos_n_disable	OUT4b disable. See output0_config1::cmos_n_disable at 0x5F:0x60.
12:11	en_pass_res	OUT4 reference voltage bias adjustment for ldo_variable (PECL, LVDS, HCSL). See output0_config1::en_pass_res at 0x5F:0x60.
10:0	bdiv_val	OUT4 buffer divider ratio, frequency plan A. See output0_config1::bdiv_val at 0x5F:0x60.

Address:	0x0079	
Name:	output4_config2	
Default:	0x03	
Type:	R/W	
Bit Field	Function Name	Description
7	en	OUT4 driver enable. See output0_config2::en at 0x61. 0 = Disabled 1 = Enabled
6	reserved	—

5	cmos_drvp	OUT4 drive strength. See output0_config2p::cmos_drvp at 0x61.
4	cmos_drvn	OUT4b drive strength. Seeoutput0_config2::cmos_drvn at 0x61.
3	cmos_edge_n[2]	Concatenated with cmos_edge_n[1:0] in the output4_config1 register at 0x77:0x78.
2:0	cmos_edge_p	OUT4 CMOS edge p control. See output0_config2::cmos_edge_p at 0x61.

Address: Name: Default: Type:	0x007A output4_config3 0x00 R/W	
Bit Field	Function Name	Description
7:5	reserved	—
4	pecl_lvds_res	Output buffer LVPECL and LVDS signal swing control. See output0_config3::pecl_lvds_res at 0x62.
3	hcsl_en42ohm	Output buffer LPHCSL output impedance selector. See output0_config3::hcsl_en42ohm at 0x62.
2	ldo_en	OUT0 buffer enable LDO selector. See output0_config3::ldo_en at 0x62.
1	en_mod18	OUT0 LVCMOS bias selector for duty cycle enhancement at 1.8V. See output0_config3::en_mod18 at 0x62.
0	cmos_p_disable	OUT0 disable. See output0_config3::cmos_p_disable at 0x62.

Address: Name: Default: Type:	0x007B:0x007C output5_config0 0x0200 R/W	
Bit Field	Function Name	Description
15	reserved	—
14:11	mode	OUT5 output buffer mode selector. See output0_config0::mode at 0x5D:0x5E.
10:0	bdiv_val_b	OUT5 buffer divider ratio, frequency plan B. See output0_config0::bdiv_val_b at 0x5D:0x5E.

Address: Name: Default: Type:	0x007D:0x007E output5_config1 0xDA00 R/W	
Bit Field	Function Name	Description
15:14	cmos_edge_n	OUT5b CMOS edge rate selector. See output0_config1::cmos_edge_n at 0x5F:0x60.
13	cmos_n_disable	OUT5b disable. See output0_config1::cmos_n_disable at 0x5F:0x60.
12:11	en_pass_res	OUT5 reference voltage bias adjustment for ldo_variable (PECL, LVDS, HCSL). See output0_config1::en_pass_res at 0x5F:0x60.
10:0	bdiv_val	OUT5 buffer divider ratio, frequency plan A. See output0_config1::bdiv_val at 0x5F:0x60.

Address:	0x007F	
Name:	output5_config2	
Default:	0x03	
Type:	R/W	
Bit Field	Function Name	Description
7	en	OUT5 driver enable. See output0_config2::en at 0x61. 0 = Disabled 1 = Enabled
6	reserved	—
5	cmos_drvp	OUT5 drive strength. See output0_config2::cmos_drvp at 0x61.
4	cmos_drvn	OUT5b drive strength. See output0_config2::cmos_drvn at 0x61.
3	cmos_edge_n[2]	Concatenated with cmos_edge_n[1:0] in the output5_config1 register at 0x7D:0x7E.
2:0	cmos_edge_p	OUT5 CMOS edge p control. See output0_config2::cmos_edge_p at 0x61.

Address:	0x0080	
Name:	output5_config3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	—
4	pecl_lvds_res	Output buffer LVPECL and LVDS signal swing control. See output0_config3::pecl_lvds_res at 0x62.
3	hcsl_en42ohm	Output buffer LPHCSL output impedance selector. See output0_config3::hcsl_en42ohm at 0x62.
2	ldo_en	OUT0 buffer enable LDO selector. See output0_config3::ldo_en at 0x62.
1	en_mod18	OUT0 LVCMOS bias selector for duty cycle enhancement at 1.8V. See output0_config3::en_mod18 at 0x62.
0	cmos_p_disable	OUT0 disable. See output0_config3::cmos_p_disable at 0x62.

Address:	0x0081	
Name:	lpflt_ctl	
Default:	0x3F	
Type:	R/W	
Bit Field	Function Name	Description
7:4	lpflt_rprop	APLL frequency plan A proportional path resistor. 0 = 12.5kΩ 1 = 10.0kΩ 2 = 8.0kΩ 3 = 6.0kΩ 4 = 4.5kΩ 5 = 3.0kΩ 6 = 2.0kΩ 7 = 1.25kΩ other = insert +3kΩ post (higher-order pole)

3:0	lpflt_cprop	APLL frequency plan A proportional path capacitor. 0 = 1pF 1 = 5pF 2 = 9pF 3 = 13pF 4 = 17pF 5 = 21pF 6 = 25pF 7 = 29pF other = +4pf post (higher-order pole)

Address: Name: Default: Type:	0x0082 apll_config0 0x01 R/W	
Bit Field	Function Name	Description
7:6	odivn	APLL PDIV integer divider ratio. 0 = disable 1 = divide by 4 2 = divide by 5 3 = divide by 6
5:4	chp_scaling	APLL frequency plan A charge pump scaling. 0 = normal 1 = lower iprop by 30% 2 = lower iint by 30% 3 = lower iprop & iintg by 30%
3:0	chp_iprop_iint	APLL frequency plan A charge pump iprop (proportional current)/iint (integral current). 0 = 100µA/25µA 1 = 200µA/25µA 2 = 300µA/25µA 3 = 400µA/25µA 4 = 500µA/50µA 5 = 600µA/50µA 6 = 700µA/50µA 7 = 800µA/50µA 8 = 1000µA/50µA 9 = 1000µA/100µA 10 = 1200µA/50µA 11 = 1200µA/100µA 12 = 1400µA/50µA 13 = 1400µA/100µA 14 = 1600µA/50µA 15 = 1600µA/100µA

Address:	0x0083	
Name:	apll_config1	
Default:	0xE8	
Type:	R/W	
Bit Field	Function Name	Description
7:6	js_order	APLL frequency plan A feedback divider sigma-delta modulation order. 0 = no sigma delta (fractional bits ignored) 1 = js1. no shaping (integer mode) 2 = js2. 20dB/decade — do not use 3 = js3. 40dB/decade (fractional mode)
5:3	pfd_ctl_432	APLL frequency plan A PFD anti-backlash width setting and PFD boost. 0 = 250ps 1 = 700ps 2 = 250ps (boost) 3 = 350ps (boost) 4 = 1000ps 5 = 1200ps 6 = 1400ps 7 = 1600ps
2:0	podivn	APLL output divider post-divider value. 0 = divide by 1 1 = divide by 2 2 = divide by 4 3 = divide by 6 other = divide by 8

Address:	0x0084:0x0085	
Name:	afbden	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0	—	APLL fractional divider denominator. Can be used with afbrem to sigma-delta modulate the APLL fractional divider lsb when 0ppm frequency conversion from CLKIN is required.

Address:	0x0086:0x0087	
Name:	afbrem	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0	—	APLL fractional divider remainder. Can be used with afbden to sigma-delta modulate the APLL fractional divider lsb when 0ppm frequency conversion from CLKIN is required.

Address:	0x0088	
Name:	afbbp	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0	—	APLL feedback divider bit position. This defines the lsb of the afbdiv register's fractional bits below which the afbrem and afbden can be used for sigma delta modulation for exact 0ppm frequency conversion from the CLKIN signal. Number of bits used is 33-bp. 0 = 9.33b (XO) ... 9 = 9.24b (MO)

Address:	0x0089:0x008E	
Name:	afbdiv	
Default:	0x001E613716AE	
Type:	R/W	
Bit Field	Function Name	Description
47:42	reserved	—
41:0	—	APLL frequency plan A feedback divider value. Bits 41-33 are integer. Bits 32:0 are fraction.

Address:	0x008F:0x0094	
Name:	afbdiv_b	
Default:	0x001E613716AE	
Type:	R/W	
Bit Field	Function Name	Description
47:42	reserved	—
41:0	—	APLL frequency plan B feedback divider value. Bits 41-33 are integer. Bits 32:0 are fraction.

Address:	0x0095	
Name:	xbar_sel01	
Default:	0x3F	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	—
5:3	sel1	OUT1 source, frequency plan A. See sel0.
2:0	sel0	OUT0 source, frequency plan A . 0 = INTDIV1 1 = INTDIV2 2 = FDIV1 3 = FDIV2 4 = CLKIN (requires sel_x_xck=1) 5-7 = Disabled

Address:	0x0096	
Name:	xbar_sel23	
Default:	0x3F	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	—
5:3	sel3	OUT3 source, frequency plan A. See xbar_sel01::sel0.
2:0	sel2	OUT2 source, frequency plan A. See xbar_sel01::sel0.

Address:	0x0097	
Name:	xbar_sel45	
Default:	0x3F	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	—
5:3	sel5	OUT5 source, frequency plan A. See xbar_sel01::sel0.
2:0	sel4	OUT4 source, frequency plan A. See xbar_sel01::sel0.

Address:	0x0098	
Name:	xbar_sel01_b	
Default:	0x3F	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	—
5:3	sel1_b	OUT1 source, frequency plan B. See sel0_b.
2:0	sel0_b	OUT0 source, frequency plan B. 0 = INTDIV1 1 = INTDIV2 2 = FDIV1 3 = FDIV2 4 = CLKIN (requires sel_x_xck=1) 5-7 = Disabled

Address:	0x0099	
Name:	xbar_sel23_b	
Default:	0x3F	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	—
5:3	sel3_b	OUT3 source, frequency plan B. See xbar_sel01_b::sel0_b.
2:0	sel2_b	OUT2 source, frequency plan B. See xbar_sel01_b::sel0_b.

Address:	0x009A	
Name:	xbar_sel45_b	
Default:	0x3F	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	—
5:3	sel5_b	OUT5 source, frequency plan B. See xbar_sel01_b::sel0_b.
2:0	sel4_b	OUT4 source, frequency plan B. See xbar_sel01_b::sel0_b.

Address:	0x009B	
Name:	oc1_divn	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	post_div	INTDIV1 post-divider, frequency plan A. 000 = 1 001 = 2 010 = 4 011 = 6 1xx = 8
4:0	div	INTDIV1 divider, frequency plan A. 0 = 32 1 = 33 2, 3 = 32 4-31 = 4-31

Address:	0x009C	
Name:	oc1_divn_pdn	
Default:	0xF	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	—
3:2	pdn_b	INTDIV1 divider power down, frequency plan B. 0 = normal operation 3 = power down
1:0	pdn	INTDIV1 divider power down, frequency plan A. 0 = normal operation 3 = power down

Address:	0x009D	
Name:	oc1_divn_b	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	post_div_b	INTDIV1 post divider, frequency plan B. See oc1_divn::post_div at 0x9B.
4:0	div_b	INTDIV1 divider, frequency plan B. See oc1_divn::div at 0x9B.

Address:	0x009E	
Name:	oc2_divn	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	post_div	INTDIV2 post-divider, frequency plan A. See oc1_divn::post_div at 0x9B.
4:0	div	INTDIV2 divider, frequency plan A. See oc1_divn::div at 0x9B.

Address:	0x009F	
Name:	oc2_divn_pdn	
Default:	0xF	
Type:	R/W	
Bit Field	Function Name	Description
7:4	reserved	—
3:2	pdn_b	INTDIV2 divider power down, frequency plan B. See oc1_divn_pdn::pdn_b.
1:0	pdn	INTDIV2 divider power down, frequency plan A. See oc1_divn_pdn::pdn.

Address:	0x00A0	
Name:	oc2_divn_b	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	pos_div_b	INTDIV2 post divider, frequency plan B. See oc1_divn::post_div at 0x9B.
4:0	div_b	INTDIV2 divider, frequency plan B. See oc1_divn::div at 0x9B.

Address:	0x00A1:0x00A5	
Name:	fd1_div	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:0	—	FDIV1 frequency plan A fractional divider value. Bits 39:36 are integer. Bits 35:0 are fraction.

Address:	0x00A6:0x00A7	
Name:	fd1_den	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0	—	FDIV1 fractional divider denominator. Can be used with fd1_rem to sigma-delta modulate FDIV1's lsb when 0ppm frequency conversion from CLKIN is required.

Address:	0x00A8:0x00A9	
Name:	fd1_rem	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0	—	FDIV1 fractional divider denominator. Can be used with fd1_den to sigma-delta modulate FDIV1's lsb when 0ppm frequency conversion from CLKIN is required.

Address:	0x00AA:0x00AB	
Name:	fd1_ss_cnt	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0	—	FDIV1 frequency plan A spread spectrum count value.

Address:	0x00AC:0x00AF	
Name:	fd1_ss_id	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0	—	FDIV1 frequency plan A spread spectrum count value.

Address:	0x00B0	
Name:	fd1_config0	
Default:	0x30	
Type:	R/W	
Bit Field	Function Name	Description
7:6	fr_pdivn	FDIV1 frequency plan A. fractional divider post-divider. 0 = div 1 (bypass; not recommended), 1 = div 2 (typical value) 2 = div 4 3 = div 8
5:4	fr_pd	FDIV1 frequency plan A fractional divider power down control. 0 = Enable 3 = Power-down
3:0	reserved	

Address:	0x00B1	
Name:	fd1_config1	
Default:	0x80	
Type:	R/W	
Bit Field	Function Name	Description
7	mode	FDIV1 div bits write mode. When writing fd1_div or fd1_div_b: 0 = Each byte latched separately when written (not recommended) 1 = All bytes of the multi-byte field are latched when the last byte (highest address) is written
6:0	fr_gain_doff_s	FDIV1 frequency plan A gain offset. Signed 7-bit integer.

Address:	0x00B2	
Name:	fd1_config2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	fr_intg_mode	FDIV1 frequency plan A integer vs. fractional. Set this bit to match the desired divide value for FDIV1. 0 = Fractional mode 1 = Integer mode
6	en_rem_den	FDIV1 frequency plan A remainder denominator enable. 0 = Disabled, use internal rem=0, den=1 1 = Enabled, use registers fd1_rem and fd1_den
5:0	bp	FDIV1 frequency plan A fraction bit position. This defines the lsb of the fd1_div register's fractional bits below which the fd1_rem and fd1_den can be used for sigma delta modulation for exact 0ppm frequency conversion from the CLKIN signal. Number of bits used is 36-bp. 0 = 36 fractional bits(default) ... 12 = 24 fractional bits

Address:	0x00B3	
Name:	fd1_config3	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	enss	FDIV1 frequency plan A spread spectrum enable. 0 = Disabled 1 = Enabled
6	dwnen	FDIV1 frequency plan A spread spectrum down vs. center spread. 0 = Center 1 = Down
5	fr_wide	FDIV1 frequency plan A phase interpolator for div=4 selector. 0 = Normal 1 = div=4
4:0	reserved	Used to store calibration information. Please do not overwrite.

Address:	0x00B4:0x00B8	
Name:	fd1_div_b	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:0	—	FDIV1 frequency plan B fractional divider value. Bits 39:36 are integer. Bits 35:0 are fraction.

Address:	0x00B9:0x00BC	
Name:	fd1_ss_id_b	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0	—	FDIV1 frequency plan B spread spectrum increment/decrement value.

Address:	0x00BD:0x00BE	
Name:	fd1_ss_cnt_b	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0	—	FDIV1 frequency plan B spread spectrum count value.

Address:	0x00BF	
Name:	fd1_config4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	en_rem_den_b	FDIV1 frequency plan B remainder denominator enable. 0 = Disabled, use internal rem=0, den=1 1 = Enabled, use registers fd1_rem and fd1_den
6:0	gain_doff_s_b	FDIV1 frequency plan B gain offset. Signed 7-bit integer.

Address:	0x00C0	
Name:	fd1_config5	
Default:	0x60	
Type:	R/W	
Bit Field	Function Name	Description
7	fr_intg_mode_b	FDIV1 frequency plan B integer vs. fractional. Set this bit to match the desired divide value for FDIV1. 0 = Fractional mode 1 = Integer mode
6:5	fr_pd_b	FDIV1 frequency plan B fractional divider power down control. 0 = Enable 3 = Power-down
4:0	reserved	Used to store calibration information. Please do not overwrite.

Address:	0x00C1	
Name:	fd1_config6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	—
4	enss_b	FDIV1 frequency plan B spread spectrum enable. 0 = Disabled 1 = Enabled

3	dwnen_b	FDIV1 frequency plan B spread spectrum down vs. center spread. 0 = Center 1 = Down
2	fr_wide_b	FDIV1 frequency plan B phase interpolator for div=4 selector. 0 = Normal 1 = div=4
1:0	fr_pdivn_b	FDIV1 frequency plan B fractional divider post-divider. 0 = div 1 (bypass; not recommended), 1 = div 2 (typical value) 2 = div 4 3 = div 8

Address: Name: Default: Type:	0x00C2:0x00C6 fd2_div 0x0000000000 R/W	
Bit Field	Function Name	Description
39:0	—	FDIV2 frequency plan A fractional divider value. Bits 39:36 are integer. Bits 35:0 are fraction.

Address: Name: Default: Type:	0x00C7:0x00C8 fd2_den 0x0000 R/W	
Bit Field	Function Name	Description
15:0	—	FDIV2 fractional divider denominator. Can be used with fd2_rem to sigma-delta modulate FDIV2's lsb when 0ppm frequency conversion from CLKIN is required.

Address: Name: Default: Type:	0x00C9:0x00CA fd2_rem 0x0000 R/W	
Bit Field	Function Name	Description
15:0	—	FDIV2 fractional divider denominator. Can be used with fd2_den to sigma-delta modulate FDIV2's lsb when 0ppm frequency conversion from CLKIN is required.

Address: Name: Default: Type:	0x00CB:0x00CC fd2_ss_cnt 0x0000 R/W	
Bit Field	Function Name	Description
15:0	—	FDIV2 frequency plan A spread spectrum count value.

Address:	0x00CD:0x00D0	
Name:	fd2_ss_id	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0	—	FDIV2 frequency plan A spread spectrum count value.

Address:	0x00D1	
Name:	fd2_config0	
Default:	0x30	
Type:	R/W	
Bit Field	Function Name	Description
7:6	fr_pdivn	FDIV2 frequency plan A fractional divider post-divider. 0 = div 1 (bypass; not recommended), 1 = div 2 (typical value) 2 = div 4 3 = div 8
5:4	fr_pd	FDIV2 frequency plan A fractional divider power down control. 0 = Enable 3 = Power-down
3:0	reserved	—

Address:	0x00D2	
Name:	fd2_config1	
Default:	0x80	
Type:	R/W	
Bit Field	Function Name	Description
7	mode	FDIV2 div bits write mode. When writing fd2_div or fd2_div_b: 0 = Each byte latched separately when written (not recommended) 1 = All bytes of the multi-byte field are latched when the last byte (highest address) is written
6:0	fr_gain_doff_s	FDIV2 frequency plan A gain offset. Signed 7-bit integer.

Address:	0x00D3	
Name:	fd2_config2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	fr_intg_mode	FDIV2 frequency plan A integer vs. fractional. Set this bit to match the desired divide value for FDIV2. 0 = Fractional mode 1 = Integer mode
6	en_rem_den	FDIV2 frequency plan A remainder denominator enable. 0 = Disabled, use internal rem=0, den=1 1 = Enabled, use registers fd2_rem and fd2_den

5:0	bp	FDIV2 frequency plan A fraction bit position. This defines the lsb of the fd2_div register's fractional bits below which the fd2_rem and fd2_den can be used for sigma delta modulation for exact 0ppm frequency conversion from the CLKIN signal. Number of bits used is 36-bp. 0 = 36 fractional bits(default) ... 12 = 24 fractional bits

Address: Name: Default: Type:	0x00D4 fd2_config3 0x00 R/W	
Bit Field	Function Name	Description
7	enss	FDIV2 frequency plan A spread spectrum enable. 0 = Disabled 1 = Enabled
6	dwnen	FDIV2 frequency plan A spread spectrum down vs. center spread. 0 = Center 1 = Down
5	fr_wide	FDIV2 frequency plan A phase interpolator for div=4 selector. 0 = Normal 1 = div=4
4:0	reserved	Used to store calibration information. Please do not overwrite.

Address: Name: Default: Type:	0x00D5:0x00D9 fd2_div_b 0x0000000000 R/W	
Bit Field	Function Name	Description
39:0	—	FDIV2 frequency plan B fractional divider value. Bits 39:36 are integer. Bits 35:0 are fraction.

Address: Name: Default: Type:	0x00DA:0x00DD fd2_ss_id_b 0x00000000 R/W	
Bit Field	Function Name	Description
31:0	—	FDIV2 frequency plan B spread spectrum increment/decrement value.

Address: Name: Default: Type:	0x00DE:0x00DF fd2_ss_cnt_b 0x0000 R/W	
Bit Field	Function Name	Description
15:0	—	FDIV2 frequency plan B spread spectrum count value.

Address:	0x00E0	
Name:	fd2_config4	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	en_rem_den_b	FDIV2 frequency plan B remainder denominator enable. 0 = Disabled, use internal rem=0, den=1 1 = Enabled, use registers fd2_rem and fd2_den
6:0	gain_doff_s_b	FDIV2 frequency plan B gain offset. Signed 7-bit integer.

Address:	0x00E1	
Name:	fd2_config5	
Default:	0x60	
Type:	R/W	
Bit Field	Function Name	Description
7	fr_intg_mode_b	FDIV2 frequency plan B integer vs. fractional. Set this bit to match the desired divide value for FDIV1. 0 = Fractional mode 1 = Integer mode
6:5	fr_pd_b	FDIV2 frequency plan B fractional divider power down control. 0 = Enable 3 = Power-down
4:0	reserved	Used to store calibration information. Please do not overwrite.

Address:	0x00E2	
Name:	fd2_config6	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	—
4	enss_b	FDIV2 frequency plan B spread spectrum enable. 0 = Disabled 1 = Enabled
3	dwnen_b	FDIV2 frequency plan B spread spectrum down vs. center spread. 0 = Center 1 = Down
2	fr_wide_b	FDIV2 frequency plan B phase interpolator for div=4 selector. 0 = Normal 1 = div=4
1:0	fr_pdivn_b	FDIV2 frequency plan B fractional divider post-divider. 0 = div 1 (bypass; not recommended), 1 = div 2 (typical value) 2 = div 4 3 = div 8

6. Electrical Characteristics

This section provides information about Absolute Maximum Ratings, Operating Ratings, DC Electrical Characteristics, AC Electrical Characteristics and Temperature Specifications.

6.1. Absolute Maximum Ratings

The following table lists the absolute maximum rating details.

Table 6-1. Absolute Maximum Ratings

Description	Min.	Max.	Units
Supply Voltage (V_{DD})	–0.5	+4.6	V
Input Voltage (V_{DD})	–0.5	V_{DD} + 0.5	V
ESD Protection (HBM)	TBD		
ESD Protection (MM)	TBD		
ESD Protection (CDM)	TBD		
Note: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions may affect device reliability.			

6.2. Operating Ratings

The following table lists the operating rating details.

Table 6-2. Operating Ratings

Description	Min.	Max.	Unit
1.8V Operating Voltage (V_{DD})	+1.71	+1.98	V
2.5V Operating Voltage (V_{DD})	+2.25	+2.75	V
3.3V Operating Voltage (V_{DD})	+2.97	+3.63	V
Note: The data sheet limits are not ensured if the device is operated beyond the recommended operating conditions.			

6.3. DC Electrical Characteristics

The following table lists the DC electrical characteristics.

Table 6-3. DC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 1.8V +10%/-5%, V_{DD} = 2.5V ±10%, V_{DD} = 3.3V ±10%, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Supply Voltage	V_{DD}	1.71	—	3.63	V	—
Power Supply Ramp	t_{PU}	0.1	—	10	ms	—
Core Total Supply Current	I_{DD}	—	72	—	mA	Digital + APLL + 2xFracDiv + 2xINTDiv
		—	37	—	mA	Digital + APLL + 1xINTDiv
Standby Current	I_{STDBY}	—	10	—	mA	All Outputs OFF

Table 6-3. DC Electrical Characteristics (continued)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 1.8V +10%/-5%, V_{DD} = 2.5V ±10%, V_{DD} = 3.3V ±10%, T_A = –55 °C to +115 °C								
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**		
Output Buffer Supply Current	I_{DDOX}	—	33.5	—	mA	LVPECL Output @ 156.25MHz		
		—	8	—	mA	LPHSCL Output @ 100MHz		
		—	20	—	mA	LVDS Output @ 156.25MHz		
		—	17.2	—	mA	3.3V LVCMOS Output @ 170MHz, 2pF load, 5” trace length	Drive strength 0	1 Output
		—	31.6	—				2 Outputs
		—	19.9	—			Drive strength 1	1 Output
		—	37.0	—				2 Outputs
		—	12.3	—	mA	2.5V LVCMOS Output @ 170MHz, 2pF load, 5” trace length	Drive strength 0	1 Output
		—	21.7	—				2 Outputs
		—	15.0	—			Drive strength 1	1 Output
		—	27.2	—				2 Outputs
		—	8.0	—	mA	1.8V LVCMOS Output @ 170MHz, 2pF load, 5” trace length	Drive strength 0	1 Output
		—	13.1	—				2 Outputs
		—	10.0	—			Drive strength 1	1 Output
		—	17.2	—				2 Outputs
Total Power Consumption	P_{DD}	—	270	—	mW	Core powered with 1.8V and enabled: 2x2.5V LVDS output @ 156.25MHz 2x1.8V HCSL output @ 100MHz 2x3.3V CMOS output @ 25MHz		
Differential Input Logic Levels	V_{IHD}	0.15	—	—	V	CLKIN, /CLKIN (differential input)		
	V_{ILD}	—	—	–0.15	V			
HCSL Single-Ended Input Common Mode Voltage	V_{SIC}	0.25	—	0.55	V	—		
Single-Ended CMOS Input Logic Levels	V_{IHSE}	0.8 x V_{DD}	—	—	V	CLKIN (Single-ended input)		
	V_{ILSE}	—	—	0.2 x V_{DD}	V			
Single-Ended CMOS CLKIN Hysteresis	$HYSf_{ISE}$	—	0.5	—	V	—		
Control Input Logic Levels	V_{IHC}	0.7 x V_{DD}	—	—	V	Control pins: GPIOs, SDA, SCL		
	V_{ILC}	–0.3	—	0.3 x V_{DD}	V			

6.3.1. LVPECL DC Electrical Characteristics

The following table lists the LVPECL DC Electrical Characteristics.

Table 6-4. LVPECL DC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Output High Voltage	V_{OH}	V_{DDO}–1.145	V_{DDO}–0.97	V_{DDO}–0.845	V	50Ω to V_{DDO} – 2V

Table 6-4. LVPECL DC Electrical Characteristics (continued)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Output Low Voltage	V_{OL}	V_{DDO}–1.945	V_{DDO}–1.77	V_{DDO}–1.645	V	50Ω to V_{DDO} – 2V
Common Mode Voltage	V_{CM}	—	V_{DDO} -1.4	—	V	—

6.3.2. LVDS DC Electrical Characteristics

The following table lists the LVDS DC electrical characteristics details.

Table 6-5. LVDS DC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Offset Voltage (Common Voltage)	V_{OS}	—	1.2	—	V	V_{DD} = 2.5V/3.3V
		—	1.1	—	V	V_{DD} = 1.8V
V_{OS} Magnitude Change	ΔV_{OS}	–50	—	50	mV	—

6.3.3. LPHCSL DC Electrical Characteristics

The following table lists the LPHCSL DC electrical characteristics details.

Table 6-6. LPHCSL DC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Output High Voltage	V_{OH}	600	750	900	mV	—
Output Low Voltage	V_{OL}	–150	0	27	mV	—
Common Voltage	V_{CM}	—	0.4	—	V	—
Differential Output Impedance	R_{OUT}	—	100	—	Ω	Default
		—	85	—	Ω	Optional (OTP option)

6.3.4. LVCMOS DC Electrical Characteristics

The following table lists the LVCMOS DC electrical characteristics details.

Table 6-7. LVCMOS DC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Output High Voltage	V_{OH}	0.8 x V_{DD0}	—	—	V	Note 1
Output Low Voltage	V_{OL}	—	—	0.2 x V_{DD0}	V	Note 2

Table 6-7. LVCMOS DC Electrical Characteristics (continued)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**

Notes:

1. V_{OH} measured at I_{OH} = –6 mA/–3.5 mA/–2 mA for drive strength 0 and I_{OH} = –10 mA/–6.5 mA/–4 mA for drive strength 1 when V_{DDO} = 3.3V/2.5V/1.8V respectively.
2. V_{OL} measured at I_{OL} = 6 mA/3.5 mA/2 mA for drive strength 0 and I_{OL} = 10 mA/6.5 mA/4 mA for drive strength 1 when V_{DDO} = 3.3V/2.5V/1.8V respectively.

6.4. AC Electrical Characteristics

The following table lists the AC electrical characteristics details.

Table 6-8. AC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, C_{LOAD} = 2pF, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Input Slew Rate	SR_{IN}	0.6	—	—	V/ns	—
Input Voltage Swing	V_{ASWING}	0.15	—	—	Vdiff	—
Differential Absolute Max Input Voltage	$V_{IN(MAX)}$	—	—	+1.15	V	Note 1, Note 2
SE CMOS Absolute Max Input Voltage		—	—	V_{DD} + 0.3	V	Note 1, Note 2
Differential Absolute Min Input Voltage	$V_{IN(MIN)}$	–0.3	—	—	V	Note 1, Note 3
SE CMOS Absolute Min Input Voltage		–0.3	—	—	V	Note 1, Note 3
Differential Input Frequency	f_{IN}	10	—	250	MHz	PLL mode (no lower limit in buffer mode)
Input Frequency (Single-Ended CMOS CLKIN)	f_{IN_SE}	10	—	200	MHz	PLL mode (no lower limit for buffer mode)
Input Duty Cycle	IDC	35	—	65	%	—
Input Capacitance	C_{IN}	—	—	5	pF	—
Output-Output Crosstalk	XTALK	—	-78	—	dBc	Note 4
Output Duty Cycle	ODC	45	50	55	%	Note 5, Figure 6-2, 50% input duty cycle, PLL mode
Output-to-Output Skew	t_{SKEW}	—		100	ps	—
Start-Up Time	t_{START}	—	3	—	ms	—
Input-to-Output Delay (single-ended)	t_{PD}	—	3	—	ns	PLL-Bypass mode
Input-to-Output Delay (Differential output mode)		—	2	—	ns	PLL-Bypass mode
Output Enable Time	t_{EN}	—	3	—	cycles	Output frequency cycle

Table 6-8. AC Electrical Characteristics (continued)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, C_{LOAD} = 2pF, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Output Disable Time	t_{DIS}	—	3	—	cycles	Output frequency cycle
Frequency Stability	Δf_S	—	—	TBD	ppm	—
Aging	Δf_A	—	—	±5	ppm	1st year @ 25ºC
		—	—	±1	ppm	Per year after 1st year
RMS Jitter Generation, PLL Locked to External Crystal Oscillator	J_{GENMO}	—	180	—	fs	INT Mode, 12kHz to 20 MHz @ 100 MHz, Note 6
		—	380	—	fs	FRAC Mode, 12 kHz to 20 MHz @ 100 MHz, Note 6
RMS Jitter as per PCIe 5.0 (PLL_BW = 0.5 to 1.8MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	12	—	fs	SSC off
		—	25	—		SSC – 0.3%
		—	25	—		SSC – 0.5%
RMS Jitter as per PCIe 6.0 (PLL_BW = 0.5 to 1MHz, CDR for 64 GT/s CC)	$t_{jPCIe\_6.0}$	—	9	—	fs	SSC off
		—	18	—		SSC – 0.3%
		—	18	—		SSC – 0.5%
RMS Jitter as per PCIe 7.0 (PLL_BW = 0.35 to 1.8MHz, CDR for 128 GT/s CC)	$t_{jPCIe\_7.0}$	—	6	—	fs	SSC off
		—	13	—		SSC – 0.3%
		—	13	—		SSC – 0.5%
Spread Spectrum Modulation Frequency	f_{SSC}	30	—	33	kHz	—
Spread Spectrum Frequency Deviation	f_{SSCdev}	–2.5	—	2.5	%	Center Spread
		–2.5	—	0	%	Down Spread

1. Measurement taken from a single-ended waveform.
2. Defined as the maximum instantaneous voltage including overshoot.
3. Defined as the minimum instantaneous voltage including undershoot.
4. Measured across two adjacent LVDS outputs with the victim running at 155.52MHz and the aggressor running at 156.25MHz, other outputs being disabled.
5. Measurement taken from differential waveform.
6. All jitter measurements are done with one output enabled @ 100MHz and set to LPHCSL differential format.

6.4.1. LVPECL AC Electrical Characteristics

The following table lists the LVPECL AC electrical characteristics details.

Table 6-9. LVPECL AC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, C_{LOAD} = 2pF, T_A = –55 °C to +115 °C.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Output Frequency	f_{OUT}	0.35	—	662	MHz	—
Output Voltage Swing	V_{SWING}	0.6	0.8	1.0	V	—

Table 6-9. LVPECL AC Electrical Characteristics (continued)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, C_{LOAD} = 2pF, T_A = –55 °C to +115 °C.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
LVPECL Output Rise/ Fall Time	t_R/t_F	—	350/420	—	ps	20% – 80%

6.4.2. LVDS AC Electrical Characteristics

The following table lists the LVDS AC electrical characteristics details.

Table 6-10. LVDS AC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, C_{LOAD} = 2pF, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Output Frequency	f_{OUT}	0.35	—	662	MHz	—
Differential Output Voltage	V_{OD}	275	350	475	mV	V_{DDO} = 2.5V/3.3V
		—	270	—	mV	V_{DDO} = 1.8V
V_{OD} Magnitude Change	ΔV_{OD}	—	—	40	mV	—
LVDS Output Rise/ Fall Time	t_R/t_F	—	200/200	—	ps	20% – 80%

6.4.3. LPHCSL AC Electrical Characteristics

The following table lists the LPHCSL AC electrical characteristics details.

Table 6-11. LPHCSL AC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, C_{LOAD} = 2pF, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Condition**
Output Frequency	f_{OUT}	0.35	—	250	MHz	—
Output Swing	—	—	0.8	—	V_{PP}	HCSL, Figure 6-1
Output Rise/Fall Time	t_R/t_F	—	260/310	—	ps	20% – 80%
Rising Edge Rate	—	0.6	—	4.0	V/ns	Note 1, Note 2
Falling Edge Rate	—	0.6	—	4.0	V/ns	Note 1, Note 2
Absolute Crossing Point Voltage	V_{CROSS}	+250	—	+550	mV	Note 3, Note 4, Note 5, Figure 6-1
Variation of V_{CROSS} over All Clock Edges	$V_{CROSS\ DELTA}$	—	—	+140	mV	Note 3, Note 4, Note 6, Figure 6-3
Ringback Voltage Margin	V_{RB}	–100	—	+100	mV	Note 1, Note 7, Figure 6-4
Time Before V_{RB} is Allowed	t_{STABLE}	500	—	—	ps	Note 1, Note 7

Table 6-11. LPHCSL AC Electrical Characteristics (continued)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, C_{LOAD} = 2pF, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Condition**

1. Measurement taken from differential waveform.
2. Measured from –150mV to +150mV on the differential waveform (derived from OUTx minus OUTxb). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
3. Measurement taken from single ended waveform.
4. Measured at crossing point where the instantaneous voltage value of the rising edge of OUTx equals the falling edge of OUTxb.
5. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
6. Defined as the total variation of all crossing voltages of Rising OUTx and Falling OUTxb. This is the maximum allowed variance in V_{CROSS} for any particular system.
7. t_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100mV differential range.

6.4.4. LVCMOS AC Electrical Characteristics

The following table lists the LVCMOS AC electrical characteristics details.

Table 6-12. LVCMOS AC Electrical Characteristics

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V +10%/-5%, C_{LOAD} = 2pF, T_A = –55 °C to +115 °C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Output Frequency	f_{OUT}	0.35	—	200	MHz	—
Output Rise/Fall Time	t_R/t_F	—	700	—	ps	20% – 80%

6.5. Temperature Specifications

The following table lists the temperature specifications.

Table 6-13. Temperature Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Temperature Ranges						
Operating Ambient Temperature Range	T_A	–55	—	115	°C	—
Junction Operating Temperature	T_J	—	—	125	°C	Note 1
Storage Temperature Range	T_S	–55	—	150	°C	—
Soldering Temperature	—	—	+260	—	°C	Soldering, 20 sec.
VQFN28 Package						
Moisture Level for VQFN package	—	MSL1				—
Junction-to-Ambient Thermal Resistance, in Air, for VQFN package (Note 3)	Θ_{JA}	—	16.2	—	ºC/W	Note 2
Junction-to-Board Thermal Resistance, in Air, for VQFN package	Θ_{JB}	—	4.2	—	°C/W	Note 2
Junction-to-Case Thermal Resistance, in Air, for VQFN package	Θ_{JC}	—	38.5	—	°C/W	Junction to top of case.

Table 6-13. Temperature Specifications (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Junction-to-Pad Thermal Resistance, in Air, for VQFN package (Note 4)	Θ_{JP}	—	0.67	—	°C/W	—
CQFP32 Package						
Junction-to-Ambient Thermal Resistance, in Air, for CQFP32 package	Θ_{JA}	—	35.3	—	°C/W	—
Junction-to-Board Thermal Resistance, in Air, for CQFP32 package	Θ_{JB}	—	18	—	°C/W	—
Junction-to-Case Thermal Resistance, in Air, for CQFP32 package	Θ_{JC}	—	35.9	—	°C/W	Junction to top of case
Junction-to-Case Thermal Resistance, in Vacuum, for CQFP32 package	Θ_{JC}	—	14	—	°C/W	Junction to top of case
Junction-to-Bottom-Package Thermal Resistance, in Vacuum, for CQFP32 package	—	—	7.3	—	°C/W	—

1. The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction to air (that is, T_A, T_J, Θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125 °C rating. Sustained junction temperature above +125 °C can impact the device reliability.
2. Package thermal resistance assumes that the exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. Θ_{JB} and Θ_{JA} values are determined for a 4-layer board in still-air number.
3. Theta-JA (Θ_{JA}) is the thermal resistance from junction to ambient when dissipating maximum power.
4. Theta-JP (Θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

Figure 6-1. Single-Ended Measurement Points for Absolute Cross Point and Swing

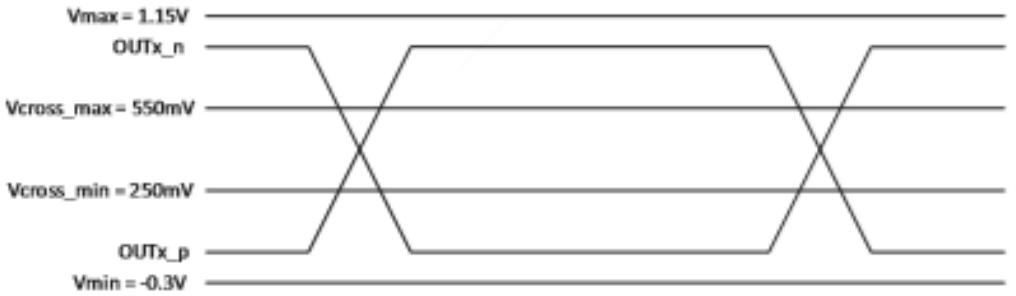


Figure 6-2. Differential Measurement Points for Duty Cycle and Period

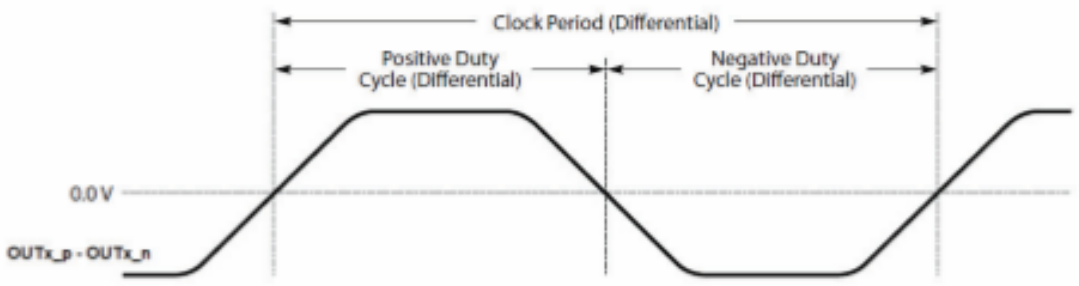


Figure 6-3. Single-Ended Measurement Points for Delta Cross Point

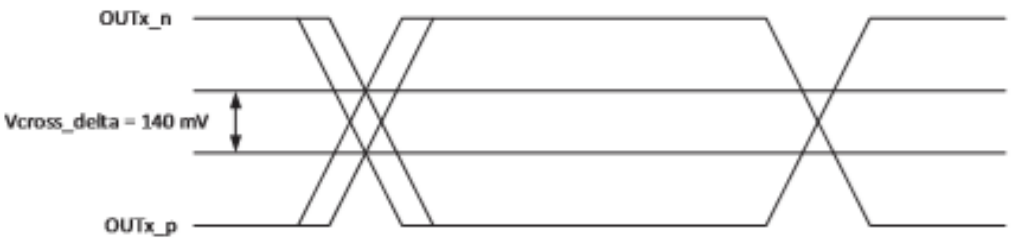
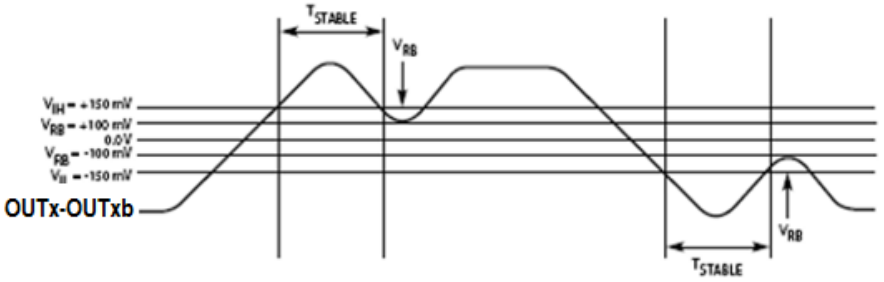
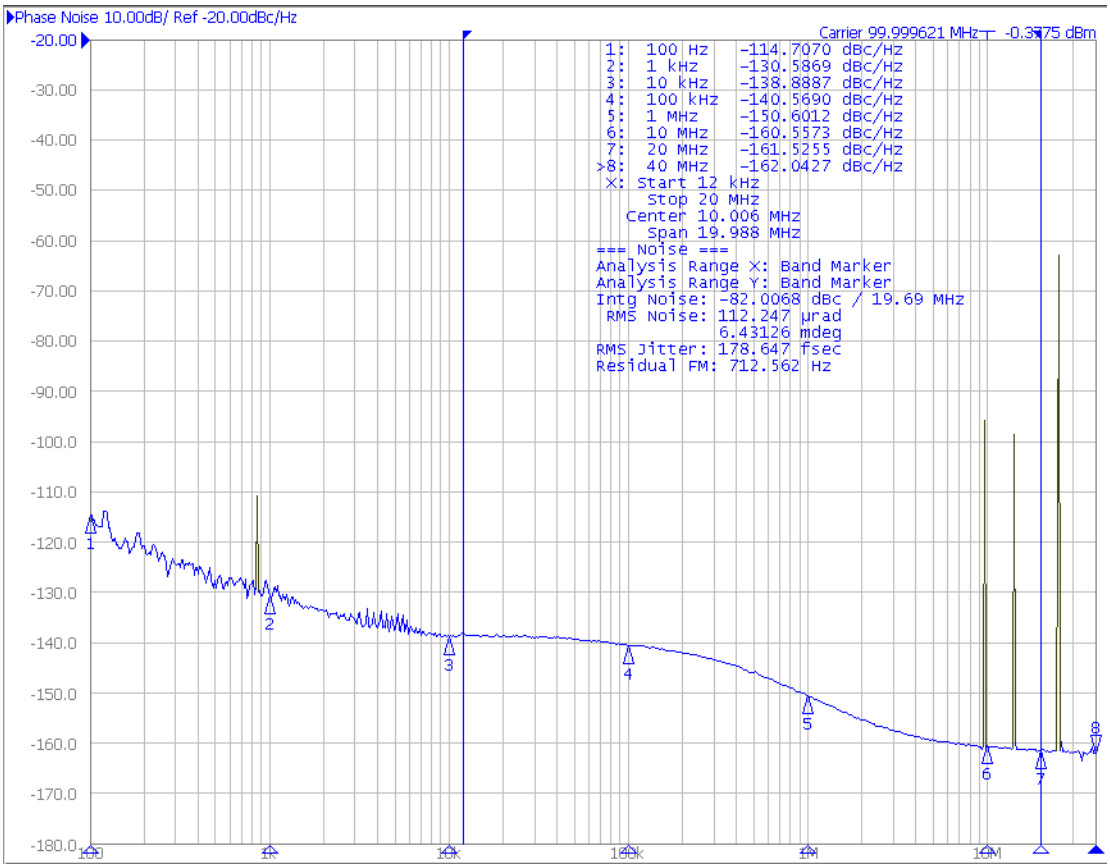


Figure 6-4. Differential Measurement Points for Ringback



7. Typical Operating Characteristics

Figure 7-1. Example of Phase Noise Plot at 100 MHz

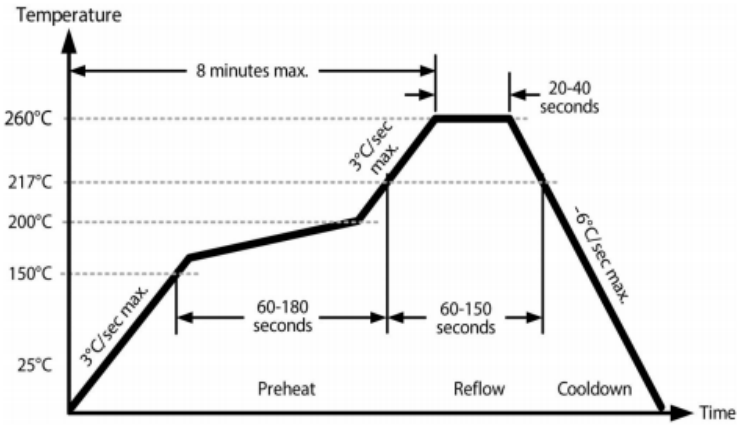


8. Solder Reflow Profile

8.1. VQFN Package

The suggested soldering flow profiles are provided as helpful guidelines.
Note: Microchip cannot guarantee results and is not responsible for any issues that may arise from following these recommendations.

Figure 8-1. Solder Reflow Profile



MSL 1 @ 250°C Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	–6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

8.2. CQFP Package

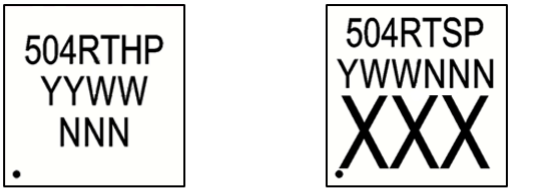
See the device's Qualpack document, which is available upon request from your Microchip Technology sales office.

9. Packaging Information

9.1. VQFN Package

9.1.1. Package Marking Drawing for VQFN Package

Figure 9-1. Package Marking Drawing for VQFN Package

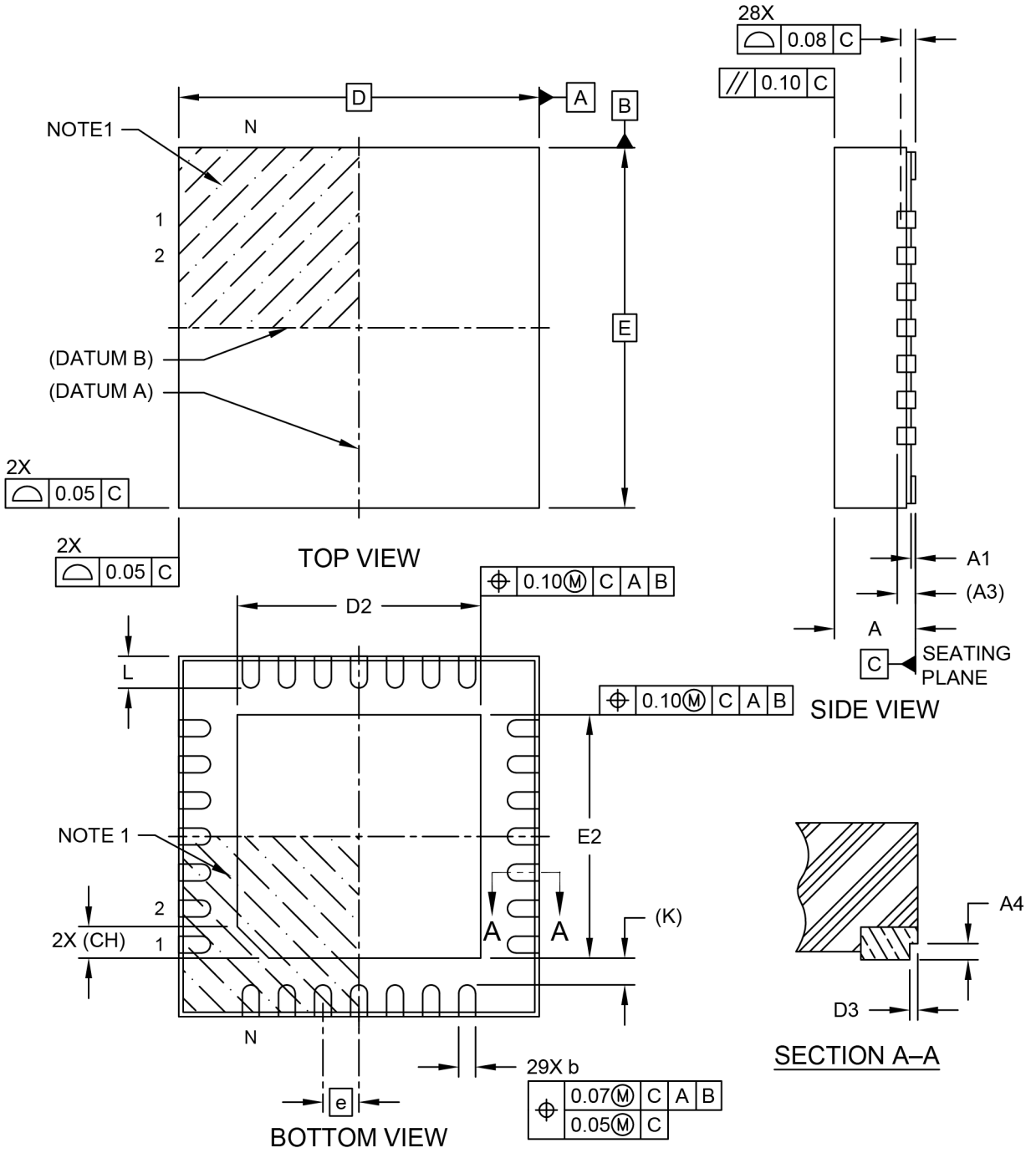


Legend	
	504RTHP : Hirel Plastic / 504RTSP : QML-P Equivalent
YY or Y:	Year code (Last 2 digit or last digit of calendar year)
WW:	Week code (week of January 1 is '01')
NNN:	Alphanumeric tracability code (week)
XXX:	Serial number for QML-P Equivalent
•	Pin one index is identified by a dot

9.1.2. Package Outline Drawing and Land Pattern for VQFN

28-Lead Very Thin Plastic Quad Flat, No Lead Package (ZXX) - 4x4x0.9 mm Body [VQFN] With 2.7 mm Exposed Pad and Stepped Wettable Flanks

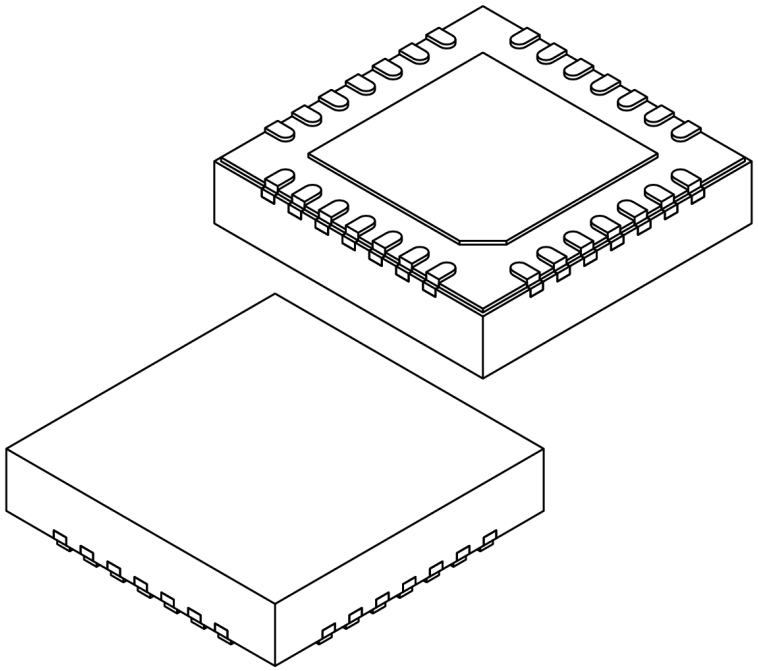
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-532 Rev B Sheet 1 of 2

28-Lead Very Thin Plastic Quad Flat, No Lead Package (ZXX) - 4x4x0.9 mm Body [VQFN] With 2.7 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.25 REF	
Exposed-Pad Index Chamfer	CH		0.35 REF	
Wettable Flank Step Cut Length	D3		0.05 REF	
Wettable Flank Step Cut Height	A4		0.10 REF	

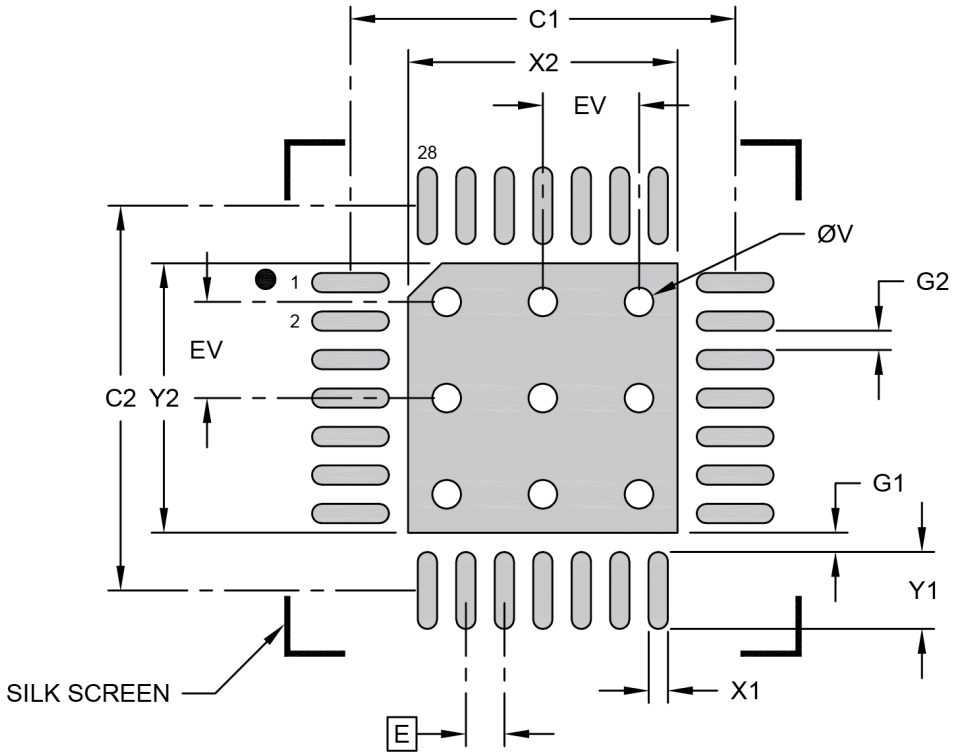
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-532 Rev B Sheet 2 of 2

28-Lead Very Thin Plastic Quad Flat, No Lead Package (ZXX) - 4x4x0.9 mm Body [VQFN] With 2.7 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			2.80
Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Contact Pad to Center Pad (X28)	G1	0.20		
Contact Pad to Contact Pad (X24)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

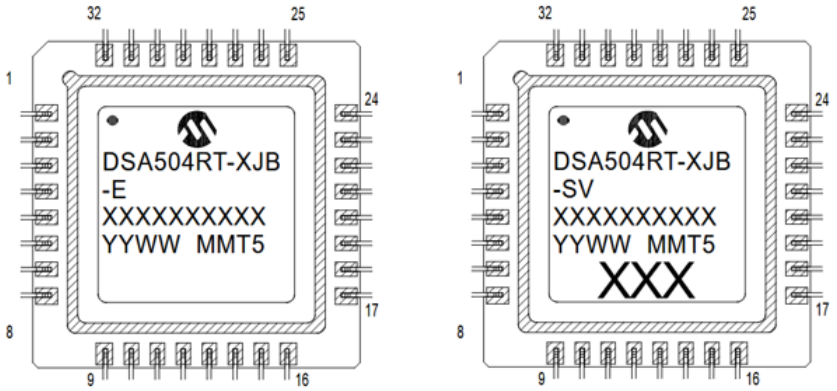
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2532 Rev B

9.2. CQFP32 Ceramic Package

9.2.1. Package Marking Drawing for CQFP32 Package

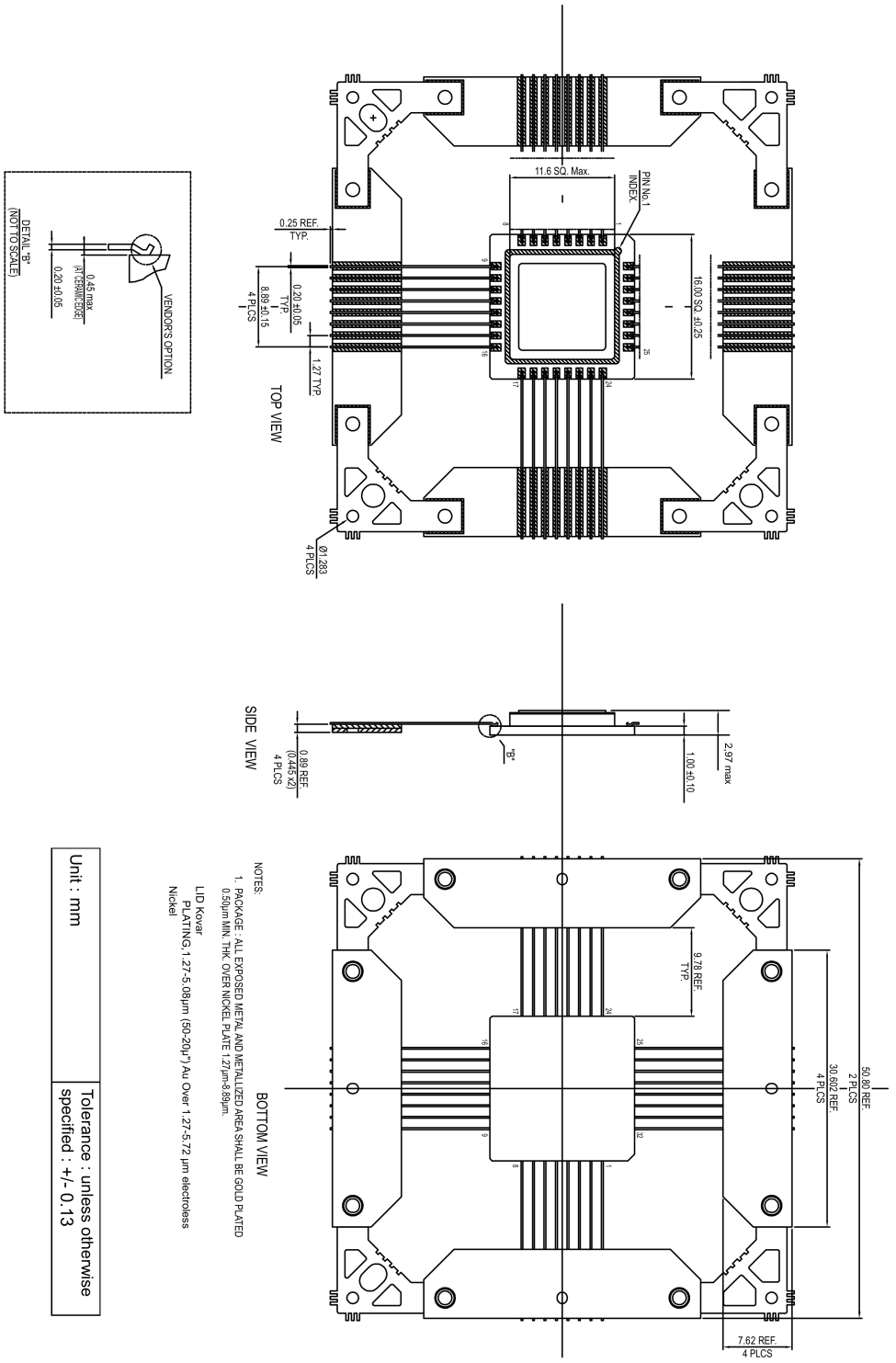
Figure 9-2. Package Marking Drawing for CQFP32 Package



Legend:	DSA504RT-XJB
-E, -MQ, -SV, -HC	Quality flow
XXXXXXXXXX:	Lot Reference Number
YY:	Year code (Last 2 digit of calendar year)
WW:	Week code (week of January 1 is '01')
MMT5	Location Code
XXX:	Serialization (SV quality flow only)
•	Pin one index is identified by a dot

9.2.2. Package Marking Outline Drawing for CQFP32 Package

Figure 9-3. Package Marking Outline Drawing for CQFP32 Package



10. Product Identification System

The following table lists the product identification code and description.

Table 10-1. Product Identification System

Part Number	-XXX	-YY	-0XXXX
	Package	Quality Flow	Configuration Code
Device	—	—	DSA504RT
Package	—	—	ZXX = 28-Lead 4 mm × 4 mm VQFN XJB = 32-Lead 16 mm × 16 mm CQFP
Quality Flow	—	—	E = Engineering Samples MQ = QML-Q Equivalent SV = QML-V Equivalent HP = Hirel Plastic HC = Hirel Ceramic SP = QML-P Equivalent
Configuration Code	—	—	0XXXX = Code generated by the factory during part creation

Note: VQFN parts are delivered in a waffle package; CQFP is delivered in an individual box.

11. Ordering Information

Note: For more information on DSA504RT device availability and ordering, contact your authorized Microchip Technology sales representative.

The following table lists the DSA504RT ordering information.

Table 11-1. DSA504RT Ordering Information

Ordering Code	Package	Operating Temperature	Quality Flow
DSA504RT-ZXX-HP	VQFN28	−55 °C to +115 °C	Hirel Plastic
DSA504RT-ZXX-SP	VQFN28	−55 °C to +115 °C	QML-P Equivalent
DSA504RT-XJB-E	CQFP32	+25 °C	Engineering Samples
DSA504RT-XJB-MQ	CQFP32	−55 °C to +115 °C	QML-Q Equivalent
DSA504RT-XJB-SV	CQFP32	−55 °C to +115 °C	QML-V Equivalent
DSA504RT-XJB-HC	CQFP32	−55 °C to +115 °C	Hirel Ceramic

12. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	6/2026	Following is a list of changes made in this revision: • Updated the Introduction section. • Updated the values of ESD and Mass in the Features section. • Updated the T_A range from –40 °C to +105 °C to –55 °C to +115 °C in the following sections: – DC Electrical Characteristics – LVPECL DC Electrical Characteristics – LVDS DC Electrical Characteristics – LPHCSL DC Electrical Characteristics – LVCMOS DC Electrical Characteristics – AC Electrical Characteristics – LVPECL AC Electrical Characteristics – LVDS AC Electrical Characteristics – LPHCSL AC Electrical Characteristics – LVCMOS AC Electrical Characteristics • Removed the *Power Supply Rejection Ratio* parameter from the Table 6-8. • Removed the *Single-Ended Measurement Points for Rise and Fall Time Matching* figure from the Temperature Specifications section. • Updated the pin descriptions of 2, 3, 8 and 28 pins. See the Table 2-1 section. • Removed the 0x004B:0x004C and 0x004D:0x004E tables from Register Map. • Updated the 0x004F:0x0050, 0x0051, 0x0052, 0x0055 and 0x0056 tables from Register Map. • Updated the values of RMS Jitter in the Table 6-8. • Replaced with a new image. See Figure 7-1. • Removed the Example of Phase Noise Plot at 156.25 MHz figure from the Figure 7-1 section. • Replaced with a new image. See Figure 9-3. • Updated the Ordering Code from DSA504RT-ZZX-HP to DSA504RT-ZXX-HP and from DSA504RT-ZZX-SP to DSA504RT-ZXX-SP. See the Ordering Information section.
A	12/2025	Initial Revision

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