

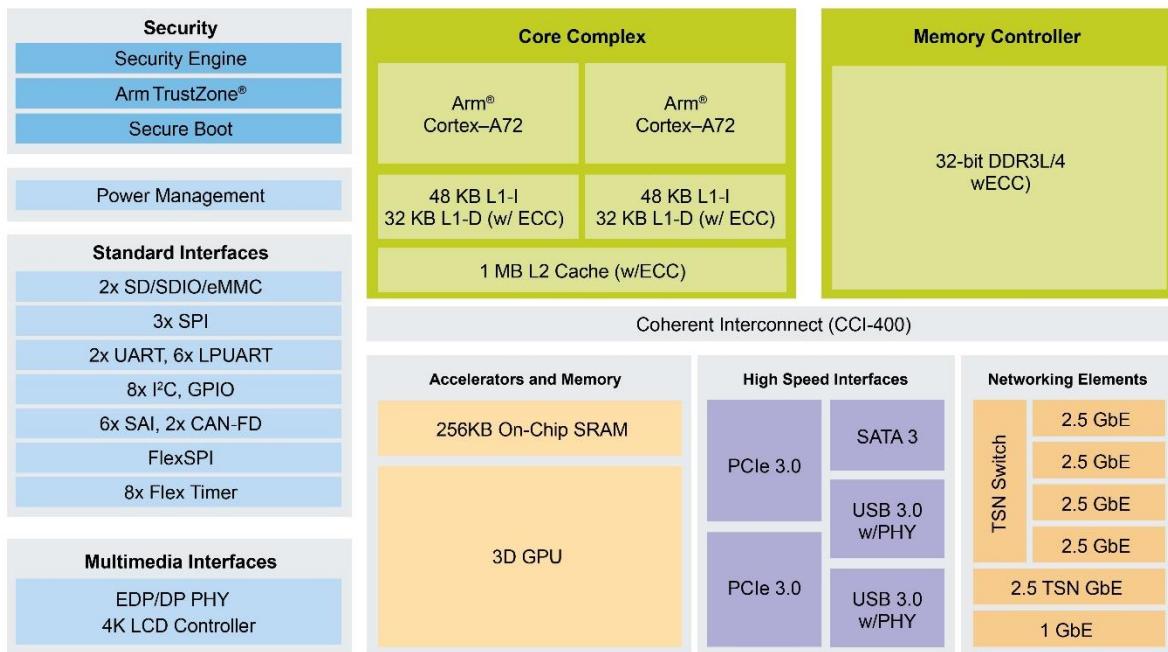
LS1028A Family Update: June 15th, 2023

Product Summary:

The Layerscape LS1028A processors for industrial and automotive applications integrate the high-performance Arm® Cortex®-A72 processor, Ethernet switching with TSN, Ethernet controller and Trust Architecture with Security Engine to support converged IT and OT networks.

Two powerful 64-bit Arm A72 cores support real-time processing for industrial control and virtual machines for edge computing in the IoT. The integrated 3D GPU with support for 4K display and LCD controller enable Human-Machine Interface (HMI) systems with next-generation interfaces. Integrated Trust Architecture with cryptographic offload provides a trusted platform with encrypted communications for secure applications and services.

LS1028A Block Diagram:



Target Market:

- Industrial
 - 3-Phase AC Induction Motor
 - Avionics
 - Brushless DC Motor (BLDC) Control
 - Building Security
 - Electricity Grid and Distribution
 - Energy Gateway
 - Industrial HMI
 - Motion Control and Robotics
 - Permanent Magnet Synchronous Motor (PMSM)
- Communication Infrastructure

- Broadband Modem
- Ethernet Switch
- Industrial and IoT Gateway
- Automotive – Gateway

LS1028A Feature List:

- Core Complex
 - Two 32/64-bit ARM® Cortex®-A72 cores— Up to 1.5 GHz operation
 - Single-threaded cores with 48KB L1 instruction cache and 32KB L1 data cache, Single cluster of two cores sharing 1MB L2 cache
- Networking Elements
 - Four SerDes lanes for high-speed peripheral interfaces
 - Two PCI Express 3.0 controllers (RC or EP)
 - Ethernet Controller with TSN functionality
 - TSN Capable Ethernet Switch with four external ports
 - 4 x 2.5 G/1 G switched Eth (TSN enabled), 1 x 2.5 G/1 G Eth (TSN enabled), 1 x 1 G Eth
 - One Serial ATA (SATA 6 Gbit/s) controller
- Accelerators and Memory Control
 - 32-bit DDR3L/DDR4 + ECC with speeds up to 1.6GT/s
 - One Queue Direct Memory Access Controller (qDMA)
 - One Enhanced Direct Memory Access Controller (eDMA)
- Basic Peripherals and Interconnect
 - Two high-speed USB 2.0/3.0 controllers with integrated PHY
 - Two Enhanced Secure Digital Host Controllers (eSDHC) supporting SD 3.0, eMMC 4.4 and eMMC 4.5 and eMMC 5.1
 - Two Controller Area Network (CAN) modules, optionally supporting Flexible Data-rate
 - Three Serial Peripheral Interface (SPI) controllers. One FlexSPI controller
 - Eight I2C controllers
 - One 16550-compliant DUART, Six LPUARTs
 - General Purpose IO (GPIO)
 - Six Synchronous Audio Interface (SAI)
- Display and GPU
 - One LCD controller and Display port/eDP interface
 - GPU supporting Geometry rate 100 Mtri/sec, Pixel rate 650 Mpixel/sec, GFLOPS(32-bit high precision) = 10.4
- Additional Features
 - Thermal Monitor Unit (TMU)
 - FC-PBGA package, 17 mm x 17 mm

Difference between family members:

Features	LS1028A	LS1027A	LS1018A	LS1017A
Arm core	2 x Cortex-A72	2 x Cortex-A72	1 x Cortex-A72	1 x Cortex-A72
GPU	1 x GC7000UltraLite	-	1 x GC7000UltraLite	-
Power (1.3GHz CPU Speed, Thermal Vdd at 105C)	7.2W	6.8W	6.4W	5.8W

Longevity:

The LS1028A product family is covered under the NXP Product Longevity Program. The products are guaranteed available until 2033. Additional details [here](#).

Layerscape Linux Enablement

- LS1028A is supported in the Layerscape Linux Distribution POC (Layerscape SDK). Latest Rev. L5.15.71-2.2.0, released 17 Feb 2023.
- LTS kernel v5.15.52 supporting Preempt RT Kernel v5.15.71
- Bootloader: U-Boot v2022.04 update
- Toolchain: gcc: glibc-2.35, binutils2.38, gdb-11.2
- DPDK 21.11, supporting L2fwd, L3fwd, L2fwd-crypto and ipsec-gw application, OVS-DPDK 2.17.
- OPTEE
- More info can be found [here](#).

Real Time Edge Software:

The real-time edge software enables real-time applications that can be easily integrated with the Yocto SDKs. Real-time edge software enables real-time capabilities via support for Preempt-RT for low latency applications, baremetal framework and support for real-time operating system (RTOS) on the Arm®-Cortex®-A or Cortex®-M cores. Real-time edge software also supports real-time protocols and stacks for IEEE1588 PTP network synchronization, time sensitive networking (real-time ethernet), EtherCAT leader, CANOpen and OPC-UA. More info can be found [here](#).

Reference Designs:

LS1028A Reference Design Board:

The LS1028A reference design board (RDB) is a computing, evaluation, and development platform that supports industrial IoT applications, human machine interface solutions, and industrial networking.

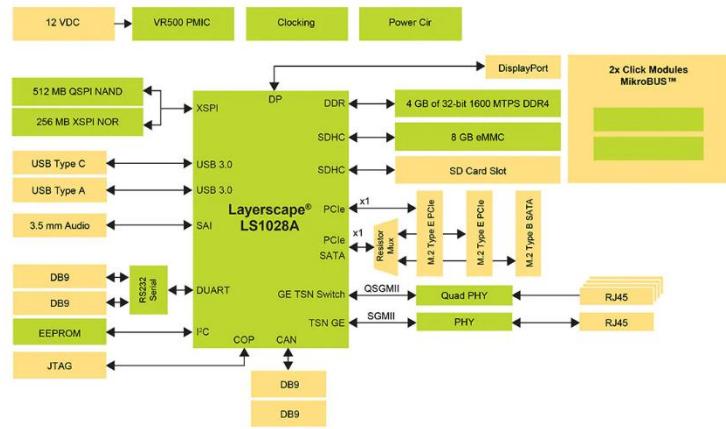
The LS1028A processor is dual-core 64-bit Arm® Cortex®-A72. The LS1028ARDB can help reduce development time by providing a reference for custom board development, a debug tool to check behavior on the board compared to custom board designs and comes pre-loaded with the embedded Linux® Software Development Kit (SDK) for Layerscape® processors



Features:

- Processor
 - Layerscape LS1028A dual-core processor based on Cortex-A72 at 1.3 GHz
 - ECC on internal L1, L2 caches for high-reliability applications
- Memory
 - 4 GB DDR4 SDRAM w/ECC
 - 32-bit DDR4 bus at data rates up to 1600 MT/s
 - 256 MB QSPI NOR flash

- 512 MB QSPI NAND flash
- 8 GB eMMC
- SDHC port connected to full-size SD slot
- Ethernet
 - x1 RJ45 connector for 1Gbps Ethernet support w/TSN, 1588
 - x4 RJ45 connector for 1Gbps Ethernet switch support w/TSN, 1588 (QSGMII)
- Basic Peripherals and Interconnect
 - 2x M.2 Type E slots with PCIe Gen 3.0 x1
 - 1x M.2 Type B slot with SATA 3.0 (resistor mux with 1 Type E slot)
 - 1x Type A USB 3.0 super-speed port
 - 1x Type C USB 3.0 super-speed port
 - 1x DisplayPort interface
 - 2x DB9 RS232 serial ports
 - 2x DB9 CAN interfaces
 - 1x 3.5 mm audio out
 - 2x MikroBUS™ sockets
- More details can be found [here](#).



Customer board-level solutions:

- Miriac MPX-LS1028A, Compact SoM with TSN, security engine and HMI. More info can be found [here](#).



- Miriac SBC-LS1028A-TSN, Single Board Computer based on LS1028A CPU. More info can be found [here](#).



- Kontron LS1028A SMARC-sAL28, SMARC MODULE WITH NXP LS1028A IN SHORT SIZE. More info can be found [here](#).



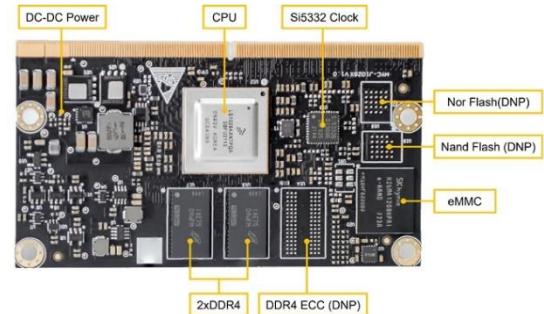
- TQ Systems, Embedded Module TQMLS1028A, Embedded module based on LS1028A with 4 Port TSN Gigabit Ethernet Switch for Real time demands. More info can be found [here](#).



- Forlinx, FET1028A-C System on Module. More info can be found [here](#).



- MYIR, MYC-J1028X CPU Module. More info can be found [here](#).



Training and On-Demand Webinars:

- Combining OT and IT Traffic on a Single Network With TSN 802.1Qbv. More info [here](#).
- Create Redundant Networks With TSN 802.1CB. More info can be found [here](#).
- Leveraging Time-Sensitive Networks for Distributed Intelligence on the Factory Floor. More info can be found [here](#).
- Synchronizing Industrial Networks with 802.1AS. More info can be found [here](#).
- MOVE.B LS1028A 5 day training course, can be found [here](#).

Publications:

- 5G enabled flexible lineless assembly systems with edge cloud controlled mobile robots. More info can be found [here](#).

Web sites:

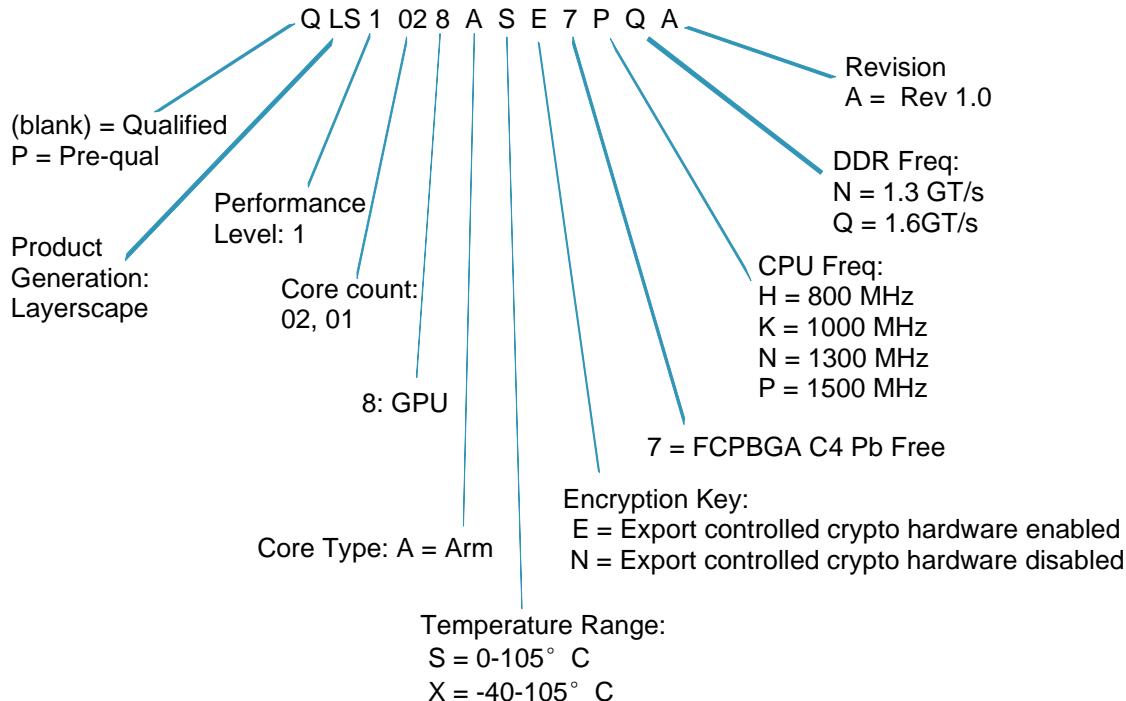
- Public web: <https://www.nxp.com/ls1028A> and <https://www.nxp.com/design/qoriq-developer-resources/layerscape-ls1028a-reference-design-board:LS1028ARDB>
- Confidential collateral is available to customers with NDA on External SharePoint site. Request access via your salesperson. Link to sharepoint is [here](#).

Collateral

Documentation	Version (on public web unless noted)
LS1027A/LS1017A Data Sheet	Rev 0, Dec 24, 2019
LS1028A/LS1018A Data Sheet	Rev 0, Dec 24, 2019
LS1028A Reference Manual	Rev 0, Dec 16, 2019
LS1028A Security (SEC) Reference Manual	Rev 0, Aug 25, 2020
LS1028A Fact Sheet	Rev 0, Dec 20, 2018
LS1028/27 Chip Errata	Rev 2, Feb, 2023, on sharepoint
LS1028/27 Chip Errata Software Disposition	Rev 0, Jan 11, 2021, on sharepoint
LCD Controller, Engineering Bulletin	Rev A, Dec 2019, on sharepoint
Application Notes	Version

Network on Chip (NOC) Performance Caveats	Rev 0, Nov 16, 2022
Thermal Management Unit Usage	Rev 0, Apr 27, 2022
Chaining FlexTimers on Layerscape Devices	Rev 0, Apr 4, 2022
Machine Inspection Demo	Rev 0, Mar 30, 2022
Enabling 5G Module on Layerscape Platforms	Rev 0, Nov 15, 2021
Xen Deployment on Layerscape Platforms	Rev 0, Mar 8, 2021
PBL Configuration using QCVS Application Note	Rev 1, Nov 30, 2020
AN12028, LS1028A Design Checklist - Application Note	Rev 0, Dec 25, 2019
AN5097, Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces - Application Note	Rev 2, Jul 10, 2019
General soldering Temperature Process Guidelines	Rev 1, Aug 16, 2017
DDR Interleaving for PowerQuicc ad QorIQ Processors	Rev 1, Jun 30, 2010
Solder Joint Temperature and Package Peak Temp	Rev 0, Aug 2, 2006
Development Tools	Version (on public web unless noted)
LS1028A Reference Board Design	LS1028A Reference Design Board Getting Started Guide, Rev 1, Apr 8, 2020
	LS1028A Reference Design Board Reference Manual, Rev 3, Feb 7, 2022
	mikroBUS click board enablement on LS1028ARDB, Rev0, Jun 25, 2019
	LS1028A Reference Design Board Errata, Rev 1, Apr 19, 2020
	LS1028A Reference Design Board - Fact Sheet, Rev 1, Feb 14, 2019
CodeWarrior	V11.5.0 available on public web
Software	Version
Layerscape Linux Distribution POC (LS SDK)	L5.15.71-2.2.0, released 17 Feb 2023
IBIS Model	Available on sharepoint

Part Number Decoder:



Note:

- For the LS1028A family of devices, parts marked with "H" require 0.9 V operating voltage.
- For the LS1028A family of devices, parts marked with "Y" are available with CPU speed 800MHz only.
- For the LS1028A family of devices, parts marked with "C" require 1.0 V operating voltage.

Production Part Numbers

These part numbers are orderable and shippable.

Parts	Description
LS1017ASE7HNA	Layerscape 64-bit Arm Cortex-A72, Single-core, 800MHz, 0 to 105C, Security enabled
LS1017ASE7KQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.0GHz, 0 to 105C, Security enabled
LS1017ASE7NQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.3GHz, 0 to 105C, Security enabled
LS1017ASE7PQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.5GHz, 0 to 105C, Security enabled
LS1017ASN7HNA	Layerscape 64-bit Arm Cortex-A72, Single-core, 800MHz, 0 to 105C, Security disabled

LS1017ASN7KQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.0GHz, 0 to 105C, Security disabled
LS1017ASN7NQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.3GHz, 0 to 105C, Security disabled
LS1017ASN7PQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.5GHz, 0 to 105C, Security disabled
LS1017AXE7HNA	Layerscape 64-bit Arm Cortex-A72, Single-core, 800MHz, -40 to 105C, Security enabled
LS1017AXE7KQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.0GHz, -40 to 105C, Security enabled
LS1017AXE7NQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.3GHz, -40 to 105C, Security enabled
LS1017AXE7PQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.5GHz, -40 to 105C, Security enabled
LS1017AXN7HNA	Layerscape 64-bit Arm Cortex-A72, Single-core, 800MHz, -40 to 105C, Security disabled
LS1017AXN7KQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.0GHz, -40 to 105C, Security disabled
LS1017AXN7NQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.3GHz, -40 to 105C, Security disabled
LS1017AXN7PQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.5GHz, -40 to 105C, Security disabled
LS1018ASE7HNA	Layerscape 64-bit Arm Cortex-A72, Single-core, 800MHz, 0 to 105C, Security enabled, 3D GPU
LS1018ASE7KQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.0GHz, 0 to 105C, Security enabled, 3D GPU
LS1018ASE7NQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.3GHz, 0 to 105C, Security enabled, 3D GPU
LS1018ASE7PQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.5GHz, 0 to 105C, Security enabled, 3D GPU
LS1018ASN7HNA	Layerscape 64-bit Arm Cortex-A72, Single-core, 800MHz, 0 to 105C, Security disabled, 3D GPU
LS1018ASN7KQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.0GHz, 0 to 105C, Security disabled, 3D GPU
LS1018ASN7NQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.3GHz, 0 to 105C, Security disabled, 3D GPU
LS1018ASN7PQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.5GHz, 0 to 105C, Security disabled, 3D GPU
LS1018AXE7HNA	Layerscape 64-bit Arm Cortex-A72, Single-core, 800MHz, -40 to 105C, Security enabled, 3D GPU
LS1018AXE7KQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.0GHz, -40 to 105C, Security enabled, 3D GPU
LS1018AXE7NQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.3GHz, -40 to 105C, Security enabled, 3D GPU
LS1018AXE7PQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.5GHz, -40 to 105C, Security enabled, 3D GPU
LS1018AXN7HNA	Layerscape 64-bit Arm Cortex-A72, Single-core, 800MHz, -40 to 105C, Security disabled, 3D GPU
LS1018AXN7KQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.0GHz, -40 to 105C, Security disabled, 3D GPU

LS1018AXN7NQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.3GHz, -40 to 105C, Security disabled, 3D GPU
LS1018AXN7PQA	Layerscape 64-bit Arm Cortex-A72, Single-core, 1.5GHz, -40 to 105C, Security disabled, 3D GPU
LS1027ASE7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, 0 to 105C, Security enabled
LS1027ASE7KQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1GHz, 0 to 105C, Security enabled
LS1027ASE7NQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, 0 to 105C, Security enabled
LS1027ASE7PQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.5GHz, 0 to 105C, Security enabled
LS1027ASN7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, 0 to 105C, Security disabled
LS1027ASN7KQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1GHz, 0 to 105C, Security disabled
LS1027ASN7NQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, 0 to 105C, Security disabled
LS1027ASN7PQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.5GHz, 0 to 105C, Security disabled
LS1027AXE7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, -40 to 105C, Security enabled
LS1027AXE7KQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1GHz, -40 to 105C, Security enabled
LS1027AXE7NQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, -40 to 105C, Security enabled
LS1027AXE7PQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.5GHz, -40 to 105C, Security enabled
LS1027AXN7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, -40 to 105C, Security disabled
LS1027AXN7KQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1GHz, -40 to 105C, Security disabled
LS1027AXN7NQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, -40 to 105C, Security disabled
LS1027AXN7PQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.5GHz, -40 to 105C, Security disabled
LS1028ACE7NQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, AEC-Q100 Grade 3, Security enabled, 3D GPU
LS1028ACN7NQ A	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, AEC-Q100 Grade 3, Security disabled, 3D GPU
LS1028ASE7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, 0 to 105C, Security enabled, 3D GPU
LS1028ASE7KQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1GHz, 0 to 105C, Security enabled, 3D GPU
LS1028ASE7NQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, 0 to 105C, Security enabled, 3D GPU
LS1028ASE7PQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.5GHz, 0 to 105C, Security enabled, 3D GPU
LS1028ASN7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, 0 to 105C, Security disabled, 3D GPU

LS1028ASN7KQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1GHz, 0 to 105C, Security disabled, 3D GPU
LS1028ASN7NQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, 0 to 105C, Security disabled, 3D GPU
LS1028ASN7PQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.5GHz, 0 to 105C, Security disabled, 3D GPU
LS1028AXE7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, -40 to 105C, Security enabled, 3D GPU
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LS1028AXE7PQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.5GHz, -40 to 105C, Security enabled, 3D GPU
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LS1028AXN7NQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.3GHz, -40 to 105C, Security disabled, 3D GPU
LS1028AXN7PQA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 1.5GHz, -40 to 105C, Security disabled, 3D GPU
LS1028AYE7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, -40 to 125C, Security enabled, 3D GPU
LS1028AYN7HNA	Layerscape 64-bit Arm Cortex-A72, Dual-core, 800MHz, -40 to 125C, Security disabled, 3D GPU