EVAL Kit Manual

KTU1133

USB 48V EPR Port Protector for CC & SBU

Brief Description

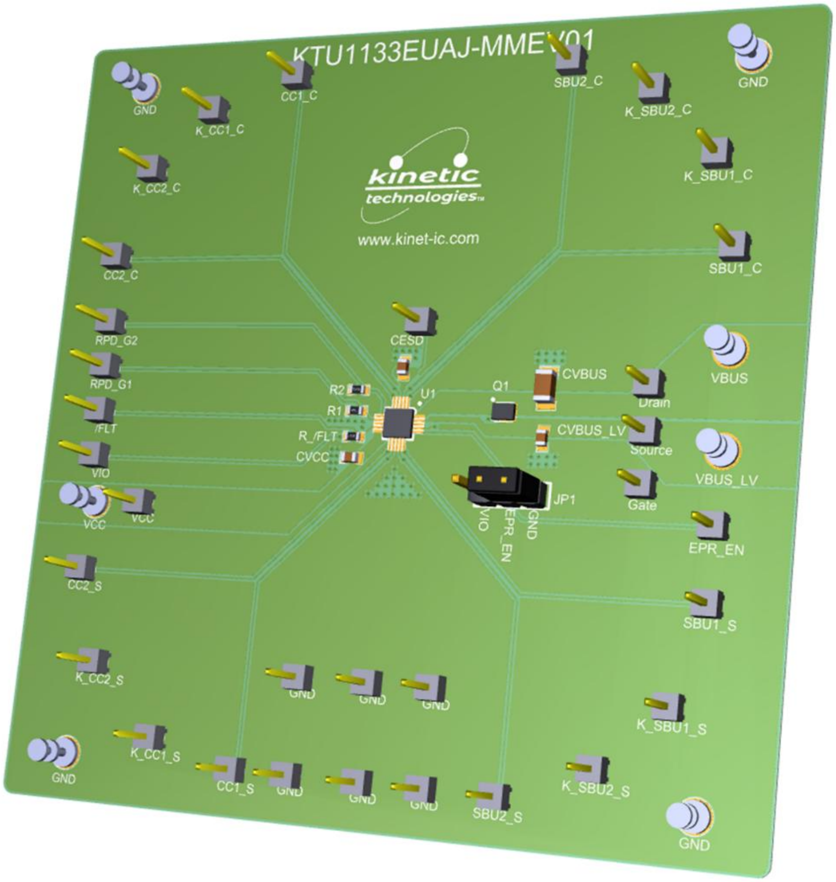
The KTU1133 provides safety management for USB PD3.1 48V EPR ports with comprehensive protection of the CC and SBU data lines. All four data lines include 63VDC withstand for short-to-VBUS fault events in the connector and integrated transient voltage suppression (TVS) for IEC surge protection and IEC level-4 ESD protection. Fast over-voltage protection (OVP) isolates downstream system circuits during fault events.

The integrated VBUS level shift circuit and external blocking NFET gate driver allow SPR-rated PD controllers to safely operate in EPR systems. The KTU1133 is packaged in RoHS and Green compliant 20-pin 3mm x 3mm WQFN package.

Ordering Information

Part Number	Description	IC Package
KTU1133EUAJ-MMEV01	KTU1133 EVAL Kit	WQFN33-20

3D CAD Image



EVAL Kit Physical Contents

Item #	Description	Quantity
1	KTU1133 EVAL fully assembled PCB	1
2	Anti-static bag	1
3	Quick Start Guide, printed (A4 or US Letter)	1
4	EVAL Kit box	1

QR Links for Documents

IC Landing Page	EVAL Kit Landing Page
https://www.kinet-ic.com/ktu1133/	https://www.kinet-ic.com/ktu1133euaj-mmev01

User-Supplied Equipment

Required Equipment

1. Bench Power Supply for VCC: 3.0V with 0.5A current limit.
2. Digital Current Meter for VCC: set range for 0.001mA or 0.0001mA resolution.
3. Bench Power Supply for CC1C: adjustable 0 to 9V with 0.5A current limit.
4. Digital Current Meter for CC1C: set range for 0.001mA or 0.0001mA resolution.
5. Digital Voltmeter for CC1S: set range for 0.001V or 0.0001V resolution.
6. Bench Power Supply for VBUS: adjustable 0 to 54V with 0.5A current limit.
7. Digital Voltmeter for VBUS_LV: set range for 50.0V or 100.0V resolution.
8. Test Leads:
    a. VCC/GND Input Power: 1x (red) banana-to-banana & pair (red/black) banana-to-clip
    b. CC1C/GND Input Voltage/Current: 1x (red) banana-to-banana & pair (red/black) banana-to-clip
    c. CC1S/GND Output Voltage: pair (red/black) banana-to-clip

Optional Equipment

1. Load: either an e-Load, power resistors, or an actual system load.
2. Oscilloscope: for dynamic testing of voltages (and currents with a current probe, if available).
3. Function Generator: for dynamic testing of on/off & fault response, debounce, and recovery times.
4. Digital Multimeter: Measure Output Voltage (CC1S/2S, SBU1/2S, VBUS_LV).

Recommended Operating Conditions

Symbol	Description	Value	Units
V_{CC}	Supply Withstand Voltage Supply Operating Voltage	-0.3 to 5 2.7 to 5.5	V
V_{LOGIC}	EPR_EN Withstand Voltage $\overline{\text{FLT}}$ Withstand Voltage	-0.3 to 6 -0.3 to 6	V
	EPR_EN Operating Voltage $\overline{\text{FLT}}$ Operating Voltage	0 to V_{CC} 2.7 to 5.5	
V_{BUS}	VBUS Withstand Voltage (continuous) VBUS Withstand Voltage (during IEC61000-4-5 surge event with external TVS)	-0.3 to 63 -4 to 70	V
	VBUS Operating Voltage	0 to 55	V
V_{BUS_LV}	VBUS_LV Withstand Voltage (continuous) VBUS_LV Operating Voltage	-0.3 to 24 0 to 23	V
V_{GATE}	GATE Withstand Voltage	-0.3 to 30	V
V_{IO}	CC1C, CC2C, RPD_G1, RPD_G2, SBU1C, SBU2C Withstand Voltage CC1S, CC2S, SB1S, SB2S Withstand Voltage	-0.3 to 63 -0.3 to 6	V
	CC1, CC2, CC1S, CC2S, RPD_G1, RPD_G2 Operating Voltage SBU1, SBU2, SB1S, SB2S Operating Voltage	-0.3 to 5.9 -0.3 to 5.9	
I_{IO}	CC Switch Continuous Current SBU Switch Continuous Current	0 to 1.25 0.1	A

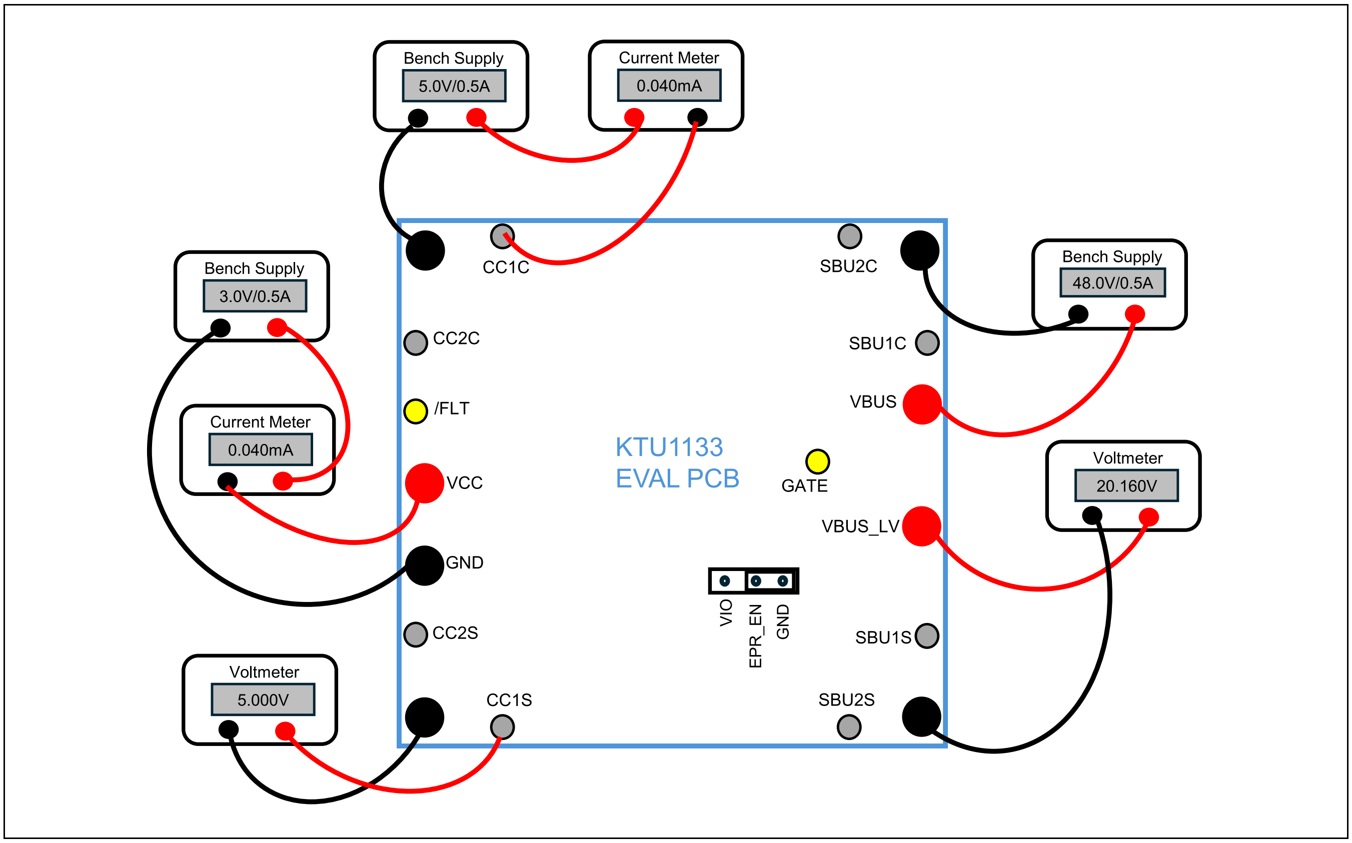
Jumper Descriptions

Designator	Name	Description	Default
JP1	EPR_EN	EPR mode enable input – logic 0 = SPR mode; logic 1 = EPR mode.	GND

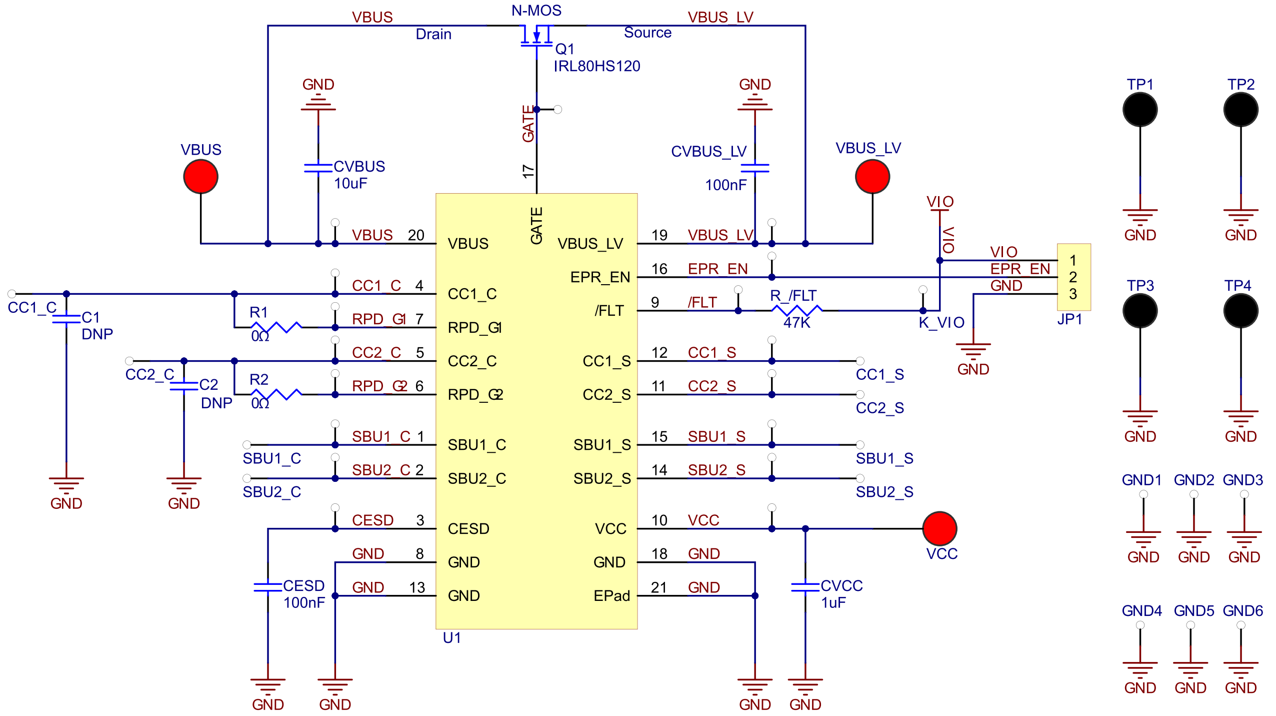
Quick Start Procedures

1. Before connecting the EVAL Kit to the Bench Power Supplies, turn on the supplies and adjust their voltages as close to 0V as possible. Also set both current limits to 0.5A.
2. Using the Test Leads, wire up the two Bench Supplies, two Current Meters, and one Voltage Meter as indicated in the *Typical Test Setup Diagram* section of this document.
3. Start slowly ramping the VCC Bench Supply to V_{CC} = 3.0V while monitoring the VCC Current Meter. If the current becomes high, quickly reduce the voltage to prevent damage. Then inspect the setup for any wiring errors.
4. Test the No-Load Supply Current at V_{CC} = 3.0V. It should measure about 0.040mA.
5. Keep VCC at 3.0V. Start slowly ramping the CC1C Bench Supply to V_{CC1C} = V_{CC1S} = 5.0V while monitoring the CC1C Current Meter. If the current becomes high, quickly reduce the voltage to prevent damage. Then inspect the setup for any wiring errors. Observe the CC1C Switch is ON by checking that the CC1S voltage is 5.0V.
6. Adjust the CC1C Bench Supply to $V_{CC1C} > 6.3V$. Observe the CC1C Switch turns OFF due to OVP fault by checking that the CC1S voltage falls to 0V.
7. Adjust the CC1 Bench Supply to V_{CC1C} = 2.6V. Observe the CC1C Switch is ON after OVP Recovery by checking that the CC1S voltage is also 2.6V.
8. Keep CC1C at 2.6V. Adjust the VCC Bench Supply as close to 0V as possible. Observe the CC1C Switch is OFF due to VCC in UVLO by checking that the CC1S voltage falls to 0V.
9. Check the CC1C Dead Battery Pull-Down Current. With CC1C voltage between 2.5V and 2.7V, the CC1C input current is 0.41mA minimum, 0.51mA typical, and 0.66mA maximum.
10. Check VBUS Level shifter. Adjust the VBUS Bench Supply to V_{BUS} = 0 to 48V. In EPR Mode (EPR_EN = High), the VBUS_LV output is proportionally scaled to 0.42x VBUS. Therefore, 48V at the VBUS input is shifted to 20V at VBUS_LV output. In SPR Mode (EPR_EN = Low), the VBUS level shifter enters 1x VBUS “pass through” operation.

Typical Test Setup Diagram



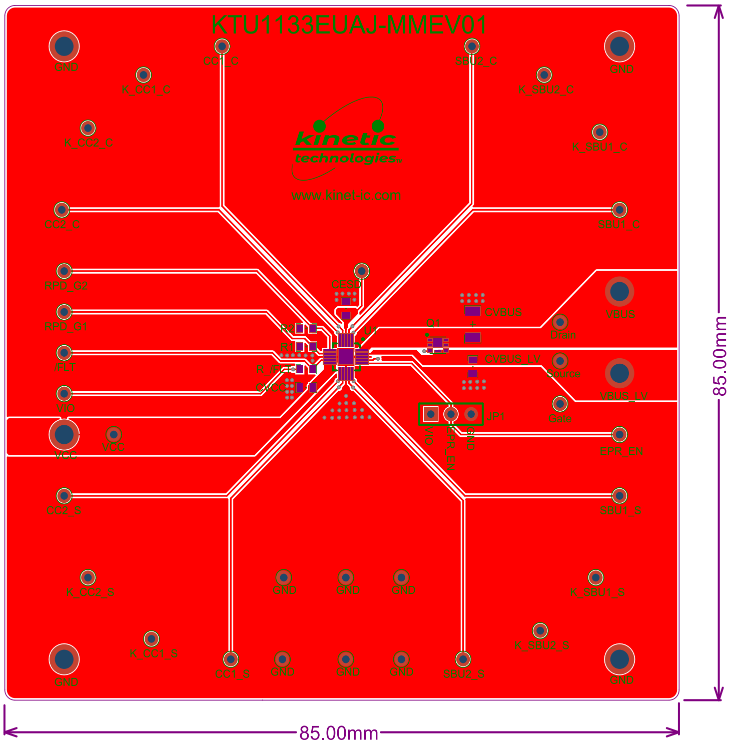
Electrical Schematic

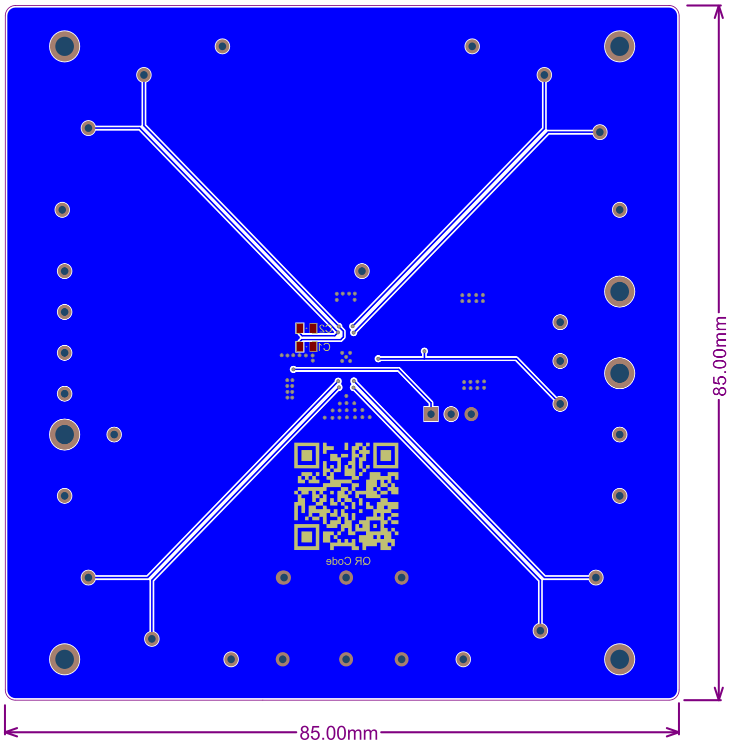


Bill of Materials (BOM)

Designator	Description	Quantity	Value	Manufacturer	Manufacturer Part Number
/FLT, CC1_C, CC1_S, CC2_C, CC2_S, EPR_EN, GATE_Test, GND1, GND2, GND3, GND4, GND5, GND6, K_CC1_C, K_CC1_S, K_CC2_C, K_CC2_S, K_SBU1_C, K_SBU1_S, K_SBU2_C, K_SBU2_S, K_VBUS, K_VBUS_LV, K_VCC, K_VIO, RPD_G1, RPD_G2, SBU1_C, SBU1_S, SBU2_C, SBU2_S, T_CESD	1x 1POS P = 2.54mm TH	32		XFCN	PZ254V-11-01P
CVCC	CAP CER 1.0µF 50V X5R 0603	1	1uF	muRata	GRT188R61H105KE13D
CVBUS	CAP CER 10µF 100V X7S 1210	1	10uF	muRata	GRM32EC72A106KE05L
CESD, CVBUS_LV	CAP CER 100nF 100V X7R 0603	2	100nF	muRata	GCJ188R72A104KA01D
C1, C2	CAP CER 330pF 100V C0G 0603	2	DNP	muRata	GCM1885C2A331JA16D
JP1	CONN HEADER VERT 3POS 2.54MM	1		MOLEX	22284031
U1	KTU1133EUAJ-TD WQFN33-20	1		Kinetic Technologies	KTU1133EUAJ-TD
Q1	MOSFET N-CH 80V 12.5A 6PQFN	1		Infineon	IRL80HS120
R1, R2	RES SMD 0Ω 1% 1/10W 0603	2	0Ω	YAGEO	RC0603JR-070RL
R_/FLT	RES SMD 47K 1% 1/10W 0603	1	47K	YAGEO	RC0603FR-0747KL
TP1, TP2, TP3, TP4, VBUS, VBUS_LV, VCC	TERM TURRET SINGLE L=5.56MM TIN	7		Keystone	1502-2

Printed Circuit Board (PCB)





Additional Test Procedures

1. Testing the CC2C, SBU1C, and SBU2C Channels: similar to testing the CC1C channel in the *Quick Start Procedures* section, test the other channels for switch turn on/off and OVP. Test the dead battery pull-down function on CC2C. The SBU1C/2C OVP threshold of 4.2V typical is lower than for CC1C/2C, so test that the switches are on at 4V and off at 5V. The test points for SBU1C, SBU2C, SB1S, and SB2S are small, exposed vias within the PCB trace to maximize the SBU signal-path bandwidth; therefore, testing SBU functionality is slightly more difficult than for the CC channels. As a tip, typical through-hole resistor leads usually fit nicely into these vias, providing easy attachment of clip test leads. Alternatively, obtain appropriate USB type-C breakout boards than can be easily connected to the EVAL PCB.
2. Testing On-Resistance (R_{ON}): add an appropriate load to either CC or SBU channel and connect a voltmeter across the channel to measure voltage drop. Calculate $R_{ON} = V_{DROP}/I_{LOAD}$. For appropriate loading range, see the *Recommended Operating Conditions* section.
3. Testing OVP Response Time (t_{OVP}): use a function generator square-wave at 100ms period and 50% duty-cycle with programmable V_{HIGH} = 7V and V_{LOW} = 4V to transition the port-side input (either CC1, CC2, SBU1, or SBU2) from below to above the OVP threshold. To program the correct output voltage levels, either put the function generator in "HighZ" output-load mode, or use 50Ω termination, or set V_{HIGH} = 3.5V and V_{LOW} = 2V if using "50Ω" output-load mode without 50Ω termination. The function generator output cannot support significant load current regardless of mode; however, it isn't necessary to apply any load at the switch output for this test. Use an oscilloscope to capture the input and output waveforms for the channel being tested. Trigger on the input rising edge at 5.9V trigger-level for the CC channels and 4.2V trigger-level for the SBU channels. Set the time-scale to 20ns/division to measure t_{OVP}. To ease measurement, position and scale the input and output waveforms to overlap each other. To check the OVP falling debounce time, simply trigger on the falling edge and adjust the time-scale to 200µs/division. Also, it is interesting to lower the V_{HIGH} level just above and just below the OVP threshold to observe the response. However, when doing so, it is important to lower the oscilloscope's trigger-threshold, as well. If obtaining a stable trigger is difficult, enable the high-frequency rejection in the trigger menu, but usually, the DC-coupled option makes it easier to measure the delay.
4. $\overline{\text{FLT}}$ Logic Output Testing: while testing OVP Response Time, connect a third oscilloscope probe to the $\overline{\text{FLT}}$ test point on the EVAL PCB. For the response time, use 20ns/division. For the recovery time, use 1ms/division.
5. Automatic EPR Mode Threshold Voltage Testing: In SPR Mode (EPR_EN = Low), when the V_{BUS} >24V, the VBUS_LV output is proportionally scaled from 1 x VBUS drops to 0.42x VBUS. When V_{BUS} <22V, the VBUS level shifter recovers 1x VBUS "pass through" operation.
6. Surge and ESD Testing: special surge and/or ESD test equipment is required. Training and prior experience is recommended before undertaking these tests.

Disabling the Dead Battery Pull-Down Function

The KTU1133 includes an optional dead battery 5.1kΩ pull-down circuits when VCC is below UVLO or above OVP thresholds. As configured, the EVAL PCB enables this feature. To disable, remove R1 and R2.

Troubleshooting

Symptom	Root Cause	Solution
The CC and SBU switches do not turn on. $\overline{\text{FLT}}$ is low.	The KTU1133 is not powered at VCC. $\overline{\text{FLT}}$ has no pull-up voltage.	Connect a valid VCC voltage supply from VCC to GND.
The CC and SBU switches do not turn on. $\overline{\text{FLT}}$ is low.	OVP is triggered at CC1C, CC2C, SBU1C, or SBU2C channels.	Check the voltages at CC1C, CC2C, SBU1C, and SBU2C. Make sure all of them are below their respective OVP thresholds of 5.9V typical for CC1C/2C and 4.2V typical for SBU1C/2C.
EPR Mode, VBUS_LV to VBUS Divider Ratio is not change	EPR_EN is not high logic level	Check VIO voltage level, set VIO voltage to 2V.
EPR Mode, VBUS_LV to VBUS Divider Ratio is not change	EPR_EN pin is floating	Check EPR_EN pin and JP1 status

Important Notices

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