5V/3A VBUS I_{SOURCE} Load Switch for 28V EPR Systems

Features

- 2.5V to 5.5V Operating Voltage Range at IN
- 35VDC Abs. Max. Rating at OUT
- Adjustable Current Limit Protection (CLP)
  - 400mA to 4.0A via R_{ISET}
- 27mΩ typ. On-Resistance from IN to OUT
- Soft-Start (SS) Limits Inrush Current
- "Ideal Diode" Reverse Current Protection (RCP)
  - 20mV Forward Voltage and 15µs Fast Recovery
- 5.8A, 150ns Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) during & after SS
- Over-Temperature Protection (OTP)
- Transient Voltage Suppression (TVS) at OUT
  - ±130V Surge Protection (IEC61000-4-5)
  - ±30kV ESD Contact Discharge (IEC61000-4-2)
  - ±30kV ESD Air Gap Discharge (IEC61000-4-2)
- EN Enable Logic Input
- FON Fast ON Logic Input for Fast Role Swap (FRS)
  - KTS1890A version only
- $\overline{FLT}$ Fault Open-Drain Logic Output
- Hiccup Mode Auto-Retry after Faults
- -40°C to 85°C Operating Temperature Range
- 20-bump WLCSP 2.49 x 1.99mm (0.5mm pitch)

Brief Description

The KTS1890 is a USB VBUS safety management load switch for 15W current-source output in systems with 28V EPR current sink input. The input operating range is 2.5V to 5.5V, but the output withstands up to 35VDC at the USB port. Current limit protection (CLP) is adjustable from 400mA to 4.0A. Low on-resistance minimizes heat and voltage droop. Soft-start (SS) limits inrush current. Reverse-current protection (RCP) acts as a 20mV "ideal diode" with fast recovery.

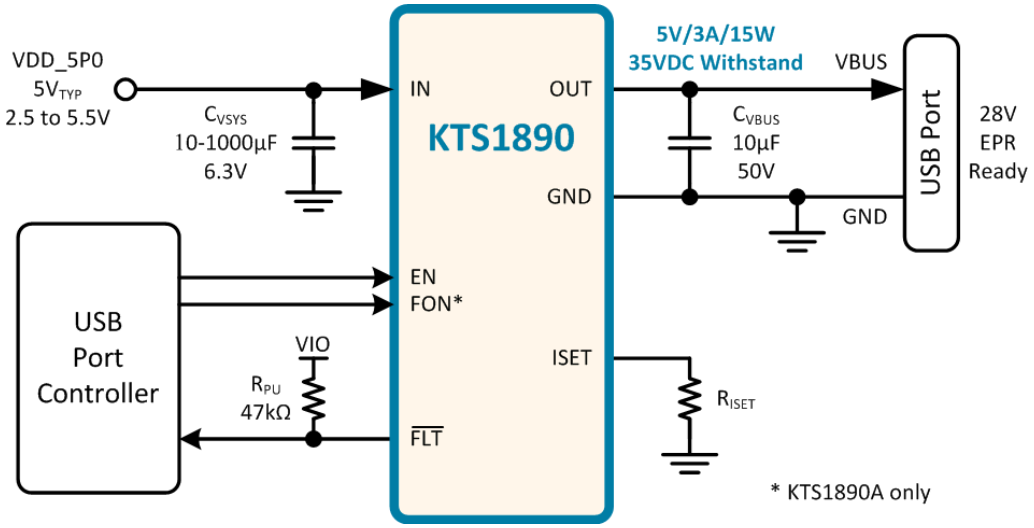
Additional safety management includes ultra-fast over-current protection (OCP), short-circuit protection (SCP) during and after soft-start, over-temperature protection (OTP), and an integrated transient voltage suppressor (TVS) for IEC industry standard ±30kV ESD and ±130V surge ratings.

The KTS1890 is packaged in advanced, fully "green" compliant, 2.49 x 1.99mm, 20-bump Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Desktop PC, Notebooks, Netbooks, Tablets
- Docking Stations, Monitors, Gaming Consoles
- Set-Top Box, Networking, any USB I_{SOURCE} Port

Typical Application

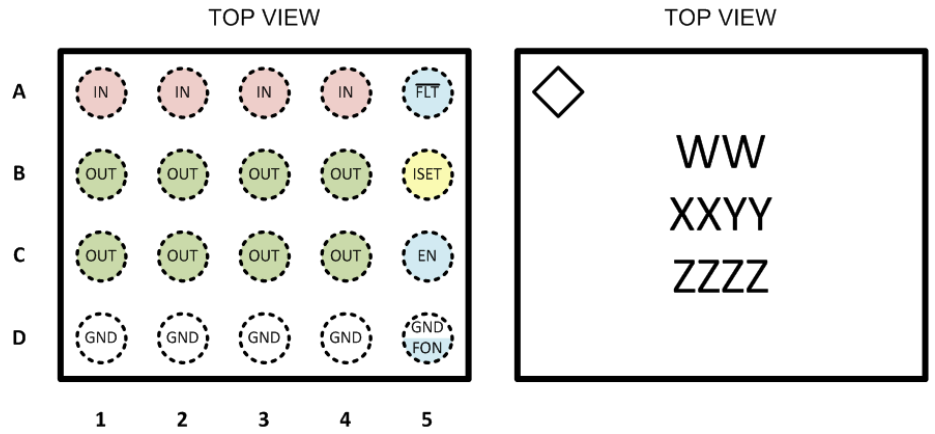


Ordering Information

Part Number	Marking[1]	Pin D5 Function	Operating Temperature	Package
KTS1890EIAC-TA	SYXXYYZZZZ	GND	-40°C to +85°C	WLCSP54-20
KTS1890AEIAC-TA[2]	TAXXYYZZZZ	FON		

Pinout Diagram

WLCSP54-20



20-bump 2.49mm x 1.99mm x 0.555mm
WLCSP Package, 0.5mm pitch
Top Mark: WW = Device ID, XX = Date Code, YY = Assembly Code, ZZZZ = Serial Number

Pin Descriptions

Pin #	Name	Function
A1, A2, A3, A4	IN	Power Switch Input – connect to system power rail in 2.5V to 5.5V range ($5.1V_{TYP}$).
B1, B2, B3, B4, C1, C2, C3, C4	OUT	Power Switch Output – connect to VBUS on USB output port.
D1, D2, D3, D4	GND	Ground – connect to system ground. This is a high-current return path to GND on USB port during TVS events.
A5	$\overline{FLT}$	Fault Logic Output – active-low, open-drain flag. Connect to GND or leave floating if unused.
B5	ISET	Current Limit Setting – a resistor from ISET to GND sets the current limit.
C5	EN	Enable Logic Input – active high with internal 1MΩ pull down
D5	GND	KTS1890 = Ground
	FON	KTS1890A = Fast ON Logic Input – active high with internal 1MΩ pull down

[1] "SY" is the device ID, "XX" is the date code, "YY is the assembly code, and "ZZZZ" is the serial number.

[2] Future version – consult Kinetic Technologies authorized representative for availability.

Absolute Maximum Ratings[3]

Symbol	Description	Value	Units
V_{IN}	IN to GND	-0.3 to 6	V
V_{OUT}	OUT to GND (continuous) OUT to GND (during IEC61000-4-5 surge event)	-0.3 to 35 -5 to 48	V V
V_{IO}	EN, FON, $\overline{FLT}$ to GND	-0.3 to 6	V
I_{SW}	Maximum Switch Current (continuous)[4]	4	A
T_J	Operating Temperature Range	-40 to 150	°C
s	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[5]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV
V_{ESD_CD}	IEC61000-4-2 Contact Discharge (OUT)	±30	kV
V_{ESD_AGD}	IEC61000-4-2 Air Gap Discharge (OUT)	±30	kV
V_{SURGE}	IEC61000-4-5 Surge (OUT, C_{OUT} = 10µF)	±130	V

Thermal Capabilities[6]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	64	°C/W
P_D	Maximum Power Dissipation at 25°C	1.95	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C (T_J = 150°C)	-15.6	mW/°C

[3] Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

[4] Internally limited.

[5] ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.

[6] Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions[7]

Symbol	Description	Value	Units
V_{IN}	Supply Voltage Operating Range	2.5 to 5.5	V
V_{OUT}	Output Voltage Range	0 to 33	V
V_{IO}	EN, FON, $\overline{FLT}$ to GND	-0 to 5.5	V
I_{SW}	Maximum Switch Current	3.7	A
R_{ISET}	Current Limit Setting Resistance	12.0 to 120	kΩ
C_{IN}	Input Capacitance	10 to 1000 6.3	µF V
C_{OUT}	Output Capacitance	10 50	µF V
T_A	Ambient Operating Temperature	-40 to 85	°C

Electrical Characteristics[8]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C and V_{IN} = 5V.

Supply Specifications (IN)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Operating Range		2.5		5.5	V
V_{UVLO}	Under-Voltage Lockout	V_{IN} rising threshold Hysteresis	2.12	2.3 100	2.48	V mV
I_Q	No-Load Supply Current	Enabled, EN = 1, FON = 0 or 1		210	360	µA
I_{SHDN}	Shutdown Supply Current	Disabled, EN = 0		0.01	5	µA

Over-Temperature Protection Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{OTP}	IC Junction Over-Temperature Protection	T_J rising threshold Hysteresis		150 20		°C

Logic Pin Specifications (EN, FON, $\overline{FLT}$)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High (EN, FON)		1.2			V
V_{IL}	Input Logic Low (EN, FON)				0.4	V
R_{I_PD}	Input Logic Pull-Down (EN, FON)		0.72	1		MΩ
V_{OL}	Output Logic Low ($\overline{FLT}$)	I_{O_SINK} = 4mA		0.02	0.3	V
I_{O_LK}	Output Logic High-Z Leakage ($\overline{FLT}$)	$V_O = V_{IN}$		0.01	1	µA

(continued next page)

[7] The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

[8] Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)[9]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C and V_{IN} = 5V.

Switch Specifications (IN, OUT)

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON}	Switch On-Resistance (IN to OUT)	V_{IN} = 3.7V to 5V		27	55	mΩ
I_{LK_OFF}	Switch Off-Leakage (at OUT)	V_{IN} = 5V, V_{OUT} = 0V, EN = 0 V_{IN} = 0V, V_{OUT} = 5V, EN = 0 V_{IN} = 0V, V_{OUT} = 28V, EN = 0		0.001 0.001 0.001	1 1 1	µA
I_{LK_RCP}	RCP Bias Current (at OUT)	V_{IN} = 5V, V_{OUT} = 28V, EN = 1		60		µA
I_{CLP}	Current-Limit Protection[10]	V_{IN} = 3.7V to 5.5V R_{ISET} = 47.5kΩ R_{ISET} = 28.7kΩ R_{ISET} = 14.3kΩ[11] R_{ISET} = 13.0kΩ[11]	 910 1510 3050 3360	 1000 1655 3320 3650	 1090 1800 3585 3940	mA
I_{CLP_SS}	Soft-Start Current-Limit Protection for SCP	FON = 0 FON = 1 (KTS1890A only)		0.8 n/a		A
V_{SCP_SS}	Short-Circuit Protection Threshold during Soft-Start	V_{OUT} < V_{SCP_SS} at end of SS		0.4V_{IN}		V
I_{OCP}	Over-Current Protection Threshold for SCP[11]			5.8		A
V_{REG_RCP}	"Ideal Diode" RCP V_{OUT} Droop Regulation Voltage	V_{IN} – V_{OUT}, V_{IN} = 3.7V to 5.5V		20		mV

TVS Surge Clamp Specifications (OUT)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OUT_WRK}	Output Clamp Working Voltage	Positive Working Voltage Negative Working Voltage	 0		35	V
V_{OUT_CLMP}	Output Clamp Breakdown Voltage	I_{OUT} = 10mA I_{OUT} = -10mA	38 -1	41 -0.6	44	V
V_{OUT_SRG}	Output Clamp Surge Voltage[11]	+130V surge -130V surge		46 -2		V

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[9] Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

[10] Specified at T_A = 25°C.

[11] Guaranteed by design, characterization and statistical process control methods; not production tested.

Electrical Characteristics (continued)[12]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C and V_{IN} = 5V.

Timing Specifications, see timing diagrams

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DEB}	Turn-On Debounce Delay	FON = 0		0.75		ms
		FON = 1 (KTS1890A only)		36	50	µs
t_R	V_{OUT} Rise Time	FON = 0		1.5		ms
		FON = 1 (KTS1890A only)		50	100	µs
t_{LIM_SS}	Soft-Start Current-Limit Time	FON = 0		7		ms
t_{DOFF}	Turn-Off Delay			3		µs
$t_{D\_\overline{FLT}}$	Fault Flag Trigger Delay	CLP fault event to $\overline{FLT}$ = 0		8		ms
$t_{RD\_\overline{FLT}}$	Fault Flag Recovery Delay	Any fault event recovery to $\overline{FLT}$ = high-Z		17		ms
t_{RCP}	Reverse-Current Protection Fast Recovery Time	$V_{OUT} < V_{IN}$ – 66mV		15		µs
t_{OCP}	Over-Current Protection Response Time			150		ns
t_{SCP_SS}	Short-Circuit Detection Time during Soft-Start	$V_{OUT} < 0.4V_{IN}$		7		ms
t_{HICCUP}	Short-Circuit Hiccup Retry Time			70		ms
t_{FON_BLNK}	Fast Turn-On CLP Blanking Time	FON = 1, time from EN going high until CLP is active (KTS1890A only)		370		µs

[12] Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Timing Diagrams

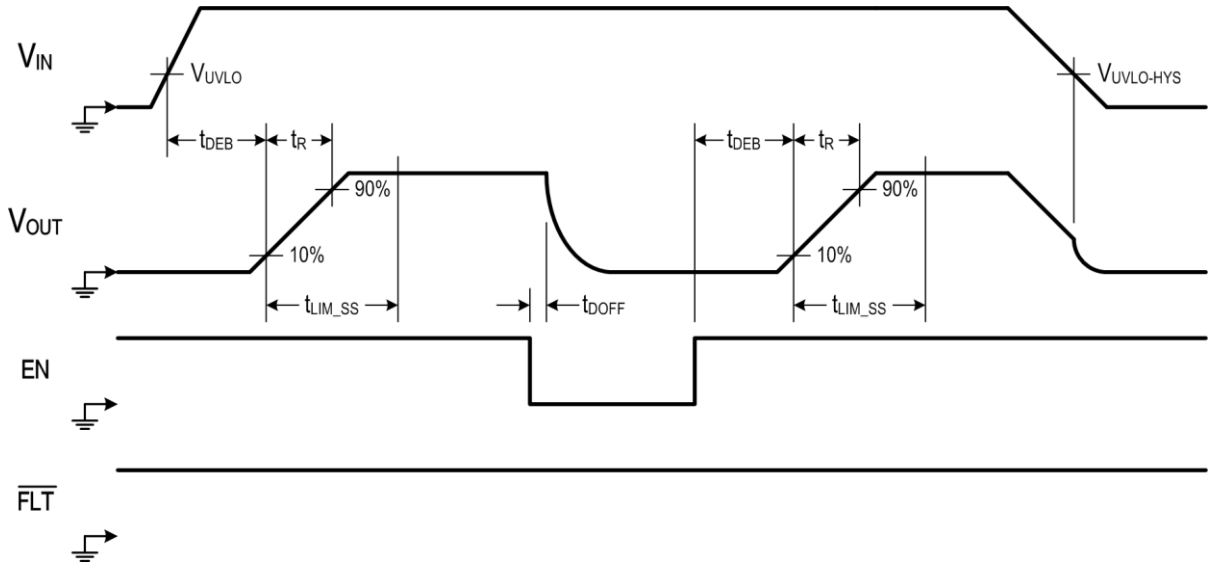


Figure 1. UVLO, Soft-Start and Turn-Off Timing Diagram

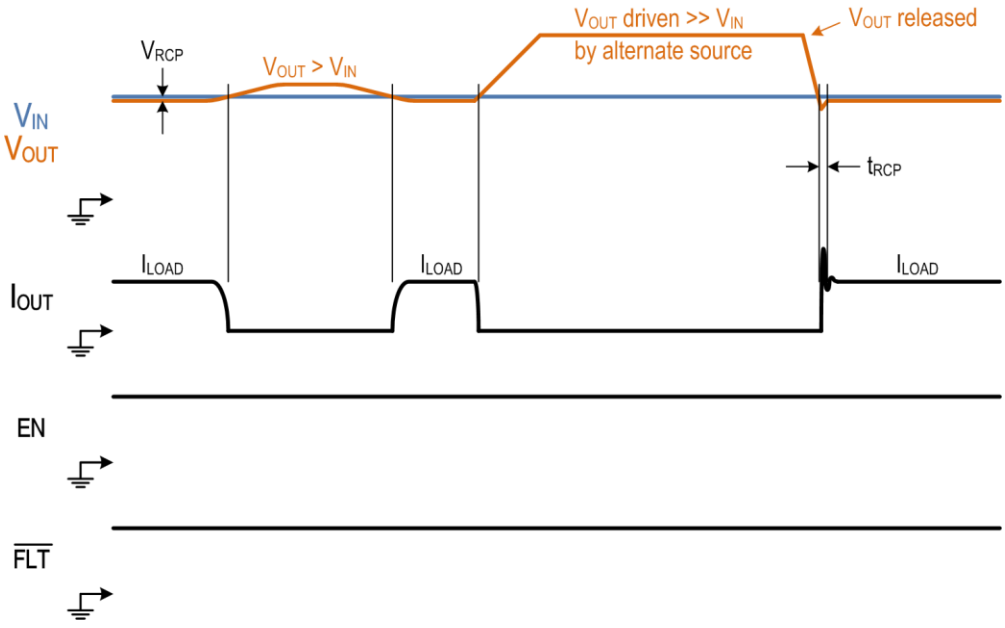


Figure 2. "Ideal Diode" RCP Timing Diagram with Fast Recovery

Timing Diagrams (continued)

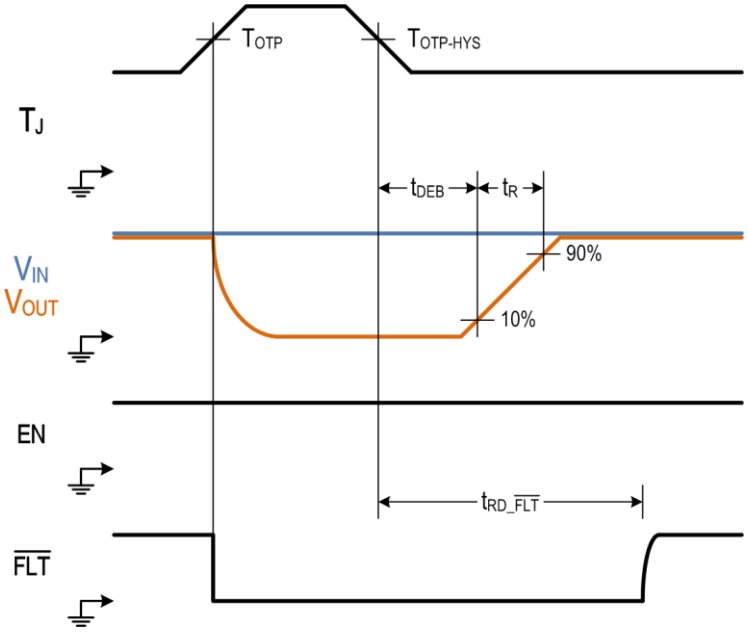
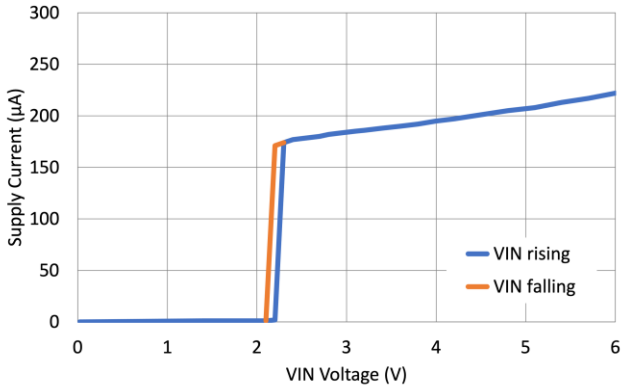


Figure 3. OTP Timing Diagram

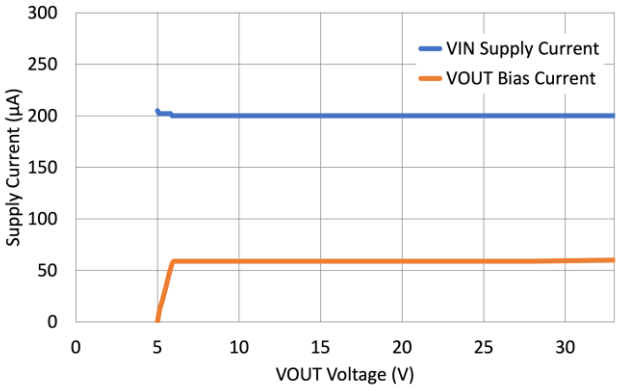
Typical Characteristics

V_{IN} = 5V, FON = 0, C_{IN} = 2x 47µF, C_{OUT} = 10µF, R_{ISET} = 14.3kΩ (3.32A CLP), T_A = 25°C, unless otherwise specified.

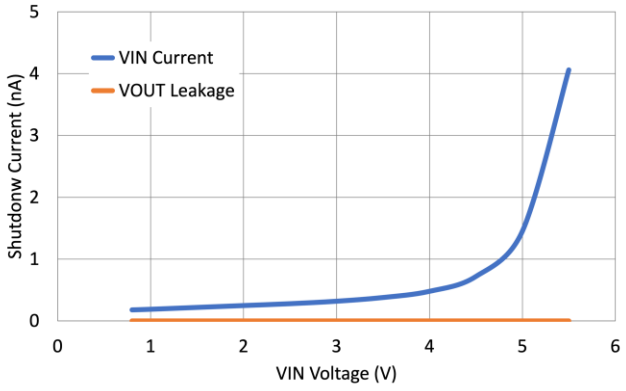
Supply Current vs. VIN
(EN = high, no output load)



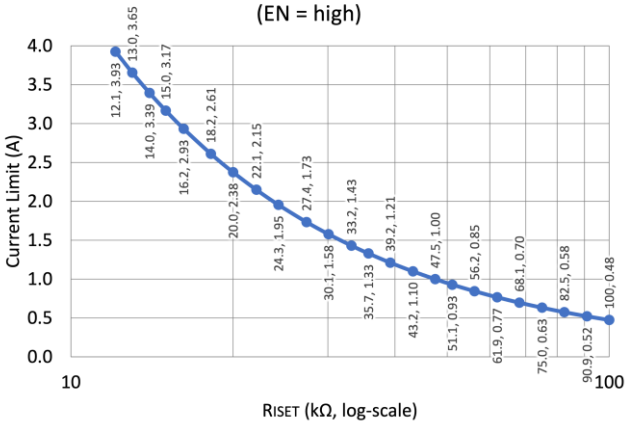
RCP Supply Current vs. VOUT
(EN = high, no output load)



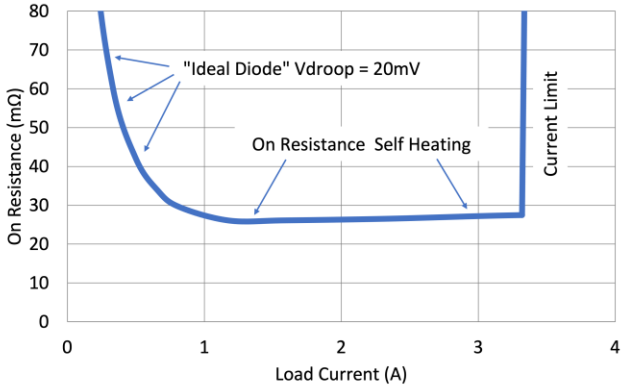
Shutdown Current & Leakage vs. VIN
(VOUT = 0V, EN = low, no CIN, no ambient light)



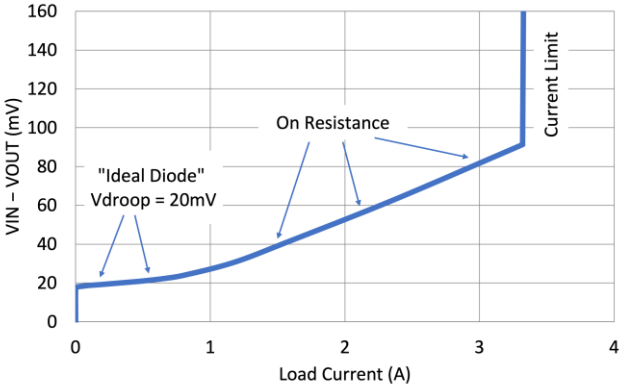
Current Limit Protection vs. RISET
(EN = high)



On Resistance vs. Load Current
(EN = high, RISET = 14.3kΩ)



"Ideal Diode" Vdroop vs. Load Current
(EN = high, RISET = 14.3kΩ)



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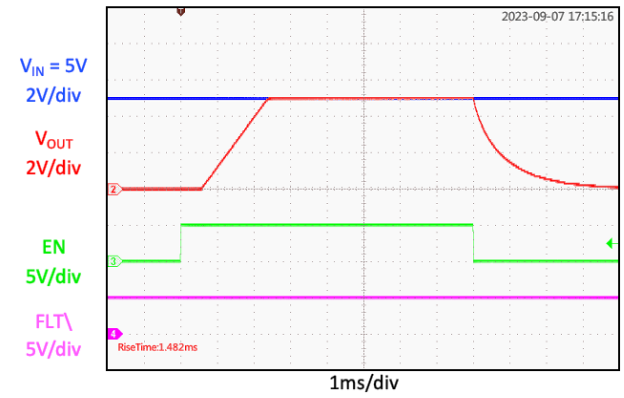
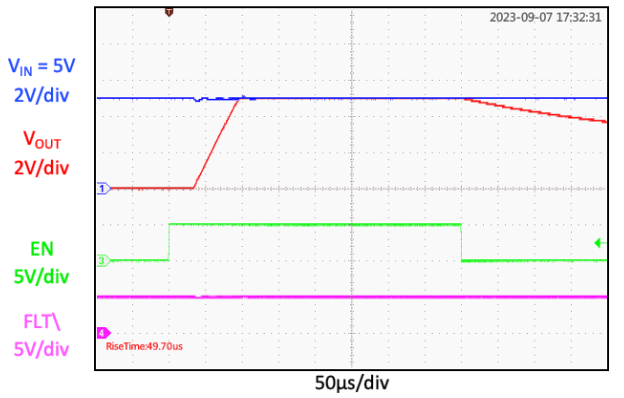
Typical Characteristics (continued)

V_{IN} = 5V, FON = 0, C_{IN} = 2x 47µF, C_{OUT} = 10µF, R_{ISET} = 14.3kΩ (3.32A CLP), T_A = 25°C, unless otherwise specified.

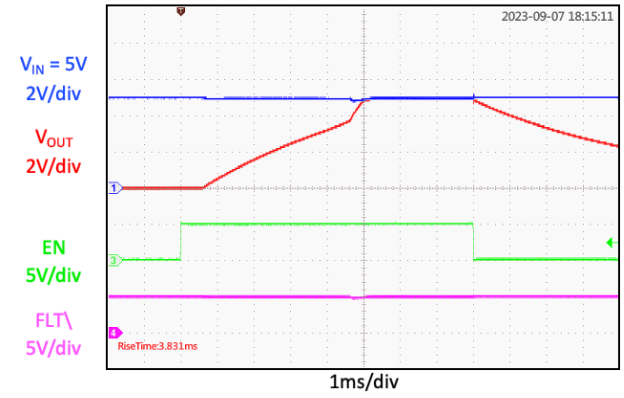
Enable, Soft-Start, Shutdown Response
(FON = low, R_{LOAD} = 100Ω)



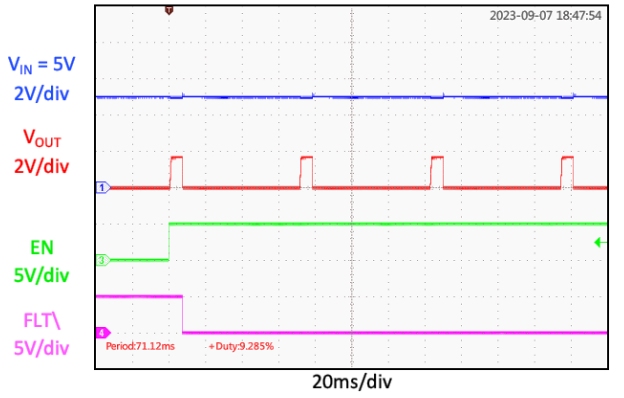
Fast On Enable, Soft-Start, Shutdown Response
(FON = high, R_{LOAD} = 100Ω)



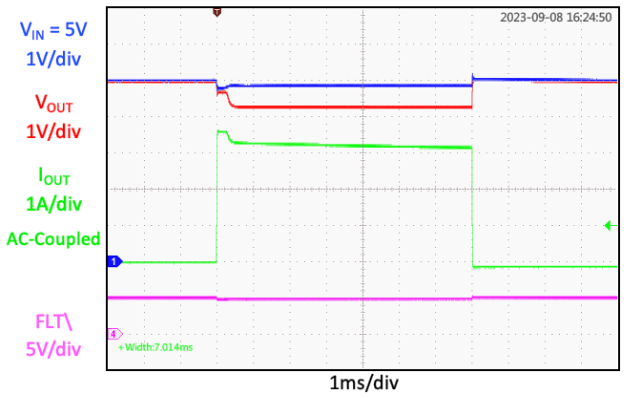
Heavy Load Soft-Start Response
(FON = low, C_{OUT} = 1000µF, R_{LOAD} = 6Ω)



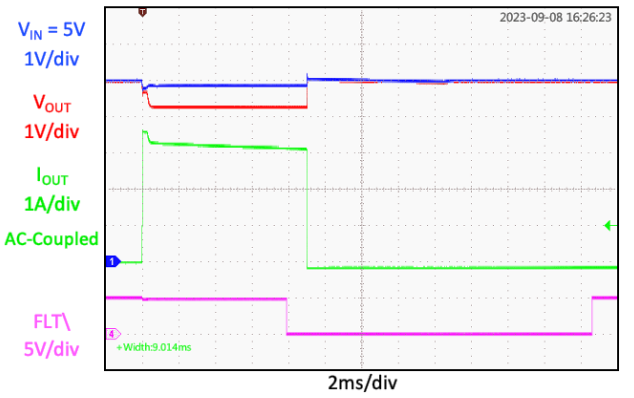
Over-Load Soft-Start & Auto-Retry Response
(FON = low, C_{OUT} = 10µF, R_{LOAD} = 1.5Ω)



CLP Response with Pulse < 8ms
(R_{LOAD} = 100Ω + 1.3Ω$_{PULSED}$)



CLP Response with Pulse > 8ms
(R_{LOAD} = 100Ω + 1.3Ω$_{PULSED}$)



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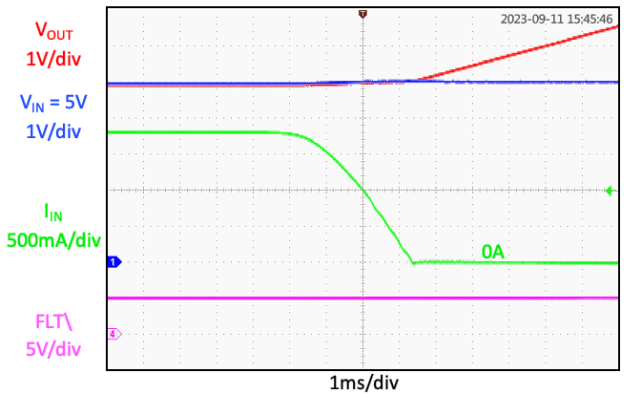
Typical Characteristics (continued)

V_{IN} = 5V, FON = 0, C_{IN} = 2x 47µF, C_{OUT} = 10µF, R_{ISET} = 14.3kΩ (3.32A CLP), T_A = 25°C, unless otherwise specified.

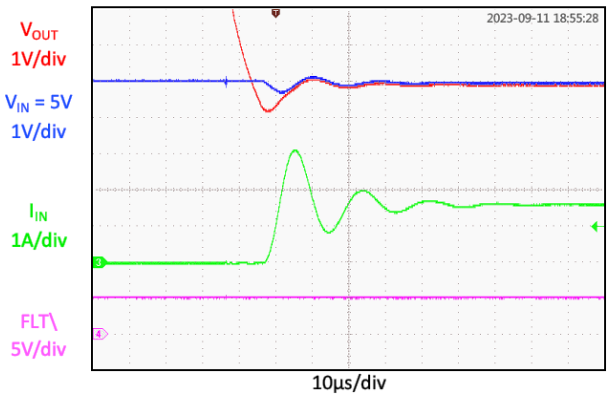
RCP Response

(R_{CABLE} = 200mΩ, R_{LOAD} = 3Ω, V_{OUT} = 5V → 9V)



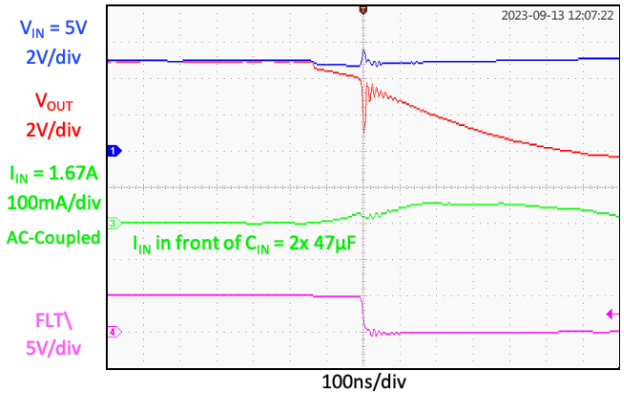
RCP Fast Recovery

(R_{CABLE} = 200mΩ, R_{LOAD} = 3Ω, V_{OUT} = 9V → 5V)



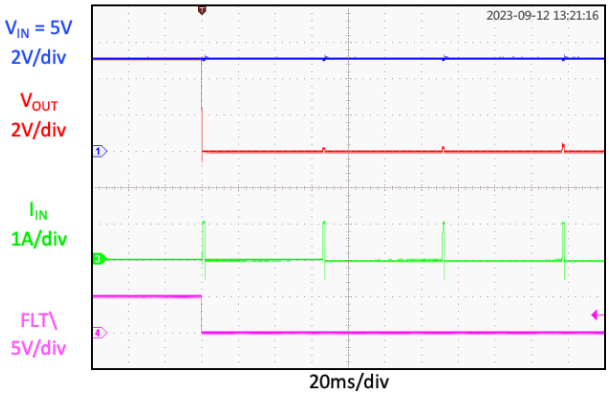
OCP/SCP Response

(R_{LOAD} = 3Ω, V_{OUT} = 5V → Short Circuit)



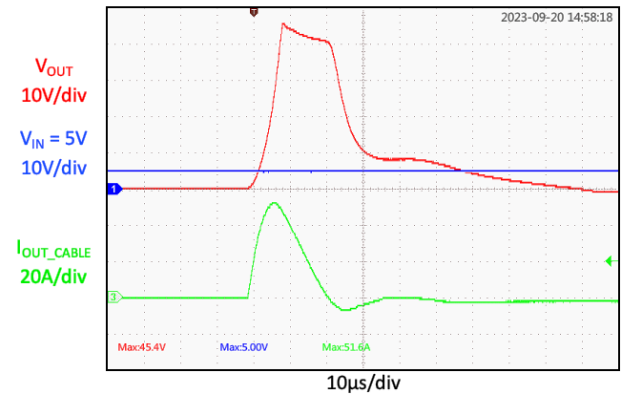
SCP Response with Auto-Retry

(V_{OUT} = 5V → Short Circuit)



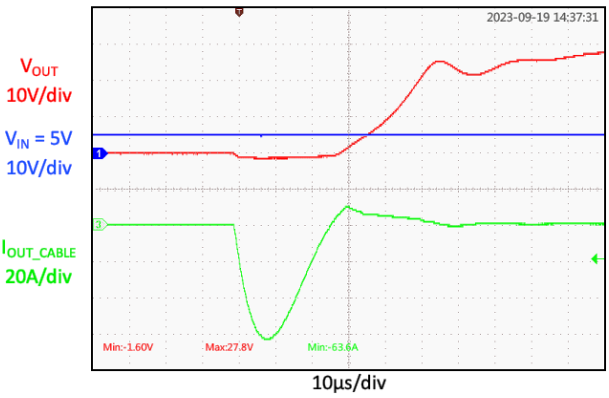
Surge Transient Response

(EN = low, V_{OUT} = +130V Surge)



Surge Transient Response

(EN = low, V_{OUT} = -130V Surge)



Functional Block Diagram

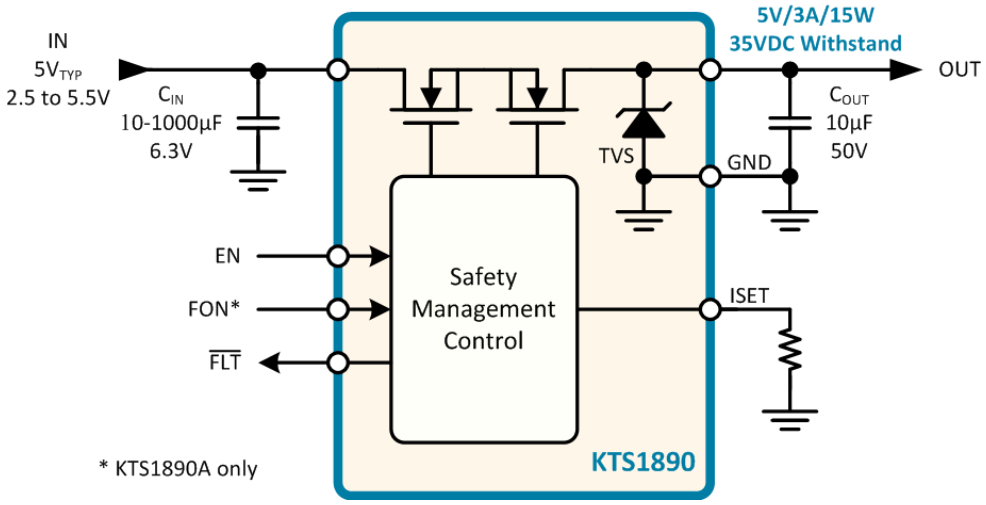


Figure 4. Functional Block Diagram

Functional Description

The KTS1890 is a 27mΩ (typ) low resistance power switch intended to be inserted between a power source and a load to isolate and protect against ESD, surge, and excessive voltage and load-current conditions at the output. It features slew-rate controlled turn ON (soft-start) to prevent input voltage droop resulting from a large inrush current when starting into capacitive loads. For USB fast role swap applications, the KTS1890A's fast turn-on feature speeds up soft-start when the FON pin is set to logic 1. The KTS1890 also features several additional protection functions, such as output surge and ESD protection, output current limit protection, output short-circuit protection, input under-voltage lockout, reverse current protection, and over-temperature protection. The KTS1890 operates over an input voltage range of 2.5V to 5.5V, and its output is designed to withstand up to 35V continuously and over 46V during IEC61000-4-5 ±130V surge events (whether in shutdown or enabled).

Shutdown and Enable

When EN is set to logic 0, the main power MOSFETs are disabled, and the device enters low-power shutdown mode. During shutdown mode, the output ESD/surge clamp continues to protect the IC and system. When EN is set to logic 1, all additional protection circuits are enabled, and if no fault condition exists, the main power MOSFETs are turned ON.

Under-Voltage Lockout (UVLO)

The UVLO function keeps the switches in the OFF state when the input voltage is below the UVLO threshold, regardless of the EN logic level. When the input voltage is above the UVLO threshold and EN is set to logic 1 and there are no fault conditions, the switches are enabled to the ON state.

Slew-Rate Controlled Turn ON (Soft-Start)

The KTS1890 has voltage slew-rate control during normal startup for suppressing inrush current. The V_{OUT} turn-on delay is 0.75ms (typ), and then the V_{OUT} rise time is 1.5ms (typ) for a total start-up time of 2.25ms (typ).

Current-Limit Controlled Turn ON (Soft-Start)

In addition to the voltage slew-rate control, the KTS1890 also includes a simultaneous 0.8A (typ.) current-limited soft-start for an extended time of 7ms. This enables soft-starting into very large capacitive loads at the output.

At the end of the 7ms soft-start current-limit time, the KTS1890 enters normal operation with current limit set by R_{ISET}. However, if the output voltage is still less than 40% of the input voltage, the switch turns off, with subsequent auto-retry at the hiccup timer interval. But if the output voltage is over 40% of the input, the R_{ISET} current-limit takes over to charge the large capacitive load at the output. See the *Heavy Load Soft-Start Response* in the *Typical Characteristics* section.

Fast Turn ON (KTS1890A only)

To support USB power delivery (PD) fast role swap (FRS), set the FON pin to logic 1. With FON = 1, the turn-on delay is reduced to 50µs (max), and the rise time is reduced to 100µs (max). There are two start-up sequences for fast turn ON:

1. If $V_{OUT} < V_{IN}$, when EN goes high, the switch performs a Fast Turn ON, and the switch turns ON within 150µs (max).
2. If $V_{OUT} > V_{IN}$, even though EN is high, the switch enters RCP mode and remains OFF. Later when V_{OUT} returns below V_{IN}, the RCP Fast-Recovery turns ON the switch within 15µs (typ).

Note that during a Fast Turn ON, inrush current is much higher than during slew-rate controlled turn ON. For this reason, increase C_{IN} to 2x 47µF or more as close to the IN pin as possible. Also note that during an RCP Fast-Recovery with FON = 0 or 1, the inrush current may also be high, depending upon how quickly V_{OUT} is collapsing.

"Ideal Diode" Droop Regulation for Reverse Current Protection (RCP)

When the switch is turned ON, the KTS1890 dynamically adjusts the MOSFET gate drive voltage to regulate the voltage droop from IN to OUT to 20mV. At light loads, the gate drive is reduced to maintain the 20mV from IN to OUT. The droop-regulation inherently provides automatic entry and exit from the reverse current protection (RCP) mode.

During heavy load conditions, the R_{ON} of the switches may cause more than 20mV droop, but the RCP control then drives the gate until the switch is fully turned ON to keep the dropout as low as possible. Dropout typically occurs when the load is greater than 20mV/27mΩ = 741mA.

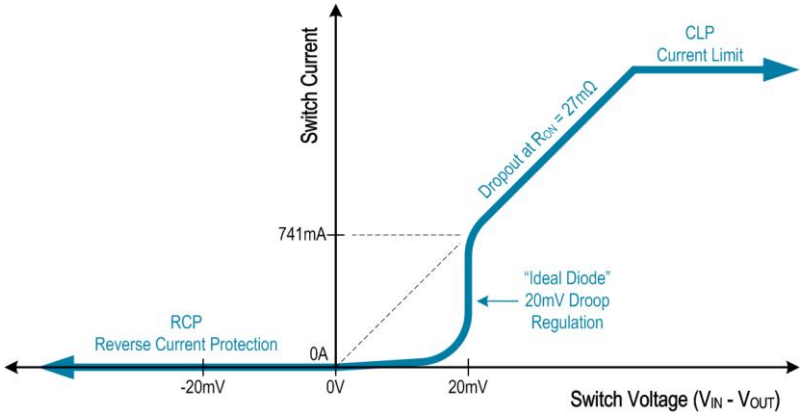


Figure 5. Switch Current vs. Voltage for RCP, Dropout, and CLP

Current Limit Protection (CLP)

Program the current limit using an external resistor, R_{ISET}, connected between the ISET and GND pins. See the *Switch Specifications* within the *Electrical Characteristics* and the *Current Limit Protection vs. R_{ISET}* graph in the *Typical Characteristics* section. Calculate the desired nominal current limit I_{CLP} per R_{ISET} using the following equation:

$$I_{CLP} = \frac{47500}{R_{ISET}}$$

Whenever the switch current reaches the programmed current limit, the current limit regulation loop takes control and reduces the MOSFET gate drive to limit the switch current. During CLP, the switch acts as a constant current source, and the output voltage reduces depending on the load current. Once the load current reduces below the current limit, the output voltage rises again.

During extended CLP events, power dissipation increases, causing the die to heat up and possibly enter over-temperature protection (thermal shutdown). When the chip temperature cools, the device recovers and turns back ON with auto-retry via hiccup delay time (to allow additional cooling) followed by soft-start.

Over-Current Protection (OCP)

During a sudden output short-circuit to ground event, switch current may ramp up very quickly, faster than the bandwidth of the CLP regulation loop. For this reason, the KTS1890 includes an additional over-current protection circuit (OCP). If the switch current exceeds the over-current threshold, OCP turns OFF the switch very quickly with 150ns (typ) response time. Once off, the switch is turned back ON with auto-retry via hiccup delay time (to allow cooling) followed by soft-start.

Short-Circuit Protection (SCP)

The OCP function provides protection for short-circuit events that occur while the switch is already enabled. But for starting into a pre-existing short at the output, the KTS1890 includes additional short-circuit protection (SCP) circuitry. During normal turn-on (FON = 0), the current limit is held to 0.8A for up to 7ms. Additionally, if the V_{OUT} fails to rise above 40% of V_{IN}, the switch is turned off, but automatically retries after the 70ms hiccup time.

CLP and SCP Use Cases

There are four use-cases for current limiting:

1. Turn ON into large capacitive load – during normal soft-start with very large capacitive loads, the slew-rate control may not be enough to prevent the switch current from reaching its soft-start current limit. In this case, the output voltage does rise, but the soft-start current limit may extend the V_{OUT} rise time. Usually, the extended rise-time is too short to trigger thermal shutdown.
2. Turn ON into an output short-circuit to ground fault – if the output is already shorted to ground prior to start up, then V_{OUT} does not rise when EN is set to logic 1. In this case, the switch current is limited to 0.8A, and the IC dissipates significant power, $P_D = V_{IN} \times I_{CLP\_SS}$, making thermal shutdown more likely. After 7ms, if thermal shutdown has not occurred, and V_{OUT} remains below $0.4V_{IN}$, the SCP detection turns off the switch. After a 70ms hiccup time to allow the IC to cool, the soft-start retries.
3. OUT over-current event while already enabled – if the load current exceeds the current limit while the switch is already ON, then the switch current is limited to the programmed CLP current level and the output voltage sags. As V_{OUT} sags, most loads typically reduce their current requirements, so V_{OUT} usually settles at an intermediate voltage without complete collapse. The power dissipation, $P_D = (V_{IN} – V_{OUT\_SAG})$

x I_{CLP}, is less than during an output short-circuit fault condition, so thermal shutdown is less likely, but still possible.

4. OUT short-circuit fault while already enabled – if the output is suddenly shorted to ground while the switch is already ON, then the switch current may rise very rapidly and temporarily exceed the programmed CLP current limit.
    a. If the switch current reaches the OCP current threshold, the switch is turned OFF very quickly, and then restarted as in use-case 2 above.
    b. If the switch current does not reach the OCP current threshold quickly, then the CLP control loop reduces the switch current to the programmed current level. In this case, the IC dissipates significant power, $P_D = (V_{IN} – V_{OUT}) \times I_{CLP}$, making thermal shutdown more likely. But if the output falls to 40% of V_{IN}, the switch is turned OFF very quickly, and then restarted as in use-case 2 above.

Reverse Current Protection (RCP) "Ideal Diode"

In situations when V_{OUT} is driven above V_{IN} (for example when USB charging with elevated voltage at VBUS), the RCP control turns the switch OFF automatically due to its 20mV droop regulation control loop. The reverse blocking MOSFET is inherently turned OFF whenever $V_{OUT} > V_{IN}$ - 20mV and turned ON again when $V_{OUT} < V_{IN}$ – 20mV.

Every time the device starts up, it prechecks if V_{OUT} is higher than V_{IN} or not. If yes, the reverse blocking MOSFET is kept OFF and reverse current is blocked. Then, after V_{OUT} returns below V_{IN}, it is turned ON quickly in about 15µs. The RCP Fast-Recovery is assisted by the internal gate-drive charge pump, which is enabled whenever EN = 1, even during RCP (when the switch is OFF). Since the gate-drive voltage is already present, a fast recovery time is easily achieved as soon as V_{OUT} falls below V_{IN} by more than 20mV.

Over Temperature Protection (OTP)

The KTS1890 features thermal shutdown to prevent the device from overheating. The internal MOSFETs turn OFF when the junction temperature exceeds +150°C (typ), and $\overline{FLT}$ is asserted. The device exits thermal shutdown after the junction temperature cools by 20°C (typ) hysteresis, followed by the hiccup delay and soft-start, and then $\overline{FLT}$ is de-asserted.

Fault Reporting ($\overline{FLT}$)

See Table 1. In a current limit protection (CLP), over current protection (OCP), short-circuit protection (SCP), or over temperature protection (OTP) condition, the open-drain $\overline{FLT}$ pin is asserted LOW. A pull-up resistor should be connected from the $\overline{FLT}$ pin to the system I/O voltage rail. The $\overline{FLT}$ output returns to the high-Z state automatically once the fault condition is removed. The RCP circuit does not trigger a $\overline{FLT}$ indication.

For CLP events, an internal 8ms (typ) timer delays the fault indication at the $\overline{FLT}$ pin. However, for other fault events, the $\overline{FLT}$ indication asserts immediately. The $\overline{FLT}$ output flag is specifically designed to not toggle during a fault event, or when transitioning from a CLP fault to an OTP fault, or when recovering from an OTP fault and going back into a CLP fault. To prevent toggling, an internal 17ms (typ) timer delays the release of the $\overline{FLT}$ pin to the high-Z state after recovery from all faults.

EN	FON	VIN	$\overline{FLT}$	Event or Condition
X	X	< V_{UVLO}	Z	UVLO, Switch Off
L	X	2.5V to 5.5V	Z	Shutdown Mode, Switch Off
H	L	2.5V to 5.5V	Z	Device Enabled, Soft-Start Slew-Rate Enabled
H	H	2.5V to 5.5V	Z	Device Enabled, Fast Turn ON Enabled
H	X	2.5V to 5.5V	Z	Device Enabled, CLP Event before $t_{D\_\overline{FLT}}$, Switch is on
H	X	2.5V to 5.5V	L	Device Enabled, CLP Event after $t_{D\_\overline{FLT}}$, Switch is on
H	X	2.5V to 5.5V	L	Device Enabled, OCP or SCP or OTP Event, Switch Open
X	X	2.5V to 5.5V & V_{OUT} > V_{IN}	Z	RCP Event, Switch Open

Table 1. $\overline{FLT}$ Open-Drain Output Flag Truth Table

Applications Information

Input Capacitor C_{IN} Selection

For most applications, connect a 10µF (local minimum) to 1000µF or higher total ceramic capacitance as close as possible to the device from IN to GND to minimize the effect of parasitic trace inductance. 6.3V rated capacitors with X5R or better dielectric are recommended.

Output Capacitor C_{OUT} Selection

For most applications, connect from 1µF to 10µF total capacitance to the output. Typical applications use 10µF to optimize surge and ESD performance. 50V rated capacitors with X5R or better dielectric are recommended to enable the 35V withstand and TVS surge clamping voltage (46V typical for +130V surge event).

Recommended PCB Layout

Good PCB thermal design is required to support heavy load currents. The KTS1890 EVB is designed with similar layout as Figure 6, but it extends the fill area for the IN, OUT, and GND copper planes to about 4 square inches total area for increased thermal performance. Due to the number of bumps on IN and OUT, these two planes are especially important and should not be ignored. Adding back-side and/or buried-layer fill area with thermal vias also helps significantly.

Other than thermal concerns, the PCB layout for the KTS1890 is quite simple. Place the input and output capacitors near the IC. Connect the capacitor ground terminals together and to the GND pins using the top-side copper layer. Route the control signals on buried layers.

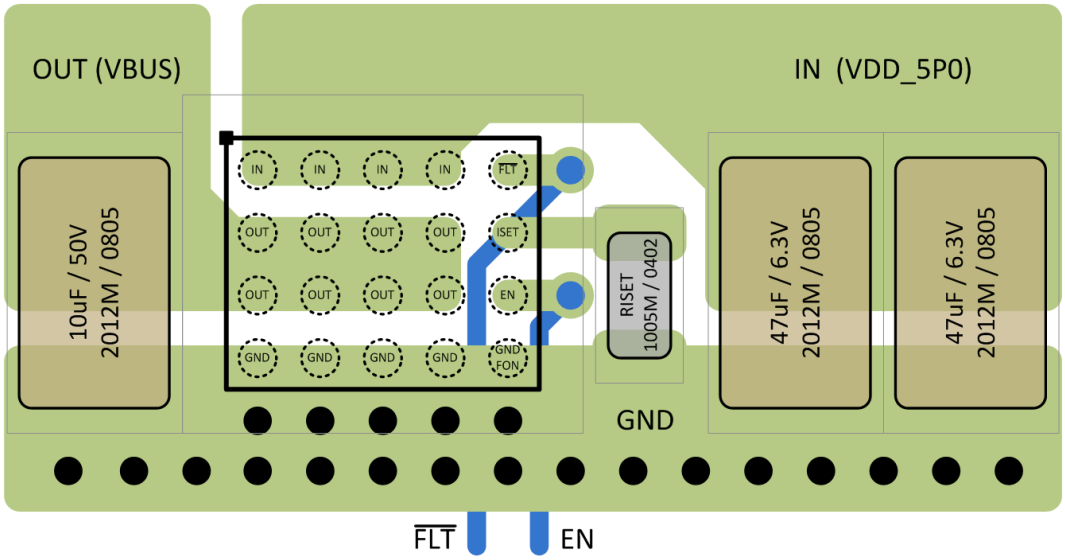


Figure 6. Recommended PCB Layout

Safe Operating Area (SOA)

See Figure 7 for the SOA of the KTS1890. SOA curves are normally associated with discrete MOSFETs (which are sometimes co-package with a controller IC). In these competing systems, precautions are necessary to stay within the SOA area. However, the KTS1890 is a monolithic IC with multiple integrated protection features to *automatically* keep its operation within the SOA area (so long as the abs. max. rating AMR voltage is observed). For example, it includes settable current limit protection (CLP). It also includes over-temperature protection (OTP) that is measured on the same monolithic die as the integrated power MOSFETs. Additionally, soft-start is controlled with a voltage ramp and current limit protection (Soft-Start CLP) to safely soft-start even in applications with very high capacitance at the output. Furthermore, the integrated TVS and back-to-back MOSFET switch are optimized to work together as a system, including their tolerances over temperature and process corners.

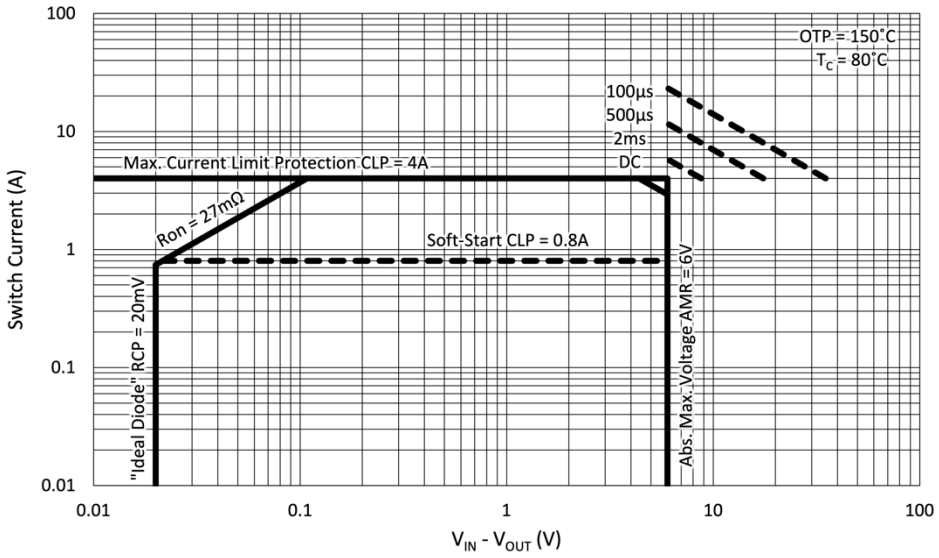
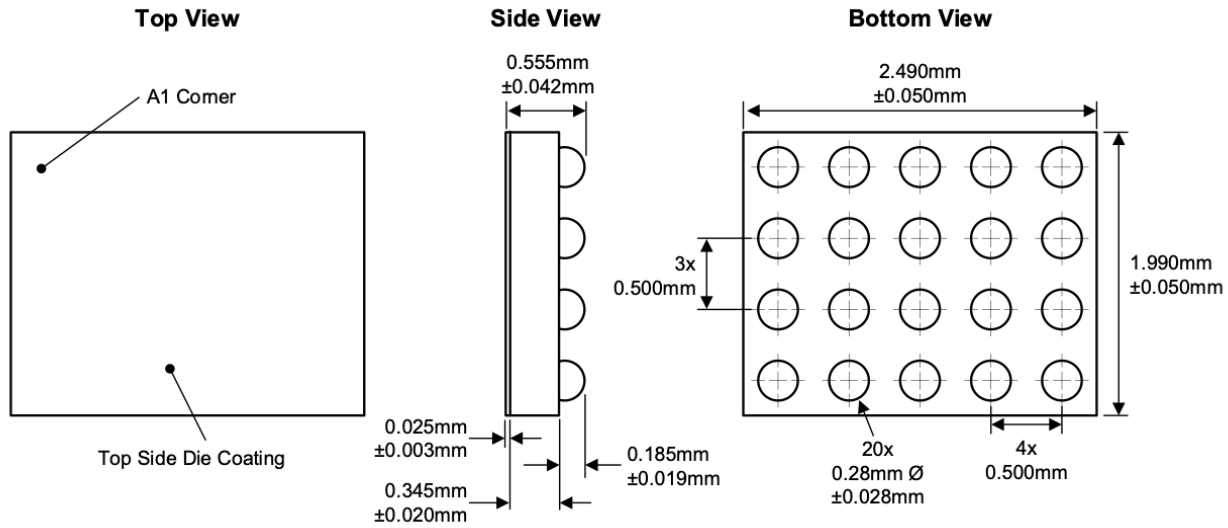


Figure 7. Safe Operating Area (SOA) for T_C = 80℃

Packaging Information

WLCSP54-20 (2.490mm x 1.990mm x 0.555mm) (Package Code: IAC)



Recommended Footprint