5A$_{RMS}$ VBUS Current-Sink Protection Load Switch

Features

- 3V to 24V Operating Voltage Range
- 29V Abs. Max. Rating at IN and OUT
- 5A Continuous Current Rating
  - ▶ 12A Pulse Current Rating (duration Pd limited)
- 25mΩ typ. On-Resistance from IN to OUT
- Soft-Start (SS) Limits Inrush Current
- Over-Voltage Protection (OVP) at IN
  - ▶ 24V Internally Fixed
  - ▶ 4V to 24V External Resistor Programmable
- "Ideal Diode" Reverse Current Protection
- 20mV Forward Voltage and 15µs Fast Recovery
- Over-Current Protection (OCP) at OUT
- Short-Circuit Protection (SCP) at OUT
- Over-Temperature Protection (OTP)
- Auto-Retry after All Faults
- EN or $\overline{EN}$ Enable Logic Input Versions
- $\overline{ACOK}$ Open-Drain Power Good Flag
- -40°C to 85°C Operating Temperature Range
- 12-bump WLCSP 2.18 x 1.64mm (0.5mm pitch)

Brief Description

KTS1672 is a low-resistance, high-current load switch with soft-start, over-voltage protection, reverse-current blocking, over-current protection, short-circuit protection, over-temperature protection. It is optimized to protect systems with USB Type-C PD ports and barrel connectors that sink up to 100W at 20V and must withstand up to 29V on VBUS.

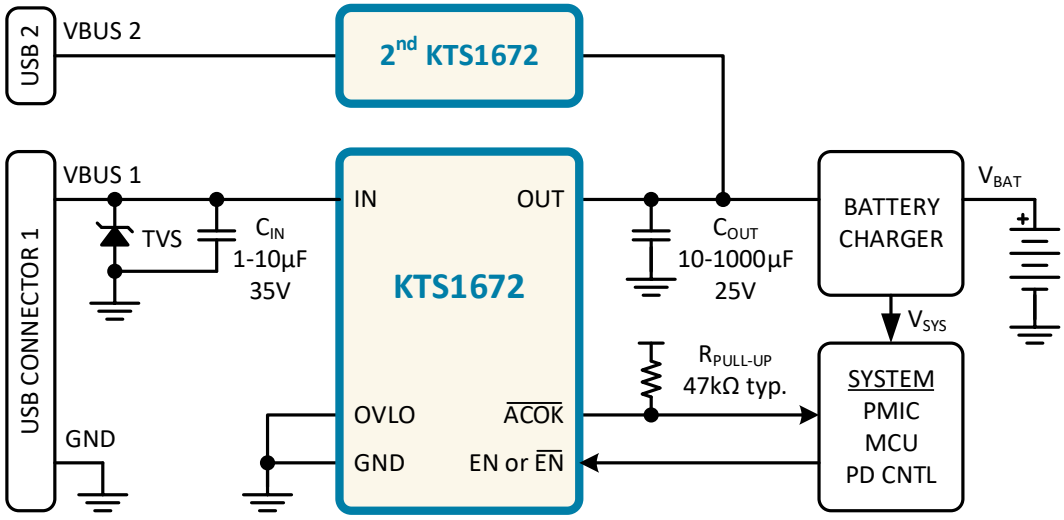
KTS1672 has automatic reverse-current blocking feature which acts as an "ideal diode" and isolates VBUS when charging or powering the system via another port. Soft-start limits inrush current when turning on with large capacitors at the output. An $\overline{ACOK}$ flag indicates when power is good.

KTS1672 is packaged in advanced, fully "green" compliant, 2.18 x 1.64mm, 12-bump Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Desktop, Notebooks, Netbooks, Ultra-Books, Tablets
- Docking Stations, Monitors, Accessories

Typical Application

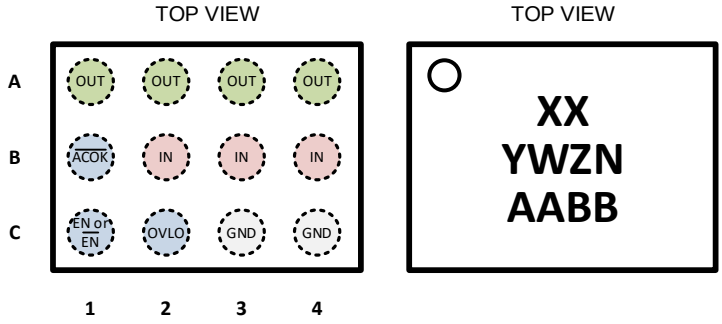


Ordering Information

Part Number	Marking[1]	Enable Polarity	Operating Temperature	Package
KTS1672AEGAE-TA	USYWZNAABB	$\overline{EN}$	-40°C to +85°C	WLCSP-12
KTS1672BEGAE-TA	UTYWZNAABB	EN	-40°C to +85°C	WLCSP-12

Pinout Diagram

WLCSP43-12



12-bump 1.64mm x 2.18mm x 0.555mm
WLCSP Package, 0.5mm pitch

Top Mark

XX = Device Code, YW = Date Code, Z = Serial Number, N = Wafer ID
AABB = Axis Coordinates

Pin Descriptions

Pin #	Name	Function
A1, A2, A3, A4	OUT	Power Switch Output – connect to battery charger IC input (or VSYS in systems without rechargeable batteries).
B2, B3, B4	IN	Power Switch Input – connect to power input port (VBUS on USB port).
B1	$\overline{ACOK}$	Power Good Flag – active-low, open-drain logic output. Connect to GND or leave floating if unused.
C1	$\overline{EN}$	$\overline{Enable}$ – active-low logic input (KTS1672A)
	EN	Enable – active-high logic input (KTS1672B)
C2	OVLO	External OVLO Adjustment – connect to GND to use the internally fixed OVLO threshold. Connect an external resistive voltage divider from IN to OVLO to GND to set an adjustable the OVLO threshold.
C3, C4	GND	Ground

1. US & UT = Device Code, YW = Date Code, Z = Serial Number, N = Wafer ID, AABB = Axis Coordinates.

Absolute Maximum Ratings[2]

Symbol	Description	Value	Units
V_{IN}	IN to GND (continuous)	-0.3 to 29	V
	IN to GND (during IEC61000-4-5 surge event with external TVS)	-5 to 36	
V_{OUT}	OUT to GND	-0.3 to 29	V
V_{IN-OUT}	IN to OUT	-29 to 29	V
V_{EN}, $V_{\overline{EN}}$	EN, $\overline{EN}$ to GND	-0.3 to 29	V
V_{OVLO}	OVLO to GND	-0.3 to V_{IN}	V
$V_{\overline{ACOK}}$	$\overline{ACOK}$ to GND	-0.3 to 6	V
I_{SW}	Maximum Switch Current (continuous)	5	A
	Peak Switch Current (duration is Pd limited)	12	
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD Ratings[3]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV

Thermal Capabilities[4]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	70.83	°C/W
P_D	Maximum Power Dissipation at 25°C	1.41	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C (T_J = 150°C)	-14.12	mW/°C

2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
3. ESD Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance.
4. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions[5]

Symbol	Description	Value	Units
V_{IN}	Supply Voltage Operating Range	3 to 24	V
V_{OUT}	Output Voltage Range	3 to 24	V
$V_{\overline{ACOK}}$	Power Good Flag Output Voltage	0 to 5.5	V
V_{OVLO}	OVLO Adjust Input Bias Voltage		V
V_{EN}, $V_{\overline{EN}}$	Enable Logic Input Voltage	0 to 24	V
C_{IN}	Input Capacitance	1 to 10	µF
		35	V
C_{OUT}	Output Capacitance	10 to 1000	µF
		25	V

Electrical Characteristics[6]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 3V to 24V or V_{OUT} = 3V to 24V. Typical values are specified at T_A = +25°C with V_{IN} = 5V or V_{OUT} = 5V.

Supply Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Operating Range		3		24	V
V_{OUT}	Output Voltage Operating Range		3		24	V
V_{UVLO}	Under-Voltage Lockout	V_{IN} rising threshold		2.7	2.95	V
		Hysteresis		200		mV
I_Q	No-Load Supply Current (Enabled)	V_{IN} = 5V, OUT = open		190		µA
		V_{IN} = 20V, OUT = open		250		
I_{SHDN}	Shutdown Supply Current	V_{IN} = 5V, OUT = open		1		µA
		V_{IN} = 20V, OUT = open		2.6		
I_{OUT_RCP}	Output Supply Current in RCP	Enabled, V_{IN} = 0V, V_{OUT} = 5V		250		µA

(continued next page)

5. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.
6. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

Electrical Characteristics (continued)[7]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 3V to 24V or V_{OUT} = 3V to 24V. Typical values are specified at T_A = +25°C with V_{IN} = 5V or V_{OUT} = 5V.

Logic Pin Specifications (EN, $\overline{EN}$, $\overline{ACOK}$)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High (EN, $\overline{EN}$)		1.2			V
V_{IL}	Input Logic Low (EN, $\overline{EN}$)				0.4	V
R_{I_PD}	Input Logic Pull-Down ($\overline{EN}$)			1		MΩ
I_{I_LK}	Input Logic Leakage (EN)	V_I = 5V	-1		1	µA
		V_I = 20V	-1		1	µA
V_{OL}	Output Logic Low ($\overline{ACOK}$)	I_{O_SINK} = 1mA		0.01	0.2	V
I_{O_LK}	Output Logic High-Z Leakage ($\overline{ACOK}$)	V_O = 5V	-1		1	µA

Switch Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON}	Switch On-Resistance	V_{IN} = 5V		25	30	mΩ
		V_{IN} = 20V		25	30	
I_{IN_OFF}	Switch Off-Leakage at IN	Shutdown, V_{IN} = 5V, V_{OUT} = 0V		1		µA
		Shutdown, V_{IN} = 20V, V_{OUT} = 0V		2.6		
I_{OUT_OFF}	Switch Off-Leakage at OUT	Shutdown, V_{IN} = 0V, V_{OUT} = 5V		1		µA
		Shutdown, V_{IN} = 0V, V_{OUT} = 20V		2.6		

Soft-Start (SS) Specifications (see Figure 1)

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DEB}	Soft-Start Debounce Time[8]	R_L = 100Ω, C_{OUT} = 300µF, V_{IN} = 5V		18		ms
t_R	Soft-Start V_{OUT} Rising Slew-Rate Ramp Time[9]	R_L = 10Ω, C_{OUT} = 300µF, V_{IN} = 5V		2.3		ms
		R_L = 100Ω, C_{OUT} = 300µF, V_{IN} = 20V		2.6		
I_{LIM_SS}	Soft-Start Current Limit	V_{IN} = 5V to 20V		2.6		A
t_{LIM_SS}	Soft-Start Current Limit Done Time[10]	V_{IN} = 5V to 20V		7		ms
$t_{\overline{ACOK}}$	Power Good Flag Delay after t_{LIM_SS}[10]	V_{IN} = 5V to 20V		3		ms
t_{DOFF}	Turn-Off Delay Time[10, 11]	V_{IN} = 5V to 20V	0		10	µs

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7. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
8. t_{DEB} is time from EN = H and $V_{UVLO} < V_{IN} < V_{OVP}$ until V_{OUT} = 10%*V_{IN}.
9. t_R is time from V_{OUT} = 10%*V_{IN} until V_{OUT} = 90%*V_{IN}.
10. Guaranteed by design, characterization and statistical process control methods; not production tested.
11. t_{DOFF} is time from disable logic until VOUT begins to fall.

Electrical Characteristics (continued)[12]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 3V to 24V or V_{OUT} = 3V to 24V. Typical values are specified at T_A = +25°C with V_{IN} = 5V or V_{OUT} = 5V.

Over-Voltage Protection (OVP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OVP}	Internally Fixed Over-Voltage Protection	V_{IN} rising OVP threshold	23	24	25	V
		Hysteresis, V_{OVLO} = 0V		800		mV
t_{OVP}	OVP Response Time[10, 13]	R_L = 100Ω, C_{OUT} = 0µF, V_{IN} > V_{OVP}, V_{OVLO} = 0V		90		ns
t_{OVP_REC}	OVP Recovery Time[10, 14]			t_{DEB}+t_R		ms
V_{OVLO}	Externally Adjustable Over-Voltage Lockout	V_{OVLO} enable threshold	0.15	0.25	0.35	V
		V_{OVLO} rising OVP threshold	1.15	1.22	1.29	V
		Hysteresis		25		mV
t_{OVLO}	OVLO Response Time[10, 15]	R_L = 100Ω, C_{OUT} = 0µF		300		ns
t_{OVLO_REC}	OVLO Recovery Time[10]			t_{DEB}+t_R		ms

Reverse-Current Protection (RCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RCP}	RCP Droop Regulation Voltage	V_{RCP} = V_{IN} – V_{OUT}, I_{OUT} = 100mA	10	20	30	mV
t_{RCP_REC}	RCP Fast Recovery Time[10, 16]			15		µs

Over-Current Protection (OCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{OCP}	Over-Current Threshold[10]		12	18		A
t_{OCP}	OCP Response Time[10, 17]			100		ns
t_{OCP_REC}	OCP Recovery Time[10]			t_{DEB}+t_R		ms

Over-Temperature Protection (OTP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{OTP}	IC Junction Over-Temperature Protection[10]	T_J rising threshold		145		°C
		Hysteresis		15		°C
t_{OTP_REC}	OTP Recovery Time[10]			t_{DEB}+t_R		ms

12. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
13. t_{OVP} is time from V_{IN} > V_{OVP} until V_{OUT} stops rising.
14. t_{OVP_REC} is time from V_{IN} < V_{OVP} until V_{OUT} = 90%*V_{IN}.
15. t_{OVLO} is time from V_{OVLO} rises above its OVP threshold until V_{OUT} stops rising
16. t_{RCP_REC} is time from V_{OUT} < V_{IN} – 90mV until switch turns back on. Before measuring, first raise V_{OUT} higher than V_{IN} + 300mV.
17. t_{OCP} is time from I_{OUT} > I_{OCP} until switch turns off.

Timing Diagrams

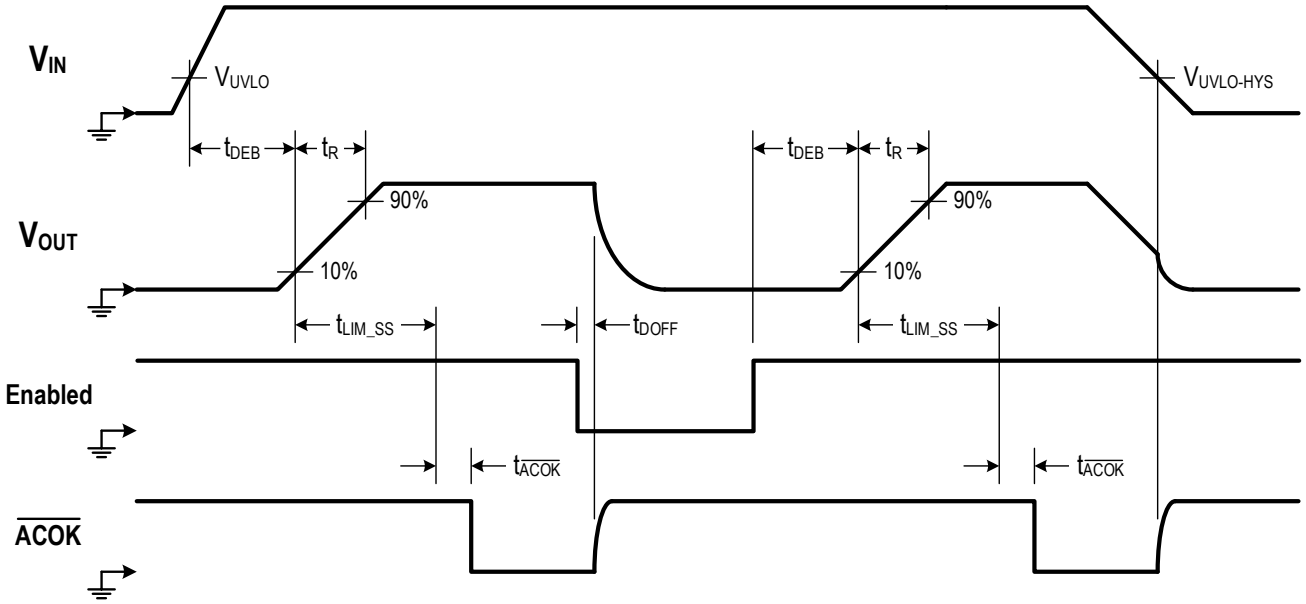


Figure 1. UVLO, Soft-Start and Turn-Off Timing Diagram

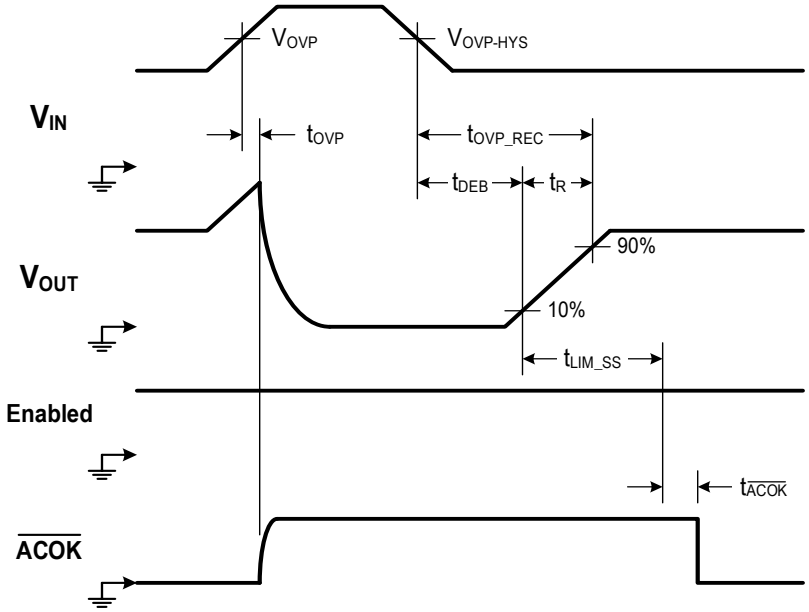


Figure 2. OVP Timing Diagram

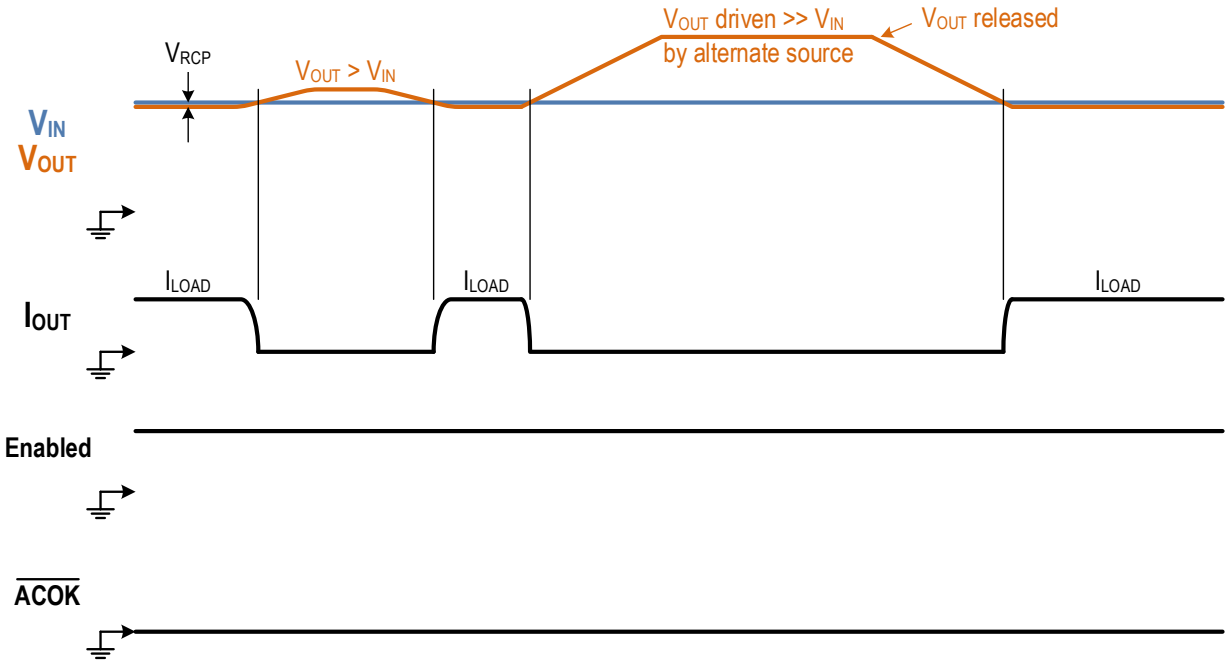


Figure 3. "Ideal Diode" RCP Timing Diagram with Fast Recovery

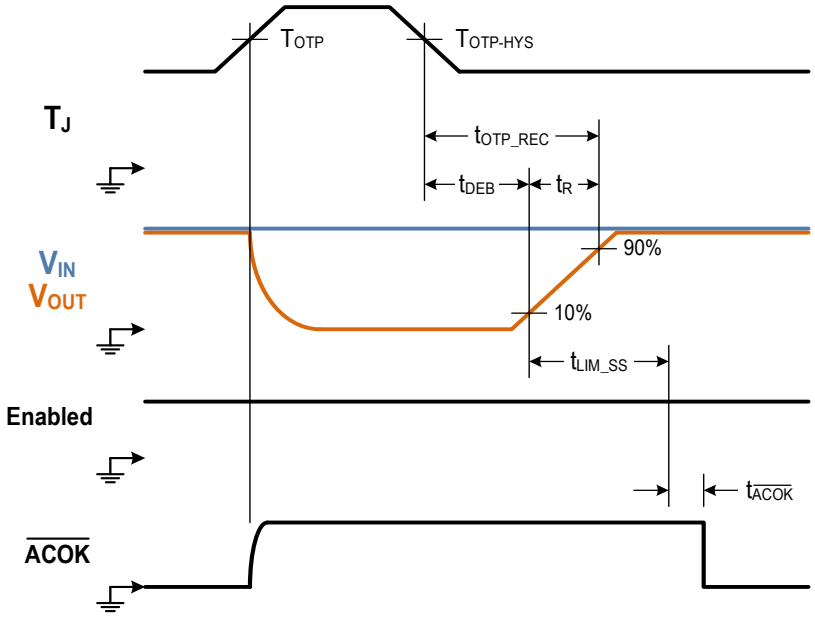


Figure 4. OTP Timing Diagram

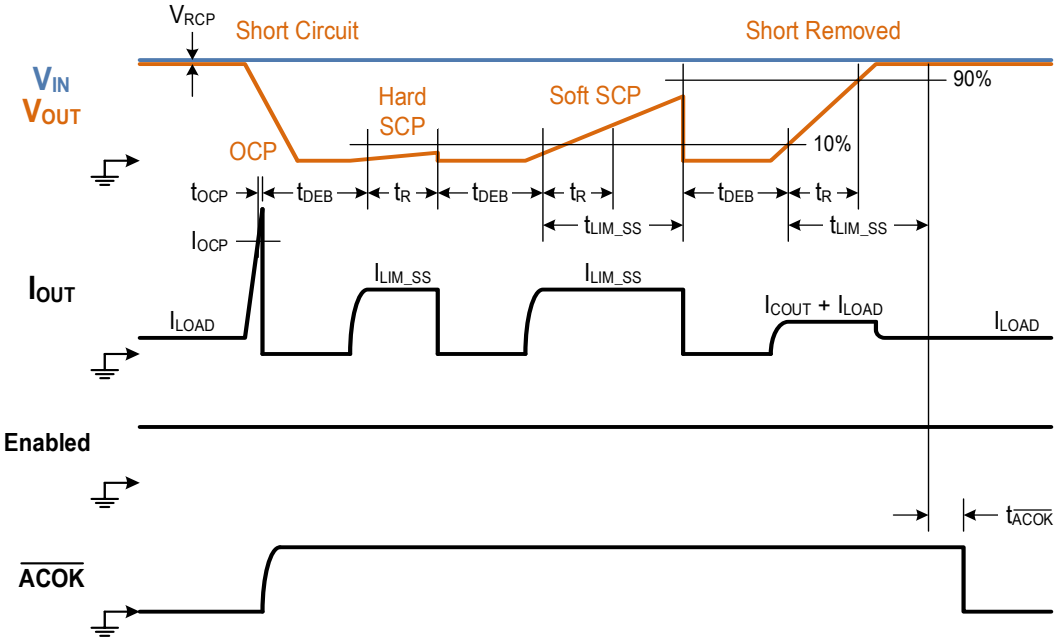
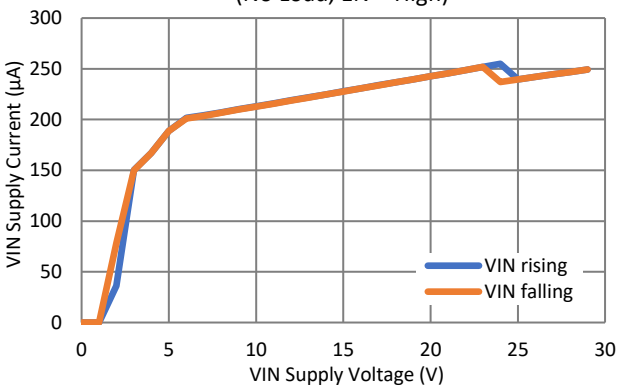


Figure 5. OCP and SCP Timing Diagram

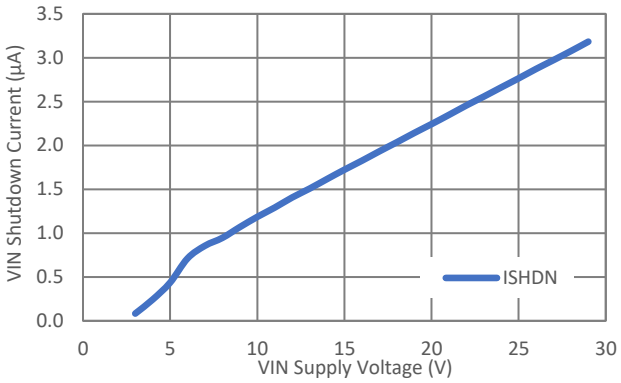
Typical Characteristics

C_{IN} = 10µF, C_{OUT} = 20µF, and T_A = +25°C unless otherwise noted.

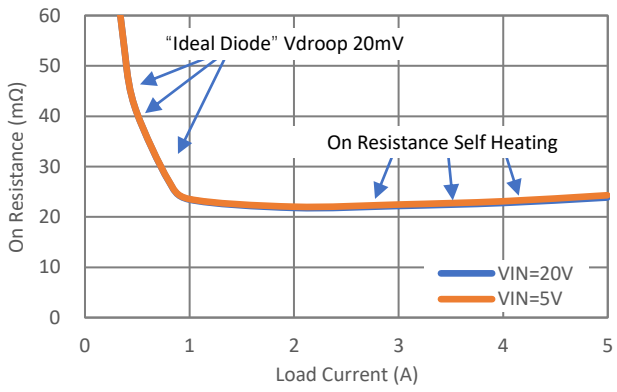
VIN Supply Current Vs. Supply Voltage
(No Load, EN = High)



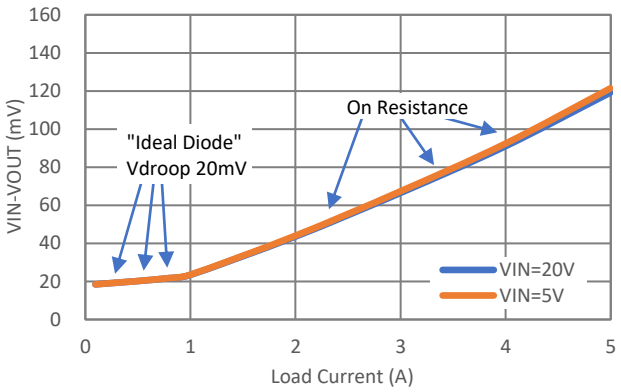
VIN Shutdown Current Vs. Supply Voltage
(No Load, EN = Low)



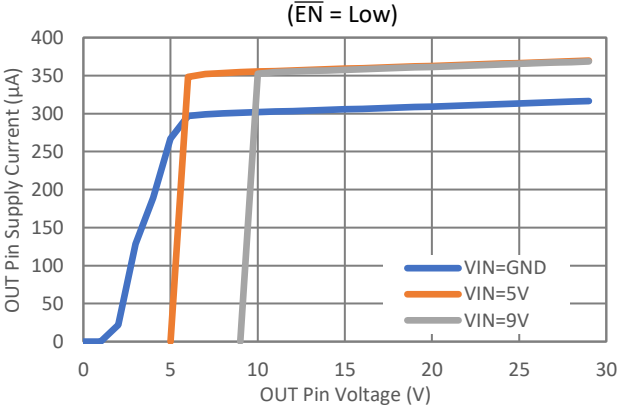
On Resistance Vs. Load Current



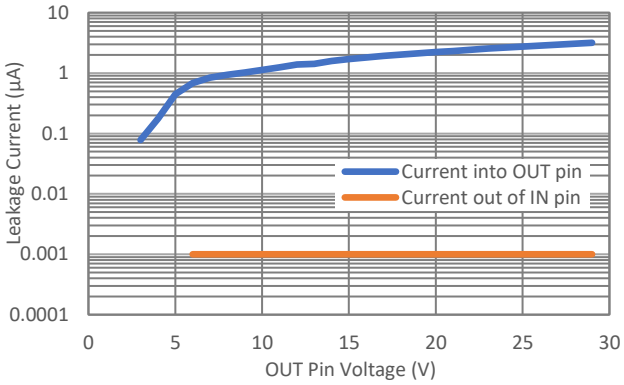
"Ideal Diode" Vdroop Vs. Load Current



RCP Supply Current at OUT Pin
($\overline{EN}$ = Low)



Reverse Leakage Current at OUT and IN Pins
($\overline{EN}$ = High)



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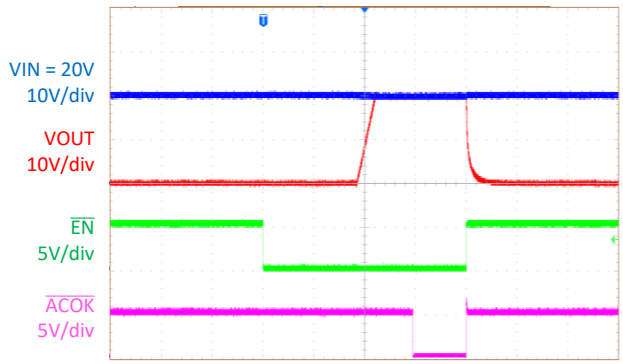
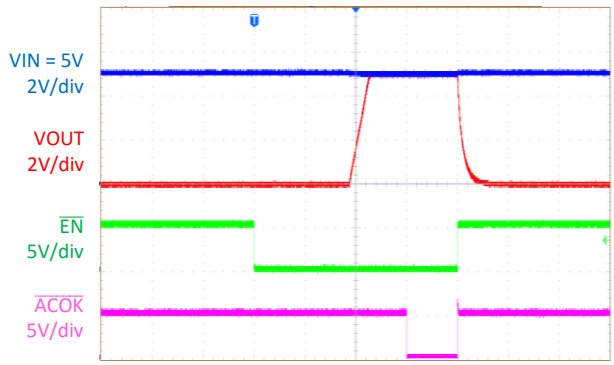
Typical Characteristics (continued)

C_{IN} = 10µF, C_{OUT} = 20µF, and T_A = +25°C unless otherwise noted.

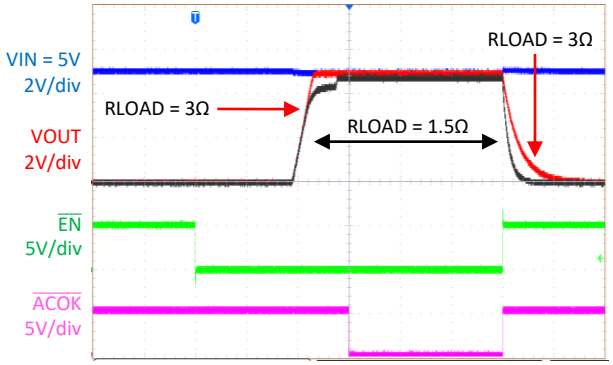
Enable, Soft-Start, Shutdown Response
(VIN = 20V)



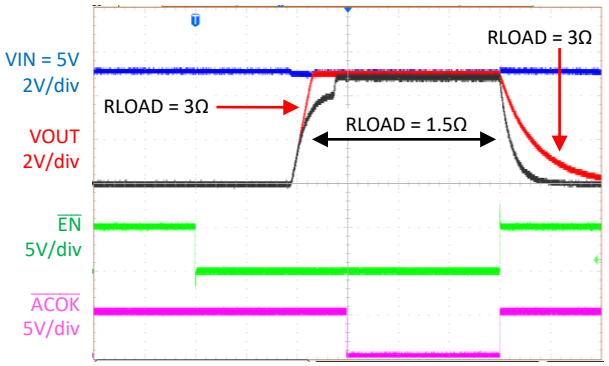
Enable, Soft-Start, Shutdown Response
(VIN = 5V)



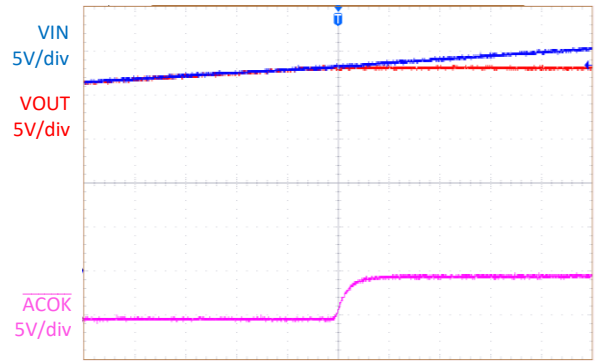
Heavy Load Soft-Start Response
(VIN = 5V, COUT=1000µF)



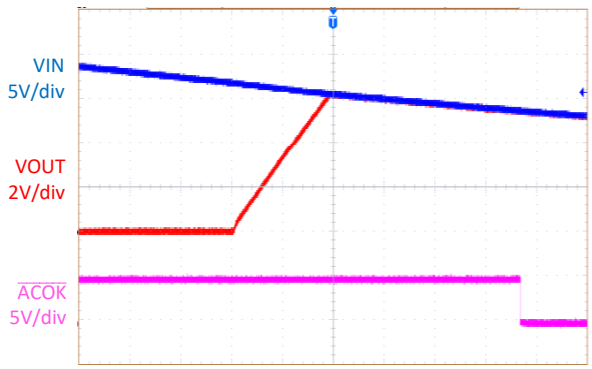
Heavy Load Soft-Start Response
(VIN = 5V, COUT = 2000µF)



OVP Response
(VIN = 15V → 28V Short)



OVP Response
(VIN = 28V Short Removal → 15V)



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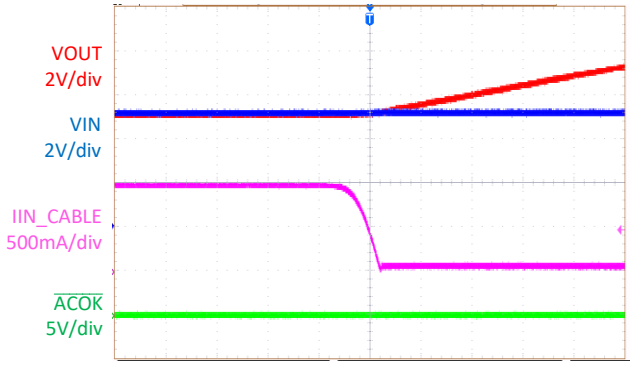
Typical Characteristics

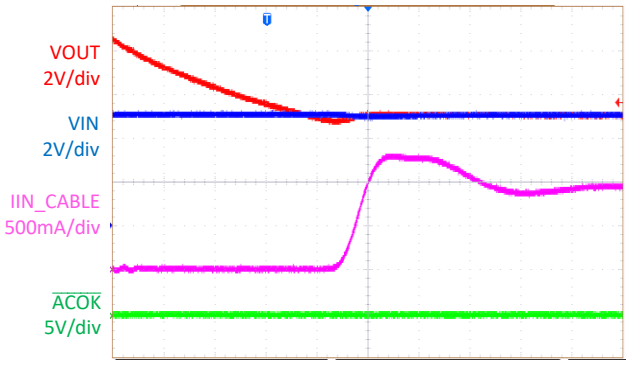
C_{IN} = 10µF, C_{OUT} = 20µF, and T_A = +25°C unless otherwise noted.

RCP Response
(VIN = 5.1V, R_{CABLE} = 200mΩ, Load = 5Ω, VOUT = 5V → 9V)



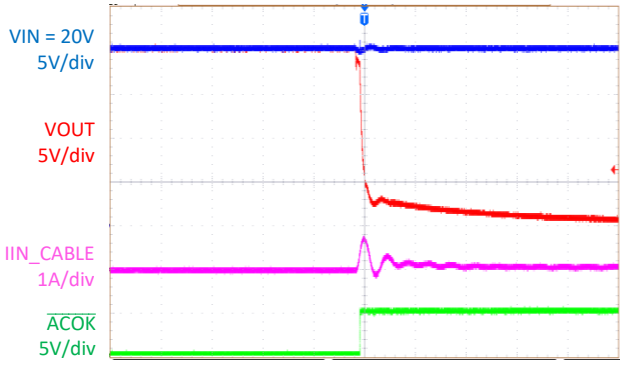
200µs/div

RCP Fast Recovery
(VIN = 5.1V, R_{CABLE} = 200mΩ, Load = 5Ω, VOUT = 9V → 5V)



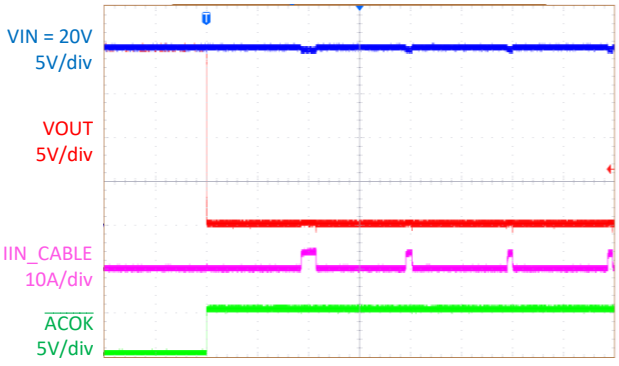
10µs/div

OCP Response
(VIN = 20V, VOUT = 20V → Short Circuit)



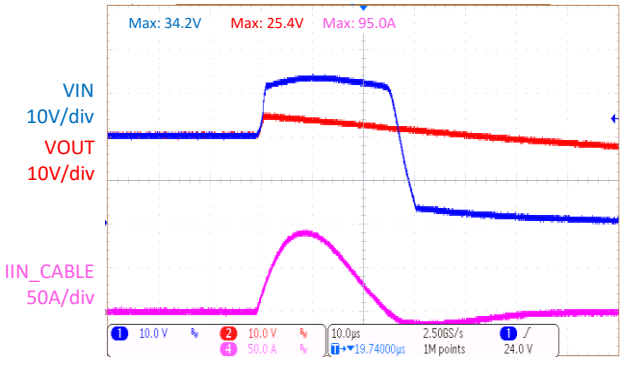
10µs/div

SCP Response with Auto - Retry
(VIN = 20V, VOUT = 20V → Short Circuit)



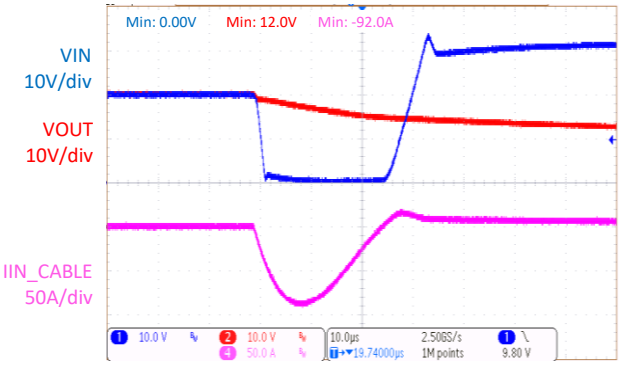
10ms/div

Surge Transient Response
(VIN = 20V + 200V Surge with KTS1650B)



10µs/div

Surge Transient Response
(VIN = 20V - 200V Surge with KTS1650B)



10µs/div

Functional Block Diagram

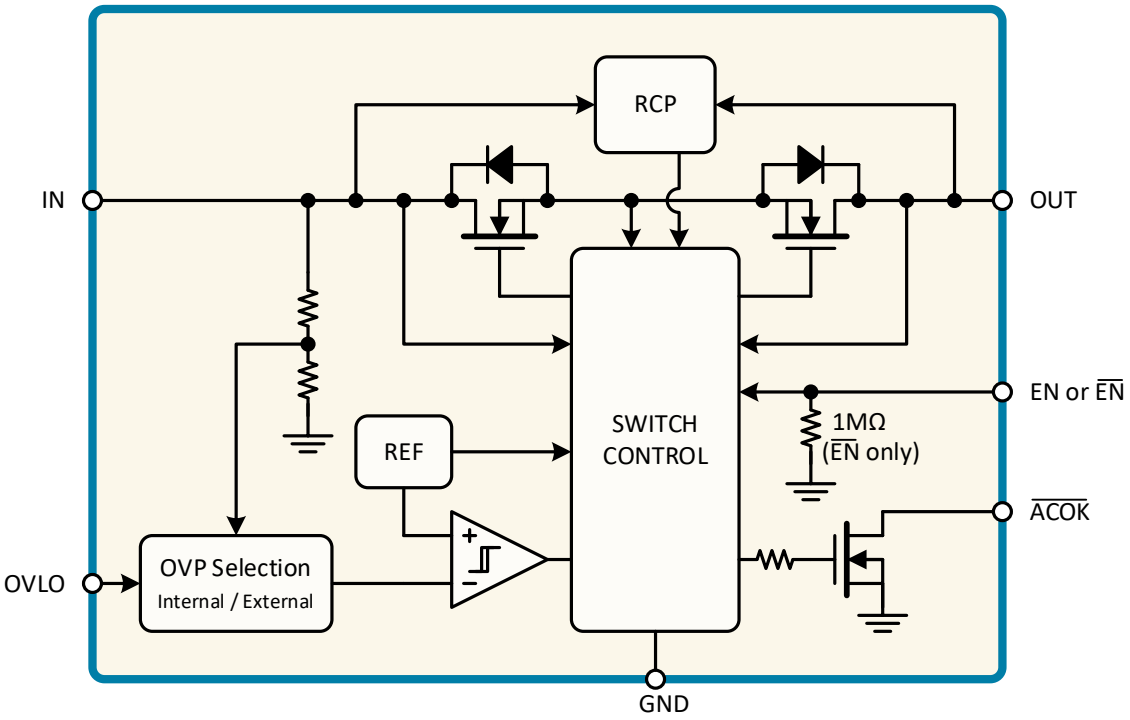


Figure 6. Functional Block Diagram

Functional Description

The KTS1672 is a slew-rate controlled, 25mΩ (typ) low resistance MOSFET switch intended to be inserted between a power source and a load to isolate and protect against abnormal voltage and current conditions. Featuring slew-rate controlled soft-start and soft-start current limit to prevent excessive large inrush current, the KTS1672 also features several additional protection functions. These include input over-voltage protection, “ideal diode” reverse-current protection with fast recovery, output short-circuit protection, over-current protection, and over-temperature protection.

Operating from a wide input voltage range of 3V to 24V, the KTS1672 is optimized for USB Type-C Power Delivery (PD) current-sink applications that require essential protection and enhanced system reliability. While in the OFF state, the KTS1672 blocks voltages of up to 29V on the IN and OUT pins and prevents current flow. While in the ON state, the KTS1672 withstands voltages of up to 29V on the IN and OUT pins, passes valid input voltages and current from IN to OUT, and blocks reverse current from OUT to IN. Due to the ideal-diode behavior, two or more KTS1672 parts connected in “diode-OR” configuration can be used in parallel to support systems that may be charged or powered from multiple ports.

Enable Input

The KTS1672A has $\overline{EN}$ active-low input logic with internal 1MΩ pull-down. The KTS1672B has EN active-high input logic. When disabled, the power switch is off and the IC is placed into low-power shutdown mode. When enabled, the protection circuits and the power switch are on. An 18ms de-bounce timer deploys before device turn-on and the soft-start ramp.

Under-Voltage Lockout (UVLO)

When $V_{IN} < V_{UVLO}$, the power switch is disabled. Once V_{IN} exceeds V_{UVLO}, the power switch is controlled by the enable pin and fault detection circuits.

Soft-Start (SS)

The internal soft-start function allows the KTS1672 to charge a total output capacitance of over 1000µF to 5V without excessive in-rush current. Soft-start controls the output voltage slew-rate ramp time. Use the below formula to calculate the current required to charge a combination of load current and output capacitance:

$$I_{IN\_SS} = I_{LOAD} + C_{OUT}\left(\frac{V_{IN}}{t_R}\right)$$

where t_R = 2.3ms. In either case, the soft-start time is somewhat fast to reduce power dissipation in the KTS1672 during soft-start.

Note that in addition to the soft-start voltage ramp, the soft-start current limit is 2.6A (typ.) to prevent excessive heat when starting into an output short-circuit condition or a large total output capacitance. This current limit is turned off after 7ms. After an additional 3ms delay, if V_{OUT} is near V_{IN}, the $\overline{ACOK}$ flag indicates a power good condition.

Over-Voltage Protection (OVP)

When logically enabled, the switch is normally on. However, if $V_{IN} > V_{OVP}$, the power switch is disabled due to an OVP fault. Once V_{IN} drops below V_{OVP}, no other fault is detected, and the enable logic is still valid, the power switch is re-enabled via the soft-start debounce and ramp time.

The OVLO pin is used to adjust the over-voltage threshold externally. The default internal over-voltage threshold is 24V when the OVLO pin is tied to GND. Biasing the OVLO pin with a resistive voltage divider adjusts the over voltage threshold from 4V to 24V as in the below formula:

$$V_{OVP} = V_{OVLO}\left(1 + \frac{R1}{R2}\right)$$

where V_{OVLO} = 1.22V. Connect R1 from IN to OVLO. Connect R2 from OVLO to ground.

"Ideal Diode" Reverse-Current Protection (RCP)

The KTS1672 offers reverse-current protection regardless of the enable logic level. When disabled, all current flow is blocked. When enabled, the RCP acts as a voltage droop regulator. Whenever the voltage on V_{OUT} is higher than V_{IN} minus 20mV, the RCP circuit reduces the MOSFET gate drive to try and maintain the regulated 20mV droop, thereby acting as an "ideal diode" with Vf = 20mV. See Figure 7. This control method blocks all reverse current. The RCP circuit makes it possible to connect two or more USB charging ports to a single battery charger IC input in a "diode-OR" configuration with autonomous reverse-current blocking. The KTS1672 includes a 15µs "fast recovery" when V_{OUT} falls back down below the "ideal diode" droop regulation point.

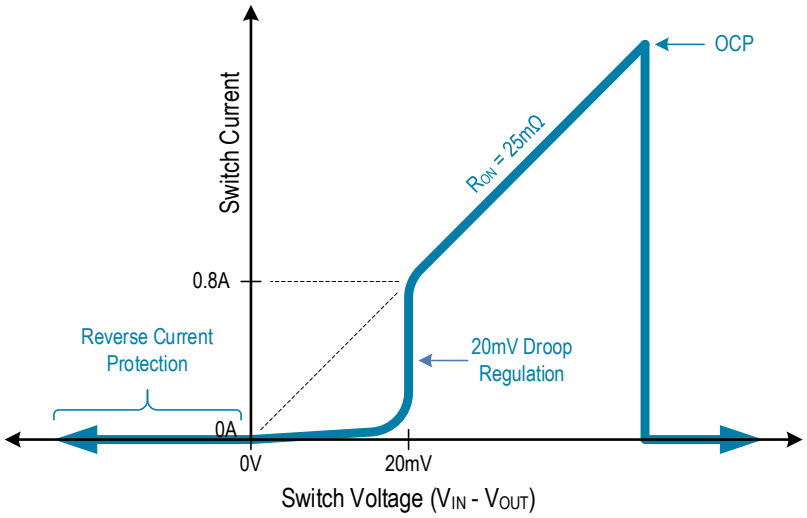


Figure 7. "Ideal Diode" Reverse-Current Protection V-I Curve

Over-Current Protection (OCP)

The KTS1672 includes output over-current protection (OCP) at 18A that protects the IC from damage when an over-current or short-circuit event suddenly appears. The OCP circuit quickly disables the power switch, so the current becomes zero. After an OCP event, if no other fault is detected, and the enable logic is still valid, the power switch is re-enabled via the soft-start debounce and ramp time.

Short-Circuit Protection (SCP)

The KTS1672 includes output short-circuit protection (SCP). If an SCP event occurs while the KTS1672 is already enabled and working, OCP is the first line of defense and responds very quickly. In this case, the current from C_{IN} through the switch to C_{OUT} increases very rapidly. For SCP events that do not reach OCP, if V_{OUT} droops significantly below V_{IN}, it is also detected as a soft-short event. In case of auto-retry or simply starting into a pre-existing SCP condition, the KTS1672 furthermore includes hard and soft SCP detection during soft-start if V_{OUT} is not ramping up. The KTS1672 remains undamaged during continuous SCP events.

Over-Temperature Protection (OTP)

When device junction temperature exceeds 145°C, the OTP circuit disables the power switch. Once the device junction temperature decreases below 130°C, if no other fault is detected, and the enable logic is still valid, the power switch is re-enabled via the soft-start debounce and ramp time.

Auto-Retry

For all fault conditions that cause the switch to open, the KTS1672 will auto-retry via the soft-start debounce and ramp time. If any fault or the same fault is detected again, the switch will open again, and auto-retry will repeat. This continues until the fault is removed (normal operation), or the device is logically disabled via the $\overline{EN}$ or EN pin, or V_{IN} is removed (UVLO).

$\overline{ACOK}$ Output Flag

The $\overline{ACOK}$ output is an open-drain output that requires an external pull-up resistor with recommended value in the 10kΩ to 200kΩ range. Connect $\overline{ACOK}$ to GND or leave floating if unused. The $\overline{ACOK}$ pin indicates the fault status. When there is no fault (UVLO, OVP, OCP, SCP, and OTP are not triggered) and the power switch is ON, then the $\overline{ACOK}$ flag is pulled low to indicate the power is good. Otherwise, the $\overline{ACOK}$ flag is high impedance. RCP is not classified as a fault condition.

Applications Information

Input Capacitor C_{IN} Section

For most applications, connect a 1µF to 10µF ceramic capacitor as close as possible to the device from IN to GND to minimize the effect of parasitic trace inductance. 35V or 50V rated capacitors with X5R or better dielectric are recommended. For optimal surge and ESD performance, 10µF is preferred.

Output Capacitor C_{OUT} Section

For most applications, connect from 10µF to 1000µF total capacitance to the output. Typical applications use 30µF to 100µF as needed for system load-transients. At minimum, connect a 10µF ceramic capacitor as close as possible to the device from OUT to GND to minimize the effect of parasitic trace inductance. 25V rated capacitors with X5R or better dielectric are recommended. Lower voltage ratings are acceptable when using the OVLO pin to set a lower over-voltage protection threshold.

TVS Selection

In order to prevent any unexpected ESD/Surge event damaging the OVP chip, a suitable uni-directional TVS must be carefully selected and used between IN(VBUS) pin and GND pin. First of all, the working voltage of TVS should be determined. A TVS with $V_{RWM} \geq 24V$ can be selected for 20V charging port. Secondly, it is necessary to meet the requirement of surge protection capability. According to IEC61000-4-5 8/20µs surge standard, if customer wants to select a TVS with the surge voltage rating of 100V, the TVS should meet the requirement of $I_{PP} \geq (100V - 30V) / 2\Omega = 35A$. When selecting the model of TVS, the maximum clamping voltage at desired IPP of the TVS should be below 34V. Too high clamping voltage of TVS will cause damage to the OVP chip.

Recommended PCB Layout

Good PCB thermal design is required to support heavy load currents. The KTS1672 EVB is designed to extend the fill area for the IN, OUT, and GND copper planes to about 4 square inches total area for increased thermal performance. Due to the number of bumps on IN and OUT, these two planes are especially important and should not be ignored. Adding back-side and/or buried-layer fill area with thermal vias also helps significantly.

Other than thermal concerns, the PCB layout for the KTS1672 is quite simple. Place the TVS, input and output capacitors near the IC. Connect the TVS, capacitor ground terminals together and to the GND pins using the top-side copper layer. Route the control signals on buried layers. For internally set 24V OVP, directly connect the OVLO pin to the adjacent GND pins.

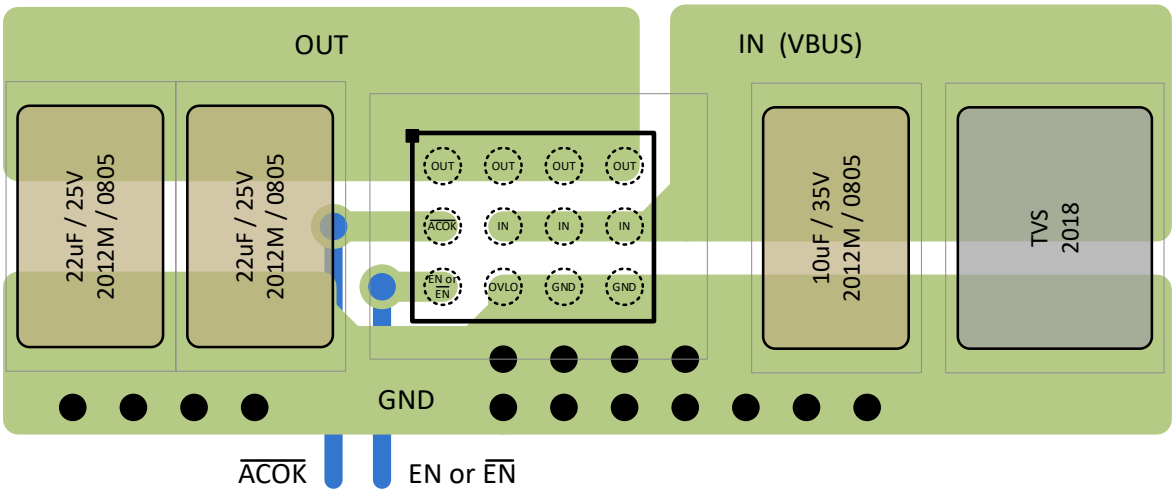


Figure 8. Recommended PCB Layout

Safe Operating Area (SOA)

See Figure 9 and Figure 10 for the SOA of the KTS1672. SOA curves are normally associated with discrete MOSFETs (which are sometimes co-package with a controller IC). In these competing systems, precautions are necessary to stay within the SOA area. However, the KTS1672 is a monolithic IC with all the integrated protection features to automatically keep its operation within the SOA area. For example, it includes over-voltage protection (OVP) and over-current protection (OCP) with very fast response times. It also includes over-temperature protection (OTP) that is measured on the same monolithic die as the integrated power MOSFETs. Additionally, soft-start is controlled with a voltage ramp and current limit protection (Soft-Start CLP) to safely soft-start even in systems with very high capacitance at the output. Furthermore, the integrated control circuit and back-to-back MOSFET switch are optimized to work together as a system, including their tolerances over temperature and process corners.

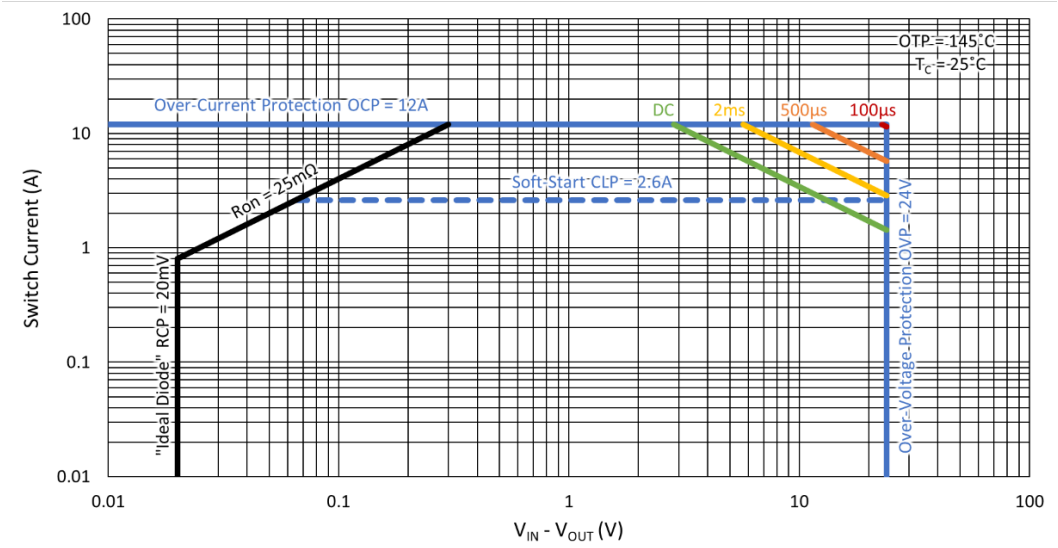


Figure 9. Safe Operating Area (SOA) for T_C = 25℃

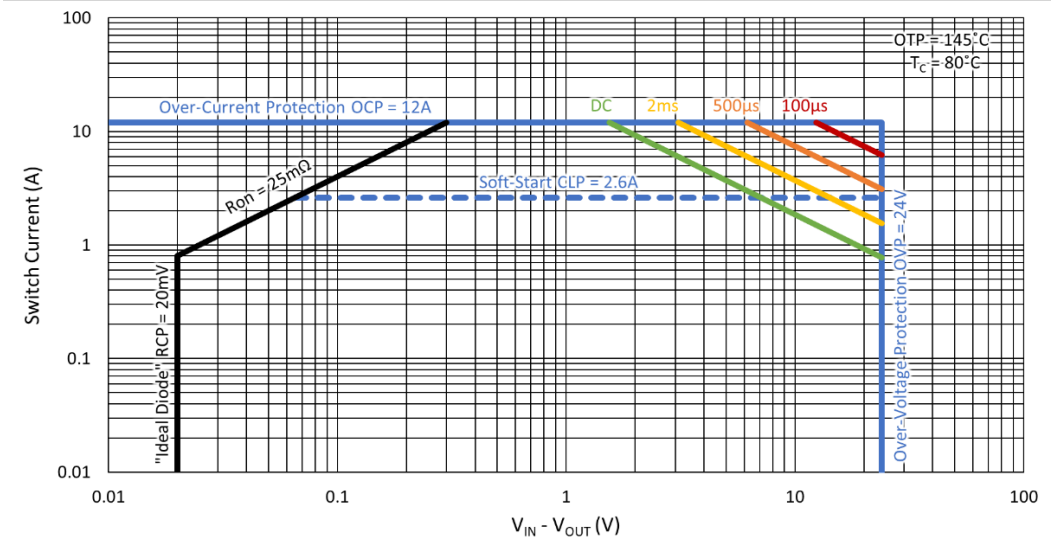
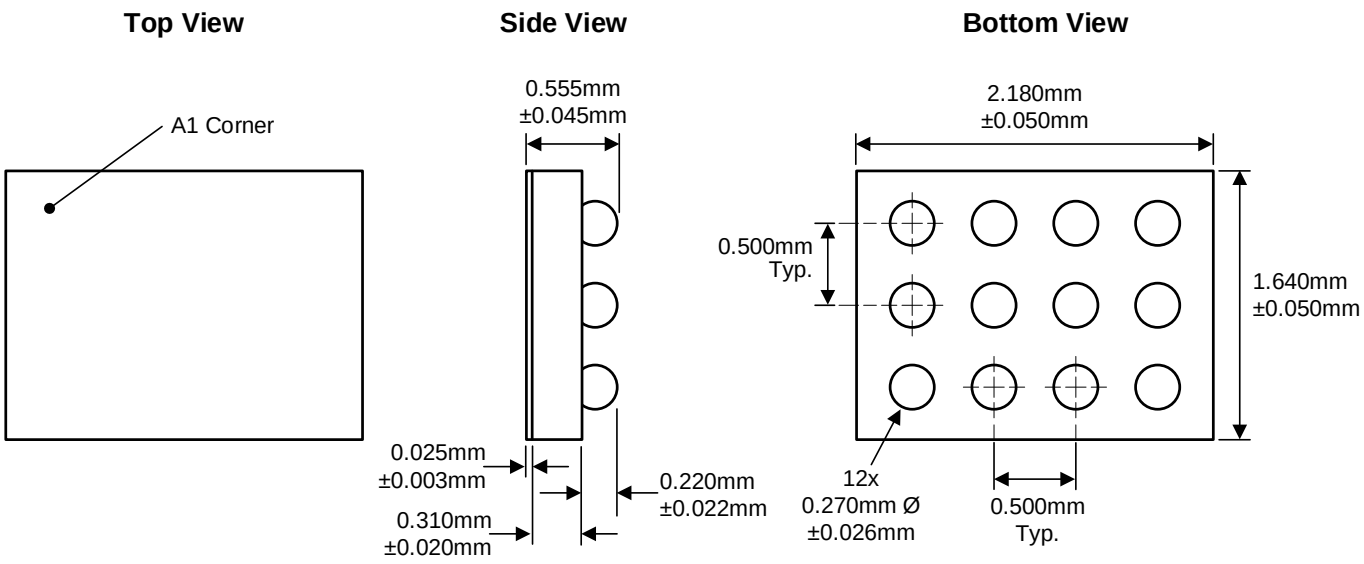


Figure 10. Safe Operating Area (SOA) for T_C = 80℃

Packaging Information

WLCSP43-12 (2.180mm x 1.640mm x 0.555mm)



Recommended Footprint