Jetson Orin NX Series and Jetson Orin Nano Series

Product Design Guide

DG-10931-001_v1.1 | April 2023

Document History

DG-10931-001_v1.1

Version	Date	Description of Change
0.1	April 25, 2022	Preliminary information – Subject to change
0.99	September 30, 2022	• Updated to include Orin Nano series modules in addition to Orin NX series modules. • Section 3.1. Added supported PCIe to NVMe configurations for secondary boot storage. • Table 6-1 and Section 6.1. Updated description of SYS_RESET* behavior when driven by carrier board. • Section 6.1. Added note that carrier boards must support VDD_IN at 5V (support for higher voltage on VDD_IN optional) • Figure 6-4. Power Up Sequence with Power Button. Added missing text for last line (carrier board supplies) • Table 7-3. USB 3.2 and PCIe Lane Mapping: Corrected column title in UPHY mapping table to Orin module instead of AGX Orin. • Various: Updated on-module I2C pull-up values to 2.2 KΩ

1.0	December 20, 2022	• Table 2-1: Added mention of storage options on USB and PCIe
		• Figure 2-1: Updated to include option for storage on USB 3.2 or PCIe
		• Section 3.1:
		  > Corrected UPHY block to UPHY2 instead of UPHY1
		  > Added USB 3.2 option for storage
		• Figure 5.1: Updated with Orin NX/Nano module
		• Updated Table 6-1:
		  > Updated SLEEP/WAKE* to remove mention of pull-up on module
		  > Updated SYS_RESET* on-module pull-up voltage
		  > Updated CLK_32K_OUT description
		• Figure 6-3, Figure 6-4, Table 6-3, and Table 6-4: Updated SYS_RESET_N delay from POWER_EN
		• Figure 6-5: Updated figure to remove arrow from SHUTDOWN_REQ* to carrier board supplies falling.
		• Table 7-2:
		  > Corrected P/N swap for Orin signal names SF_PCIE7_CLK (Pins 52/54)
		  > Corrected +/- swap for SF_PCIE9_CLK descriptions (Pins 227/229)
		• Figure 9-1: Corrected P/N swap for SoC DPAUX pins
		• Figure 9-2: Corrected P/N swap for SoC DPAUX and PIAUX221Z device.
		• Figure 9-8: Corrected P/N swap for SoC DPAUX

Version	Date	Description of Change
		• Table 10-1 and Figure 10-1: Updated to show swapped P/N on two data lanes • Table 10-3: Separated clock and data for all lanes. • Figure 11-1: Updated notes to correct I2C pull-up resistor value on module. • Table 12-10: Updated CAN max data rate
1.1	April 7, 2023	• General: Updated to use Orin Nano DevKit Carrier Board as reference design. • Table 2-2: Updated legend • Updated Chapter 4: Developer Kit Feature Considerations; also updated USB Hub part number. • Section 5.1: Replaced mention of Xavier NX SCL with Orin NX/Orin Nano SCL. • Section 6.1.1 and Figure 6-7: Updated Power Button Supervisor MCU part # • Figure 6-5: Added note above figure about possible discharge circuits. • Table 7-1: Added mention of Recovery mode for USB_D_N/P interface. • Updated: Table 7-3 and Table 7-4: > Split UPHY mapping options into separate tables per UPHY block > Updated text above tables allowing more configuration flexibility. > Separated RP and EP into separate configurations within tables. > Added two options for PCIe x4 (C4) in UPHY0 table with limitations. • Section 7.1: Added mention of polarity inversion support for USB 3.2. • Table 7-11: Removed mention of Root Port and Endpoint for PCIe interface 1 (x1). Also changed from Endpoint to Root Port in title of PCIe interface 3 (x1). • Table 7-6, Table 7-8, Table 9-3, Table 9-5: Moved smaller figures inside the table instead of following the table. • Table 8-2: Added Max Inter-Pair (Pair to Pair) skew requirement for MDI. • Table 9-1: Corrected HDMI_CEC Pin Type. See Jetson Orin NX 16GB Hardware Errata for more details. • Figure 9-1: Updated HDP connections to include series & pulldown resistors and breakout details for level shifter. • Figure 9-2: Removed CEC circuit from DP++ figure and added weak pull-up to pin 14 of DP connector. • Table 9-4: Updated Termination for DP1_AUX and DP1_HPD. • Updated Figure 9-6: > Added pulldown and series resistors on HPD after level shifter. > Added details of HDMI_CEC circuit & HPD/DDC level shifters. • Figure 10-1 and Figure 10-2: Separated 2-lane and 4-lane configuration option examples.

Version	Date	Description of Change
		• Table 10-3: Updated 2-lane configuration names in "Cameras" row. • Table 12-1 and Figure 12-1: Added I2C usage on the module for I2C0 and I2C2. • Table 13-2: Updated pull-up voltage and/or pull-up resistor values for several pins.

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Chapter 1. Introduction

This design guide contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from the interfaces supported by the NVIDIA® Jetson™ Orin NX and Jetson Orin Nano System-on-Module (SOM).

This design guide provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to software release documentation for information on supported capabilities.

Notes:

- References to Orin module refers to the Jetson Orin module series. Modules include Jetson Orin NX 16GB, Jetson Orin NX 8GB, Jetson Orin Nano 8GB, and Jetson Orin Nano 4GB.
- All occurrences of USB 3.2 refer to "USB 3.2 Gen 1x1: SuperSpeed USB 5Gbps" and "USB 3.2 Gen 2x1: SuperSpeed USB 10Gbps" only. Also note that Gen 1x1 and Gen 2x1 are referred to simply as Gen1 and Gen2 in this design guide.

1.1 References

Refer to the following list of documents or models for more information. Use the latest revision of all documents.

- Jetson Orin NX Series Data Sheet
- Jetson Orin Nano Series Data Sheet
- Orin (SoC) Technical Reference Manual
- Jetson Orin NX and Jetson Orin Nano Series Pinmux
- Jetson Orin NX Series and Jetson Orin Nano Series Thermal Design Guide
- Jetson Orin NX Series and Jetson Orin Nano Series SCL (Supported Component List)

1.2 Attachments

The following files are attached to this design guide.

- Jetson_Orin_NX_Orin_Nano_Pin_Descriptions.nvxlsx
- Jetson_Orin_NX_Orin_Nano_Schematic_Checklist.nvxlsx
- Jetson_Orin_NX_Orin_Nano_Layout_Checklist.nvxlsx

To access the attached files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the documents. Excel files with the .nvxlsx extension will need to be saved as .xlsx.

1.3 Abbreviations and Definitions

Table 1-1 lists the abbreviations that may be used throughout this design and guide and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
CAN	Controller Area Network
CEC	Consumer Electronic Control
CSI	Camera Serial Interface
Diff	Differential
DP	DisplayPort
eDP	Embedded DisplayPort
ESD	Electrostatic Discharge
EMI	Electromagnetic Interference
FET	Field Effect Transistor
GPIO	General Purpose Input Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
I2C	Inter IC Interface
I2S	Inter IC Sound Interface
LDO	Low Dropout (voltage regulator)
LPDDR5	Low Power Double Data Rate DRAM, Fifth generation
MDI	Medium-Dependent Interface
MIPI	Mobile Industry Processor Interface
mm	Millimeter
ms	Milliseconds

Abbreviation	Definition
PCIe	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Interface (that is, USB PHY)
ps	Pico-Seconds
PMIC	Power Management Integrated Circuit
RJ45	8P8C modular connector used in Ethernet and other data links
RTC	Real Time Clock
SE	Single-Ended
SoC	System on Chip
SOM	System on Module
SPI	Serial Peripheral Interface
TMDS	Transition-Minimized Differential Signaling
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

Chapter 2. Jetson Orin Module

The Jetson Orin module resides at the center of the embedded system solution and includes:

- Power (Power sequencer, regulators, and so on)
- DRAM (LPDDR5)
- Gigabit Ethernet PHY
- QSPI NOR (Boot device)

In addition, a wide range of interfaces are available at the main connector for use on the carrier board as shown in Table 2-1 and Figure 2-1.

Table 2-1. Jetson Orin Module Interfaces

Category	Function		Category	Function
USB	USB 2.0 interface (3x)		LAN	Gigabit ethernet
	USB 3.2 (3x). Note: SSD via USB 3.2 is one option for storage.		I2C	4x
PCIe	PCIe (1 x1, 1 x2 or 2 x1, and 1 x4). Note: NVMe via PCIe is one option for storage.		UART	3x
Camera	CSI (8 lanes 2 x4 or 4 x2)		SPI	2x
	Control, clock		CAN	1x
Display	HDMI/eDP/DP (1x)		Fan	FAN PWM and tach input
	DP_AUX/HPD, CEC		Debug	UART
Audio	I2S interface (2x)		System	Power control, reset, alerts
	Codec clock		Power	Main input and pin for optional battery back-up for Real-Time Clock

Figure 2-1. Jetson Orin Module Block Diagram

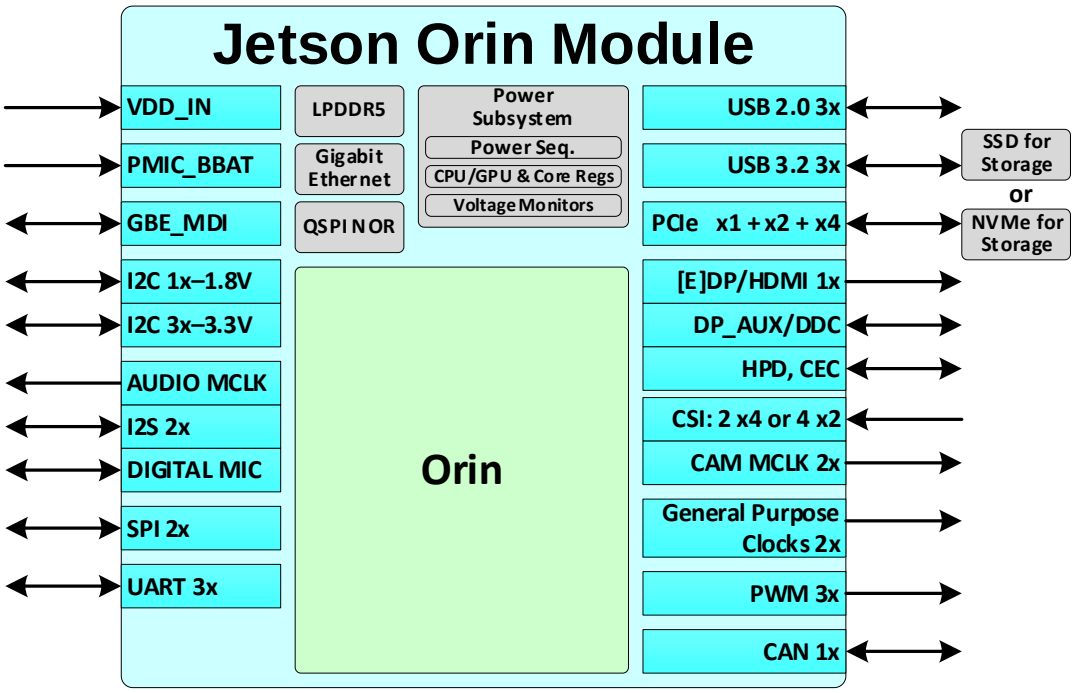


Table 2-2. Jetson Orin Module Connector 260-Pin SO-DIMM Pinout Matrix

Module Signal Name	Jetson Orin Module Function	Pin #		Pin #	Module Signal Name	Jetson Orin Module Function
GND	GND	1		2	GND	GND
CSI1_D0_N	CSI1_D0_N	3		4	CSI0_D0_N	CSI0_D0_N
CSI1_D0_P	CSI1_D0_P	5		6	CSI0_D0_P	CSI0_D0_P
GND	GND	7		8	GND	GND
CSI1_CLK_N	CSI1_CLK_N	9		10	CSI0_CLK_N	CSI0_CLK_N
CSI1_CLK_P	CSI1_CLK_P	11		12	CSI0_CLK_P	CSI0_CLK_P
GND	GND	13		14	GND	GND
CSI1_D1_N	CSI1_D1_N	15		16	CSI0_D1_N	CSI0_D1_N
CSI1_D1_P	CSI1_D1_P	17		18	CSI0_D1_P	CSI0_D1_P
GND	GND	19		20	GND	GND
CSI3_D0_N	CSI3_D0_N	21		22	CSI2_D0_N	CSI2_D0_N
CSI3_D0_P	CSI3_D0_P	23		24	CSI2_D0_P	CSI2_D0_P
GND	GND	25		26	GND	GND
CSI3_CLK_N	CSI3_CLK_N	27		28	CSI2_CLK_N	CSI2_CLK_N
CSI3_CLK_P	CSI3_CLK_P	29		30	CSI2_CLK_P	CSI2_CLK_P
GND	GND	31		32	GND	GND
CSI3_D1_N	CSI3_D1_N	33		34	CSI2_D1_N	CSI2_D1_N
CSI3_D1_P	CSI3_D1_P	35		36	CSI2_D1_P	CSI2_D1_P
GND	GND	37		38	GND	GND
DP0_TXD0_N	USBSS1_RX_N	39		40	CSI4_D2_N	PCIE2_RX0_N
DP0_TXD0_P	USBSS1_RX_P	41		42	CSI4_D2_P	PCIE2_RX0_P
GND	GND	43		44	GND	GND
DP0_TXD1_N	USBSS1_TX_N	45		46	CSI4_D0_N	PCIE2_TX0_N

Module Signal Name	Jetson Orin Module Function	Pin #		Pin #	Module Signal Name	Jetson Orin Module Function
DP0_TXD1_P	USBSS1_TX_P	47		48	CSI4_D0_P	PCIE2_TX0_P
GND	GND	49		50	GND	GND
DP0_TXD2_N	USBSS2_RX_N	51		52	CSI4_CLK_N	PCIE2_CLK_N
DP0_TXD2_P	USBSS2_RX_P	53		54	CSI4_CLK_P	PCIE2_CLK_P
GND	GND	55		56	GND	GND
DP0_TXD3_N	USBSS2_TX_N	57		58	CSI4_D1_N	PCIE2_RX1_N (PCIE3_RX0_N)
DP0_TXD3_P	USBSS2_TX_P	59		60	CSI4_D1_P	PCIE2_RX1_P (PCIE3_TX0_P)
GND	GND	61		62	GND	GND
DP1_TXD0_N	DP1_TXD0_N	63		64	CSI4_D3_N	PCIE2_TX1_N (PCIE3_TX0_N)
DP1_TXD0_P	DP1_TXD0_P	65		66	CSI4_D3_P	PCIE2_TX1_P (PCIE3_TX0_P)
GND	GND	67		68	GND	GND
DP1_TXD1_N	DP1_TXD1_N	69		70	DSI_D0_N	RSVD
DP1_TXD1_P	DP1_TXD1_P	71		72	DSI_D0_P	RSVD
GND	GND	73		74	GND	GND
DP1_TXD2_N	DP1_TXD2_N	75		76	DSI_CLK_N	RSVD
DP1_TXD2_P	DP1_TXD2_P	77		78	DSI_CLK_P	RSVD
GND	GND	79		80	GND	GND
DP1_TXD3_N	DP1_TXD3_N	81		82	DSI_D1_N	RSVD
DP1_TXD3_P	DP1_TXD3_P	83		84	DSI_D1_P	RSVD
GND	GND	85		86	GND	GND
GPIO00	GPIO00	87		88	DP0_HPD	RSVD
SPI0_MOSI	SPI0_MOSI	89		90	DP0_AUX_N	RSVD
SPI0_SCK	SPI0_SCK	91		92	DP0_AUX_P	RSVD
SPI0_MISO	SPI0_MISO	93		94	HDMI_CEC	HDMI_CEC
SPI0_CS0*	SPI0_CS0*	95		96	DP1_HPD	DP1_HPD
SPI0_CS1*	SPI0_CS1*	97		98	DP1_AUX_N	DP1_AUX_N
UART0_TXD	UART0_TXD	99		100	DP1_AUX_P	DP1_AUX_P
UART0_RXD	UART0_RXD	101		102	GND	GND
UART0_RTS*	UART0_RTS*	103		104	SPI1_MOSI	SPI1_MOSI
UART0_CTS*	UART0_CTS*	105		106	SPI1_SCK	SPI1_SCK
GND	GND	107		108	SPI1_MISO	SPI1_MISO
USB0_D_N	USB0_D_N	109		110	SPI1_CS0*	SPI1_CS0*
USB0_D_P	USB0_D_P	111		112	SPI1_CS1*	SPI1_CS1*
GND	GND	113		114	CAM0_PWDN	CAM0_PWDN
USB1_D_N	USB1_D_N	115		116	CAM0_MCLK	CAM0_MCLK
USB1_D_P	USB1_D_P	117		118	GPIO01	GPIO01
GND	GND	119		120	CAM1_PWDN	CAM1_PWDN
USB2_D_N	USB2_D_N	121		122	CAM1_MCLK	CAM1_MCLK
USB2_D_P	USB2_D_P	123		124	GPIO02	GPIO02
GND	GND	125		126	GPIO03	GPIO03
GPIO04	GPIO04	127		128	GPIO05	GPIO05
GND	GND	129		130	GPIO06	GPIO06
PCIE0_RX0_N	PCIE0_RX0_N	131		132	GND	GND
PCIE0_RX0_P	PCIE0_RX0_P	133		134	PCIE0_TX0_N	PCIE0_TX0_N
GND	GND	135		136	PCIE0_TX0_P	PCIE0_TX0_P
PCIE0_RX1_N	PCIE0_RX1_N	137		138	GND	GND
PCIE0_RX1_P	PCIE0_RX1_P	139		140	PCIE0_TX1_N	PCIE0_TX1_N
GND	GND	141		142	PCIE0_TX1_P	PCIE0_TX1_P
CAN_RX	CAN_RX	143		144	GND	GND
KEY	KEY	KEY		KEY	KEY	KEY

Module Signal Name	Jetson Orin Module Function	Pin #		Pin #	Module Signal Name	Jetson Orin Module Function
CAN_TX	CAN_TX	145		146	GND	GND
GND	GND	147		148	PCIE0_TX2_N	PCIE0_TX2_N
PCIE0_RX2_N	PCIE0_RX2_N	149		150	PCIE0_TX2_P	PCIE0_TX2_P
PCIE0_RX2_P	PCIE0_RX2_P	151		152	GND	GND
GND	GND	153		154	PCIE0_TX3_N	PCIE0_TX3_N
PCIE0_RX3_N	PCIE0_RX3_N	155		156	PCIE0_TX3_P	PCIE0_TX3_P
PCIE0_RX3_P	PCIE0_RX3_P	157		158	GND	GND
GND	GND	159		160	PCIE0_CLK_N	PCIE0_CLK_N
USBSS_RX_N	USBSS0_RX_N	161		162	PCIE0_CLK_P	PCIE0_CLK_P
USBSS_RX_P	USBSS0_RX_P	163		164	GND	GND
GND	GND	165		166	USBSS_TX_N	USBSS0_TX_N
PCIE1_RX0_N	PCIE1_RX0_N	167		168	USBSS_TX_P	USBSS0_TX_P
PCIE1_RX0_P	PCIE1_RX0_P	169		170	GND	GND
GND	GND	171		172	PCIE1_TX0_N	PCIE1_TX0_N
PCIE1_CLK_N	PCIE1_CLK_N	173		174	PCIE1_TX0_P	PCIE1_TX0_P
PCIE1_CLK_P	PCIE1_CLK_P	175		176	GND	GND
GND	GND	177		178	MOD_SLEEP*	MOD_SLEEP*
PCIE_WAKE*	PCIE_WAKE*	179		180	PCIE0_CLKREQ*	PCIE0_CLKREQ*
PCIE0_RST*	PCIE0_RST*	181		182	PCIE1_CLKREQ*	PCIE1_CLKREQ*
PCIE1_RST*	PCIE1_RST*	183		184	GBE_MDI0_N	GBE_MDI0_N
I2C0_SCL	I2C0_SCL	185		186	GBE_MDI0_P	GBE_MDI0_P
I2C0_SDA	I2C0_SDA	187		188	GBE_LED_LINK	GBE_LED_LINK
I2C1_SCL	I2C1_SCL	189		190	GBE_MDI1_N	GBE_MDI1_N
I2C1_SDA	I2C1_SDA	191		192	GBE_MDI1_P	GBE_MDI1_P
I2S0_DOUT	I2S0_DOUT	193		194	GBE_LED_ACT	GBE_LED_ACT
I2S0_DIN	I2S0_DIN	195		196	GBE_MDI2_N	GBE_MDI2_N
I2S0_FS	I2S0_FS	197		198	GBE_MDI2_P	GBE_MDI2_P
I2S0_SCLK	I2S0_SCLK	199		200	GND	GND
GND	GND	201		202	GBE_MDI3_N	GBE_MDI3_N
UART1_TXD	UART1_TXD	203		204	GBE_MDI3_P	GBE_MDI3_P
UART1_RXD	UART1_RXD	205		206	GPIO07	GPIO07
UART1_RTS*	UART1_RTS*	207		208	GPIO08	GPIO08
UART1_CTS*	UART1_CTS*	209		210	CLK_32K_OUT	CLK_32K_OUT
GPIO09	GPIO09	211		212	GPIO10	GPIO10
CAM_I2C_SCL	CAM_I2C_SCL	213		214	FORCE_RECOVERY*	FORCE_RECOVERY*
CAM_I2C_SDA	CAM_I2C_SDA	215		216	GPIO11	GPIO11
GND	MODULE_ID	217		218	GPIO12	GPIO12
SDMMC_DAT0	PCIE2_RST*	219		220	I2S1_DOUT	I2S1_DOUT
SDMMC_DAT1	PCIE2_CLKREQ*	221		222	I2S1_DIN	I2S1_DIN
SDMMC_DAT2	PCIE3_RST*	223		224	I2S1_FS	I2S1_FS
SDMMC_DAT3	PCIE3_CLKREQ*	225		226	I2S1_SCLK	I2S1_SCLK
SDMMC_CMD	PCIE3_CLK_N	227		228	GPIO13	GPIO13
SDMMC_CLK	PCIE3_CLK_P	229		230	GPIO14	GPIO14
GND	GND	231		232	I2C2_SCL	I2C2_SCL
SHUTDOWN_REQ*	SHUTDOWN_REQ*	233		234	I2C2_SDA	I2C2_SDA
PMIC_BBAT	PMIC_BBAT	235		236	UART2_TXD	UART2_TXD
POWER_EN	POWER_EN	237		238	UART2_RXD	UART2_RXD
SYS_RESET*	SYS_RESET*	239		240	SLEEP/WAKE*	SLEEP/WAKE*
GND	GND	241		242	GND	GND
GND	GND	243		244	GND	GND
GND	GND	245		246	GND	GND
GND	GND	247		248	GND	GND
GND	GND	249		250	GND	GND

Module Signal Name	Jetson Orin Module Function	Pin #		Pin #	Module Signal Name	Jetson Orin Module Function
VDD_IN	VDD	251		252	VDD_IN	VDD
VDD_IN	VDD	253		254	VDD_IN	VDD
VDD_IN	VDD	255		256	VDD_IN	VDD
VDD_IN	VDD	257		258	VDD_IN	VDD
VDD_IN	VDD	259		260	VDD_IN	VDD

Legend	Ground	Power	Function Significantly Different than Module Pin Name Implies

Chapter 3. Jetson Orin Module Boot Considerations

The Jetson Orin Module can boot in two ways:

- QSPI – normal operation
- USB Recovery Mode – development and production programming

3.1 QSPI Boot

The Jetson Orin module normally boots from QSPI. However, the QSPI's 64 MB of storage is not expected to contain all the files for a fully functioning system. Secondary storage must be provided. Support is available for the following configurations.

- NVMe through PCIe
  - PCIE0, x4 (Orin UPHY0 Lanes [7:4]), C4
  - PCIE2, x2 (Orin UPHY2 Lanes 1:0]), C7
  - PCIE2, x1 (Orin UPHY2 L0), C7
  - PCIE3, x1 (Orin UPHY2 L1), C9
- SSD through USB 3.2
  - USB 3.2 Port 0, 1, or 2

3.2 USB Recovery Mode

USB Recovery mode provides an alternate boot device (USB). In this mode, the system is connected to a host system and boots over USB. This is used when a new image needs to be flashed. To enter USB recovery mode, the FORCE_RECOVERY* pin is held low when SYS_RESET* goes high which can be when the system is powered on or SYS_RESET* is asserted after the system is powered on. FORCE_RECOVERY* is the SoC RCM0 strap Only USB0_D_N/P supports USB Recovery Mode

No other signals are required or supported for entering Force Recovery mode. Neither VBus or USB ID detection is needed. If the force recovery strap is held low coming out of reset, Jetson Orin module will configure USB0 as a device and enter recovery mode.

See the USB section (Section 0) for an example figure that shows USB0 connected to a USB Micro B connector.

Chapter 4. Developer Kit Feature Considerations

The Jetson Orin Nano Developer Kit carrier board design files are provided as a reference design. Both Jetson Orin Nano and Jetson Orin NX modules are compatible with this carrier board. This chapter describes details necessary for designers to know to replicate certain features implemented on the NVIDIA Jetson Orin Nano Developer Kit carrier board if desired. In addition, aspects of the design that are specific to the NVIDIA developer kit usage but not useful or supported on a custom carrier board are also identified.

Most of the features implemented on the reference design can be duplicated by copying the connections from the reference design. Some of the following features have aspects that would require additional information.

- Button Power MCU (EFM8SB10F2G)
- USB SuperSpeed Hub (Realtek RTS5420-GR)
- Power over Ethernet (PoE)
- TI TXB0108 level shifters
- ID EEPROM (Not to be copied from reference design)

4.1 Button Power MCU

The reference design implements a button power MCU (EFM8SB10F2G). This device is programmed with firmware that is available on the Jetson Download Center. It is recommended that the connections used on the reference design are followed exactly to be compatible with the firmware provided to ensure correct functionality.

4.2 USB SuperSpeed Hub

The USB 3.2 hub design uses a Realtek RTS5420 device. The hub circuit includes a SPI FLASH device which holds configuration information. A design intending to duplicate the reference design hub implementation should include the same SPI FLASH programmed to match, or the hub should be customized with fuses with the same settings. The configuration in the SPI FLASH includes the following:

- Power enables (DPS1/2/3/4_PWR) set to be active high
- Charging feature disabled
- SSC valid

4.3 Power over Ethernet

The reference design includes a 4-pin Power over Ethernet (PoE) header (J19) which brings out the VC power pins of the Ethernet connector. To use this alternate PoE power mechanism to power a custom carrier board, the design would require a PoE PD controller or converter to take the high voltage PoE supply (38V-60V) and convert it to the correct voltage for the custom carrier board. The output of the PoE converter would be supplied where the DC Jack power comes in on the NVIDIA Orin Nano DevKit. The DevKit has an optional PoE Backpower jumper (J18) for this purpose.

4.4 TI TXB0108 Level Shifters

The reference design uses these level shifters to shift many of the signals going to the 40-pin header from 1.8V to 3.3V. The design of these level shifters supports bidirectional signaling without the use of a direction signal but has some side effects that should be considered. See the *Jetson Nano Developer Kit 40-Pin Expansion Header GPIO Usage Considerations Applications Note* for details.

4.5 Features Not to Be Implemented

The reference design features that should not be copied as they are not required or useful for a custom carrier board design. The ID EEPROM (U17) is a feature that is used for NVIDIA internal purposes, but not recommended on a custom design. If a similar functionality is desired for a custom design, avoid using address 7'h57 on the I2C2 interface.

Chapter 5. Modular Connector

5.1 Module Connector Details

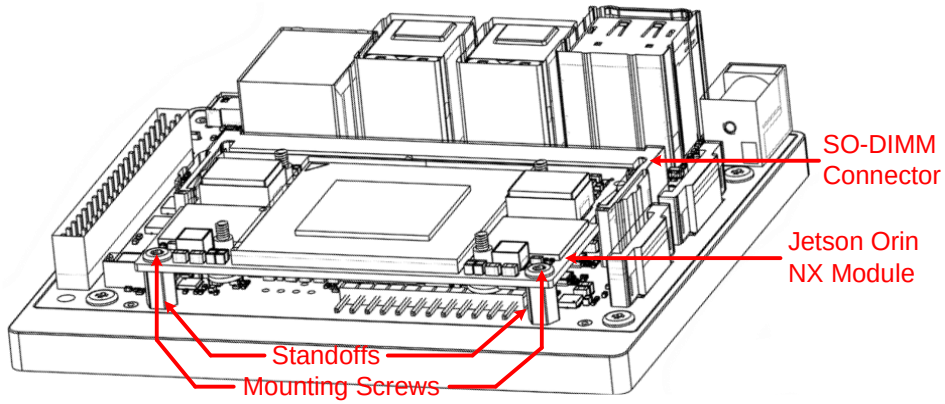
Jetson Orin modules connect to the carrier board using a 260-pin SODIMM connector. The mating connector used on the reference design carrier board is listed in the Jetson Orin NX and Jetson Orin Nano Supported Components List. This connector is a DDR4 SODIMM, 260-pin, right-angle, standard key type. The full height of the connector is 9.2 mm. Refer to the connector specification for details. Other heights are available.

5.2 Module to Mounting Hardware

The Jetson Orin module is installed in the SODIMM connector which has latching mechanisms to hold the board in place. In addition, it is required that the module is mounted to the main carrier board PCB using metal standoffs and screws (or equivalent), both for mechanical integrity and to provide additional grounding points. The recommended standoffs used on the carrier board are threaded standoffs that are hex, 4.5 mm widths (narrow diameter) × 6.57 ± 0.1 mm length with M2.5 threads (or equivalent). The screws that match the described standoffs are M2.5 × 3.7 mm, pad head.

Other SODIMM connector heights are available. If a different height connector is used, the standoff height will have to be adjusted accordingly to account for the difference in height from main PCB to module PCB.

Figure 5-1. Jetson Orin Module Installed in SODIMM Connector



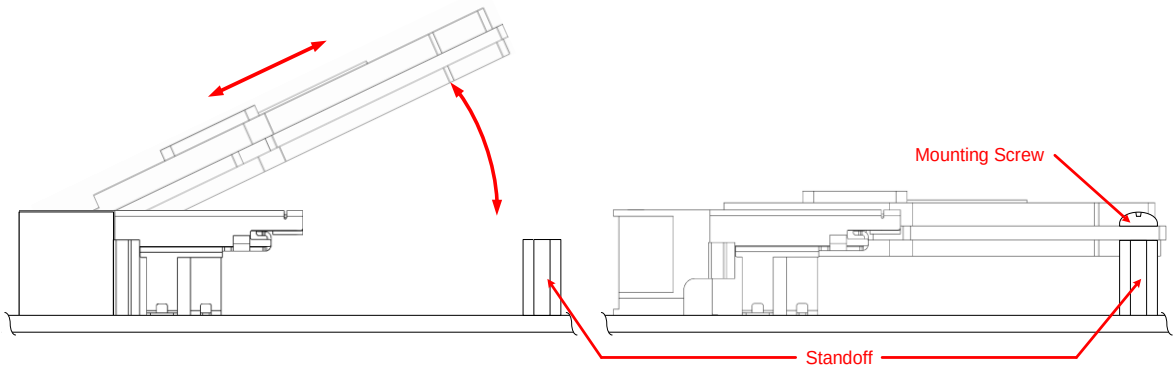
5.3 Module Installation and Removal

To install the Jetson Orin module correctly, follow the sequence and mounting hardware instructions:

Here are some suggested assembly guidelines.

1. Assemble any required thermal solution on the module.
2. Install the module
   a). Start with baseboard that has suitable standoff to match SODIMM connector height.
   b). Insert module fully at an angle of 25-35 degree into the SODIMM connector.
   c). Arc down the module board until the SODIMM connector latch engages.
   d). Secure the module to the baseboard with screws into the standoff or spacer (shown in Figure 5-2).

Figure 5-2. Module to Connector Assembly Diagram



To remove the module correctly, follow the installation sequence in reverse.

Chapter 6. Power

Power for the module is supplied on the VDD_IN pins and is nominally 5.0V to 20V (see the *Jetson Orin Module Data Sheet* for supply tolerance and maximum current).

> **!** CAUTION: Jetson Orin module is not hot-pluggable. Before installing or removing the module, the main power supply (to VDD_IN pins) must be disconnected and adequate time allowed for the various power rails to fully discharge.

Table 6-1. Jetson Orin Module Power and System Pin Description

Pin #	Module Pin Name	Orin Pin Name	Usage and Description	Recommended Usage	Direction	Pin Type
251 ↓ 260	VDD_IN	–	Main power – Supplies Power Sequencer / PMIC and other regulators.	Main DC input	Input	5V or 5.0V to 20V See Note 1
235	PMIC_BBAT	–	Real-Time-Clock back-up. Optionally used to provide back-up power for the RTC in the Power Sequencer / PMIC. Connects to a Lithium Cell or similar power source. The cell sources power for the RTC when system is disconnected from power. **Note:** *This pin is input only and rechargeable cells or devices such as Super Caps cannot be supported.*	Battery Back-up using coin cell, etc..	Input	1.85V to 5.5V
214	FORCE_ RECOVERY*	GP107_ RECOVERY0_ STRAP	Force Recovery strap pin. Held low when SYS_RESET* goes high (i.e. during power-on) places system in USB recovery mode. 10kΩ pull-up to 1.8V on the module.	System	Input	CMOS – 1.8V
240	SLEEP/WAKE*	GPIO4	Sleep/Wake. Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	System	Input	CMOS – 5.0V
233	SHUTDOWN_ REQ*	–	When driven/pulled low by the module, requests the carrier board to shut down. ~5kΩ pull-up to VDD_IN on the module.	System	Output	Open Drain, VDD_IN level
237	POWER_EN	–	Signal for module on/off: high level on, low level off. Connects to module Power Sequencer / PMIC power on/off control input through converter logic. POWER_EN is routed to a	System	Input	Analog 5.0V

Pin #	Module Pin Name	Orin Pin Name	Usage and Description	Recommended Usage	Direction	Pin Type
			Schmitt trigger buffer on the module. A 100kΩ pulldown is on the module.			
239	SYS_RESET*	–	Module Reset. Reset to the module when driven low by the carrier board (only resets the SoC and QSPI boot device). Used as carrier board supply enable when pulled high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. 10kΩ pull-up to 1.8V on the module.	System	Bidir	Open Drain, 1.8V
178	MOD_SLEEP*	SF_PWR_SOC_EN	Module Sleep. When active (low), indicates module has gone to Sleep (SC7) mode.	Control of devices to be disabled in sleep mode.	Output	CMOS – 1.8V
210	CLK_32K_OUT	(Power sequencer 32K CLK Out)	Sleep/Suspend clock. Buffered on the module.	Sleep/suspend clock for devices such as M.2 Key E	Output	CMOS – 1.8V
217	GND (Module ID)	–	Module ID strap: Indicates whether the module is a legacy type supporting only 5V on VDD_IN (tied to GND on the module) or an advanced type supporting from 5V to 20V on VDD_IN (floating on the module - pulled high on the carrier board. See Note 1).	Pulled high on the carrier board if it can support more than the legacy 5V on VDD_IN.	Not applicable	Not applicable. See Note 1

Notes:
1. Modules with pin 217 (Module ID) tied to GND support only 5V on VDD_IN. Modules with pin 217 floating (pulled high on carrier board) support full voltage range. Pull-up voltage on the carrier board on the module ID strap pin is up to the carrier board designer.
2. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
3. The directions for FORCE_RECOVERY* and SLEEP/WAKE* signals are true when used for those functions. Otherwise as GPIOs, the direction is bidirectional.

6.1 Power Supply and Sequencing

The carrier board receives the main power source and uses this to generate the enable to Jetson Orin module (POWER_EN) after the carrier board has ensured the main supply is stable and the associated decoupling capacitors have charged. The carrier board supplies are not enabled at this time. Once POWER_EN is driven active (high), the module begins to Power-ON. When the module Power-ON sequence has completed, the SYS_RESET* signal is released (pulled high on module) and this is used by the carrier board to enable its various supplies.

Note: The carrier board cannot drive high or pull high any signals that are associated with the module when the module rails are off. If the designer cannot guarantee a signal will not be driven or pulled high, then either the power rail related to that signal should be left off, or the signals would need to be buffered to isolate them from the module pins. The buffers should only be enabled towards the module when SYS_RESET* goes high.

POWER_EN

- POWER_EN is a level active signal. When high, the system powers on or stays on. When low, the system powers down or stays off.

SYS_RESET*

- SYS_RESET* is bidirectional. The signal is controlled by the Power Sequencer or PMIC during power-on and power-off. When the system is powered on, SYS_RESET* can be driven by the carrier board to reset the SoC and QSPI boot device. This will not result in a full system power cycle.
- SYS_RESET* is not asserted externally during the power-down sequence. When POWER_EN is de-asserted, the Power Sequencer or PMIC performs a power down sequence which includes asserting SYS_RESET*.

SHUTDOWN_REQ*

- SHUTDOWN_REQ* is driven active (low) by the module if the system must be shut down, due to a software shutdown request, over-temperature event, undervoltage event, or other faults. The power control logic on the carrier board must drive POWER_EN inactive (low) if SHUTDOWN_REQ* is asserted.
- SHUTDOWN_REQ* is not driven during power-on. It is pulled up to the VDD_IN supply, so stays inactive. If the system is on and reset is driven low, the Power Sequencer or PMIC will initiate a full power cycle and start the power-on sequence. Again, SHUTDOWN_REQ* is not asserted. SHUTDOWN_REQ* will only go low when the module determines the system needs to shut down.
- SHUTDOWN_REQ* comes from a latch on module and is cleared when POWER_EN goes low.
- If SHUTDOWN_REQ* is asserted, the carrier board must de-assert POWER_EN as soon as possible.

Power Rail Discharge

To satisfy the power down sequencing requirement and prevent unwanted back drive from the carrier board to the module, the following must be true:

- The carrier board 3.3V power supply that powers any module I/O must be off within 1.5 ms of SYS_RESET* assertion.
- The 1.8V power supply that powers any module I/O must be off within 4 ms.
- The power rails should be fully discharged before attempting to power back up.

Module ID

To support both legacy modules that take 5V only on VDD_IN as well as the wide range that advanced modules can support (5V-20V) on VDD_IN, one of the original SODIMM GND pins (Pin 217) is re-tasked as a module ID pin. Legacy modules will have this pin tied to GND. Advanced modules will have this pin floating. A pull-up is required on the carrier board on Pin 217 (GND or module ID) if it will support the wide range VDD_IN input voltage. This pull-up will cause the module ID level to be high if an advanced module is installed. The module ID pin level should be used on the carrier board to determine if only 5V is supplied to VDD_IN (legacy module) or the full advanced module VDD_IN range.

Note: The carrier board must support VDD_IN at 5V. Supporting the extended range of 5V – 20V is optional.

Figure 6-1. System Power and Control Block Diagram

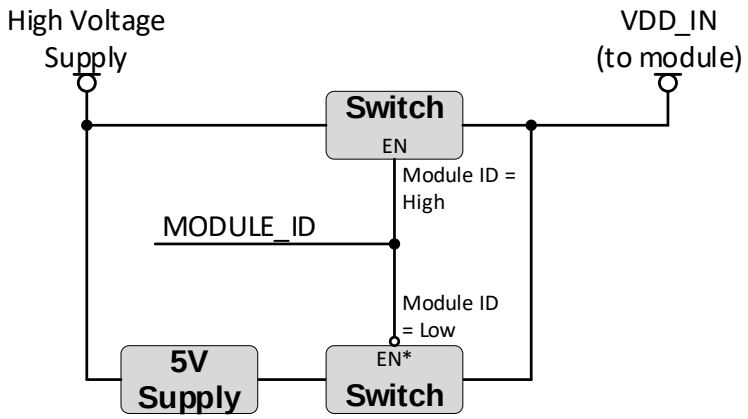
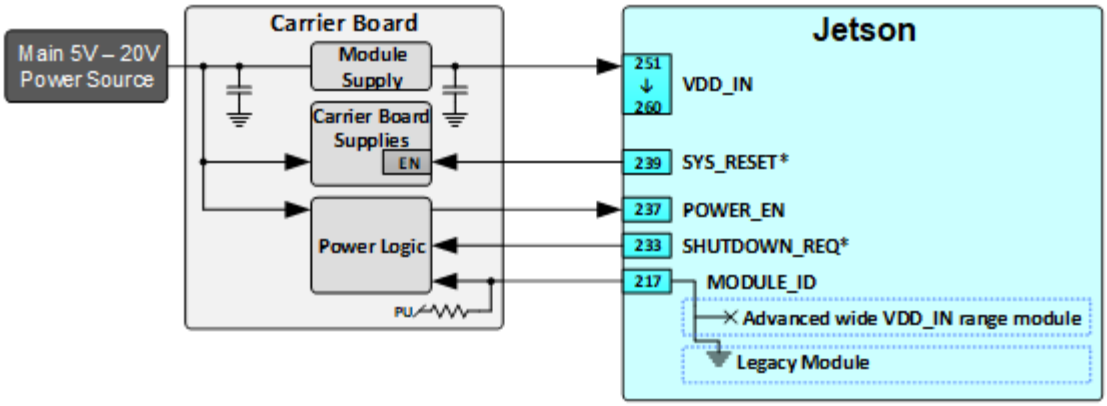


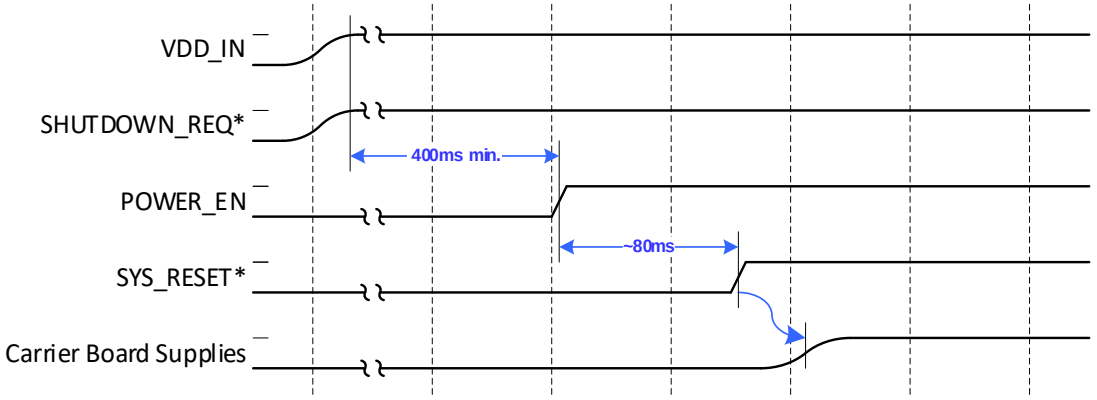
Figure 6-2. System Power and Control Block Diagram



Notes:

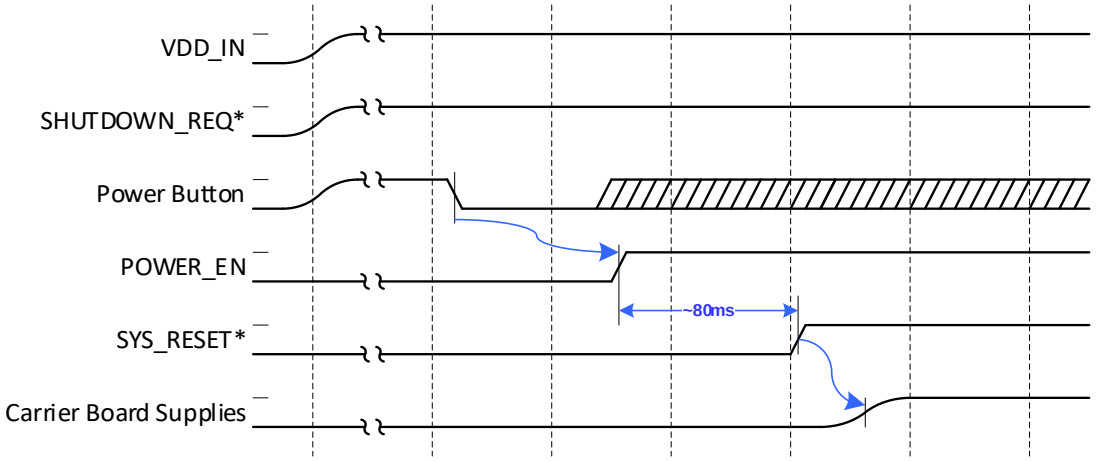
1. MODULE_ID indicates the capability of the module. Low: Legacy module with VDD_IN = 5V nominal. High: Advanced module supporting wide VDD_IN range (5V-20V).
2. Designs which implement an eFUSE or current limiting device on the input power rail of the module should select a part that DOES NOT limit reverse current.

Figure 6-3. Power Up Sequence No Power Button – Auto Power On



Notes:
1. SHUTDOWN_REQ* is not driven during power up. The signal is pulled to VDD_IN.
2. SYS_RESET* is driven by the Power Sequencer or PMIC during power up.

Figure 6-4. Power Up Sequence with Power Button

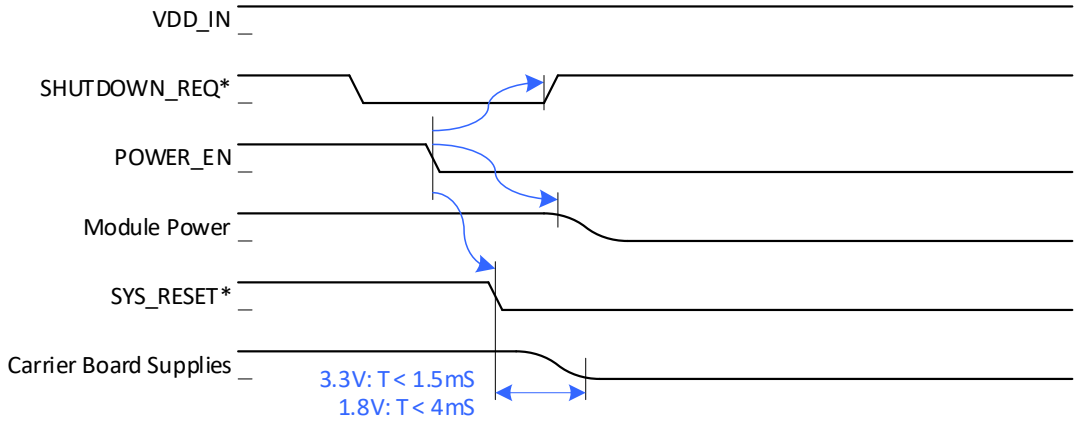


Notes:
1. SHUTDOWN_REQ* is not driven during power up. The signal is pulled to VDD_IN.
2. SYS_RESET* is driven by the Power Sequencer or PMIC during power up.

Note: For designs that intend to follow the NVIDIA carrier board design and include the EFM8SB10F2G-A-QFN20 MPU for Power Button control, see 6.1.1 Power Button Supervisor MCU Power-On.

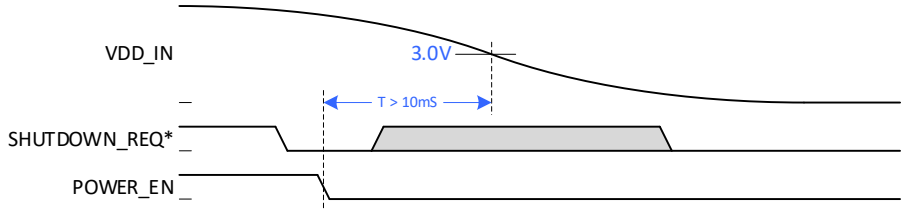
Note: If the carrier board 3.3V or 1.8V supplies are not low in the times shown below, discharge may be required. See the Orin Nano DevKit carrier board reference design for examples. The discharge circuits should be tuned to meet the timing requirements.

Figure 6-5. Power Down Initiated by SHUTDOWN_REQ* Assertion



Note: SYS_RESET* is driven by the Power Sequencer or PMIC during power down.

Figure 6-6. Power Down Sudden Power Loss



Note: SHUTDOWN_REQ* must always be serviced by the carrier board to toggle POWER_EN from high to low, even in cases of sudden power loss.

6.1.1 Power Button Supervisor MCU Power-On

The NVIDIA carrier board reference design implements a power button supervisor. This supervisor is a low power device meant to intercept push-button (momentary) switches to control ON/Enable signals to the module Power Sequencer or PMIC and main processor. This supervisor is always powered and allows close to complete system power OFF while providing proper timing for ON/OFF signals to the system. The selected MCU to perform this function is the EFM8SB10F2G-A-QFN20 from Silicon Labs.

Note: Designs that intend to follow the NVIDIA carrier board design and include the EFM8SB10F2G-A-QFN20 MPU for Power Button control need to replicate the circuitry on the latest P3768 carrier board exactly. NVIDIA provides the binary and source on the Jetson Download Center. The customer should get the flashing instructions from Silicon Labs. Otherwise, another solution designed to meet the requirements earlier in this chapter can be used.

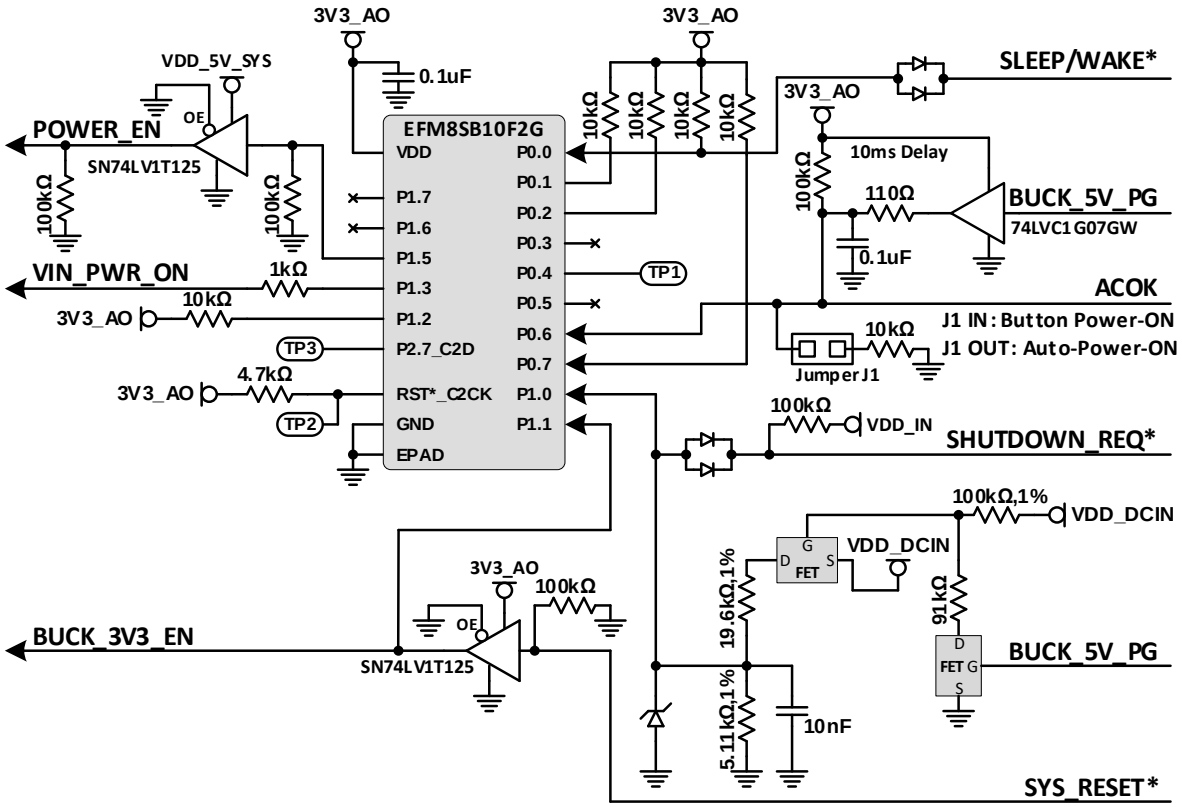
Table 6-2. Power Button Supervisor Control Signals

Button MCU Signal Name	Associated Orin Module Pin Name	Associated Module Pin #	I/O Type	Trigger Level	Drive Mode	Description	MCU Pin
BMCU_PWR_BTN*	SLEEP/WAKE*	240	Input (debounced)	Level	OD (HiZ)	Power Button	P0.0
BMCU_P01	–	–		–	–	10kΩ Pull-up to 3V3_AO	P0.1
BMCU_P02	–	–		–	–	10kΩ Pull-up to 3V3_AO	P0.2
BMCU_P03	–	–		–	–	No Connect	P0.3
BMCU_UART_TX	–	–		–	PP	Test point for FW debug	P0.4
BMCU_P05	–	–	–	–	–	No Connect	P0.5
BMCU_ACOK	–	–	Input (debounced)	Edge	OD (HiZ)	Determine when VDD_5V_SYS power is supplied. Used to select either button power on or auto-power on.	P0.6
BMCU_GOOD	–	–	Input	Level	OD (HiZ)	10kΩ Pull-up to 3V3_AO	P0.7
FORCE_OFF*	SHUTDOWN_REQ*	233	Input	Level	OD (HiZ)	Triggers shutdown sequence	P1.0
BUCK_3V3_EN	SYS_RESET*	239	Input	Edge	OD (HiZ)	Carrier board supply enable	P1.1
BMCU_BRD_SEL	–	–	Input		OD (HiZ)	10kΩ Pull-up to 3V3_AO	P1.2
VIN_PWR_ON	–	–	Output		PP	Enables power to module if wide range (5V-20V)	P1.3
BMCU_POWER_EN	POWER_EN	237	Output		PP	Power On/Off control to Power Sequencer/PMC. Also Enable input to main 5V supply (VDD_5V)	P1.5
PWR_BTN_BUF*	–	–	–	–	–	No Connect	P1.6
BMCU_P17	–	–	–	–	–	No Connect	P1.7
BMCU_C2D	–	–	–	–	–	Data for programming/debug	P2.7_C2D

Button MCU Signal Name	Associated Orin Module Pin Name	Associated Module Pin #	I/O Type	Trigger Level	Drive Mode	Description	MCU Pin
BMCU_C2CK	–	–	–	–	–	Clock for programming/debug. 4.7kΩ Pull-up to 3V3_AO.	RST*_C2CK

Note: OD – Open-drain. PP = Push-pull.

Figure 6-7. Power-On Button Circuit



Note: Button initiated power on is enabled if the ACOK line is pulled to GND (J1 in figure installed). Auto-Power-On is enabled if the ACOK line is not pulled to GND (J1 not installed - circuit drives ACOK high).

6.1.1.1 Defined Behaviors

For all actions triggered by SLEEP/WAKE* or ACOK, there will be a de-bounce time before triggering any output signal. The minimum I/O delay for these signals is therefore the de-bounce time. De-bounce time is 20 ms. If both signals above are triggered within the 20 ms de-bounce time started by the first detected signal, then the de-bounce time for the subsequent signals might extend up to 25 ms.

Note: The time values in the following timing diagrams have an accuracy of ± 10%.

6.1.1.2 Power-Off -> Power-On (Power Button Case)

Power button press use case: User presses the Power Button briefly, and the MCU sends the power enable signal to the module (POWER_EN) and on to the Power Sequencer on the Orin module. The signal representing the Power Button to the Orin Module (SLEEP/WAKE* pin), will have the same (brief) duration of the Power Button input to the MCU. Once the power button is pressed, the power OK input (ACOK) is ignored, as the power-on sequence is already initiated by the power button.

If power-on is successful, SHUTDOWN_REQ* goes high.

Figure 6-8. Power-Off to On Sequence Power Button Case

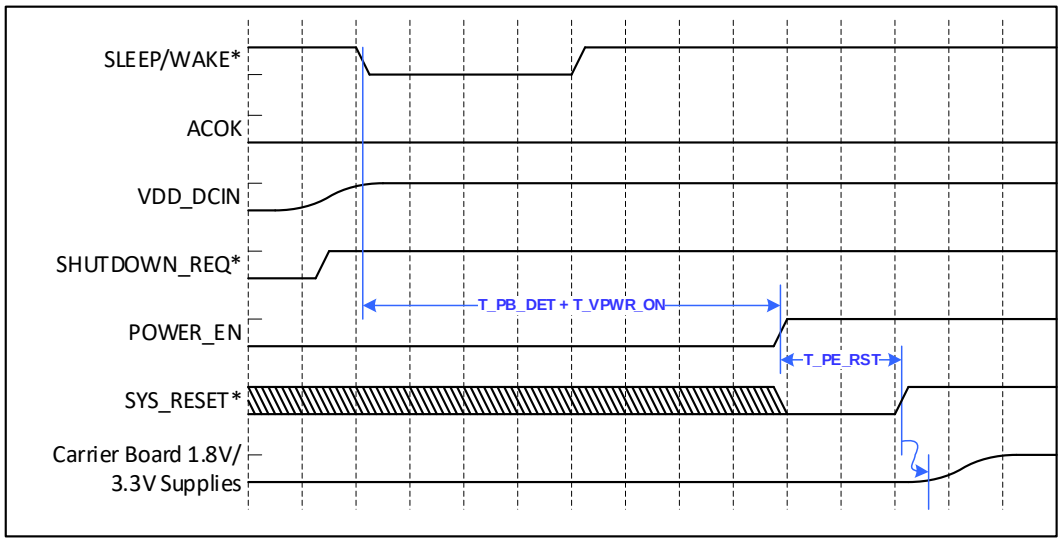


Table 6-3. Power-Off to On Timing Power Button Case

Timing	Parameter	Typical	Units
T_PB_DET	SLEEP/WAKE* (power button) detect (de-bounce only)	20	ms
T_VPWR_ON	Delay from power button active to POWER_EN	80	ms
T_PE_RST	SYS_RESET* inactive delay from POWER_EN rising edge	80	ms

6.1.1.3 Power-Off -> Power-On (Auto-Power-On Case)

In the auto power on case, the MCU enables POWER_EN as soon as the user connects the main power source. This case is selected when MCU ACOK is driven high.

The signal representing the power button to the Orin module (SLEEP/WAKE* pin) will continue following the power button behavior. However, once the power ON sequence is initiated by the connection of the main power source, and ACOK is driven high (by push-pull driver powered from 3V3_AO), the power button signals will not affect the MCU behavior until the PWR_GOOD signal verification is complete.

Figure 6-9. Power-Off to On Sequence Auto Power-On Case

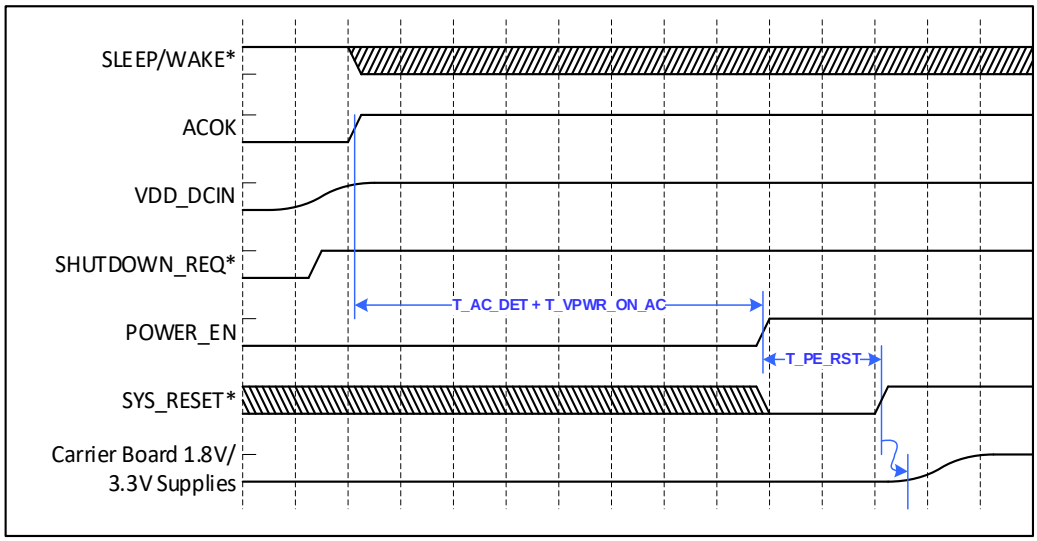


Table 6-4. Power-Off to On Timing Auto Power-On Case

Timing	Parameter	Typical	Units
T_AC_DET	ACOK assertion detect (de-bounce only)	20	ms
T_VPWR_ON_AC	Delay from ACOK detected high with main power source applied to POWER_EN	80	ms
T_PE_RST	SYS_RESET* inactive delay from POWER_EN rising edge	80	ms

6.1.1.4 Power-On -> Power-Off (Long Power Button Press)

With the system in power-on state, the user holds the power button for either more than about 4 seconds (medium button press) or about 10 seconds (long button press). The same button signal is relayed to Orin module through the POWER_EN signal. For the medium button press case, the system will do a software-controlled shutdown. For the long button press case, system is forced to shut down at about the 10 second mark without software involvement.

Figure 6-10. Power-On to Off Power Button Held Low > 10 Seconds

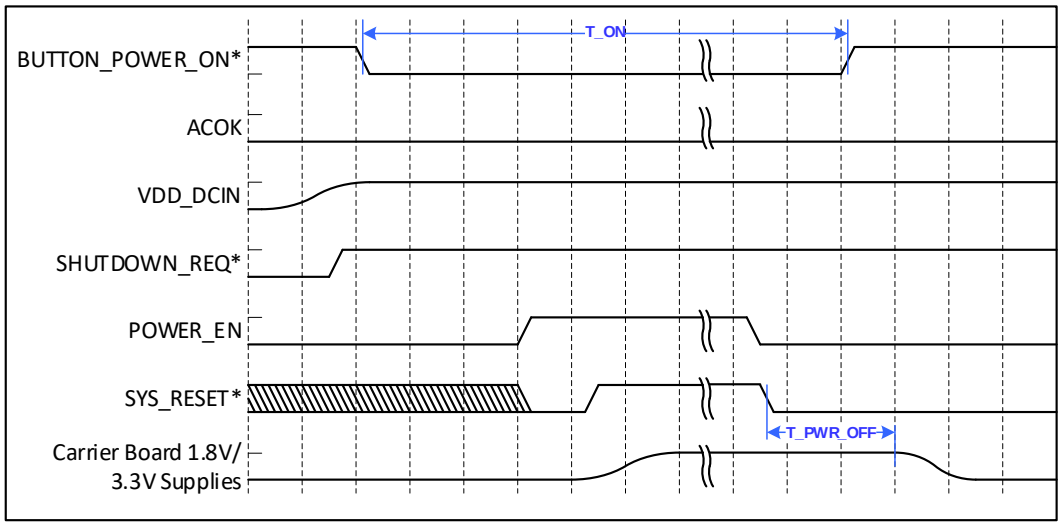


Table 6-5. Power-On to Off Timing Power Button Held Low > 10 Seconds

Timing	Parameter	Typical	Units
T_ON	Power button active duration for forced OFF (T_PWR_ON + T_MPO_ON + T_CPO + T_MPO_OFF1)	> 10	s
T_PWR_OFF	Delay to first rail OFF	10	ms

Chapter 7. USB and PCIe

Jetson Orin module allows multiple USB 2.0, USB 3.2, and PCIe interfaces to be brought out of the module.

- USB 2.0: 3x
- USB 3.2: 3x
- PCIe:
  - 1 x1 + 1 x2 + 1 x4

    or
  - 3 x1 + 1 x4

See Table 7-3 for the supported USB 3.2 and PCIe lane mapping options. These are the only options supported. The PCIe x4 interface supports both Root Port and Endpoint operation. The PCIe x1 and x2 interfaces do not support Endpoint operation. Only supports Root Port.

Table 7-1. Jetson Orin Module USB 2.0 Pin Description

Pin #	Module Pin Name	Orin Pin Name	Usage and Description	Recommended Usage	Direction	Pin Type
87	GPIO00	USB_VBUS_EN0	GPIO #0 (USB 0 VBUS Detect)	USB 2.0 Micro B	Bidir	Open Drain, 1.8V
109	USB0_D_N	HS_USB0_P0_N	USB 2.0 Port 0 Data	USB (for Recovery mode) conn/device/hub (i.e. Micro B)	Bidir	USB PHY
111	USB0_D_P	HS_USB0_P0_P				
115	USB1_D_N	HS_USB0_P1_N	USB 2.0 Port 1 Data	USB conn/device/hub (i.e. USB 3.2 Hub)	Bidir	USB PHY
117	USB1_D_P	HS_USB0_P1_P				
121	USB2_D_N	HS_USB0_P2_N	USB 2.0, Port 2 Data	USB conn/device/hub (i.e. M.2 Key E)	Bidir	USB PHY
123	USB2_D_P	HS_USB0_P2_P				

Note: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Table 7-2. Jetson Orin Module USB 3.2 and PCIe Pin Description

Pin #	Module Pin Name	Orin SoC Pin Name (See Note 4)	Usage and Description	Recommended Usage	Direction	Pin Type
131	PCIE0_RX0_N	HS_UPHY0_L4_RX_N	PCIe #0 Receive 0 (PCIe Ctrl #4 Lane 0)	PCIe x4 conn/device (i.e. M.2 Key M)	Input	PCIe PHY
133	PCIE0_RX0_P	HS_UPHY0_L4_RX_P				
137	PCIE0_RX1_N	HS_UPHY0_L5_RX_N	PCIe #0 Receive 1 (PCIe Ctrl #4 Lane 1)			
139	PCIE0_RX1_P	HS_UPHY0_L5_RX_P				
149	PCIE0_RX2_N	HS_UPHY0_L6_RX_N	PCIe #0 Receive 2 (PCIe Ctrl #4 Lane 2)			
151	PCIE0_RX2_P	HS_UPHY0_L6_RX_P				
155	PCIE0_RX3_N	HS_UPHY0_L7_RX_N	PCIe #0 Receive 3 (PCIe Ctrl #4 Lane 3)			
157	PCIE0_RX3_P	HS_UPHY0_L7_RX_P				
134	PCIE0_TX0_N	HS_UPHY0_L4_TX_N	PCIe #0 Transmit 0 (PCIe Ctrl #4 Lane 0)		Output	PCIe PHY
136	PCIE0_TX0_P	HS_UPHY0_L4_TX_P				
140	PCIE0_TX1_N	HS_UPHY0_L5_TX_N	PCIe #0 Transmit 1 PCIe Ctrl #4 Lane 1)			
142	PCIE0_TX1_P	HS_UPHY0_L5_TX_P				
148	PCIE0_TX2_N	HS_UPHY0_L6_TX_N	PCIe #0 Transmit 2 (PCIe Ctrl #4 Lane 2)			
150	PCIE0_TX2_P	HS_UPHY0_L6_TX_P				
154	PCIE0_TX3_N	HS_UPHY0_L7_TX_N	PCIe #0 Transmit 3 (PCIe Ctrl #4 Lane 3)			
156	PCIE0_TX3_P	HS_UPHY0_L7_TX_P				
181	PCIE0_RST*	GP184_PCIE4_RST_N	PCIe #0 Reset (PCIe Ctrl #4). 4.7kΩ pull-up to 3.3V on the module. Output when module is Root Port or input when module is Endpoint.		Bidir	Open Drain 3.3V
180	PCIE0_CLKREQ*	GP183_PCIE4_CLKREQ_N	PCIE #0 Clock Request (PCIe Ctrl #4). 47kΩ pull-up to 3.3V on the Orin module. Input when Orin module is Root Port or output when Orin module is Endpoint.			
160	PCIE0_CLK_N	SF_PCIE4_CLK_N HS_UPHY0_REFCLK2_N	PCIe #0 Reference Clock controlled by on-module mux by SoC GP21. When GP21 is low, SF_PCIE4_CLK is selected (reference clock when Orin module is Root Port). When GP21 is high, UPHY0_REFCLK2_IN is selected (reference clock input when Orin module is an Endpoint).		Bidir	PCIe PHY
162	PCIE0_CLK_P	SF_PCIE4_CLK_P HS_UPHY0_REFCLK2_P				
167	PCIE1_RX0_N	HS_UPHY0_L3_RX_N	PCIe #1 Receive 0 (PCIe Ctrl #1 Lane 0)	PCIe x1 conn/device (i.e. M.2 Key E)	Input	PCIe PHY
169	PCIE1_RX0_P	HS_UPHY0_L3_RX_P				
172	PCIE1_TX0_N	HS_UPHY0_L3_TX_N	PCIe #1 Transmit 0 (PCIe Ctrl #1 Lane 0)		Output	PCIe PHY
174	PCIE1_TX0_P	HS_UPHY0_L3_TX_P				
183	PCIE1_RST*	GP178_PCIE1_RST_N	PCIe #1 Reset (PCIe Ctrl #1). 4.7kΩ pull-up to 3.3V on the module.		Output	Open Drain 3.3V
182	PCIE1_CLKREQ*	GP177_PCIE1_CLKREQ_N	PCIE #1 Clock Request (PCIe Ctrl #1). 47kΩ pull-up to 3.3V on the module.		Bidir	Open Drain 3.3V

Pin #	Module Pin Name	Orin SoC Pin Name (See Note 4)	Usage and Description	Recommended Usage	Direction	Pin Type
173	PCIE1_CLK_N	SF_PCIE1_CLK_N	PCIe #1 Reference Clock (PCIe Ctrl #1)		Output	PCIe PHY
175	PCIE1_CLK_P	SF_PCIE1_CLK_P				
40	CSI4_D2_N	HS_UPHY2_L0_RX_N	PCIe 2 Receive 0– (PCIe Ctrl #7 Lane 0)	PCIe x2 (Ctrl #7) or 2 x PCIe x1 (Ctrl #7 and Ctrl #9)	Input	PCIe PHY
42	CSI4_D2_P	HS_UPHY2_L0_RX_P	PCIe 2 Receive 0+ (PCIe Ctrl #7 Lane 0)		Input	PCIe PHY
58	CSI4_D1_N	HS_UPHY2_L1_RX_N	PCIe #2 Receive 1– (PCIe Ctrl #7 Lane 1) or PCIe #3 Receive 0– (PCIe Ctrl #9 Lane 0)		Output	PCIe PHY
60	CSI4_D1_P	HS_UPHY2_L1_RX_P	PCIe #2 Receive 1+ (PCIe Ctrl #7 Lane 1) or PCIe #3 Receive 0+ (PCIe Ctrl #9 Lane 0)		Output	PCIe PHY
46	CSI4_D0_N	HS_UPHY2_L0_TX_N	PCIe #2 Transmit 0– (PCIe Ctrl #7 Lane 0)		Output	PCIe PHY
48	CSI4_D0_P	HS_UPHY2_L0_TX_P	PCIe #2 Transmit 0+ (PCIe Ctrl #7 Lane 0)		Output	PCIe PHY
64	CSI4_D3_N	HS_UPHY2_L1_TX_N	PCIe #2 Transmit 1– (PCIe Ctrl #7 Lane 1) or PCIe #3 Transmit 0– (PCIe Ctrl #9 Lane 0)		Output	PCIe PHY
66	CSI4_D3_P	HS_UPHY2_L1_TX_P	PCIe #2 Transmit 1+ (PCIe Ctrl #7 Lane 1) or PCIe #3 Transmit 0+ (PCIe Ctrl #9 Lane 0)		Output	Open Drain 3.3V
52	CSI4_CLK_N	SF_PCIE7_CLK_N	PCIe #2 Reference Clock– (PCIe Ctrl #7)		Input	Open Drain 3.3V
54	CSI4_CLK_P	SF_PCIE7_CLK_P	PCIe #2 Reference Clock+ (PCIe Ctrl #7)		Input	PCIe PHY
219	SDMMC_DAT0	GP188_PCIE7_RST_N	PCIe #2 Reset (PCIe Ctrl #7). 4.7kΩ pull-up to 3.3V on the module.		Output	PCIe PHY
221	SDMMC_DAT1	GP187_PCIE7_CLKREQ_N	PCIE #2 Clock Request (PCIe Ctrl #7). 47kΩ pull-up to 3.3V on the module.		Bidir	Open Drain 3.3V
229	SDMMC_CLK	SF_PCIE9_CLK_P	PCIe #3 Reference Clock+ (PCIe Ctrl #9)	PCIe x1 (Ctrl #3)	Output	Open Drain 3.3V
227	SDMMC_CMD	SF_PCIE9_CLK_N	PCIe #3 Reference Clock – (PCIe Ctrl #9)		Output	PCIe PHY
223	SDMMC_DAT2	GP192_PCIE9_RST_N	PCIe #3 Reset (PCIe Ctrl #9). 4.7kΩ pull-up to 3.3V on the module.		Output	PCIe PHY
225	SDMMC_DAT3	GP191_PCIE9_CLKREQ_N	PCIE #3 Clock Request (PCIe Ctrl #9). 47kΩ pull-up to 3.3V on the module.		Bidir	PCIe PHY
179	PCIE_WAKE*	GP185_PCIE_WAKE_N	PCIe Wake. 47kΩ pull-up to 3.3V on the module.	Shared between PCIe interfaces.	Input	Open Drain 3.3V
161	USBSS_RX_N	HS_UPHY0_L0_RX_N	USB 3.2 Receive (Port #0)	USB 3.2 connector, device or hub	Input	USB 3.2 PHY
163	USBSS_RX_P	HS_UPHY0_L0_RX_P				
166	USBSS_TX_N	HS_UPHY0_L0_TX_N	USB 3.2 Transmit (Port #0)		Output	USB 3.2 PHY
168	USBSS_TX_P	HS_UPHY0_L0_TX_P				
39	DP0_TXD0_N	HS_UPHY0_L1_RX_N	USB 3.2 Receive (Port #1)	USB 3.2 connector, device or hub	Input	USB 3.2 PHY
41	DP0_TXD0_P	HS_UPHY0_L1_RX_P				
45	DP0_TXD1_N	HS_UPHY0_L1_TX_N	USB 3.2 Transmit (Port #1)		Output	USB 3.2 PHY
47	DP0_TXD1_P	HS_UPHY0_L1_TX_P				

Pin #	Module Pin Name	Orin SoC Pin Name (See Note 4)	Usage and Description	Recommended Usage	Direction	Pin Type
51	DP0_TXD2_N	HS_UPHY0_L2_RX_N	USB 3.2 Receive (Port #2)	USB 3.2 connector, device or hub	Input	USB 3.2 PHY
53	DP0_TXD2_P	HS_UPHY0_L2_RX_P				
57	DP0_TXD3_N	HS_UPHY0_L2_TX_N	USB 3.2 Transmit (Port #2)		Output	USB 3.2 PHY
59	DP0_TXD3_P	HS_UPHY0_L2_TX_P				

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction shown in this table for GPxxx_PCIEx_RST* and GP185_PCIE_WAKE* signals is true when used for those PCIe functions. Otherwise, if used as GPIOs, the direction is bidirectional.
3. The light blue highlighting for some of the module pins/functions is just to highlight the different functionality on those pins.
4. The table above shows Module Pin Names and Orin SoC Pin Names. For the Orin Module Function, which can be very different than the Module Pin name, see the Pinout Matrix, full Pin Desc. xls attached to this document, or Table 7-3 below.

The following tables shows the supported UPHY mapping for the UPHY blocks [2,0]. The mapping tables indicate which lanes of each UPHY block can be assigned for USB or PCIe. Only one of the supported configurations per UPHY block can be used in a design. Each UPHY block is programmed independently. It is not required to select the same configuration on both UPHY blocks.

Table 7-3. UPHY0 Mapping Options (USB 3.2 and PCIe)

Orin Module Pin Names	Orin Module Functions	UPHY0 Lanes	Orin Module Configurations		
			Option #1	Option #2	Option #3
PCIE0_RX0/TX0	PCIe #0 Lane 0	UPHY0, Lane 4	PCIe x4 (C4), RP	PCIe x4 (C4), EP	PCIe x4 (C4), EP
PCIE0_RX1/TX1	PCIe #0 Lane 1	UPHY0, Lane 5			
PCIE0_RX2/TX2	PCIe #0 Lane 2	UPHY0, Lane 6			
PCIE0_RX3/TX3	PCIe #0 Lane 3	UPHY0, Lane 7			
PCIE1_RX0/TX0	PCIe #1 Lane 0	UPHY0, Lane 3	PCIe x1 (C1), RP	PCIe x1 (C1), RP Limited to Gen2	PCIe x1 (C1), RP
USBSS_RX/TX	USB 3.2 #1	UPHY0, Lane 0	USB 3.2 (P0)	USB 3.2 (P0)	USB 3.2 (P0)
DP0_TXD[1:0]_N/P	USB 3.2 #2	UPHY0, Lane 1	USB 3.2 (P1)	USB 3.2 (P1)	USB 3.2 (P1)
DP0_TXD[3:2]_N/P	USB 3.2 #3	UPHY0, Lane 2	USB 3.2 (P2)	USB 3.2 (P2)	Unused

Table 7-4. UPHY2 Mapping Options (PCIe)

Orin Module Pin Names	Orin Module Functions	UPHY2 Lanes	Orin Module Configurations	
			Option #1	Option #2
CSI4_D[0:2]_RX0/TX0	PCIe #2 Lane 0	Lane 0	PCIe x2 (C7), RP	PCIe x1 (C7), RP
CSI4_D[1:3]_RX1/TX1	PCIe #2 Lane 1	Lane 1		PCIe x1 (C9), RP

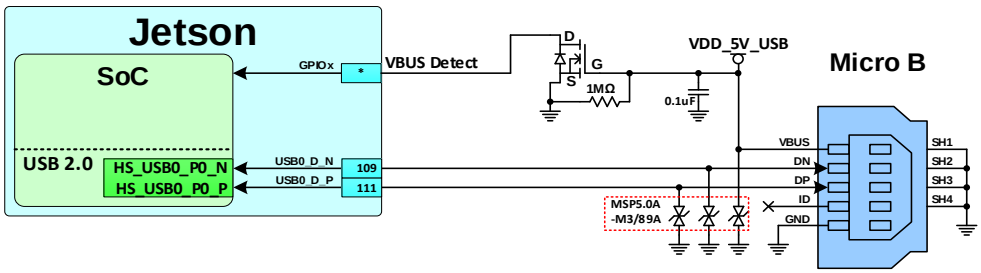
7.1 USB

Orin module supports up to three USB 2.0 ports and up to three USB 3.2 ports. Two examples are shown in Figure 7-1 and Figure 7-2. Polarity inversion (P/N swapping) is supported for the USB 3.2 interfaces.

Note: Some non-compliant USB 3.0 devices will not function correctly unless USB 3.2 Gen2 is disabled.

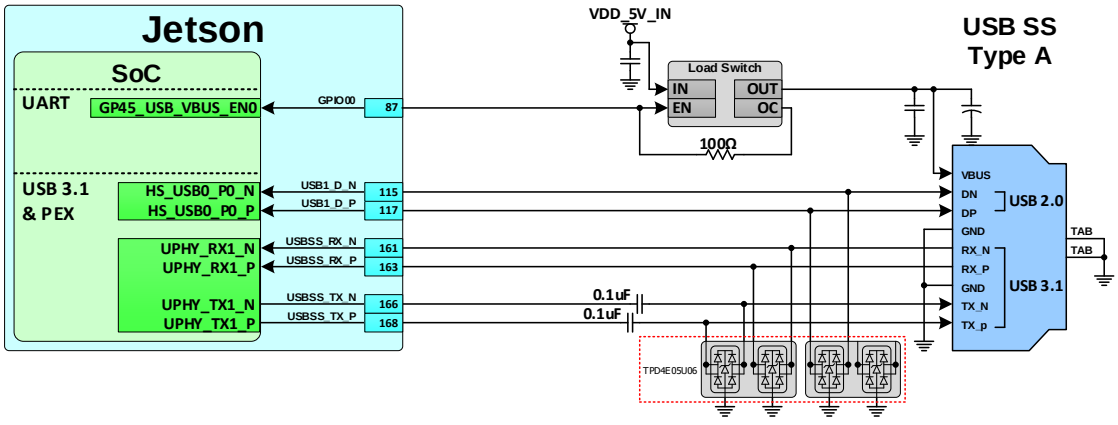
The example shown in Figure 7-1 is for connections to a USB device only connector to be used to support recovery mode (See Section 3.2 "USB Recovery Mode" for details on recovery mode) or a USB device if booted normally. A USB Micro B connector is shown in the example.

Figure 7-1. USB Micro B USB Device and Recovery Connection Example



The example shown in Figure 7-2 is for connections to a USB 3.2 Type A connector to support host only. Recovery mode is not supported.

Figure 7-2. USB 3.2 Type A Host Only Connection Example



Notes:

1. AC capacitors should be located close to either the USB connector, or the Orin module pins.
2. Connector used must be USB Implementers Forum certified if USB 3.2 is implemented.

7.1.1 USB 2.0 Routing Guidelines

The following table details the requirements that apply to the USB 2.0 controller PHY interfaces: USB[2:0]_D_N/P.

Table 7-5. USB 2.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency (high speed): Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max loading: High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	Max loading should include any passive and active components on the trace such as CMC, Switch, ESD etc.
Reference plane	GND		
Trace impedance: Diff pair / SE)	90 / 50	Ω	±15%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Max trace length/delay	6 (960)	In (ps)	
Max intra-pair skew between **USBx_D_P** and **USBx_D_N**	7.5	ps	

Notes:

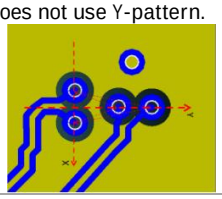
1. Up to four signal vias can share a single GND return via.
2. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

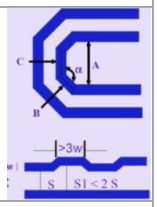
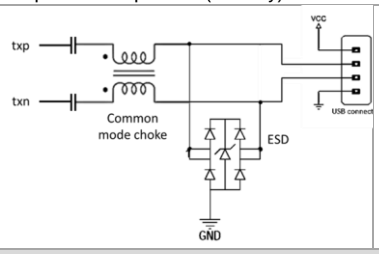
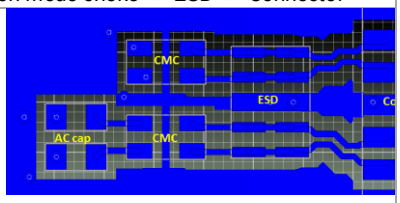
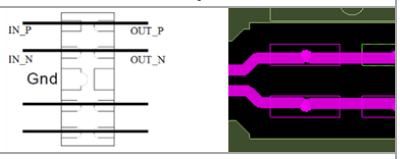
7.1.2 USB 3.2 Routing Guidelines

The following table details the requirements that apply to the USB 3.2 PHY interfaces.

Table 7-6. USB 3.2 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI period Gen1 Gen2	 5.0 / 200 10.0 / 100	 Gbps / ps	Device mode supports Gen1 speed only.
Max Number of Loads	1	load	
Termination	90 differential	Ω	On-die termination at TX and RX
Electrical Specification			
Insertion Loss (IL) Gen1 Host (Type C) Gen1 Host (Type A) Gen1 Device (Type C) Gen1 Device (Micro AB) Gen2 (Dual role mode) Resonance Dip Frequency	 ⩾ -3.8 ⩾ -7.3 ⩾ -3.8 ⩾ -2.5 [*] ⩾ -4.5 > 8	 dB @ 2.5GHz dB @ 2.5GHz dB @ 2,5GHz dB @ 2.5GHz dB @ 5GHz GHz	Only the PCB (and connector) without added-on components such as CMC, ESD, and Mux, is considered. The connector is included. For Gen2 the loss budget is the same for all connector types. For dual role mode, host and device have the same loss budget [*] the consideration of Gen1 fixture loss
Time-domain Reflectometer (TDR) Dip Gen1 Gen2	 75 75	 Ω	@ Tr = 200ps (10%-90%) @ Tr = 61ps (10%-90%)

Parameter	Requirement	Units	Notes
Near End Crosstalk (NEXT)	≤ –45	dB	DC – 5GHz per each TX-RX NEXT
Impedance			
Trace Impedance: Diff pair / Single Ended	85 / 43	Ω	±15%. Intrinsic Zdf, does not account for coupling from other trace pairs
Reference plane	GND		
Trace Length/Skew			
Trace loss characteristic: Gen1 Gen2	 < 0.6 < 1	 dB/in @ 2.5 GHz dB/in @ 5G Hz	Based on the dielectric material EM370(Z). The following max length is derived based on this characteristic. The length constraint must be re-defined if the loss characteristic is changed. Note that microstrip loss could be similar to stripline due to humidity effect.
Breakout Region – Max length	11	mm	Minimum trace width and spacing
Max Trace Length (delay) Gen1 Host Gen1 Device Gen2 Host or Device	 160 (1071) 107 (714) 114 (765)	mm (ps)	Stripline (6.7ps/mm) assumed. CMC use length reduction = 30 mm (Gen1/2). ESD use length reduction = 10 mm (Gen1), 12.5 mm (Gen2).
Max Intra-Pair Skew (**RX/TX_N** to **RX/TX_P**)	0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Trace length matching should be done before discontinuities.
Differential pair uncoupled length	6.29 (41.9)	mm (ps)	
Trace Spacing for TX/RX Interleaving			
Trace Spacing: Microstrip / Stripline Pair-Pair To Ref plane and SMT pad To unrelated high-speed signals	 4x / 3x 4x / 3x 4x / 3x	 Dielectric height	
Trace Spacing for TX/RX Non-interleaving			
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.			
If routing on the same layer, strongly recommend not interleaving TX and RX lanes			
If have to have interleaving routing in breakout, all the inter-pair spacing should follow the rule of inter-S_{NEXT} (between TX/RX pair spacing)			
The breakout trace width is suggested to be the minimum to increase inter-pair spacing			
Do not perform serpentine routing for intra-pair skew compensation in the breakout region			
Min Inter-S_{NEXT} (between TX/RX) Breakout Main-route	 4.85x 3x	 Dielectric height	This is the recommended dimensions for meeting the NEXT requirement. Stripline structure in a GSSG structure is assumed (holds in broadside-coupled stripline structure)
Max length Breakout Main-route	 11 Max trace length - L_{BRK}	 mm	
Via			
Topology	Y-pattern is recommended Keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of the pair-pair distance. Review needed (NEXT/FEXT check) if via placement does not use Y-pattern. 
GND via	Place **GND** via as symmetrically as possible to data pair vias. Up to 4		**GND** via is used to maintain return path, while its Xtalk suppression is limited

Parameter	Requirement	Units	Notes
	signal vias (2 diff pairs) can share a single **GND** return via		
Max # of Vias PTH vias Micro Vias	4 if all vias are PTH via Not limited if total channel loss meets IL spec		
Max Via Stub Length	0.4	mm	long via stub requires review (IL and resonance dip check)
Serpentine			
Min bend angle	135	deg (a)	
Dimension Min A Spacing Min B, C Length Min Jog Width	 4x 1.5x 3x	Trace width	S1 must be taken care in order to consider Xtalk to adjacent pair. 
Additional Component Placement Order			
	Chip – AC capacitor (TX only) – common mode choke – ESD – Connector		
			
AC Cap			
Value on TX – Min/Max	100/265	nF	100nF recommended. Only required for TX pair when routed to connector.
Value on RX (connector case) – Min/Max	297/363	nF	Optional. 330 nF recommended if placed.
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Voiding	**GND**/**PWR** void under/above cap is preferred		Voiding is required if AC cap size is 0603 or larger
ESD (On-chip protection diode can withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max Junction capacitance (IO to GND) Gen1 Gen2	 0.8 0.35	pF	 Gen1: SEMTECH RClamp0524p Gen2: TPD4E02B04DQA
Footprint	Pad should be on the net – not trace stub		
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues). See Chapter 17 for details on CMC if implemented.			
FPC (Additional length of Flexible Printed Circuit Board)			
The FPC routing should be included for PCB trace calculations (max length, etc.)			
Characteristic Impedance	Same as PCB		
Loss characteristic	Strongly recommend being the same as the PCB or better		If worse than PCB, the PCB and FPC length must be re-estimated
Connector			
SMT Connector **GND** Voiding	**GND** plane under signal pad should be voided. Size of void should be the same size as the pad.		
Connector used must be USB-IF certified			

Parameter	Requirement	Units	Notes
General: See Chapter 17 for guidelines related to serpentine routing, routing over voids and noise coupling			

The following figures show the USB 3.2. Interface signal routing requirements.

Figure 7-3. IL/NEXT Plot

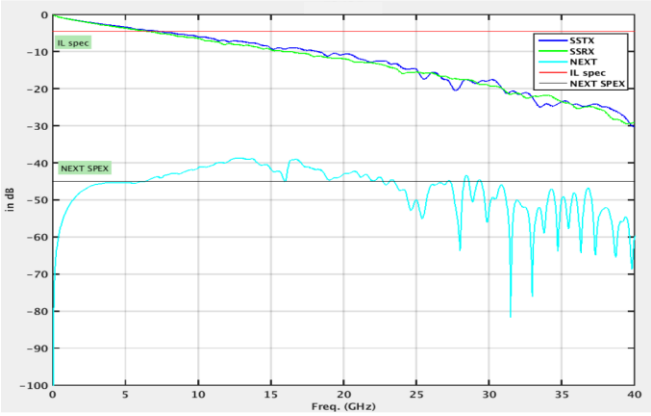
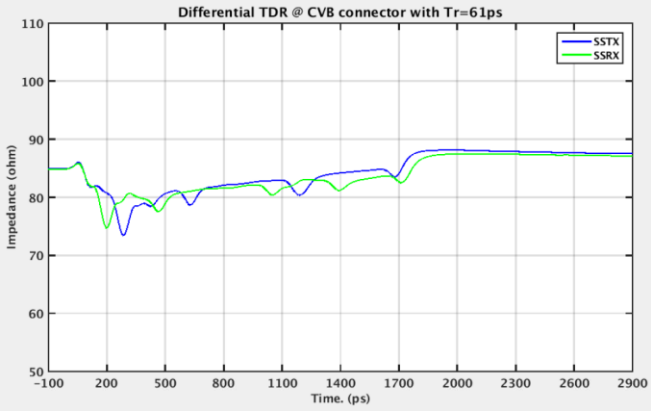


Figure 7-4. TDR Plot



7.1.2.1 Common USB Routing Guidelines

If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs and flexes must be used for the max trace and skew calculations.

Keep critical USB related traces away from other signal traces or unrelated power traces and areas or power supply components.

Table 7-7. Orin USB 2.0 Signal Connections

Module Ball Name	Type	Termination	Description

USB[2:0]_D_P USB[2:0]_D_N	DIFF I/O	If used, 90Ω common-mode chokes close to connector. ESD Protection between choke and connector on each line to GND	USB Differential Data Pair: Connect to USB connector, Mini-Card socket, hub, or another device on the PCB.

Table 7-8. Miscellaneous USB 2.0 Signal Connections

Module Pin Name	Type	Termination	Description
GPIO00 (USB_VBUS_EN0)	I/O		USB0 VBUS Enable: Connect to enable and overcurrent pins of load switch (through 100ohm series resistor to OC pin).
GPIO (VBUS Detect)	I	5V to 1.8V level shifter	VBUS Detect: Connect to VBUS pin of USB connector receiving USB0_+/– interface through level shifter.

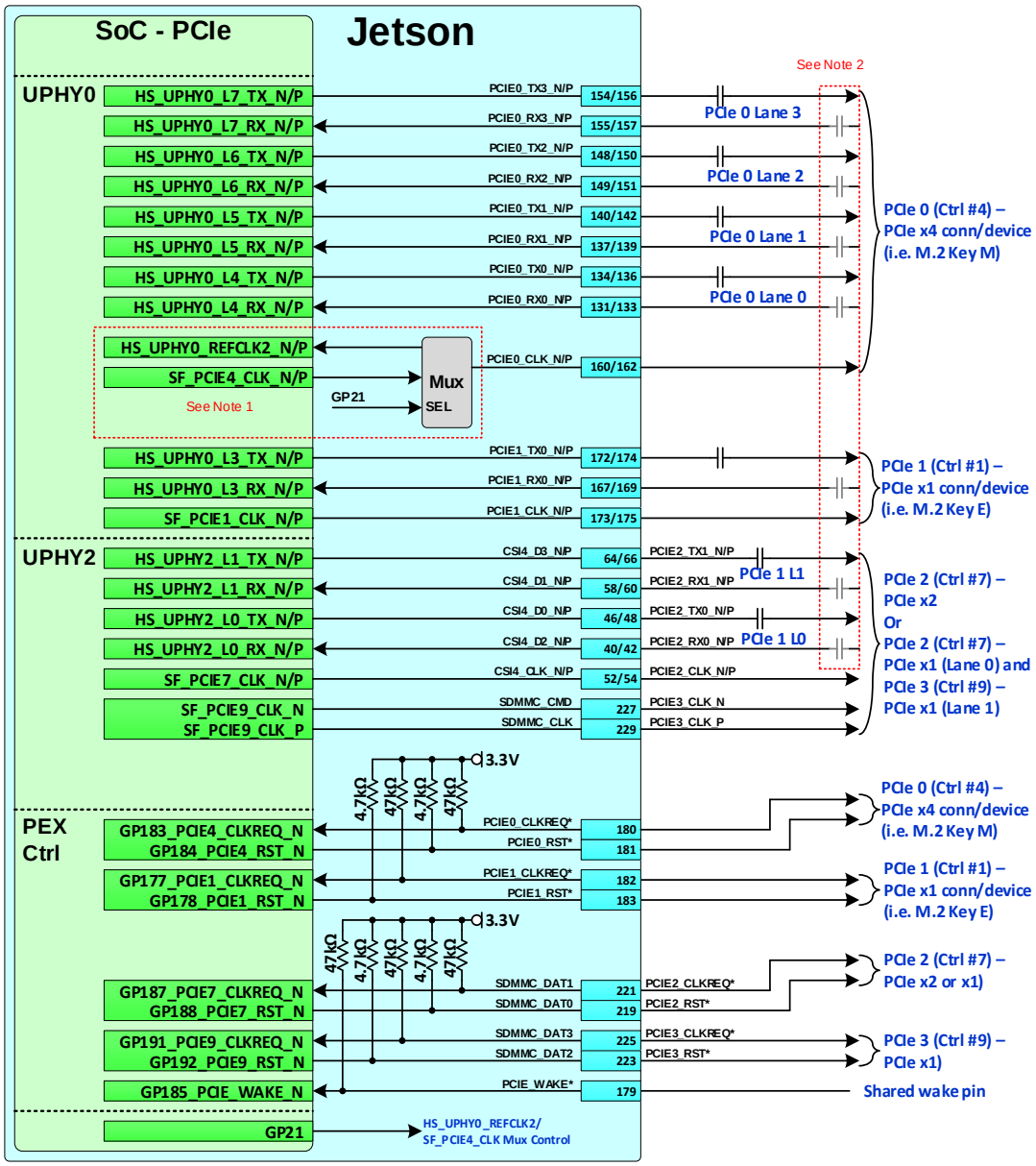
Table 7-9. Orin USB 3.2 Signal Connections

Module Pin Name	Type	Termination	Description
USBSS_TX_N/P (USB 3.2 Port #0) DP0_TXD1_N/P (USB 3.2 Port #1) DP0_TXD3_N/P (USB 3.2 Port #2)	DIFF Out	Series 0.1uF caps. ESD Protection near connector if required.	USB 3.2 Differential Transmit Data Pairs: Connect to USB 3.2 connectors, hubs, or other devices on the PCB.
USBSS_RX_N/P (USB 3.2 Port #0) DP0_TXD0_N/P (USB 3.2 Port #1) DP0_TXD2_N/P (USB 3.2 Port #2)	DIFF In	If routed directly to a peripheral on the board, AC caps are needed for the peripheral TX lines. ESD protection near connector if required.	USB 3.2 Differential Receive Data Pairs: Connect to USB 3.2 connectors, hubs, or other devices on the PCB.

7.2 PCIe

Orin module brings four PCIe interfaces to the module pins for up to seven total lanes (1 x4 + 1 x1 + 1x2) for use on the carrier board. The PCIe x4 interface (PCIE0) operates up to Gen4 speed and supports both Root Port and Endpoint operation. The PCIe x1 interface (PCIE1) operates up to Gen4 speed and support only Root Port operation. The PCIe x2 interface (PCIE2) can also be broken into two x1 interfaces (PCIE2 x1 and PCIE3 x1). PCIE2 and PCIE3 operate up to Gen4 speed and support only Root Port operation. Figure 7-5 shows all possible interfaces as Root Ports. Figure 7-6 shows the x4 interfaces as an Endpoint. Lane reversal and polarity inversion (P/N swapping) is supported per controller.

Figure 7-5. PCIe Root Port Connections Example

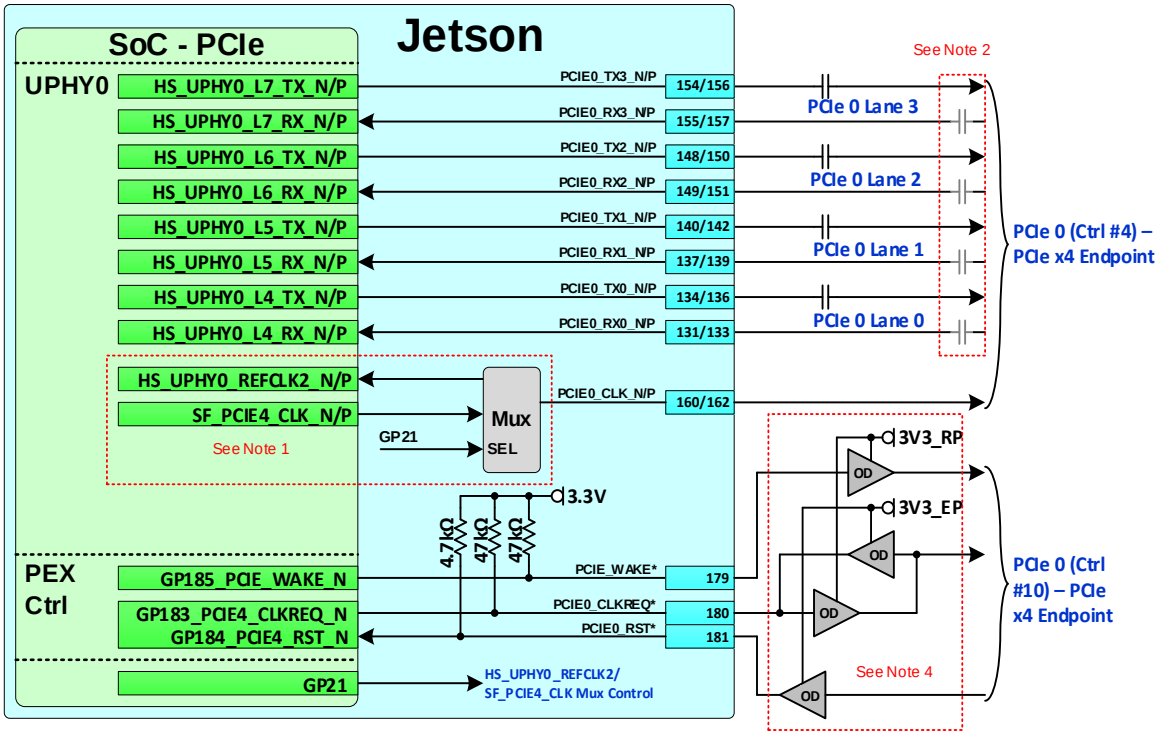


Notes:

1. For Root Port operation, the mux should be set to output the SF_PCIE10_CLK signals. SoC GP21 which is used for the mux select should be set low.
2. AC Capacitors required on RX lines on carrier board if connected directly to device. They should not be on the carrier board if connected to PCIe connector, M.2 Key M, etc. In those cases, the AC caps are on the board connected to those connectors.
3. See design guidelines for correct AC capacitor values.
4. The PCIe REFCLK inputs and CLK outputs comply to the PCIe CEM specification "REFCLK DC Specifications and AC Timing Requirements." The clocks are HCSL compatible.

Figure 7-6 shows the x4 interface configured as Endpoint for the PCIe Endpoint connections.

Figure 7-6. PCIe Endpoint Connections Example



Notes:

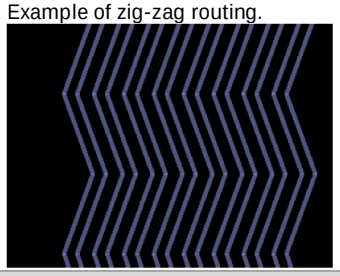
1. For Endpoint operation, the mux should be set to output the HS_UPHY2_REFCLK2 signals. SoC GP21 which is used for the mux select should be set high.
2. AC capacitors required on RX lines on carrier board if connected directly to device. They should not be on the carrier board if connected to PCIe connector, M.2 Key M, etc. In those cases, the AC caps are on the board connected to those connectors.
3. See design guidelines for correct AC capacitor values.

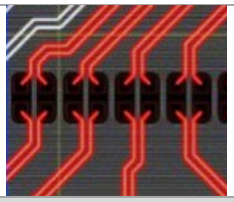
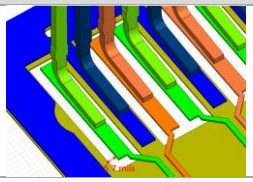
4. Isolation circuitry is required on the PCIe control signals when Orin module is configured as Endpoint. These isolate the lines from the on-module pull-ups as well as ensure the Endpoint and Root Port devices do not have their pads driven high before power is applied.
5. The PCIe REFCLK inputs and PCIEx_CLK clock outputs comply to the PCIe CEM specification "REFCLK DC Specifications and AC Timing Requirements." The clocks are HCSL compatible.

7.2.1 PCIe Routing Guidelines

The following table provides the PCIe routing guidelines for Gen3 and Gen4.

Table 7-10. PCIe Interface Signal Routing Requirements up to Gen4

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period Gen3 Gen4	 8.0 / 125 16.0 / 62.5	Gbps / ps	
Topology	Point-point		Unidirectional, differential. Driven by 100MHz common reference clock
Termination	43	Ω	To **GND** Single Ended for P and N
Impedance			
Trace Impedance differential / Single Ended	 85 / 50	 Ω	±15%
Reference plane	GND		
Fiber-weave effect (Only required for Gen4)	• Use spread-glass (denser weave) instead of regular-glass (sparse weave) to minimize intra-pair skew • Use zig-zag route instead of straight to minimize skew, this is mandatory for PCIe gen4 design		Example of zig-zag routing. 
Spacing			
Trace Spacing (Stripline) Pair – Pair To plane and capacitor pad To unrelated high-speed signals	 4x 4x 4x	 Dielectric height	TX and RX should not be routed on the same layer. If this is required in a design, they should not be interleaved, and the spacing between the closest RX and TX lanes must be 9x Dielectric height spacing.
Length/Skew			
Breakout region (Max delay)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Gen 4.0 max trace loss / length (delay): Direct to device: Insertion loss / length (delay) Routing to 2nd Orin Module Insertion loss / length (delay)	 -20.51 / 345 (2208) -14.74 / 248 (1587)	 dB / mm (ps)	Direct to device Insertion loss budget is for PCB routing, connectors, and end device (See Note 1). EM-370(Z) PCB material is assumed in the length/delay calculations:

Parameter	Requirement	Units	Notes
Routing to M.2 (NVMe) connector/card: Insertion loss / length (delay)	 -11.01 / 185 (1185)		Gen 4.0: -1.51 dB/in @ 8Ghz Gen 3.0: -0.86 dB/in @ 4GHz
Gen 3.0 max trace: Direct to device: Insertion loss / length (delay) Routing to 2nd Orin Module Insertion loss / length (delay) Routing to PCIe/M.2 connector/module: Insertion loss / length (delay)	 -15.8 / 467 (2987) -10.5 / 310 (1985) -7.6 / 224 (1437)	dB / mm (ps)	Length to delay calculations assumes 6.4 ps/mm (average of stripline and microstrip). The 2nd Orin Module loss assumption is: Gen 4.0: -8 dB @ 8GHz Gen 3.0: -6.5 dB @4GHz The PCIe/M.2 connector/card loss assumption is: Gen 4.0: -9.5 dB @ 8GHz Gen 3.0: -8.2 dB @4GHz
Max PCB via delay from the Device/Connector	41.9	ps	Max distance from Device ball or Connector pin to first PCB via.
PCB within pair (intra-pair) skew	0.15 (1)	mm (ps)	Do trace length (delay) matching before hitting discontinuities.
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (1)	mm (ps)	
Differential pair uncoupled delay	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias	4		Use micro via or back drilled via - no via stub allowed.
Max Via stub length	N/A		Not Allowed
AC Cap			
Value Min/Max	0.22	uF	20%, 0402 X5R or better. Only required for TX pair when routed to connector. Place close to TX side.
Voiding	Voiding the plane directly under the pad ~0.1mm larger than the pad size is required.		
Serpentine (See USB 3.2 Guidelines)			
Serpentine			
Min bend angle	135	deg (a)	S1 must be taken care in order to consider Xtalk to adjacent pair. (
Dimension Min A Spacing Min B, C Length Min Jog Width	 4x 1.5x 3x	Trace width	
Miscellaneous			
GND fill rule	Remove unwanted GND fill that is either floating or act like antenna		
Connector			
Voiding	Void all layers of golden finger area under the pad ~0.15mm larger than the pad size is recommended.		

Parameter	Requirement	Units	Notes
Keep critical PCIe traces such as PEX_TX/RX, etc. away from other signal traces or unrelated power traces and areas or power supply components			

Note:

1. This does not consider the loss of the end device or any additional connectors. These need to be accounted for and will reduce the loss budget which will affect the max length or delay possible.
2. The max length and delay numbers are examples. These should be updated based on the actual PCB material loss and the loss for the end device and any additional connections.

Figure 7-7. Insertion Loss S-Parameter Plot SDD21

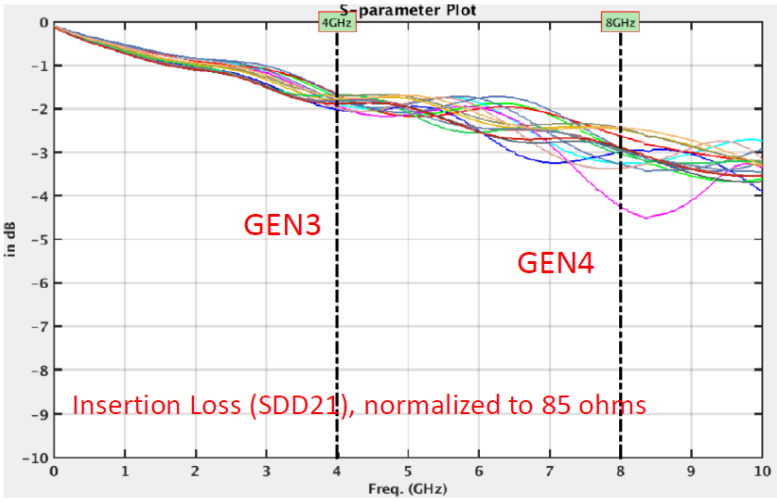


Figure 7-8. Insertion Loss S-Parameter Plot SDD11

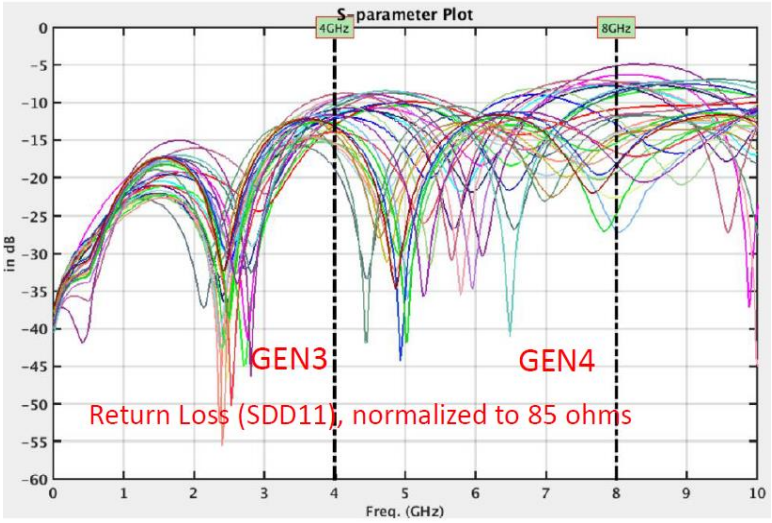


Table 7-11. PCIe Signal Connections

Module Pin Name (Function)	Type	Termination	Description
PCIe Interface 0 (x4 – Controller #4, Root Port or Endpoint)			
PCIE0_TX3_N/P PCIE0_TX2_N/P PCIE0_TX1_N/P PCIE0_TX0_N/P	DIFF OUT	Series 0.22uF Capacitor	**Differential Transmit Data Pairs:** Connect to TX_N/P pins of PCIe connector or RX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE0_RX3_N/P PCIE0_RX2_N/P PCIE0_RX1_N/P PCIE0_RX0_N/P	DIFF IN	Series 0.22uF capacitors near Orin Module pins or device if device on main PCB.	**Differential Receive Data Pairs:** Connect to RX_N/P pins of PCIe connector or TX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE0_CLK_N/P Root Port Endpoint	 DIFF OUT DIFF IN		**Differential Reference Clock Output:** Connected to a mux on the module that selects either SF_PCIE10_CLK or UPHY2_REFCLK2. Connect to REFCLK_N/P pins of PCIe device/connector. For Root Port operation, set the mux to select SF_PCIE10_CLK (GP21 = 0). For Endpoint, set the mux to select UPHY2_REFCLK2 (GP21 = 1).
PCIE0_CLKREQ* Root Port Endpoint	 I O	47kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Clock Request for PCIE0_CLK:** Connect to **CLKREQ** pins on device or connectors. If the module is configured as an Endpoint, include isolation between the clock request pin on the module and the device/connector. One isolator should have the output to the module and be powered by the 3.3V rail on the module. The other isolator should have the output pointing at the connector or device and be powered by the 3.3V rail at the connector or device. These isolate the on-module pull-up resistors as well as ensures the pins on both the Root Port and Endpoint sides will not be driven high before the associated power is enabled.
PCIE0_RST* Root Port Endpoint	 O I	4.7kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Reset:** Connect to **PERST** pins on device/connector(s). If the module is configured as an Endpoint, include a isolator between the reset pin on the module and the device/connector powered by the 3.3V rail at the connector or device. The isolator should have the output toward the module. This isolates the on-module pull-up resistor as well as ensures this signal will not be pulled or driven high before the module is powered on.
PCIe Interface 1 (x1 – Controller #1, Root Port only)			
PCIE1_TX0_N/P	DIFF OUT	Series 0.22uF Capacitor	**Differential Transmit Data Pair:** Connect to TX_N/P pins of PCIe connector or RX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE1_RX0_N/P	DIFF IN	Series 0.22uF capacitors near Orin Module pins or device if device on main PCB.	**Differential Receive Data Pair:** Connect to RX_N/P pins of PCIe connector or TX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE1_CLK_N/P	DIFF OUT		**Differential Reference Clock Output:** Connect to REFCLK_N/P pins **of PCIe device/connector**
PCIE1_CLKREQ*	I/O	47kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Clock Request for PCIE1_CLK:** Connect to **CLKREQ** pins on device/connector(s)
PCIE1_RST*	O	4.7kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Reset:** Connect to **PERST** pins on device/connector(s)
PCIe Interface 2 (x1 or x2 – Controller #7. Root Port only)			
CSI4_D3_N/P (PCIE2_TX1_N/P) CSI4_D0_N/P (PCIE2_TX0_N/P)	DIFF OUT	Series 0.22uF Capacitor	**Differential Transmit Data Pair:** Connect to TX_N/P pins of PCIe connector or RX_N/P pin of PCIe device through AC cap according to supported configuration.
CSI4_D1_N/P (PCIE2_RX1_N/P) CSI4_D2_N/P (PCIE2_RX0_N/P)	DIFF IN	Series 0.22uF capacitors near module pins or device if device on main PCB.	**Differential Receive Data Pair:** Connect to RX_N/P pins of PCIe connector or TX_N/P pin of PCIe device through AC cap according to supported configuration.

Module Pin Name (Function)	Type	Termination	Description
CSI4_CLK_N/P (PCIE2_CLK_N/P)	DIFF OUT		**Differential Reference Clock Output:** Connect to REFCLK_N/P pins **of PCIe device/connector**
SDMMC_DAT1 (PCIE2_CLKREQ*)	I/O	47kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Clock Request for PCIE1_CLK:** Connect to **CLKREQ** pins on device/connector(s)
SDMMC_DAT0 (PCIE2_RST*)	O	4.7kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Reset:** Connect to **PERST** pins on device/connector(s)
PCIe Interface 3 (x1 – Controller #9. Available if PCIe IF #2 is used as x1 only. Supports Root Port only)			
CSI4_D3_N/P (PCIE3_TX0_N/P)	DIFF OUT	Series 0.22uF Capacitor	**Differential Transmit Data Pair:** Connect to TX_N/P pins of PCIe connector or RX_N/P pin of PCIe device through AC cap according to supported configuration.
CSI4_D1_N/P (PCIE3_RX0_N/P)	DIFF IN	Series 0.22uF capacitors near module pins or device if device on main PCB.	**Differential Receive Data Pair:** Connect to RX_N/P pins of PCIe connector or TX_N/P pin of PCIe device through AC cap according to supported configuration.
SDMMC_CMD (PCIE3_CLK_N) SDMMC_CLK (PCIE3_CLK_P)	DIFF OUT		**Differential Reference Clock Output:** Connect to REFCLK_N/P pins **of PCIe device/connector**
SDMMC_DAT3 (PCIE3_CLKREQ*)	I/O	47kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Clock Request for PCIE1_CLK:** Connect to **CLKREQ** pins on device/connector(s)
SDMMC_DAT2 (PCIE3_RST*)	O	4.7kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Reset:** Connect to **PERST** pins on device/connector(s)
Common			
PCIE_WAKE*	I	47kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Wake:** Connect to **WAKE** pins on device or connector. If the module is configured as an Endpoint, include a isolator between the wake pin on the module and the device/connector powered by the 3.3V rail at the connector or device. The isolator should have the output toward the connector or device. This isolates the on-module pull-up resistors as well as ensures this signal will not be pulled or driven high before the Root Port is powered on.

Chapter 8. Gigabit Ethernet

Orin module integrates a Gigabit Ethernet PHY. The magnetics and RJ45 connector are implemented on the carrier board.

Table 8-1. Orin Module Gigabit Ethernet Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
194	GBE_LED_ACT	–	Ethernet Activity LED (Yellow)	LAN	Output	
188	GBE_LED_LINK	–	Ethernet Link LED (Green)		Output	
184	GBE_MDI0_N	–	GbE Transformer Data 0		Bidir	MDI
186	GBE_MDI0_P	–				
190	GBE_MDI1_N	–	GbE Transformer Data 1			
192	GBE_MDI1_P	–				
196	GBE_MDI2_N	–	GbE Transformer Data 2			
198	GBE_MDI2_P	–				
202	GBE_MDI3_N	–	GbE Transformer Data 3			
204	GBE_MDI3_P	–				

Notes: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Figure 8-1. Orin Module Ethernet Connections

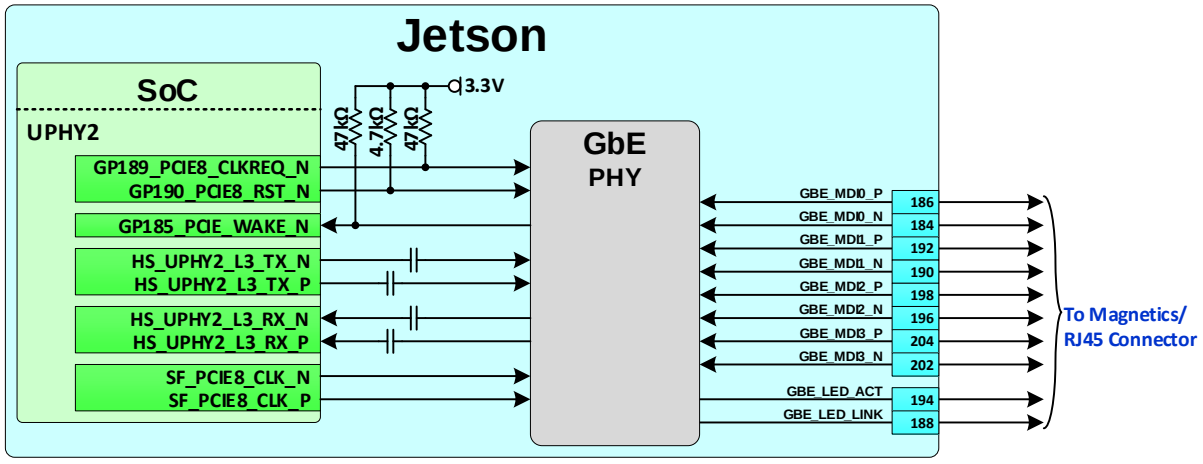
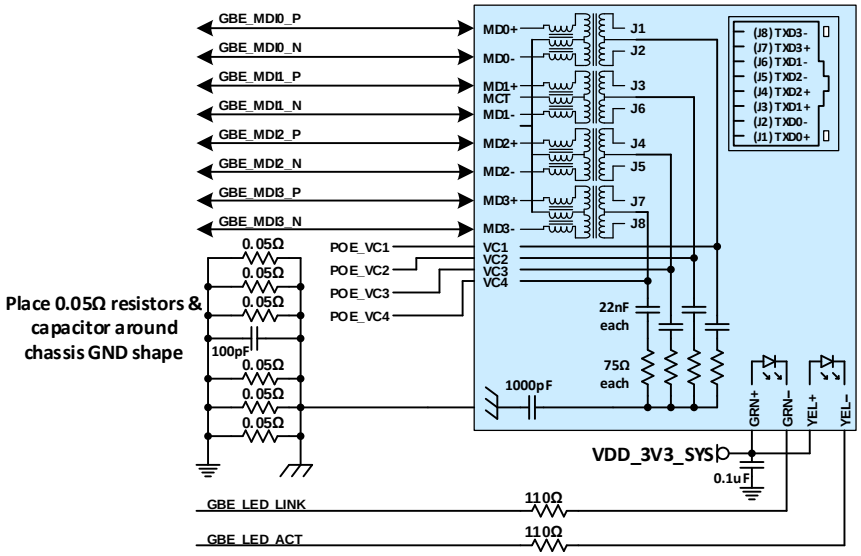


Figure 8-2. Gigabit Ethernet Magnetics and RJ45 Connections



8.1.1 Ethernet MDI Routing Guidelines

The following tables describes the ethernet signal routing requirements and connections.

Table 8-2. Ethernet MDI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND		
Trace impedance (Diff pair / Single Ended)	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min trace spacing (pair-pair)	0.763	mm	
Max trace length/delay	109 (690)	mm (ps)	
Max within pair (intra-pair) skew	0.15 (1)	mm (ps)	
Max pair to pair (inter-pair skew)	0.22 (1.5)	mm (ps)	
Number of vias	minimum		Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.

Notes: NVIDIA Orin does not support delay or skewing of clock vs. data. This must be enabled in the PHY.

Table 8-3. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
GBE_MDI[3:0]_N/P	DIFF I/O		Gigabit Ethernet MDI IF Pairs: Connect to Magnetics -/+ pins
GBE_LED_LINK	O	110Ω (minimum) series resistor	Gigabit Ethernet Link LED: Connect to green LED cathode on RJ45 connector. Anode connected to VDD_3V3_SYS
GBE_LED_ACT	O	110Ω (minimum) series resistor	Gigabit Ethernet Activity LED: Connect to yellow LED cathode on RJ45 connector. Anode connected to VDD_3V3_SYS

Chapter 9. Display

Orin module designs can select from either VESA® Embedded DisplayPort® (eDP) for embedded displays, and HDMI™ or DisplayPort (DP) for external displays. Only one interface is available. However, DisplayPort does support multi-head display through MST.

Table 9-1. Orin Module eDP, DP, and HDMI Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
98	DP1_AUX_N	SF_DPAUX01_N	Display Port 1 Aux– or HDMI DDC SDA	HDMI Connector	Bidir	DP_AUX (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)
100	DP1_AUX_P	SF_DPAUX01_P	Display Port 1 Aux+ or HDMI DDC SCL			
63	DP1_TXD0_N	HS_DISP0_HDMI_D2_DP0_N	DisplayPort 1 Lane 0 or HDMI Lane 2		Output	HDMI / DP
65	DP1_TXD0_P	HS_DISP0_HDMI_D2_DP0_P				
69	DP1_TXD1_N	HS_DISP0_HDMI_D1_DP1_N	DisplayPort 1 or HDMI Lane 1			
71	DP1_TXD1_P	HS_DISP0_HDMI_D1_DP1_P				
75	DP1_TXD2_N	HS_DISP0_HDMI_D0_DP2_N	DisplayPort 1 Lane 2 or HDMI Lane 0			
77	DP1_TXD2_P	HS_DISP0_HDMI_D0_DP2_P				
81	DP1_TXD3_N	HS_DISP0_HDMI_CK_DP3_N	DisplayPort 1 Lane 3 or HDMI Clk Lane			
83	DP1_TXD3_P	HS_DISP0_HDMI_CK_DP3_P				
96	DP1_HPD	GP74_HPD0_N	Display Port 1 or HDMI Hot Plug Detect. Must be active high for DP. For HDMI, the polarity can be changed in SW.		Input	CMOS – 1.8V
94	HDMI_CEC	GP05_HDMI_CEC	HDMI CEC		Bidir	Open Drain, 3.3V

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction shown in this table for DP_AUX_CH[1:0]_HPD is true when used for Hot-plug Detect. Otherwise, if used as GPIOs, the direction is bidirectional.

A standard DP 1.4 or HDMI v2.0 interface is supported. These share the same set of interface pins. Therefore, either DisplayPort or HDMI can be supported natively.

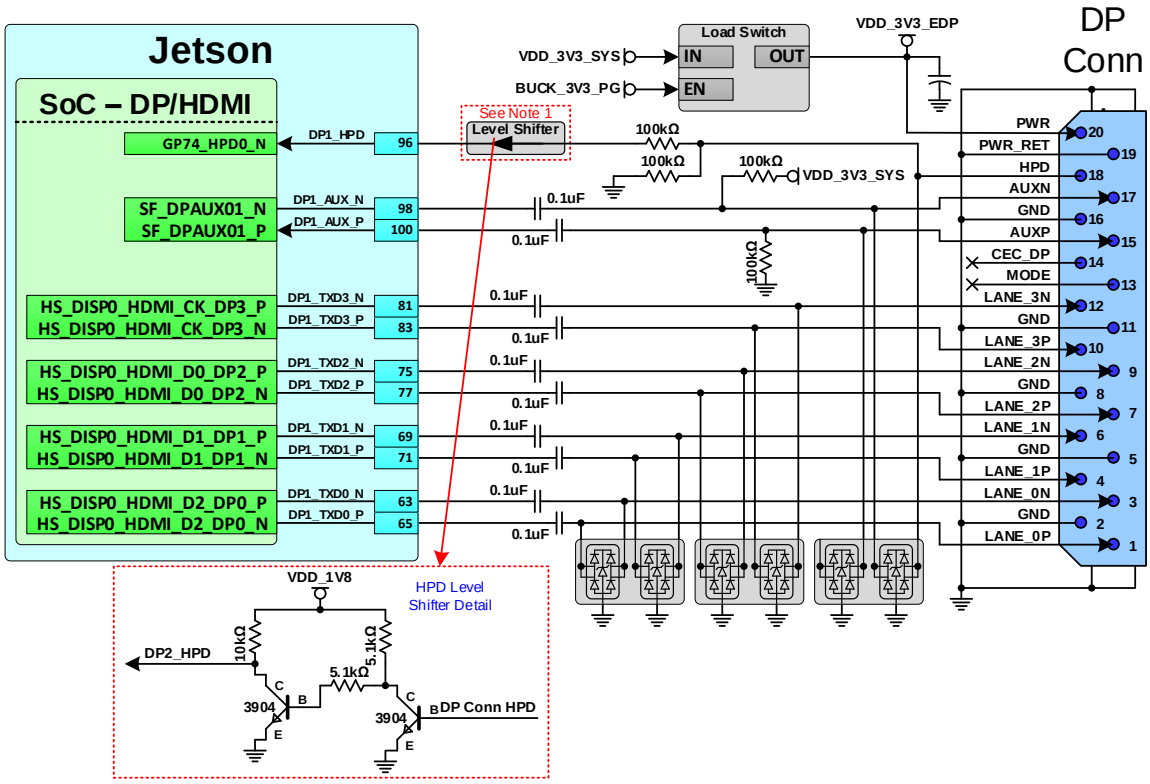
Table 9-2. DP and HDMI Pin Mapping

Module Pin Name	Module Pin #s	HDMI	DP
DP1_TXD3_P DP1_TXD3_N	83 81	TXC+ TXC –	TX3+ TX3–
DP1_TXD2_P DP1_TXD2_N	77 75	TX0+ TX0–	TX2+ TX2–
DP1_TXD1_P DP1_TXD1_N	71 69	TX1+ TX1–	TX1+ TX1–
DP1_TXD0_P DP1_TXD0_N	65 63	TX2+ TX2–	TX0+ TX0–

9.1 eDP and DP

The following figure shows a basic the DP and eDP connection example.

Figure 9-1. DP and eDP Connection Example



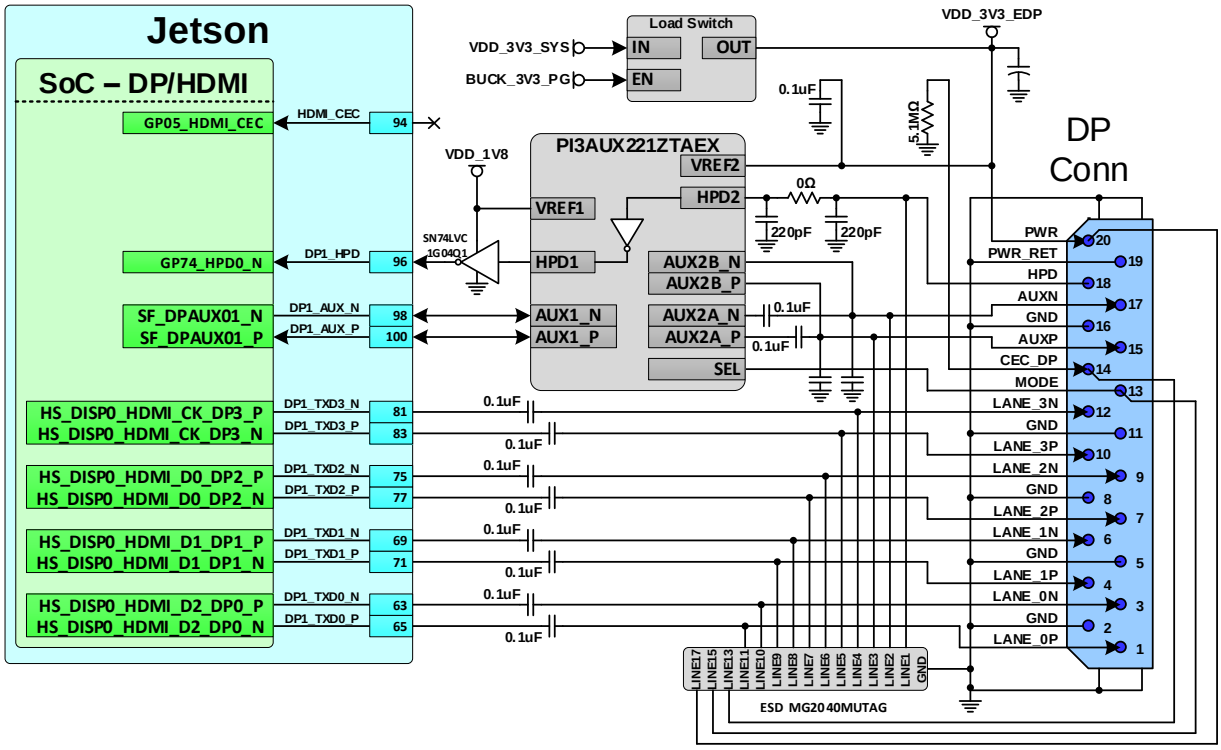
Notes:

1. Level shifter required on DP0_HPD to avoid the pin from being driven when Orin module is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display). See the HPD level shifter detail block in the figure above.

2. Load Switch enable is from power-good pin of main 3.3V supply.

The following figure shows an example of a DP++ connection.

Figure 9-2. DP++ Connection Example



9.1.1 eDP and DP Routing Guidelines

The following routing requirements meet the eDP and DP routing guidelines.

Figure 9-3. eDP and DP Differential Main Link Topology

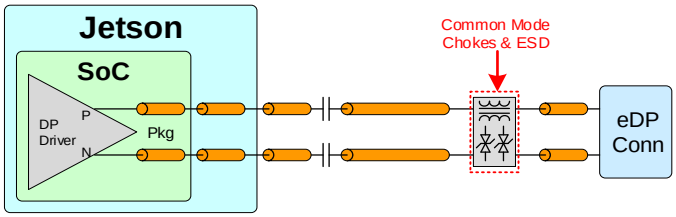
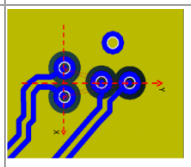
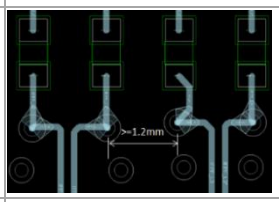


Table 9-3. eDP and DP Main Link Signal Requirements Including DP_AUX

Parameter	Requirement	Units	Notes
Specification			
Max Data Rate / Min UI HBR3 HBR2 HBR RBR	 8.1 / 123 5.4 / 185 2.7 / 370 1.62 / 617	 Gbps / ps	Per data lane
Number of Loads / Topology	1	load	Point-Point, Differential, Unidirectional
Termination	100	Ω	On die at TX/RX
Electrical Specification			
Insertion Loss E-HBR @ 0.675GHz PBR 0.68GHz HBR 1.35GHz HBR2 @ 2.7GHz HBR3 @ 4.05GHz	 <=0.7 <=0.7 <=1.2 <=4.5 <=5.5	 dB	
Resonance dip frequency HBR2 HBR3	 >8 >12	 GHz	
TDR dip	>85	Ω	@ Tr-200ps (10%-90%)
FEXT @ DC @ 2.7GHz @ 5.4GHz	 <= -40dB <= -30dB <= -30dB	IL/FEXT plot – up to HBR2. See Figure 9-4. IL/FEXT plot – HBR3. See Figure 9-5.	
Impedance			
Trace Impedance (Diff pair)	100 90 85	Ω (±10%)	100Ω is the spec. target. 95/85Ω are implementation options (Zdiff does not account for trace coupling) 95Ω should be used to support DP-HDMI co-layout as HDMI 2.0 requires 100Ω impedance (see HDMI section for addition of series resistor Rs). 85Ω can be used if eDP/DP only and is preferable as it provides better trace loss characteristic performance. See Note 1.
Reference Plane	**GND**		
Trace Length (delay), Spacing and Skew			
Trace loss characteristic HBR2 or lower (@ 2.7GHz) HBR3 (@4GHz)	 < 0.64 <=0.9	 dB/in	The following max length (delay) is derived based on this characteristic. The length (delay) constraint must be re-defined if loss characteristic is changed.
Max PCB Via dist. from module conn. **RBR/HBR** **HBR2 and HBR3**	 No requirement 7.62	 mm	
Max trace length (delay) from module to connector **RBR/HBR** Stripline Microstrip **HBR2** Stripline Microstrip **HBR3**	 215 (1137.5) 215 (975) 184 (1260) 178 (1050)	 mm (ps)	6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.

Parameter	Requirement	Units	Notes
Stripline Microstrip	162 (1120) 155 (900)		
Trace spacing (Pair-Pair) Stripline Microstrip (**HBR/RBR**) Microstrip (**HBR2/HBR3**)	 3x 4x 5x to 7x	 dielectric height	
Trace spacing (Main Link to AUX): Stripline/Microstrip	3x / 5x	dielectric height	
Max Intra-pair (within pair) Skew	0.15 (1)	mm (ps)	Do not perform length (delay) matching within breakout region. Do trace length (delay) matching before hitting discontinuity (i.e. matching to <1ps before the vias or any discontinuity to minimize common mode conversion).
Max Inter-pair (pair-pair) Skew	150	ps	
Via			
Max GND transition Via distance	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical GND stitching Via near signal Vias.
Impedance dip Recommended via dimension for impedance control Drill/Pad Antipad Via pitch	≥97 ≥92 200/400 >840 ≥880	Ω @ 200ps Ω @ 35ps um um um	The via dimension must be required for the HDMI-DP co-layout condition.
Topology	Y-pattern is recommended keep symmetry Xtalk suppression is best using the Y-pattern. It can also reduce the limit of pair-pair distance.		
	For in-line via, the distance from a via of one lane to the adjacent via from another lane >= 1.2 mm center-center.		
GND via	Place GND via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Max # of Vias PTH vias Micro Vias	 4 if all vias are PTH via Not limited if total channel loss meets IL spec		
Max Via Stub Length	0.4	mm	
AC Cap			
Value	0.1	uF	Discrete 0402
Max Dist. from AC cap to connector RBR/HBR HBR2/HBR3	 No requirement 0.5	 in	

Parameter	Requirement	Units	Notes
Voiding RBR/HBR HBR2/HBR3	 No requirement Voiding required		**HBR2**: Voiding the plane directly under the pad ~0.1mm larger than the pad size is recommended.
Serpentine (See USB 3.2 Guidelines)			
Connector			
Voiding RBR/HBR HBR2/HBR3	 No requirement Voiding required		HBR2: Standard DP Connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7 mil larger than the connector pad.
General			
Keep critical PCIe traces away from other signal traces or unrelated power traces/areas or power supply components			

Notes:

1. For eDP and DP, the specification puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85 Ω for impedance, it is important to make sure the selected stack-up, material and trace dimension can achieve the needed low loss characteristic.
2. The average of the differential signals is used for length and delay matching.
3. Do not perform length and delay matching within breakout region. Recommend doing trace length and delay matching to <1ps before vias or any discontinuity to minimize common mode conversion.

The following figures show the eDP and DP interface signal routing requirements.

Figure 9-4. S-Parameter Up to HBR2

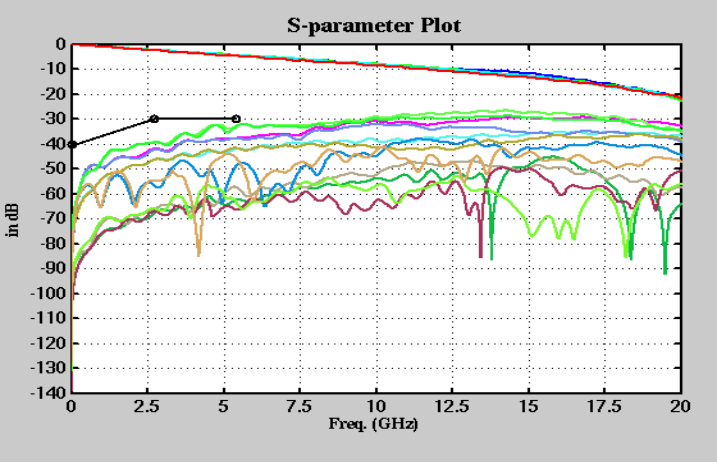


Figure 9-5. S-Parameter Up to HBR3

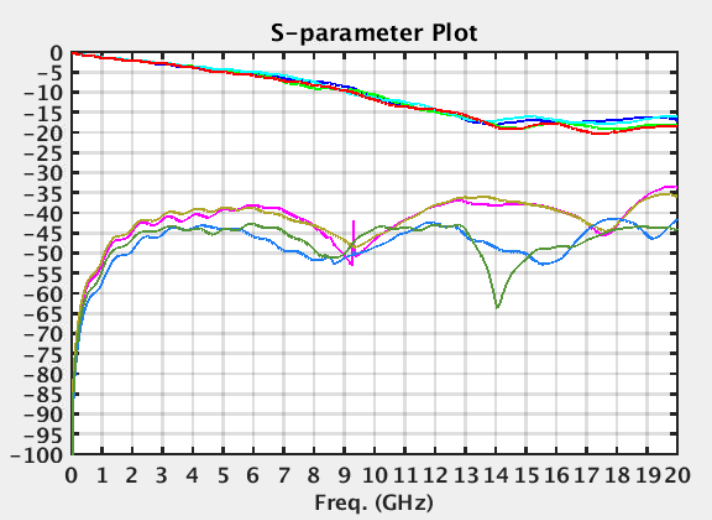


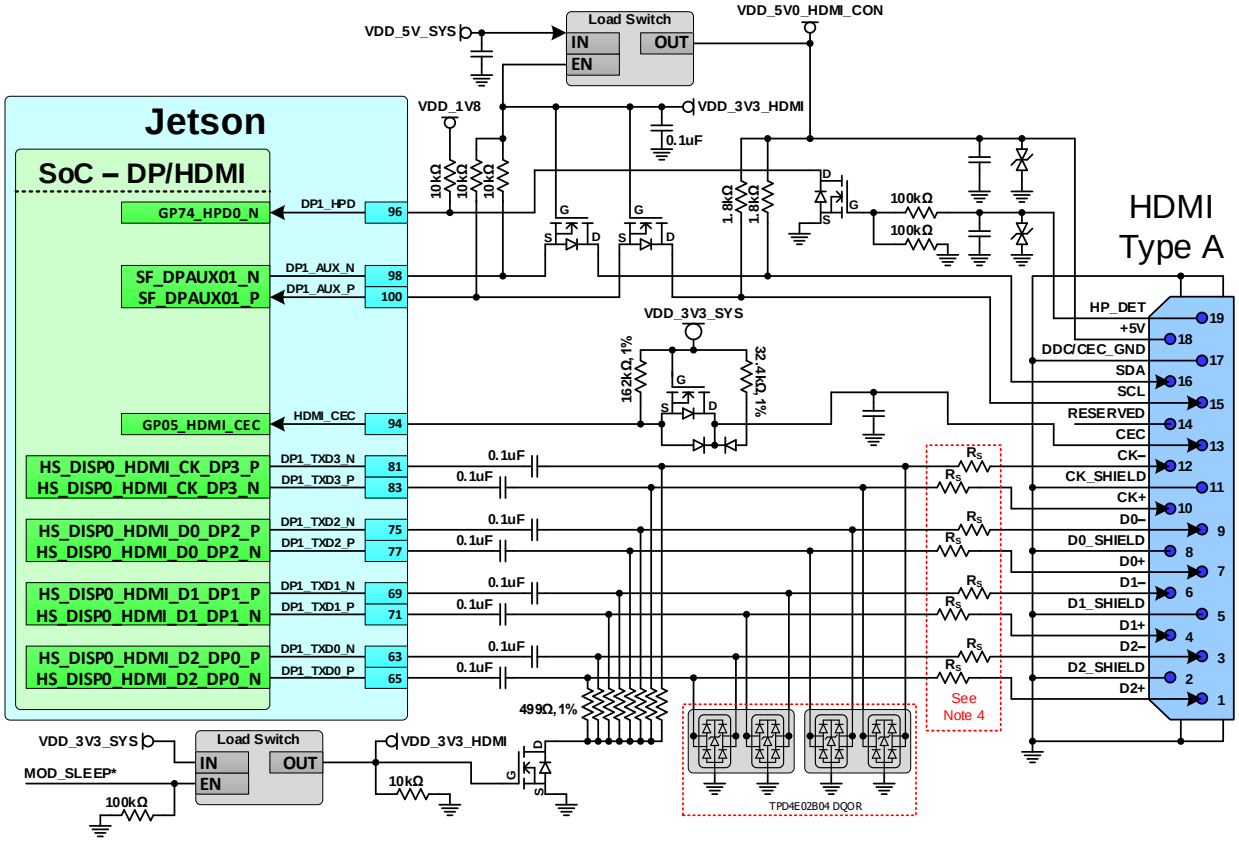
Table 9-4. eDP and DP Signal Connections

Module Pin Name	Type	Termination	Description
DP1_TXD[3:0]_N/P	O	Series 0.1uF capacitors and ESD to **GND** on all.	eDP/DP Differential CLK/Data Lanes: Connect to matching pins on display connector.
DP1_AUX_N/P	I/OD	Series 0.1uF capacitors DP1_AUX_CH_P pulled to GND through 100kΩ resistor. DP1_AUX_CH_N pulled to VDD_3V3_DP through 100kΩ resistor.	eDP/DP: Auxiliary Channels: Connect to **AUX_CH**-/+ on display connector.
DP1_HPD	I	100kΩ series resistor and 100kΩ resistor to GND then Level shifter (non-inverting) between connector and module pin.	eDP/DP: Hot Plug Detect: Connect to **HPD** pin on display connector through level shifter.

9.2 HDMI

A standard DP 1.4 or HDMI v2.1 interface is supported. See Figure 9-6 for more details.

Figure 9-6. HDMI Connection Example



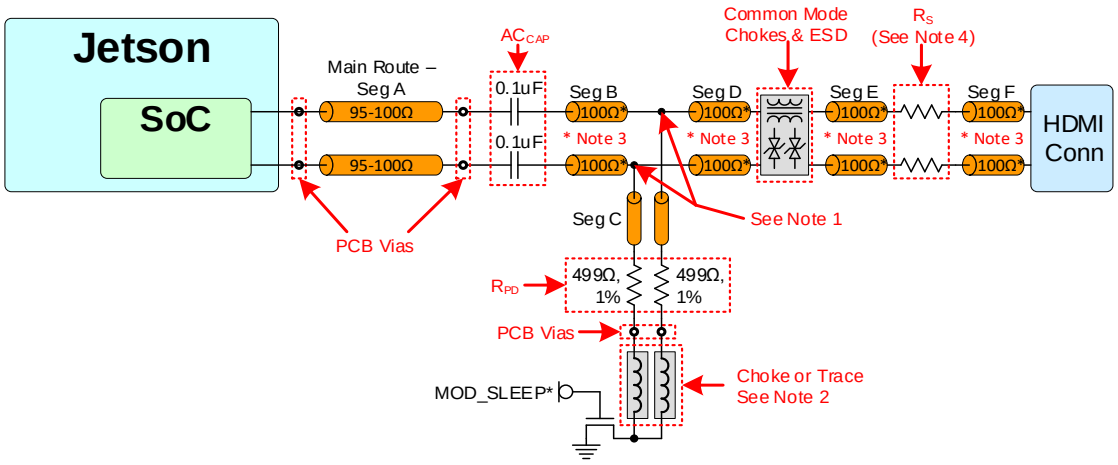
Notes:

1. Level shifters required on DDC/HPD. NVIDIA Orin pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting. The HPD level shifter in the reference design is inverting. The reference design uses a BJT level shifter, and a resistor divider is needed. See the reference design if a similar approach will be used.
2. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the HDMI specification for the modes to be supported. See requirements and recommendations in the related sections of the "HDMI Interface Signal Routing Requirements" table (Table 9-5).
3. The DP1_TXx pads are native DP pads and require series AC capacitors (ACCAP) and pull-downs (RPD) to be HDMI compliant. The 499 Ω, 1% pull-downs must be disabled when Orin module is off or in sleep mode to meet the HDMI VOFF requirement. The enable to the FET, enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
4. See the RS section in Table 9-5 for details.

9.2.1 HDMI Routing Guidelines

This section describes the HDMI routing guidelines for the Orin module.

Figure 9-7. HDMI CLK and Data Topology

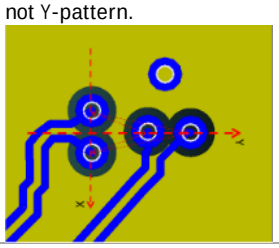
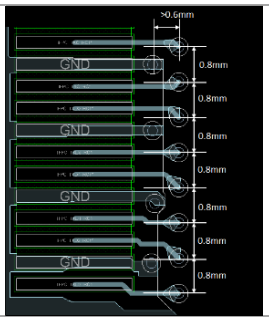
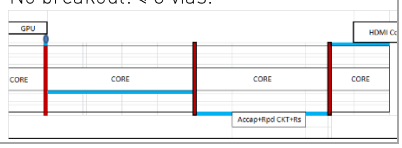


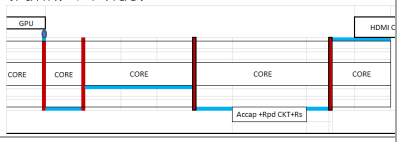
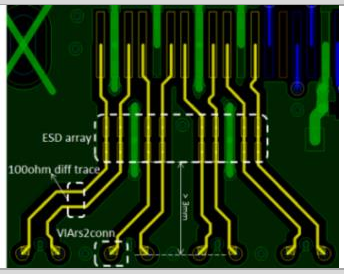
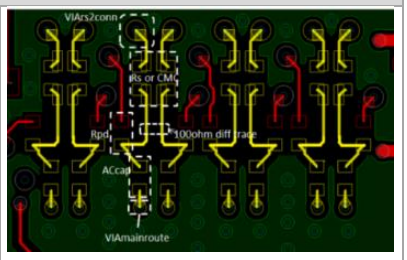
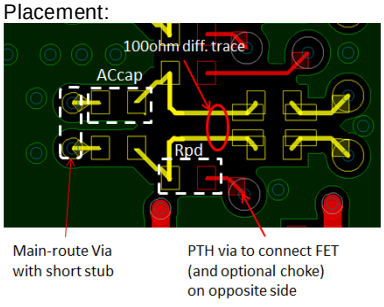
Notes:

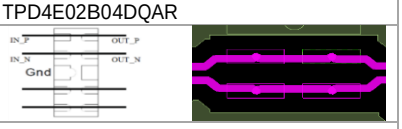
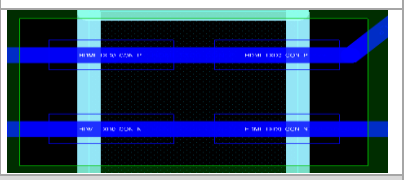
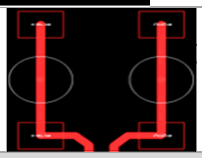
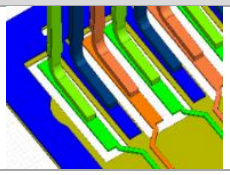
1. RPD pad must be on the main trace. RPD and ACCAP must be on same layer.
2. Chokes (600 Ω @ 100 MHz) or narrow traces (1 uH @ DC-100 MHz) between pull-downs and FET are chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
3. The trace after the main route via should be routed on the top or bottom layer of the PCB, and either with 100 ohm differential impedance, or as uncoupled 50 ohm SE traces.
4. See the RS section in Table 9-5 for details.

Table 9-5. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Electrical Specification			
IL Resonance dip frequency	<= 1.7 <= 2 <= 3 < 4.3 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	For HDMI 2.0, 6 dB and 6 GHz is supported.
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85 ohm that dip width should < 250 ps
FEXT	<= -50 <= -40 <= -40	dB at DC dB at 3GHz dB at 6GHz	
	IL/FEXT plot: See HDMI Guideline Figure 9-8		TDR plot: See Figure 9-9
Impedance			
Trace impedance: Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout and main route is an implementation option.
Reference plane	**GND**		
Trace spacing/Length/Skew			

Parameter	Requirement	Units	Notes
Trace loss characteristic:	< 1.1 < 0.8 < 0.4	dB/in. @ 6GHz dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length (delay) is derived based on this characteristic. The length (delay) constraint must be re-defined if the loss characteristic is changed. See Note 1.
Min Trace spacing (Pair-Pair) Stripline: 2.1 Stripline: 1.4b/2.0 Microstrip: 2.1 Microstrip: 1.4b/2.0	 4x 3x 7x 5x to 7x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Trace spacing (Main link to DDC) Stripline Microstrip	 3x 5x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Max Total Delay (2.1) Stripline (4x spacing) Microstrip (7x spacing)	 76 (535) 63.5 (375)	mm (ps)	Propagation delay: 6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.
Max Total Delay (1.4b/2.0) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 101 (700) 88.5 (525) 101 (600)	mm (ps)	Propagation delay: 6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See notes 1, 2, and 3
Max inter-pair (pair to pair) skew	150	ps	See notes 1, 2, and 3
Max **GND** transition via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	- Y-pattern is recommended - keep symmetry		Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern.
Minimum impedance dip	97 92	Ω@200ps Ω@35ps	
Recommended via dimension drill/pad Antipad via pitch	 200/400 840 880	uM	
GND via	Place **GND** via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single **GND** return via		**GND** via is used to maintain return path, while its Xtalk suppression is limited
Connector pin via	The break-in trace to the connector pin via should be routed on the BOTTOM in order to avoid via stub effect Equal spacing (0.8mm) between adjacent signal vias. The x-axis distance between signal and GND via should be > 0.6mm		
Max # of vias PTH via u-via	2 if all vias are PTH via Not limited if total channel loss meets IL spec.		No breakout: ≤ 3 vias: 

Parameter	Requirement	Units	Notes
			Breakout on the same layer as main trunk: ≤ 4 vias: 
Max via stub length	0.4	mm	long via stub requires review (IL and resonance dip check)
Topology			
The main route via dimensions should comply with the via structure rules (See via section)			See topology in Figure 9-7
For the connector pin vias, follow the rules for the connector pin vias (See via section)			
The traces after main route via should be routed as 100Ω differential or as uncoupled 50ohm SE traces on PCB top or bottom.			
Max distance from R_{PD} to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	
Add-on Components			
Example of a case where space is limited for placing components.			
AC Cap			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-via design	Place cap on bottom layer if main route above core Place cap on top layer if main route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		
Pull-down Resistor (R_{PD}), choke/FET			
Value	500	Ω	
Location.	Must be placed after AC cap		Placement:
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer thru a PTH via		

Parameter	Requirement	Units	Notes
Choke between R_{PD} and FET choke Max trace Rdc Max trace length	 600 or 1 ⩽20 4	 ΩΩ100MHz uH@DC-100MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	**GND**/**PWR** void under/above cap is preferred		
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues) See Chapter 17 for details on CMC if implemented**.**			
ESD (On-chip protection diode can withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to **GND**)	0.35	pF	e.g. Texas Instruments TPD4E02B04DQAR
Footprint	Pad right on the net instead of trace stub		
Location	After pull-down resistor/CMC and before R_S		
Void	**GND**/**PWR** void under/above the cap is needed. Void size = 1 mm x 2 mm for one pair		
Series Resistor (RS): Series resistor on P/N path for HDMI 2.0 but not required for HDMI 2.1 (Mandatory to meet HDMI 2.0 Compliance).			
Value	⩽ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the R_S value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	**GND**/**PWR** void under/above the R_S device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Trace at Component Region			
Value	100	Ω	± 10%
Location	At component region (Microstrip)		
Trace entering the SMT pad	One 45°		
Trace between components	Uncoupled structure		
HDMI connector			
Connector voiding	Voiding the ground below the signal lanes 0.1448 (5.7 mil) larger than the pin itself		

Parameter	Requirement	Units	Notes
General: See Chapter 17 for guidelines related to Serpentine routing, routing over voids and noise coupling			

Notes:

1. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
2. The average of the differential signals is used for length matching.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion
4. If routing includes a flex or 2nd PCB, the max trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

The following figures show the HDMI interface signal routing requirements.

Figure 9-8. IL/FEXT Plot

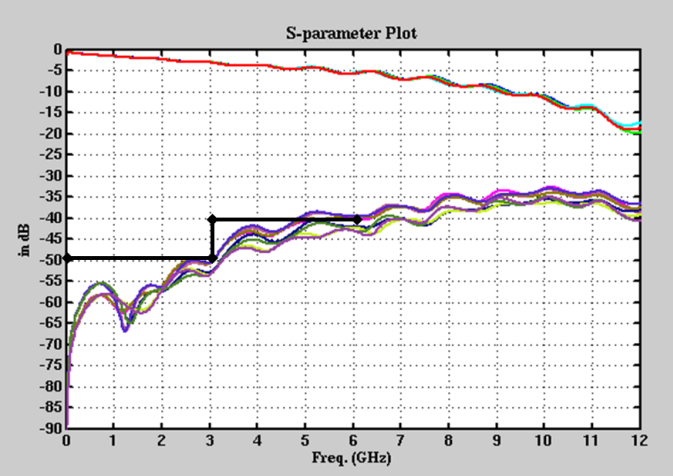


Figure 9-9. TDR Plot

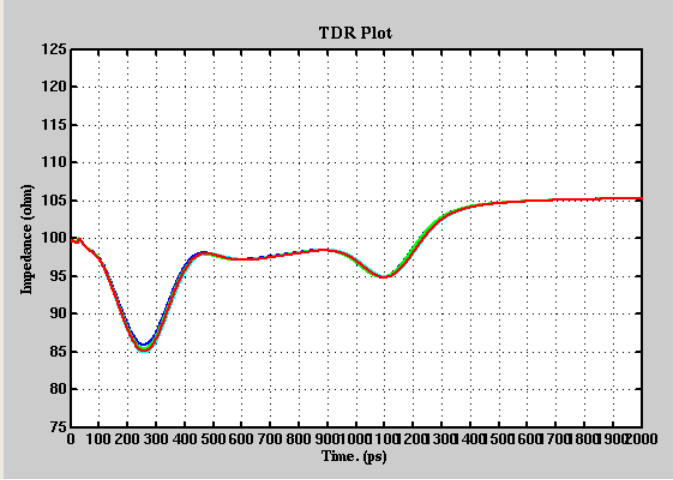


Table 9-6. HDMI Signal Connections

Module Pin Name	Type	Termination (see note on ESD)	Description
DP1_TXD3_N/P	DIFF OUT	0.1uF series AC_{CAP} → 500Ω R_{PD} (controlled by FET) → ESD to **GND** →.≤6Ω Rs (series resistor)	HDMI Differential Clock: Connect to **C–/C+** and pins on HDMI connector
DP1_TXD[2:0]_N/P	DIFF OUT		HDMI Differential Data: Connect to HDMI Data pins (Table 9-2)
DP1_HPD	I	From module pin: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to **GND** on connector side → 100pF/12pF caps to **GND** → ESD to **GND**.	HDMI Hot Plug Detect: Connect to **HPD** pin on HDMI connector
HDMI_CEC	I/OD	Gating circuitry, See connection figure for details.	HDMI Consumer Electronics Control: Connect to CEC on HDMI connector through circuitry.
DP1_AUX_N/P	I/OD	From module pins: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → ESD to **GND.** See connection figure for level shifter details.	HDMI: DDC Interface – **Clock and Data**: Connect **DP1_AUX_N** to **SDA** and **DP1_AUX_P** to **SCL** on HDMI connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector and ESD to **GND**.	HDMI 5V supply to connector: Connect to +5V on HDMI connector.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

Chapter 10. MIPI CSI Video Input

Orin Module brings eight MIPI CSI lanes to the connector. Up to two quad-lane camera streams or up to four dual-lane camera streams are supported. Each data lane has a peak bandwidth of up to 2.5 Gbps.

Table 10-1. Orin Module CSI Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
10	CSI0_CLK_N	HS_CSI0_CLK_N	Camera, CSI 0 Clock	2-lane Camera #1, 4-lane Camera #1 (lower 2 lanes)	Input	MIPI D-PHY
12	CSI0_CLK_P	HS_CSI0_CLK_P				
4	CSI0_D0_N	HS_CSI0_D0_N	Camera, CSI 0 Data 0			
6	CSI0_D0_P	HS_CSI0_D0_P				
16	CSI0_D1_N	HS_CSI0_D1_P	Camera, CSI 0 Data 1			
18	CSI0_D1_P	HS_CSI0_D1_N				
9	CSI1_CLK_N	HS_CSI1_CLK_N	Camera, CSI 1 Clock	2-lane Camera #2, 4-lane Camera #1 (upper 2 lanes)		
11	CSI1_CLK_P	HS_CSI1_CLK_P				
3	CSI1_D0_N	HS_CSI1_D0_P	Camera, CSI 1 Data 0			
5	CSI1_D0_P	HS_CSI1_D0_N				
15	CSI1_D1_N	HS_CSI1_D1_N	Camera, CSI 1 Data 1			
17	CSI1_D1_P	HS_CSI1_D1_P				
28	CSI2_CLK_N	HS_CSI2_CLK_N	Camera, CSI 2 Clock	2-lane Camera #3, 4-lane Camera #2 (lower 2 lanes)		
30	CSI2_CLK_P	HS_CSI2_CLK_P				
22	CSI2_D0_N	HS_CSI2_D0_N	Camera, CSI 2 Data 0			
24	CSI2_D0_P	HS_CSI2_D0_P				
34	CSI2_D1_N	HS_CSI2_D1_N	Camera, CSI 2 Data 1			
36	CSI2_D1_P	HS_CSI2_D1_P				
27	CSI3_CLK_N	HS_CSI3_CLK_N	Camera, CSI 3 Clock	2-lane Camera #4, 4-lane Camera #2 (upper 2 lanes)		
29	CSI3_CLK_P	HS_CSI3_CLK_P				
21	CSI3_D0_N	HS_CSI3_D0_N	Camera, CSI 3 Data 0			
23	CSI3_D0_P	HS_CSI3_D0_P				
33	CSI3_D1_N	HS_CSI3_D1_N	Camera, CSI 3 Data 1			
35	CSI3_D1_P	HS_CSI3_D1_P				

Notes: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

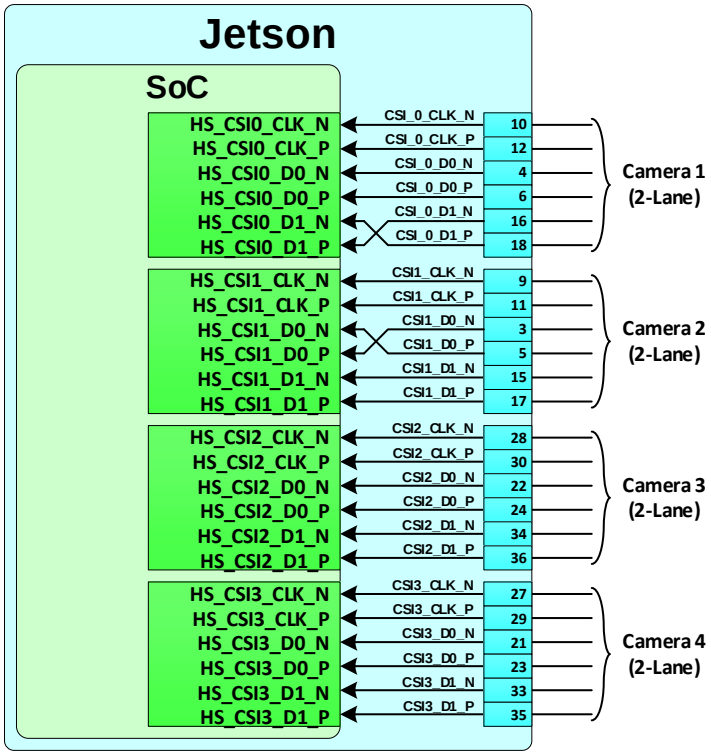
Table 10-2. Orin Module Camera Miscellaneous Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
213	CAM_I2C_SCL	GP54_I2C3_CLK	Camera I2C. 2.2 kΩ pull-up to 3.3V on the module.	Cameras (shared)	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	GP55_I2C3_DAT				
116	CAM0_MCLK	GP52_CLK1	Camera 0 Reference Clock	Camera #1	Output	CMOS – 1.8V
114	CAM0_PWDN	GP121_UART4_CTS_N	Camera 0 Powerdown or GPIO			
122	CAM1_MCLK	GP53_CLK2	Camera 1 Reference Clock	Camera #2		
120	CAM1_PWDN	GP161_SPI5_CLK	Camera 1 Powerdown or GPIO			
118	GPIO01	GP65	GPIO #1 or Generic Clock Output #1	Camera #3	Output (note)	
216	GPIO11	GP66	GPIO #11 or Generic Clock Output #2	Camera #4		

Notes:

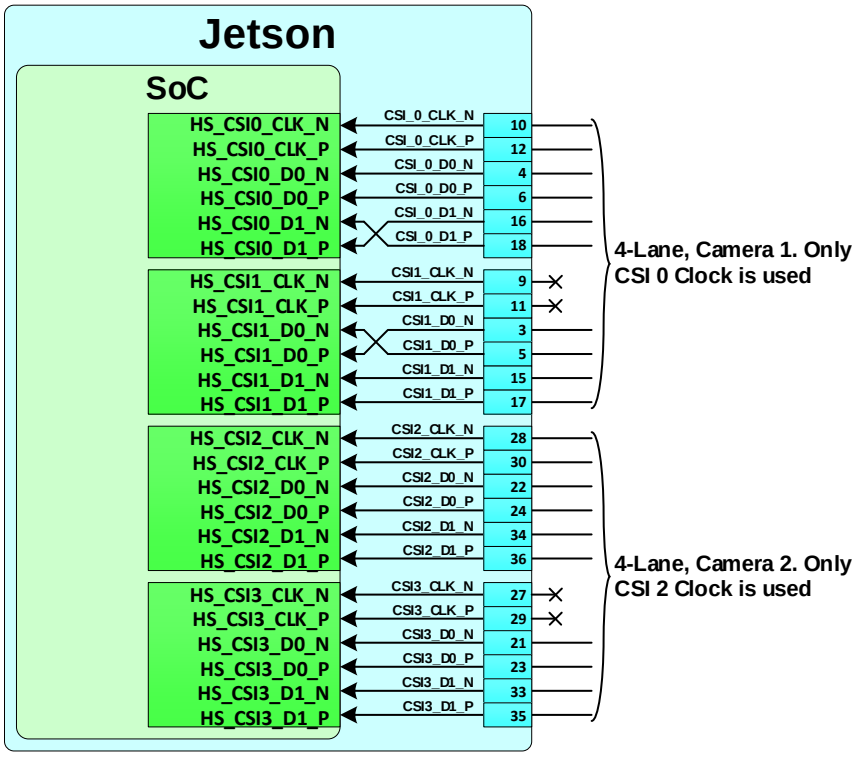
1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction shown in this table for CAM[1:0]_MCLK and CAM[1:0]_PWDN is true when used for those functions. These pins are GPIOs and can support input or output (bidirectional). The direction indicated for GPIO01 and GPIO11 is associated with their use as clock outputs.

Figure 10-1. CSI 2-Lane Connection Options



Note: CSI_0_D1 and CSI_1_D0 have P/N swapped on the module.

Figure 10-2. CSI 4-Lane Connection Options



Note: CSI_0_D1 and CSI_1_D0 have P/N swapped on the module.

Figure 10-3. Available Camera Control Pins

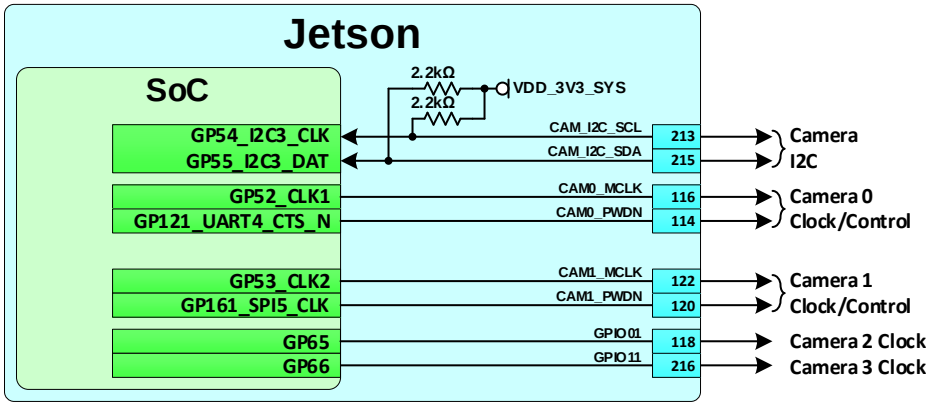


Table 10-3. CSI Configurations

Cameras	CSI0 CLK	CSI0 Data[1:0]	CSI1 CLK	CSI1 Data[1:0]	CSI2 CLK	CSI2 Data[1:0]	CSI3 CLK	CSI3 Data[1:0]
2-Lanes Each								
1 of 4 cameras	√	√						
2 of 4 cameras			√	√				
3 of 4 cameras					√	√		
4 of 4 cameras							√	√
4-Lanes Each								
1 of 2 cameras	√	√		√				
2 of 2 cameras					√	√		√

10.1 CSI Routing Guidelines

The following tables describe the routing guidelines for the CSI design.

Table 10-4. MIPI CSI D-PHY Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) for High-Speed mode Max Frequency (for Low Power mode)	2.5 10	Gbps MHz	
Number of loads	1	load	
Reference plane	GND		
Trace impedance: Diff pair / SE	90-100 / 45-50	Ω	±10%
Via proximity (signal to reference)	< 0.65 (3.8)	mm (ps)	
Intra-pair trace spacing	0.15mm	mm	Can be adjusted to meet Differential Impedance.
Trace spacing: Microstrip / Stripline	2x / 2x	dielectric	
Max PCB breakout delay	48	ps	
Max Insertion loss 1 Gbps 1.5 Gbps 2.5 Gbps	 3.00 2.90 1.92	 dB	
Max trace delay / length 1 Gbps (Stripline/Microstrip) 1.5 Gbps 2.5 Gbps	 2526 (421) / 2487 (421) 1913 (319) / 1885 (319) 900 (150) / 886 (150)	 ps (mm)	
Max intra-pair skew	1	ps	

Parameter	Requirement	Units	Notes
Max trace delay skew between DQ and CLK 1 / 1.5 / 2.5 Gbps	40 / 26.7 / 16	ps	**DQ** includes all the data lines associated with a single clock. This may be 2 differential data lanes for a x2 interface, or 4 differential data lanes for a x4 interface.
Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components			

Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

Table 10-5. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
CSI[3:0]_CLK_N/P Camera #[4:1]	I	See note	CSI Differential Clocks: Connect to clock pins of camera. See Table 10-3 for details
CSI[3:0]_D[1:0]_N/P Camera #[4:1]	I	See note	CSI Differential Data Lanes: Connect to data pins of camera. See Table 10-3 for details

Table 10-6. Miscellaneous Camera Connections

Module Pin Name	Type	Termination	Description
CAM_I2C_CLK CAM_I2C_DAT	O I/O	21.5 kΩ pull-ups VDD_3V3_SYS (on Orin module).	Camera I2C Interface: Connect to I2C SCL and SDA pins of imager.
CAM[1:0]_MCLK GPIO01 (opt. MCLK2) GPIO11 (opt. MCLK3)	O		Camera Initiator Clocks: Connect to camera reference clock inputs.
CAM[1:0]_PWDN	O		Camera Power Control signals (or GPIOs [1:0]): Connect to power down pins on camera(s).

Chapter 11. Audio

NVIDIA Orin supports multiple PCM and I2S audio interfaces. It also includes a flexible audio port switching architecture.

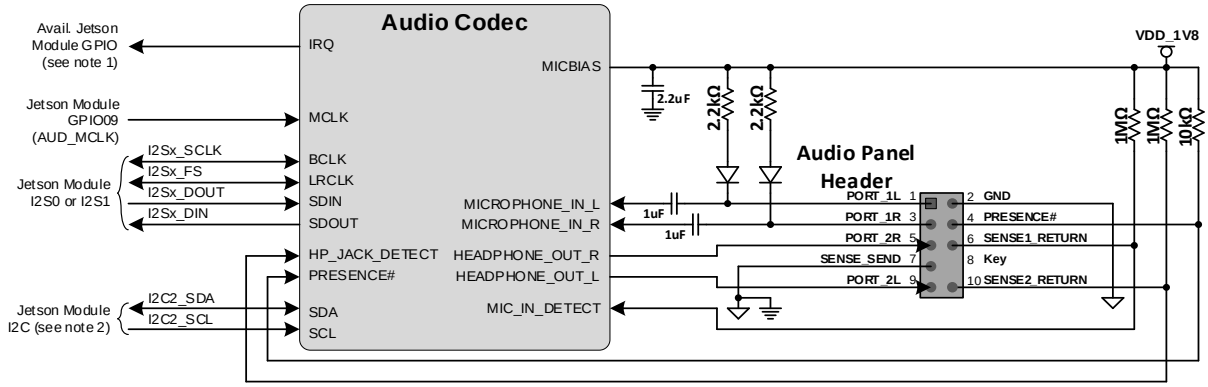
Table 11-1. Orin Module Audio Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage/Description	Recommended Usage	Direction	Pin Type
199	I2S0_SCLK	GP122	I2S Audio Port 0 Clock	Audio Device	Bidir	CMOS – 1.8V
197	I2S0_FS	GP125	I2S Audio Port 0 Left/Right Clock		Bidir	
193	I2S0_DOUT	GP123	I2S Audio Port 0 Data Out		Output (note)	
195	I2S0_DIN	GP124	I2S Audio Port 0 Data In		Input (note)	
226	I2S1_SCLK	GP206_DAP4_CLK	I2S Audio Port 1 Clock	Audio Device (i.e. M.2 Key E)	Bidir	
224	I2S1_FS	GP209_DAP4_FS	I2S Audio Port 1 Left/Right Clock		Bidir	
220	I2S1_DOUT	GP207_DAP4_DOUT	I2S Audio Port 1 Data Out		Output (note)	
222	I2S1_DIN	GP208_DAP4_DIN	I2S Audio Port 1 Data In		Input (note)	
211	GPIO09	GP167	GPIO #9 or Audio Codec Initiator Clock	Audio Device	Output (note)	

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction indicated for I2S[1:0]_DOUT and _DIN are associated with their use as I2S data lines. The direction for GPIO09 is associated with its use as Audio Initiator Clock. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 11-1. Audio Connection Example



Notes:

1. The Interrupt pin from the audio codec can connect to any available Orin module GPIO. If the pin must be wake-capable, choose one of the GPIOs that supports this function.
2. I2C2 supports 1.8V operation since the interface is pulled to 1.8V through 2.2 kΩ resistors on the module. If another I2C interface on Orin module is used, a level shifter will be required as all the others are 3.3V.
3. Refer to the Intel High Definition Audio/AC'97 website for the latest information: https://www.intel.com/content/www/us/en/support/articles/000005512/boards-and-kits/desktop-boards.html.

11.1.1 I2S Routing Guidelines

This section describes the I2S routing guidelines.

Table 11-2. I2S Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration and device organization	1	load	
Max loading	8	pF	
Reference plane	GND		
Breakout region impedance	Min width/spacing		
Trace impedance	50	Ω	±20%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See note
Trace spacing Microstrip or Stripline	2x	dielectric	
Max trace length/delay	~22 (3600)	In (ps)	
Max trace length/delay skew between SCLK and SDATA_OUT/IN	~1.6 (250)	In (ps)	

Note: Up to four signal vias can share a single GND return via.

Table 11-3. Audio Signal Connection

Module Pin Name	Type	Termination	Description
I2S[1:0]_SCLK	I/O		I2S Serial Clock: Connect to I2S/PCM CLK pin of audio device.
I2S[1:0]_FS	I/O		I2S Frame Select (Left/Right Clock): Connect to corresponding pin of audio device.
I2S[1:0]_DOUT	I/O		I2S Data Output: Connect to data input pin of audio device.
I2S[1:0]_DIN	I		I2S Data Input: Connect to data output pin of audio device.
GPIO09	O		Audio Codec Initiator Clock: Connect to clock pin of audio codec.

Chapter 12. Miscellaneous Interfaces

12.1 I2C

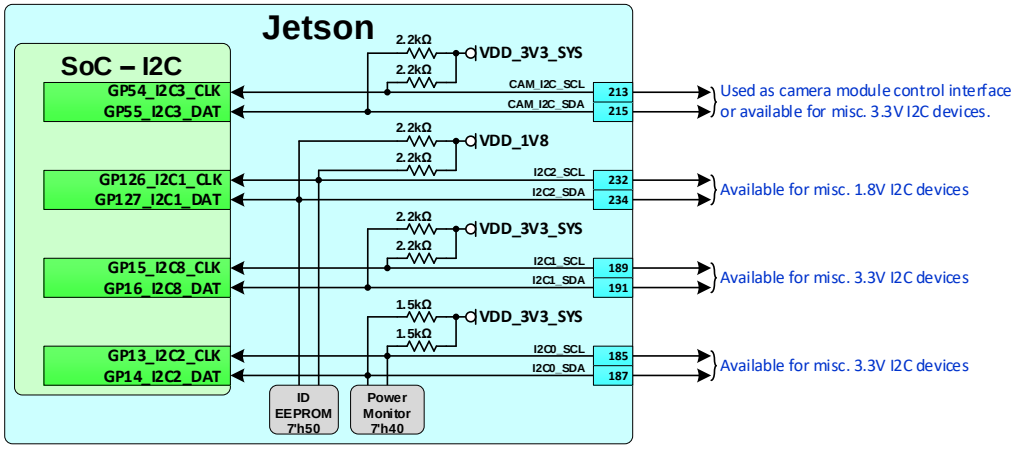
Orin module brings four I2C interfaces to the connector pins. CAM_I2C is included in the camera pin description table earlier in this design guide. The assignments in the "I2C Interface Mapping" table should be used where applicable for the I2C interfaces.

Table 12-1. Orin Module I2C Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage/Description	Recommended Usage	Direction	Pin Type
185	I2C0_SCL	GP13_I2C2_CLK	General I2C 0 Clock/Data. 1.5 kΩ pull-up to 3.3V on module. This I2C interface connects to a power monitor on the module with I2C address 7/h40.	I2C (general)	Bidir	Open Drain – 3.3V
187	I2C0_SDA	GP14_I2C2_DAT				Open Drain – 3.3V
189	I2C1_SCL	GP15_I2C8_CLK	General I2C 1 Clock/Data. 2.2 kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
191	I2C1_SDA	GP16_I2C8_DAT				Open Drain – 3.3V
232	I2C2_SCL	GP126_I2C1_CLK	General I2C 2 Clock/Data. 2.2 kΩ pull-up to 1.8V on the module. This I2C interface connects to an ID EEPROM on the module with I2C address 7/h50.			Open Drain – 1.8V
234	I2C2_SDA	GP127_I2C1_DAT				Open Drain – 1.8V

Notes: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Figure 12-1. I2C Connections



12.1.1 I2C Design Guidelines

Care must be taken to ensure I2C peripherals on the same I2C bus connected to the Orin module, do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the read/write bit removed or 8-bit including the read/write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format).

Note: The Orin module I2C interfaces have pull-ups on the module (See Table 12-1 or Table 12-3 for values). Pads for additional pull-ups are recommended in case a stronger pull-up is required due to additional loading on the interfaces.

12.1.2 I2C routing Guidelines

This section describes the I2C routing guidelines for Orin module.

Table 12-2. I2C Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency: Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology	Single ended, bi-directional, multiple initiators/targets		
Max loading: Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane	GND or PWR		
Trace impedance	50 – 60	Ω	±15%
Trace spacing	1x	dielectric	
Max trace length/delay Standard Mode Fm, Fm+ Modes	 3400 (~20) 1700 (~10)	ps (in)	

Notes:

1. Fm = Fast-mode, Fm+ = Fast-mode Plus
2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
3. No requirement for decoupling caps for PWR reference.

Table 12-3. I2C Signal Connections

Module Pin Name	Type	Termination	Description
I2C0_SCL/SDA	I/OD	1.5 kΩ pull-ups to **VDD_3V3** on the module.	**I2C #0 Clock and Data.** Connect to CLK and Data pins of any 3.3V devices
I2C1_SCL/SDA	I/OD	2.2 kΩ pull-ups to **VDD_3V3** on the module.	**I2C #1 Clock and Data.** Connect to CLK and Data pins of 3.3V devices.
I2C2_SCL/SDA	I/OD	2.2 kΩ pull-ups to **VDD_1V8** on the module.	**I2C #2 Clock and Data.** Connect to CLK and Data pins of any 1.8V devices
CAM_I2C_SCL/SDA	I/OD	2.2 kΩ pull-ups to **VDD_3V3** on the module.	**Camera I2C Clock and Data.** Connect to CLK and Data pins of any 3.3V devices

Notes:

1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the RCV_33_18_SEL option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the RCV_33_18_SEL option. The RCV_33_18_SEL option is selected in the Pinmux registers.

12.2 SPI

The Orin module brings out two of the Orin SPI interfaces. See Figure 12-2.

Table 12-4. Orin Module SPI Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
91	SPI0_SCK	GP47_SPI1_SCK	SPI 0 Clock	SPI #0 Device #0 or #1	Bidir	CMOS – 1.8V
93	SPI0_MISO	GP48_SPI1_MISO	SPI 0 Initiator In / Target Out			
89	SPI0_MOSI	GP49_SPI1_MOSI	SPI 0 Initiator Out / Target In			
95	SPI0_CS0*	GP50_SPI1_CS0	SPI 0 Chip Select 0	SPI #0 Device #0		
97	SPI0_CS1*	GP51_SPI1_CS1	SPI 0 Chip Select 1	SPI #0 Device #1		
106	SPI1_SCK	GP36_SPI3_SCK	SPI 1 Clock	SPI #1 Device #0 or #1		
108	SPI1_MISO	GP37_SPI3_MISO	SPI 1 Initiator In / Target Out			
104	SPI1_MOSI	GP38_SPI3_MOSI	SPI 1 Initiator Out / Target In			
110	SPI1_CS0*	GP39_SPI3_CS0	SPI 1 Chip Select 0	SPI #1 Device #0		
112	SPI1_CS1*	GP40_SPI3_CS1	SPI 1 Chip Select 1	SPI #1 Device #1		

Notes: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Figure 12-2. SPI Connections

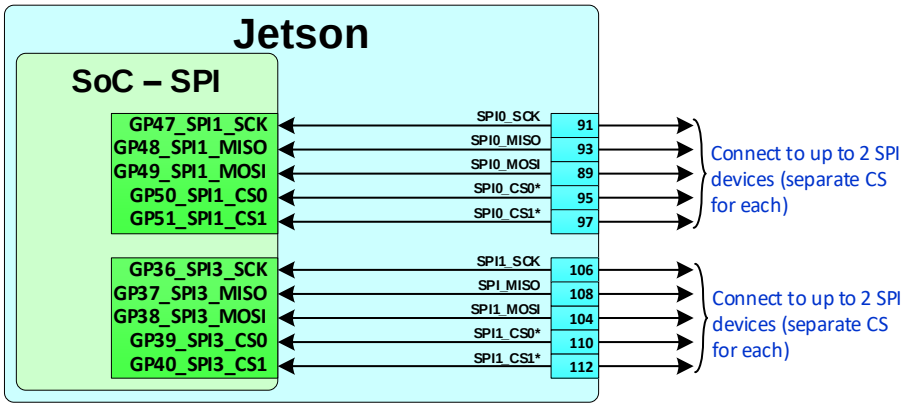
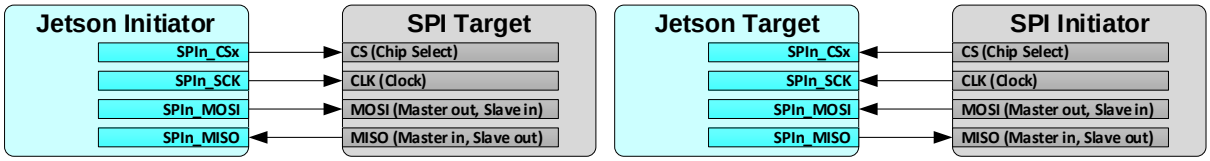


Figure 12-3. Basic SPI Initiator and Target Connections



12.2.1 SPI Routing Guidelines

The following guidelines meet the SPI routing guidelines.

Figure 12-4. SPI Topologies

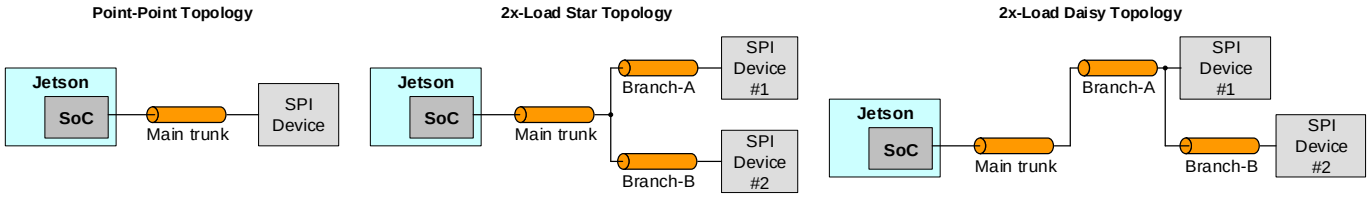


Table 12-5. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency	65	MHz	
Configuration / device organization	4	load	
Max loading (total of all loads)	15	pF	
Reference plane	**GND**		
Breakout region impedance	Minimum width and spacing		
Max PCB breakout delay	75	ps	
Trace impedance	50 – 60	Ω	±15%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See Note
Trace spacing: Microstrip / Stripline	4x / 3x	dielectric	
Max trace length/delay (PCB main trunk) For MOSI, MISO, SCK and CS Point-point 2x-load star/daisy	 195 (1228) 120 (756)	mm (ps)	

Parameter	Requirement	Units	Notes
Max trace length/delay (Branch-A) for **MOSI, MISO, SCK** and **CS** 2x-load star/daisy	75 (472)	mm (ps)	
Max trace length/delay skew from **MOSI, MISO** and **CS** to **SCK**	16 (100)	mm (ps)	At any point
Note: Up to four signal vias can share a single GND return via			

Table 12-6. SPI Signal Connections

Module Pin Names (Function)	Type	Termination	Description
SPI[1:0]_CLK	I/O		**SPI Clock.:** Connect to peripheral CLK pins
SPI[1:0]_MOSI	I/O		**SPI Data Output:** Connect to target peripheral MOSI pins
SPI[1:0]_MISO	I/O		**SPI Data Input:** Connect to target peripheral MISO pins
SPI[1:0]_CS[1:0]*	I/O		**SPI Chip Selects.:** Connect one CSx* pin per SPI interface to each target peripheral CS pin on the interface

12.3 UART

The Orin module brings three UARTs out to the main connector. See Figure 12-5 for typical assignments of the three available UARTs.

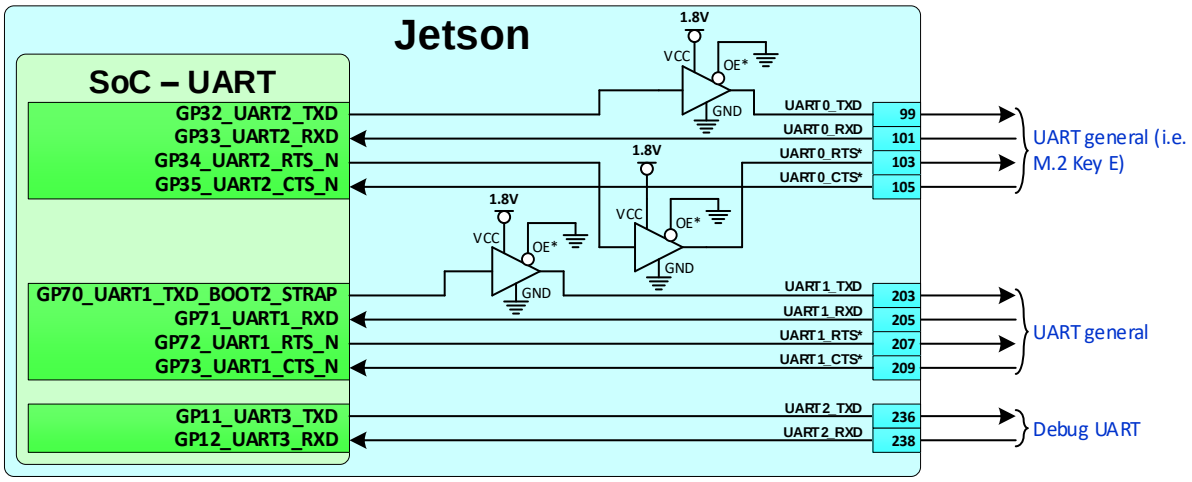
Table 12-7. Orin Module UART Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
99	UART0_TXD	GP32_UART2_TXD	UART 0 Transmit	UART general (i.e. M.2 Key E)	Output	CMOS – 1.8V
101	UART0_RXD	GP33_UART2_RXD	UART 0 Receive		Input	
103	UART0_RTS*	GP34_UART2_RTS_N	UART 0 Request to Send		Output	
105	UART0_CTS*	GP35_UART2_CTS_N	UART 0 Clear to Send		Input	
203	UART1_TXD	GP70_UART1_TX_BOOT2_STRAP	UART 1 Transmit	UART general	Output	
205	UART1_RXD	GP71_UART1_RXD	UART 1 Receive		Input	
207	UART1_RTS*	GP72_UART1_RTS_N	UART 1 Request to Send		Output	
209	UART1_CTS*	GP73_UART1_CTS_N	UART 1 Clear to Send		Input	
236	UART2_TXD	GP11_UART3_TXD	UART 2 Transmit.	Debug UART	Output	
238	UART2_RXD	GP12_UART3_RXD	UART 2 Receive		Input	

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction indicated for the UART pins except for is true when used for that function. Otherwise, these pins support GPIO functionality and most can support both input and output (bidirectional) functionality. The exception is UART0_TXD, UART0_RTS* and UART1_TXD. These have output-only buffers on the module to keep them from being affected by connected devices during boot as they are associated with SoC strapping pins.

Figure 12-5. Orin Module UART Connections



Note: The buffers on UART0_TXD, UART0_RTS* and UART1_TXD are there to prevent connected devices from changing the pin state during power-on. These pins are associated with SoC Strapping pins

Table 12-8. UART Signal Connections

Ball Name	Type	Termination	Description
UART[2:0]_TXD	O		UART Transmit: Connect to peripheral RXD pin of device
UART[2:0]_RXD	I		UART Receive: Connect to peripheral TXD pin of device
UART[1:0]_CTS*	I		UART Clear to Send: Connect to peripheral RTS pin of device
UART[1:0]_RTS*	O		UART Request to Send: Connect to peripheral CTS pin of device

12.4 CAN

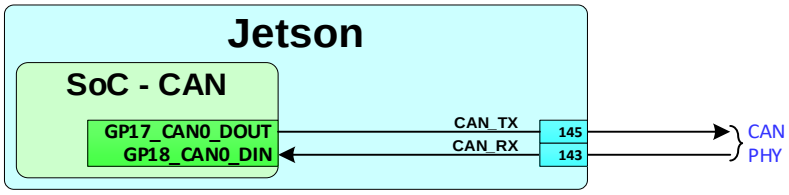
Orin module brings a single controlled area network (CAN) interface to the main connector.

Table 12-9. Orin Module CAN Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
143	CAN_RX	GP17_CAN0_DOUT	CAN Receive	CAN PHY	Input	CMOS – 3.3V
145	CAN_TX	GP18_CAN0_DIN	CAN Transmit		Output	CMOS – 3.3V

Notes:
1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction indicated for the CAN signals are associated with that usage. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 12-6. Orin Module CAN Connections



12.4.1 CAN Routing Guidelines

The section describes the CAN routing guidelines for Orin module.

Table 12-10. CAN Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate / Frequency	8	Mbps / MHz	
Configuration / Device Organization	1	load	
Reference plane	**GND**		
Trace Impedance	50	Ω	±15%
Via proximity (Signal via to **GND** return via)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing: Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length (for **RX** and **TX** only)	223 (1360)	mm (ps)	See Note 2
Max Trace Length/Delay Skew from **RX** to **TX**	8 (50)	mm (ps)	See Note 2

Table 12-11. CAN Signal Connections

Module Pin Name	Type	Termination	Description
CAN_TX	O		CAN Transmit: Connect to matching pin of device
CAN_RX	I		CAN Receive: Connect to Peripheral pin of device

12.5 Fan

Orin module provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution. Information on the PWM and Tachometer pins and functions can be found in the following locations:

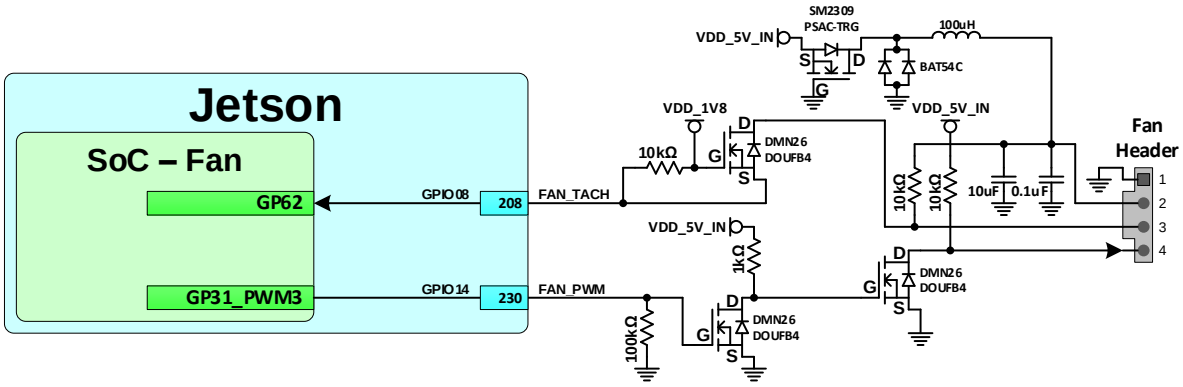
- Orin Module Pin Mux
  - This is used to configure GPIO14 (PWM) for FAN_PWM and GPIO08 for FAN_TACH. The pin used for FAN_PWM is configured as GP_PWM6. The pin used for FAN_TACH is configured as a GPIO.
- Orin (SoC) Technical Reference Manual (TRM)
  - Functional descriptions and related registers can be found in the TRM for the FAN_PWM (PWM chapter).

Table 12-12. Orin Module Fan Pin Descriptions

Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
230	GPIO14	GP31_PWM3	Fan PWM	Fan	Output (note)	CMOS – 1.8V
208	GPIO08	GP62	Fan tachometer	Fan	Input (note)	CMOS – 1.8V

Notes:
1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction indicated for GPIO014 and GPIO08 is associated with their use as Fan PWM/Tach. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 12-7. Orin Module Fan Connections



12.6 Debug

Orin Module supports a UART for debugging purposes. The UART intended for debug is UART2.

Table 12-13. Orin Module Debug UART Pin Descriptions

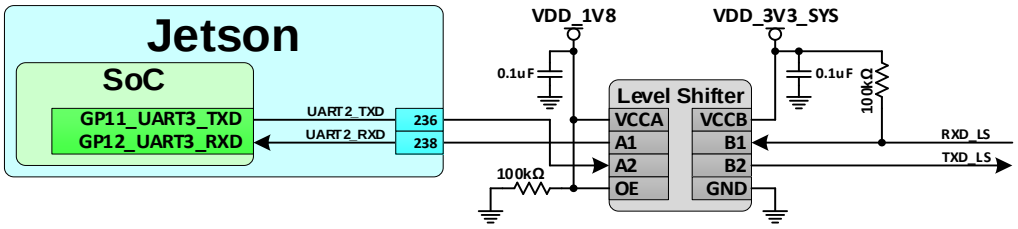
Pin #	Module Pin Name	Orin Signal	Usage and Description	Recommended Usage	Direction	Pin Type
238	UART2_RXD	GP11_UART3_TXD	UART 2 receive	Debug UART	Input	CMOS – 1.8V
236	UART2_TXD	GP12_UART3_RXD	UART 2 transmit		Output	

Note: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Table 12-14. Debug UART Connections

Module Pin Name	Type	Termination	Description
UART2_TXD	O		UART #2 Transmit: Connect to RX pin of serial device
UART2_RXD	I	If level shifter implemented, 100kΩ to supply on the non-Orin module side of the device.	UART #2 Receive: Connect to TX pin of serial device

Figure 12-8. Debug UART Connections



Note: If level shifter is implemented, pull-up is required on the RXD line on the non-Orin module side of the level shifter. This is required to keep the input from floating and toggling when no device is connected to the debug UART.

Chapter 13. PADS

Orin module signals that come from the SoC may glitch when the associated power rail is enabled. This may affect pins that are used as GPIO outputs. Designers should take this into account. GPIO outputs that must maintain a low state even while the power rail is being ramped up may require special handling.

13.1 Internal Pull-Ups for Dual Voltage Block Pins Power at 1.8V

Several of the MPIO pads are on blocks designed to be powered at either 1.8V or 3.3V. These blocks are powered at 1.8V on Orin module, and the internal pull-up at initial Power-On is not effective. The signal may only be pulled up a fraction of the 1.8V rail. Once the system boots, software can configure the pins for 1.8V operation and the internal pull-ups will work correctly. If these signals need the pull-ups during Power-On, external pull-up resistors should be added. The following pins listed are the affected pins. These are the Orin module pins on the dual voltage blocks powered at 1.8V with Power-On reset default of Internal pull-up enabled.

- SPI1_CS0*
- SPI1_CS1*

13.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt-trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt-trigger mode provides better noise immunity and can help avoid extra edges from being "seen" by the Orin inputs. Input clocks include the I2S and SPI clocks (I2Sx_SCLK and SPIx_SCK) when Orin is in target mode. The FAN_TACH pin [GPIO8] is another input that could be affected by noise on the signal edges. Care should be taken if the Schmitt-trigger mode setting is changed from the default initialization mode as this can influence interface timing.

13.3 Pins Pulled or Driven High During Power-On

The Orin module is powered up before the carrier board (See Section 6.1 for power sequencing). Table 13-1 lists the pins on Orin module that default to being pulled or driven high. Care must be taken on the carrier board design to ensure that any of these pins that connect to devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer or shifter should be disabled until the device power is enabled.

Table 13-1. Pins Pulled or Driven High by Orin Prior to SYS_RESET* Inactive

Orin Module Pin	Power-On Reset Default	Pull-up Strength (kΩ)
MOD_SLEEP*	Driven high	na
FORCE_RECOVERY*	Internal pull-up	~50

Table 13-2. Pins with External Pull-Ups to Supply on before SYS_RESET* Inactive

Orin Module Pin	Pull-Up Supply Voltage (V)	External Pull-Up (kΩ)		Orin Module Pin	Pull-Up Supply Voltage (V)	External Pull-Up (kΩ)
I2C0_SCL/SDA	3.3	1.5		GPIO00	1.8	100
I2C1_SCL/SDA	3.3	2.2		PCIE[3:0]_CLKREQ*	3.3	47
I2C2_SCL/SDA	1.8	2.2		PCIE[3:0]_RST*	3.3	4.7
CAM_I2C_SCL/SDA	3.3	2.2		PCIE_WAKE*	3.3	47

Chapter 14. Unused Interface Terminations

14.1 Unused Multi-Purpose Standard CMOS Pad Interfaces

The following Orin module pins (and groups of pins) are Orin MPIO pins that support either special function I/Os (SFIO) and GPIO capabilities. Any unused pins or portions of pin groups listed in Table 14-1 that are not used can be left unconnected.

Table 14-1. Unused MPIO Pins and Pin Group

Orin Module Pins and Pin Groups		Orin Module Pins and Pin Groups
FORCE_RECOVERY*		I2S
PCIE[1:0]_CLK/RST/CLKREQ/WAKE		UART
GPIO xx		I2C
DP1_HPD, HDMI_CEC		SPI
CAM Control, Clock		

14.2 Unused Dedicated Special Purpose Pad Interfaces

See the Unused SFIO (Special Function I/O) interface pins section in the design checklist attached to this design guide.

Chapter 15. Design and Bring-Up Checklists

The design checklist is intended to help ensure that the correct connections have been made in a design. The check items describe connections for the various interfaces and the "Same/Diff/NA" column is intended to be used to indicate whether the design matches the check item description, is different, or is not applicable to the design. The bring-up checklist is intended to provide basic items to check during bring-up for power delivery and the various interfaces used in a design.

To access the attached files, click the Attachment icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (Open, Save) to retrieve the documents. Excel files with the .nvxlsx extension will need to be renamed to .xlsx to open.

Chapter 16. Orin Module Pin Descriptions

The Orin module pin description is attached to this design guide.

To access the attached files, click the Attachment icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (Open, Save) to retrieve the documents. Excel files with the .nvxlsx extension will need to be renamed to .xlsx to open.

Chapter 17. General Routing Guidelines

17.1 Signal Naming Convention

The following conventions are used in describing the signals for Orin module:

- Signal names use a mnemonic to represent the function of the signal. For example, I2S interface #0 shift clock signal is represented as I2S0_SCK. All active-low single-ended signals are identified by an asterisk (*) after the signal name. For example, SYS_RESET* indicates an active-low signal. Active-high signals do not have the (*) after the signal names. For example, I2S0_FS indicates an active-high signal. Differential signals are identified as a pair with the same names that end with _P and _N (for positive and negative, respectively). For example, CSI_0_D0_P and CSI_0_D0_N indicate a differential signal pair.
- The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The following table lists the I/O codes used in the signal description tables.

Table 17-1. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

17.2 Routing Guidelines Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from BGA ball either to a point beyond the ball array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 12.5 mm unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max and min trace delays where specified. Trace delays are typically shown in mm or in terms of signal delay in pico-seconds (ps) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing
  - Spacing to other signals and pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) and inner (stripline) layers of a PCB.

17.3 Signal Routing Conventions

Throughout this design guide, the following signal routing convention is used:

- SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing
  - SE impedance of trace (along with diff impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip and stripline.

Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing and trace widths are chosen to meet differential impedance requirements.

17.4 Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI, DP, USB 3.2, PCIe, or CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay or flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this design guide.

- Controlled Impedance
  Each interface has different trace impedance requirements and spacing to other traces. It is up to designer to calculate trace width and spacing required to achieve specified SE and Diff impedances. Unless otherwise noted, trace impedance values are ±15%.

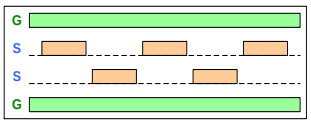
- Max Trace Lengths/Delays
  Trace lengths or delays should include the carrier board PCB routing (where the Orin module mating connector resides) and any additional routing on a Flex or secondary PCB segment connected to main PCB. The max length or delay should be from Orin module to the actual connector (that is USB, HDMI, and so on) or device (that is, onboard USB device, camera imager IC, and so on).
- Trace Delay or Flight Time Matching
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - It is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 5.9 ps/mm and inner-layer 6.9 ps/mm. If one signal is routed 250 mm on the outer layer and second signal is routed 250 mm in the inner layer, the difference in flight time between two signals will be 250 ps! That is a big difference if required matching is 15 ps (trace delay matching). To fix this, inner trace needs to be 36 mm shorter or outer trace needs to be 42 mm longer.
  - In this design guide, terms such as intra-pair and inter-pair are used when describing differential pair delays. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pair average delays.

17.4.1 General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (see Figure 17-1).

Do not route other signals or power traces and areas directly under or over critical high-speed interface signals.

Figure 17-1. General PCB Routing Guidelines



Note: The requirements detailed in the interface signal routing requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.

17.5 Common High-Speed Interface Requirements

The following table describes the common high-speed interface requirements.

Table 17-2. Common High-Speed Interface Requirements

Parameter		Requirement	Units	Notes
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues)				
Preferred device				Type: TDK ACM2012D-900-2P. Only if needed. Place near connector. Refer to Common Mode Choke Requirement section.
Location - Max distance from to adjacent discontinuities – ex, connector, AC cap)		8 (53)	mm (ps)	TDK ACM2012D-900-2P See Figure 17-2
Common-mode impedance @ 100MHz Min/Max		65/90	Ω	
Max Rdc		0.3	Ω	
Differential TDR impedance		90	Ω	@T_R-200ps (10%-90%)
Min Sdd21 @ 2.5GHz		2.22	dB	
Max Scc21 @ 2.5GHz		19.2	dB	
Serpentine				
Min bend angle		135	deg (α)	S1 must be taken care to consider Xtalk to adjacent pair. See USB 3.2 Guideline in Figure 17-3.
Dimension	Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	
General				
Routing over Voids		Routing over voids not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling		Keep critical high-speed traces away from other signal traces or unrelated power traces and areas or power supply components		

The following figures show the common high-speed interface signal routing requirements.

Figure 17-2. Common Mode Choke

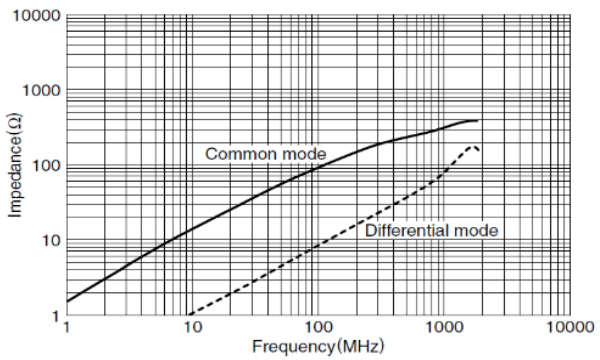
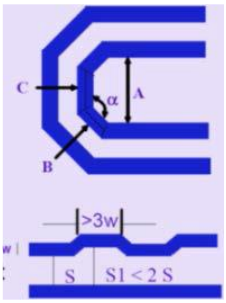


Figure 17-3. Serpentine



17.6 Test Points for High-Speed Interfaces

Ideally, test points are not preferred on very high-speed interface traces as they can degrade signal integrity. However, to be able to do compliance testing, or interface tuning where applicable, it may be necessary to include test points at least for early revisions of a design. The test points are generally required near the receiver. If a connector or some other device (capacitor, resistor, and so on) exists near the receiver, the pins can be used as test points without creating additional signal degradation. Where connector or discrete device pins are not accessible near the receiver end of an interface, it may be necessary to include test points. When test points are needed for very high-speed interface signals, follow these recommendations:

- Test points should be very small (less than 0.5 mm).
- Test points should be located on the existing trace (no stub).
- If the test points are placed on differential signals, they should be symmetric for each P and N signal.

Chapter 18. USB 3.2 and Wireless Coexistence

USB 3.2 supports a 5 Gbps or 10 Gbps signaling rate. The USB 3.2 specification requires USB 3.2 data to be scrambled and spread-spectrum is required. The noise from the USB 3.2 data spectrum has been found from around DC to 4 GHz and beyond. This noise can desensitize nearby receivers operating in the cellular and WiFi 2.4 GHz band. This includes, for example, WiFi 802.11b/g/n or Bluetooth® including Bluetooth mouse devices, Bluetooth keyboards, and. This noise causes the following:

- WiFi sensitivity degradation
- Wireless link throughput drop
- Wireless operation range degradation

This chapter is focusing on USB 3.2, but other high-speed interfaces such as HDMI, DP, and so on, can also cause issues with wireless subsystems. The issues and recommended mitigation techniques would be similar.

18.1 Mitigation Techniques

Each design is different due to unique construction and relative location of USB 3.2 circuits and connectors and receiving antenna. Depending on the level of noise generated, emitted, radiated, and coupled to receiver antenna, some or all the recommendations might need to be implemented to limit unwanted noise from radiating from the circuit.

The following mitigation techniques described will help minimize the USB 3.2 de-sense.

INCREASE THE USB 3.2 TO ANTENNA SEPARATION

During the placement phase of the design, care must be taken to identify the noise source and try to physically increase the separation between the noise source and antenna. One of the major noise sources is the USB 3.2 connector itself. If possible, the antenna or USB 3.2 location can be changed to increase physical isolation. In general, doubling the distance between antenna and noise source, reduces the coupling by around 6 dB.

USB SS CONNECTOR PART SELECTION: CHOOSE A BETTER USB 3.2 PART

A USB 3.2 connector has many metal fingers that are perfect in length for radiating in and around the 2.4 GHz band and beyond. A USB 3.2 connector should be selected to minimize radiation from the USB 3.2 part itself. Some recommendations are:

- Connector is fully enclosed by metal
- No slots in the connector walls, or if there are slots, the size is very small. Also, the number of slots should be minimal.
- Connector has as many grounding legs as possible. More legs provide better grounding from the USB 3.2 exterior to the PCB and the structure is less likely to radiate. Choose four legged connectors over two legged connectors and so on.

The quality of the external USB 3.2 device used in the USB 3.2 port will have impact on the overall experience. If the external USB 3.2 device used in the USB 3.2 port is of poor quality, the part itself will radiate and issues will continue. A plastic base USB 3.2 device works inferior compared to fully metalized USB 3.2 devices.

GROUND THE USB 3.2 PART SOLIDLY

The USB 3.2 connector is grounded through "the grounding legs" previously mentioned. Care must be taken to ensure the leg area is a very good RF ground. One way to do this is to increase the number of ground vias placed in the "grounding leg" area.

IMPROVE THE ROUTING AND GROUNDING AROUND THE USB 3.2 PART AREA

The routing and grounding around the USB 3.2 connector part area must be handled carefully. Since this area is very "hot," any traces running on the surface layer below the physical connector part can pick up noise and transfer it to other areas or radiate the noise. These traces need to be moved to an inner layer, and this area needs to be made a very good ground.

BURY THE USB 3.2 LINES IN INNER LAYERS

The USB 3.2 lines should be routed as impedance controlled differential pairs, with ground on either side and on the layers above and below.

SHIELD THE USB 3.2 CONNECTOR PART

The radiation from the USB 3.2 connector part is very strong. Need to make a "shield" and put on top of the USB 3.2 connectors. The shield must touch the USB 3.2 body in multiple points. The shield track must have number of grounding vias so that any emitted noise from the USB 3.2 connector is swiftly grounded.

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