

J-Link-OB use notes for u-blox nRF5 based EVKs

Bluetooth® Low Energy
Application note



Abstract

This application note contains various hints and tips for using the J-Link-OB debugger present on the EVKs for ANNA-B1, BMD-3, NINA-B1, NINA-B3, NINA-B4, and NORA-B1.

Document information

Title	J-Link-OB use notes for u-blox nRF5 based EVKs	
Subtitle	Bluetooth® Low Energy	
Document type	Application note	
Document number	UBX-20009734	
Revision and date	R01	1-Dec-2020
Disclosure restriction	C1-Public	

This document applies to the following products:

Product name
EVK-ANNA-B112
EVK-BMD-30/33/35/36
EVK-BMD-34/38
EVK-BMD-345
EVK-NINA-B1
EVK-NINA-B3
EVK-NINA-B4
EVK-NORA-B1

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1 Module SWD interface

The ANNA-B1, BMD-3, NINA-B1, NINA-B3, NINA-B4, and NORA-B1 modules from u-blox utilize the Serial Wire Debug (SWD) interface – a low-pin-count debug interface found in Arm® Cortex®-M processors. This interface is implemented over two pins, **SWDIO** and **SWDCLK**. Along with **VCC** and **GND**, this provides the minimum interface for interactive application development.

Additional debug and trace signals are available on many of these modules. Table 1 describes the full set of signals:

SWD signal	Description
SWDCLK	Serial wire debug clock input to CPU for debug and programming
SWDIO	Serial wire debug I/O for debug and programming
SWO/TRACEDATA[0] ^{1,2,3}	Serial Wire Output from CPU / Trace buffer, bit 0 from CPU
TRACEDATA[1] ^{1,2,3}	Trace buffer, bit 1 from CPU
TRACEDATA[2] ^{1,2,3}	Trace buffer, bit 2 from CPU
TRACEDATA[3] ^{1,2,3}	Trace buffer, bit 3 from CPU
TRACECLK ^{1,2,3}	Trace buffer clock from CPU
VT _{REF}	Target reference voltage – VCC from target circuit
GND	Target signal ground

Table 1: SWD interface signals

¹ TRACE signals not available on BMD-330 and BMD-360

² TRACE signals not defined on ANNA-B1 and NINA-B1, though available. See nRF52832 Product Specification [5].

³ TRACE signals not supported by J-Link-OB. An external J-Trace debug probe is required.

2 J-Link

2.1 J-Link-OB

The u-blox EVKs for Nordic Semiconductor based Bluetooth Low Energy modules provide an on-board SEGGER J-Link-OB debug interface from SEGGER Microcontroller. This debug interface connects to the Bluetooth Low Energy module mounted on the EVK to create a complete development system. All features of the J-Link BASE debug probe are supported, though use is limited to Nordic Semiconductor nRF5 based products. This includes the ANNA-B1, BMD-3, NINA-B1, NINA-B3, NINA-B4, and NORA-B1 modules from u-blox.

In addition to the on-board module, custom target hardware utilizing a u-blox module noted above can also be used with the EVK.

The official J-Link documentation [2] applies to the J-Link-OB interface. This document provides additional usage notes that we have compiled over time. References to J-Link and J-Link-OB are considered equivalent throughout this document.

2.2 Virtual COM port (VCP)

The J-Link-OB circuit provides one or more Virtual COM Ports. This provides a communication path from the host PC to the u-blox module. These ports may also be used for debug logging when enabled in the Nordic Semiconductor nRF5 SDK. A single VCP is provided on the ANNA, BMD, and NINA EVKs. Three VCPs are provided on the NORA EVK – one for each processor core and one unused.

2.3 Mass Storage Device (MSD)

When plugged into a host over USB, the J-Link-OB provides a virtual disk drive that appears as a USB thumb drive. This is used to easily program the target module by simply copying an application firmware file to the drive.

2.4 J-Link Commander

SEGGER makes available the J-Link “Software and Documentation pack” [2]. This download must be installed in order to provide the command-line J-Link commander. Versions are available for Windows, macOS, and Linux.

3 EVK J-Link use notes

It is assumed the following software is installed:

- SEGGER J-Link Software pack (including J-Link Commander) [2],
- SEGGER Embedded Studio [3], and
- Nordic Semiconductor nRF Command Line Tools [6].

3.1 Mass Storage Device

When using the J-Link Virtual COM Port (VCP) UART to perform firmware updates, it may be necessary to disable the J-Link Mass Storage Device (MSD) for the updates to be successful.

Disabling the MSD also helps host systems with limited resources maintain an interactive debug session, for example when using breakpoints or single-stepping through an application.

Enabling and disabling the MSD is accomplished through the J-Link Commander command line interface (JLink.exe on Windows, JLinkExe on macOS and Linux).

From a J-Link prompt, enter “msddisable”:

```
J-Link>msddisable
Probe configured successfully.
J-Link>
```

The MSD may be enabled again with “msdenable”:

```
J-Link>msdenable
Probe configured successfully.
J-Link>
```

 Be sure to power-cycle the EVK after entering either command.

3.2 J-Link firmware update

When the EVK is first used, the J-Link firmware may need updated. If so, a dialog box will be displayed.

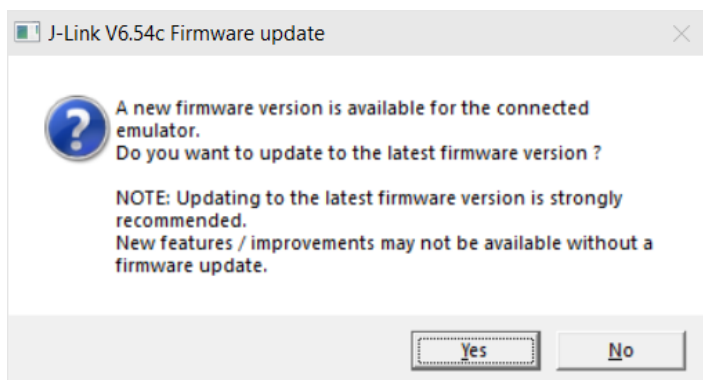


Figure 1: J-Link firmware update

 It is good practice to keep the J-Link firmware up to date.

3.3 Re-program J-Link firmware

If the EVK becomes unresponsive, the J-Link firmware may be corrupted. It is easy to re-program the firmware by following these steps:

1. Download the J-Link debugger BIN file [4].
2. Hold down the reset button while powering on the EVK.
3. A drive called "BOOTLOADER" will be mounted.

4. Copy the J-Link binary downloaded in step 1 onto this Bootloader drive. The LED should "fast blink" after programming is done.
5. Power-cycle the board and the LED will return to on with some flicker indicating USB activity.
6. If an update notice is displayed when using the EVK, perform the update as noted in section 3.2 above.

👉 Reprogramming the J-Link firmware with the BOOTLOADER drive method is currently not available on the EVK-NORA-B1.

3.4 External debug probe

3.4.1 EVK BMD-30/33/35/36

Use of a separate, external debug probe is not supported.

3.4.2 EVK BMD-34/38 and EVK BMD-345

Jumper J26 is a “9-pin JTAG/SWD connector” for an external debug probe as described by the SEGGER J-Link / J-Trace User Guide [2], section 18.3. The connector is a 2x5 pin header with centers at 1.27 mm.

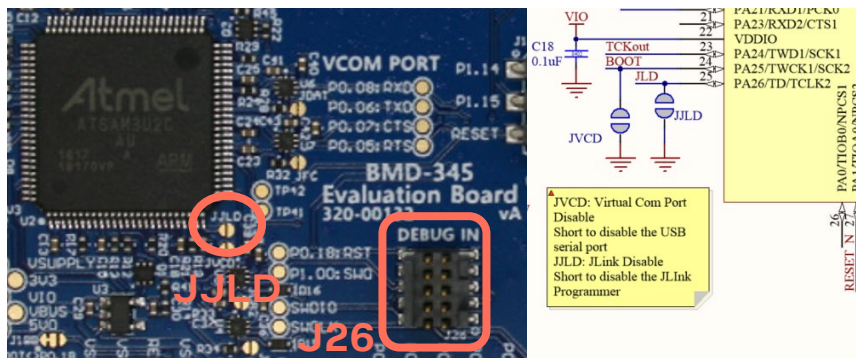


Figure 2: EVK BMD-34/38 and EVK BMD-345 J-Link-OB - disable interface

 When using an external debug probe, the J-Link-OB interface must be disabled by soldering across “JJLD”, which located to the left of J26.

3.4.3 EVK ANNA-B1/NINA-B1/NINA-B3/NINA-B4

Jumper J12 is a “9-pin JTAG/SWD connector” for an external debug probe as described by the SEGGER J-Link / J-Trace User Guide [2], section 18.3. The connector is a 2x5 pin header with centers at 1.27 mm.

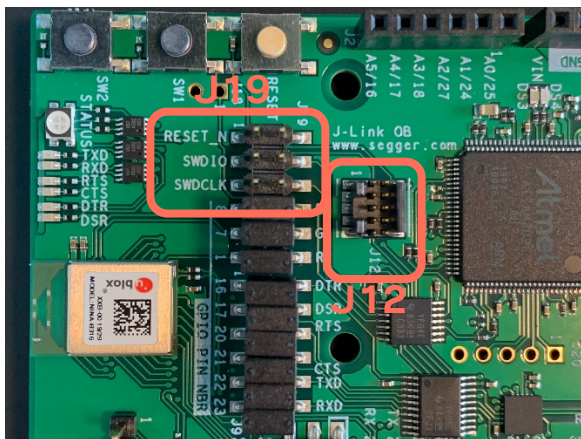


Figure 3: EVKs ANNA-B and NINA-B J-Link-OB - disable interface

⚠ When using an external debug probe, the J-Link-OB interface must be disabled by removing the shunts across **RESET_N**, **SWDIO**, and **SWDCLK** on J19, located to the left of J12.

3.4.4 EVK NORA-B1

Use of the DEBUG IN connector, J20, is sensed by the EVK. No jumpers need changed.

3.5 External target devices

3.5.1 EVK BMD-3 (all) and NORA-B1

The EVKs for the BMD-3 and NORA-B1 modules support connecting the J-Link-OB to external target devices based on Nordic Semiconductor nRF5 CPUs. This interface is provided by J3 on the EVK BMD-3 and J10 on the EVK-NORA-B1, which is located near the upper-left of the board.

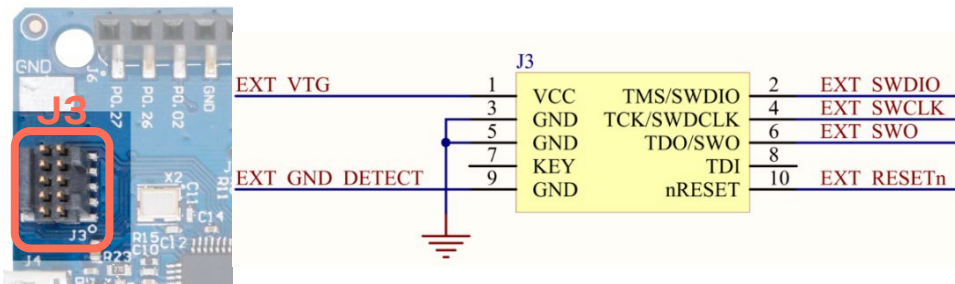


Figure 4: EVK BMD-3 debug interface for target hardware

The DEBUG OUT connector is implemented with a 2x5 10-pin header on 0.05" centers. The signals have a slightly different definition when compared to the SEGGER J-Link "9-pin JTAG/SWD connector".

To enable the external J-Link connection, ensure the connections shown in Table 2 are implemented on the target hardware.

Pin	Signal	Direction	Comments
1	EXT_VTG	I	Connect EXT_VTG to the power supply (VCC) on the target hardware ⁴ 👉 Only 3.0 VDC to 3.3 VDC is supported 👉 If the target design does not operate at 3.0 VDC -3.3 VDC, then an external SEGGER J-Link interface is required to prevent damage to the target hardware.
2	EXT_SWDIO	I/O	Connect to SWDIO on the target hardware
3	GND		Connect to GND on the target hardware
4	EXT_SWCLK	O	Connect to SWDCLK on the target hardware
5	GND		Connect to GND on the target hardware
6	EXT_SWO	I	(Optional) connect to SWO on the target hardware
7	–		Not connected
8	–		Not connected
9	EXT_GND_DETECT	I	Detect the presence of external target hardware. Connect EXT_GND_DETECT to GND on the target hardware in order to program the external hardware rather than the on-board module. 👉 Not connected on EVK-NORA-B1
10	EXT_RESET_N	I/O	(Optional) connect to RESET_N on the target hardware

Table 2: EVK BMD-3 and NORA-B1 debug interface for target hardware

⁴ The target hardware must be powered independently.

 The J-Link-OB firmware is provided by SEGGER Microcontroller to Nordic Semiconductor and limited to nRF5 devices. SEGGER Microcontroller permits Nordic Semiconductor's partners to use the J-Link-OB firmware “as is” for evaluation boards – provided that the EVK is not used to program production devices.

3.5.2 EVK ANNA-B1, EVK-NINA-B

The EVK ANNA-B1 and all EVK NINA-B are not intended for external target hardware connections.

Appendix

A Glossary

Abbreviation	Definition
ARM	Arm (Advanced RISC Machines) Holdings
CPU	Central Processing Unit
DC	Direct Current
EVK	Evaluation kit
MSD	Mass storage device
SWD	Serial Wire Debug
VCP	Virtual communication port

Table 3: Explanation of the abbreviations and terms used

Related documents

- [1] SEGGER Microcontroller [J-Link-OB](#)
- [2] SEGGER Microcontroller [J-Link Software and Documentation pack](#)
- [3] SEGGER Microcontroller [Embedded Studio](#)
- [4] SEGGER Microcontroller [J-Link-OB firmware](#)
- [5] Nordic Semiconductor [nRF52832 product specification](#)
- [6] Nordic Semiconductor [nRF Command Line Tools](#)

 For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Comments
R01	1-Dec-2020	Initial release

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