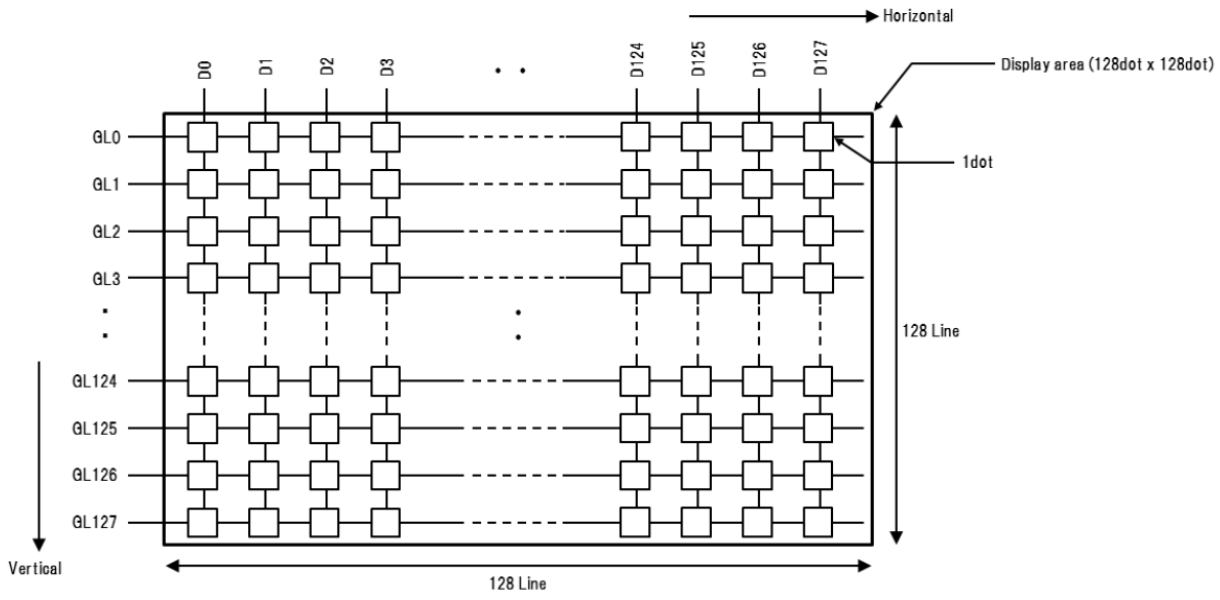
Interfacing to the MIP display

The MIP (Memory in Pixel) technology was designed for simplicity and low power consumption. While the MIP has a different interface scheme from a traditional LCD interface, it is still very straight forward. The interface is a three wire SPI bus. The serial interface allows a wide variety of devices to interface to the LCD module. Since the display has internal memory, no external memory or controllers are required to drive the module. The MIP display can easily be driven by 8 bit microcontrollers without any external hardware. This allows the MIP display to add a graphic display with minimal update to the existing system.

Overview.

Each pixel in a MIP display contains a single memory bit. The bit can be written to, but not read back from. Since only a single bit is written the display only supports black and white. The MIP technology currently does not support gray levels. The individual bits are arranged into a matrix.

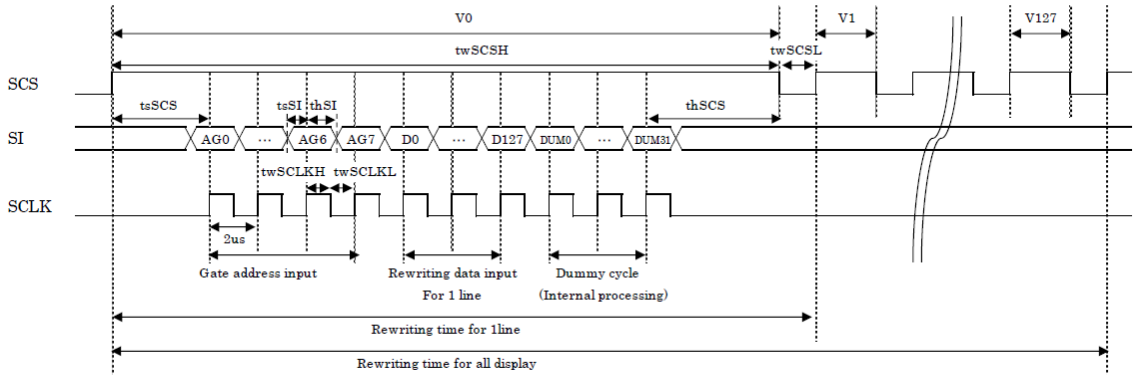


Data is written to the display a line at a time. In general operation, the display works like a shift register. Data is shifted into the display one bit at a time until the entire line is loaded. The entire line must be

loaded, single bit or partial line writes are not supported. The line of data being entered into the display is divided into to three section. The line address, display data, and trailer of 32 dummy bits.

Data Format

9-1. Rewriting timing <SCS activating period: 1 line>



The line of data being begins with the line address. This consist of eight bits that has the address of the line to write to. This will range from zero to 255. The maximum value is the number of the lines the display has. Any address greater than the last line on the display will be ignored. The LSB of the address is the first bit transmitted followed by the remaining address bits in ascending order. Example line three would have the following address:

A0 A1 A2 A3 A4 A5 A6 A7

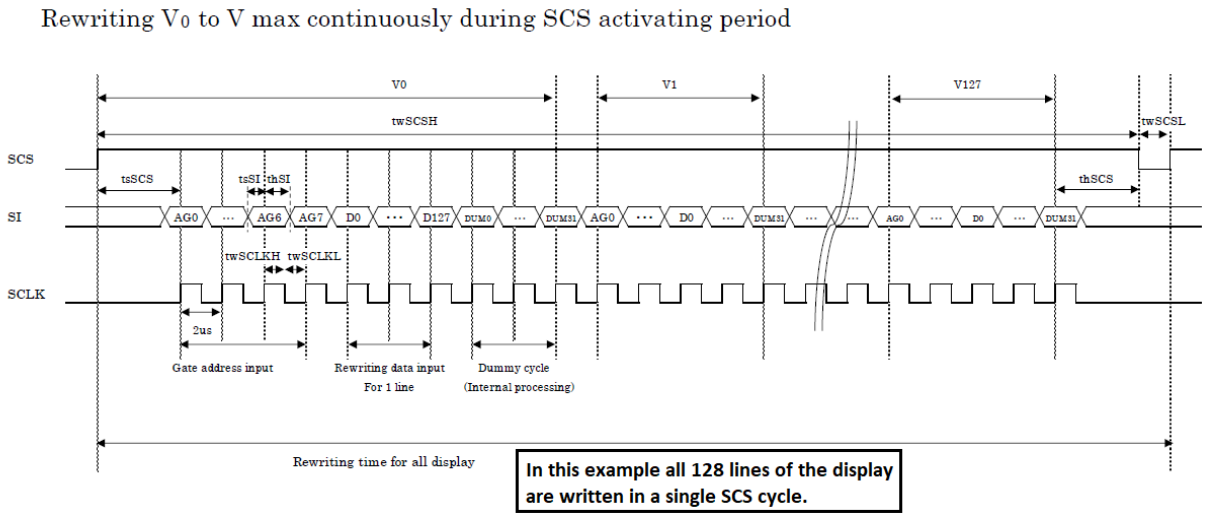
1 1 0 0 0 0 0 0

Directly after the last address bit (A7) the data to be displayed is sent. The data is sent in the order to be displayed. The first bit is the left most pixel (Column 0), followed by the next bit to be displayed. A data one will result in a black pixel being displayed, a data zero is white or blank. This is always true regardless if the display is normally back or normally white. An entire line of data must be sent. If the display is 128 pixels wide, 128 bits must be sent. After the last data bit is sent. Another 32 bits must be sent. The dummy bits at the end line allow the display time to complete some internal operations and display the data.

Timing sequence

The data is sent to the display using standard SPI bus protocol. The sequence starts with the chip select (SCS) signal being asserted high, the data (SI) is driven, then data is latched with the rising edge of the clock (SCLK). Once the line is completed SCS has returned to zero. If desired, multiple lines of data can be sent with a single assertion of SCS. Once the last bit of the previous line is sent, the next line can

begin without having to release SCS. Once a line is started, the entire line must be sent before releasing SCS.



VCOM

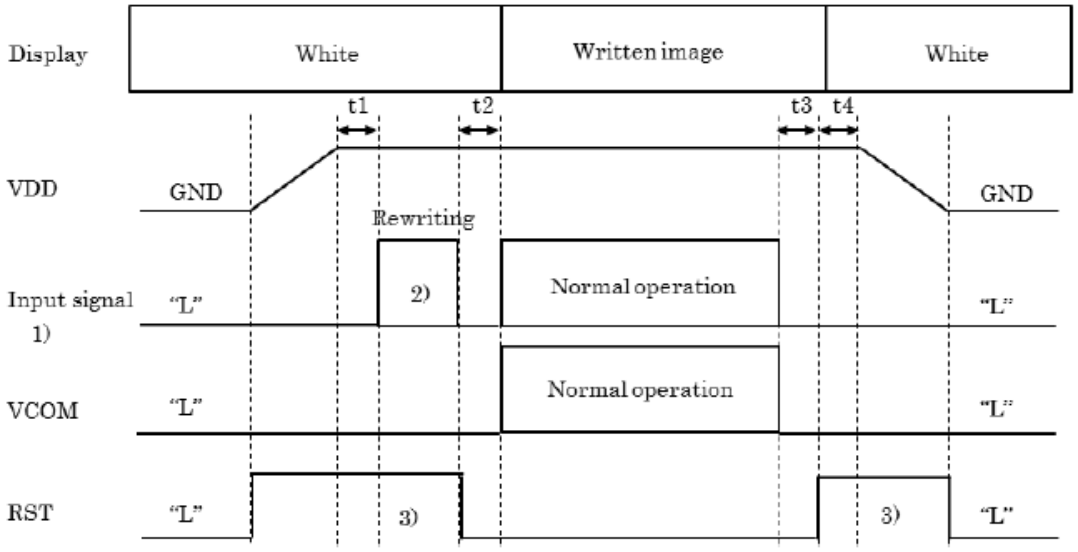
The VCOM is an external signal used to drive the MIP cell. It should be a 1Hz signal with a 50% duty cycle. This signal is important. If VCOM is not driven the MIP display may develop image retention. When changing the screen the old image may fade away slowly, or even stay long term even if the display is powered off if the VCOM is not used.. The VCOM wave form is used to generate a bias voltage that is applied the cell. Alternating the polarity of VCOM changes the polarity of the bias voltage applied to the MIP cell. This alternating voltage eliminates any DC offset voltage in the MIP cell. The alternating voltage prevents foreign particles in the LCD fluid being attracted to the anode/cathode due to DC voltage of the cell drive circuitry and plating the electronics. The VCOM signal can be operated independently of the SPI bus and does not require any synchronization.

Conclusion

The techniques describe will work with most of the Kyocera MIP displays. The only changes will be to the resolution. Different resolutions will require different write times to accommodate the correct number of display lines. The display is very robust, it is virtually impossible to damage the display by writing incorrect data. Once data is written to the display it will remain as long as power is applied. Once power is removed the data in the memory is lost.

Power up/Power down

6-2. Power ON-OFF sequence



Item	Symbol	Min.	Typ.	Max.	Unit
Power ON-OFF sequence	t1	0	—	—	μsec
	t2	(1)	(10)	—	msec
	t3	(1)	(10)	—	msec
	t4	(1)	(10)	—	msec

Powering the MIP display is straight forward. Once VDD is valid the internal controller becomes active. Even though reset (RST) is applied the controller is active and data can be written to the MIP memory. The RST signal suppresses the operation of the display circuitry so no image will be displayed while the signal is asserted. It is recommended that the user writes zeros into memory before releasing the reset signal. When the display is powered up the MIP memory will be in a random state. If RST is released before memory is cleared random data will be displayed on the screen until the memory is written. This does not damage the MIP display but some users will find the random data objectionable. It is also recommended to apply the RST during power down. This will blank the screen immediately. Not applying reset may result in the image slowly fading away. This does not damage the display but may look objectionable.