Preliminary Product Specification | Rev. 0.85|

G2 **Silver**

M.2 2280 PCIe NVMe SSD datasheet

120GB – 1,920GB

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1. Product Summary

Capacity Range	**120GB – 1,920GB**
Form Factor	**M.2 2280-S2-M**
Host Interface	**PCIe Gen 3 x 4 lanes**
Command Set	**NVMe1.3d**
Performance	**Sequential read: up to 2,450 MB/s** **Sequential write: up to 1,900 MB/s** **Random read: up to 270K IOPS** **Random write: up to 420K IOPS**
Reliability	**MTBF: 2 million hours** **UBER: <1 sector / 10^{16} bits read**
Operating Temperature	
	Standard: 0°C ~ 70°C
Or	**Industrial: -40°C ~ 85°C**
Storage Temperature	**-40°C ~ 85°C**
Special Features	**Thermal throttling** **Security: AES256,** **TCG OPAL2.0(optional)** **Thermal Monitor**
Compliances	**RoHS*, CE*, FCC*, WEEE***

*Note: Please contact with Intelligent Memory represent for the detail of compliance conformity.

2. Order Information

Table 1 – Part Numbers

Part Number	Capacity	Operating Temperature range
IMP3M8B1E2A2A1C3A9A0000	120GB	0°c ~ 70°c
IMP3M8B3E2A2A1C3B2A0000	240GB	
IMP3M8B5E2A2A1C3B4A0000	480GB	
IMP3M8B7E2A2A1C3B6A0000	960GB	
IMP3M8B9E2A2A1C3B8A0000	1,920GB	
IMP3M8B1E2A2A1I3A9A0000	120GB	-40°c ~ 85°c
IMP3M8B3E2A2A1I3B2A0000	240GB	
IMP3M8B5E2A2A1I3B4A0000	480GB	
IMP3M8B7E2A2A1I3B6A0000	960GB	
IMP3M8B9E2A2A1I3B8A0000	1,920GB	

3. Product Information

I'M's M.2 2280 PCIe product family features a PCIe Gen3 x4 interface with a high sustained sequential data throughput of up to 2,450MB/s read & 1,900MB/s write. It is available in capacities up to 1,920GB, with customizable settings for Overprovisioning or Thermal Throttling.

3.1 Block Diagram

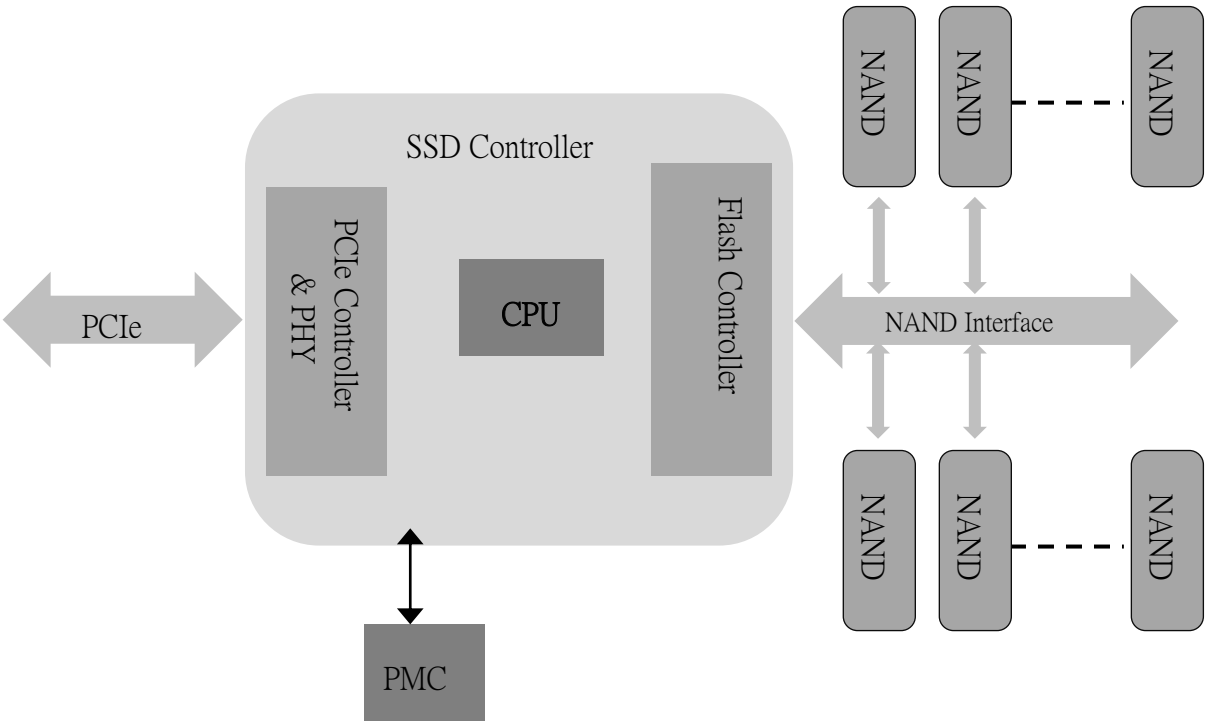


Figure 1 – Block Diagram

3.2 Product Features

Electrical/Physical Interface: *PCIe*

- PCIe Gen 3 x 4 lanes
- backward compatible to PCIe Gen 2 and Gen 1
- Compliant with NVMe 1.3d
- PCIe Express Base Ver. 3.1

Advanced Flash Management Features

LDPC ECC (Low Density Parity Check Error Correction Code)

The deterioration of the flash memory cell over time and the disruptions from neighboring flash memory pages can lead to random bit errors in the stored data. While the chances of any given data bit being corrupted is quite small, the vast number of data bits in a storage system makes the likelihood of data corruption a very real possibility. Error detection and correction codes are used in flash memory storage systems to protect the data from corruption.

Static and Dynamic Wear Leveling

Wear leveling is a process that helps reduce premature wearing out of NAND Flash devices. The Flash controller manages access to the NAND Flash memory devices and determines how the NAND Flash blocks are used. In most cases, the NAND Flash controller maintains a lookup table to translate the memory array's physical block address (PBA) to the logical block address (LBA) used by the host system known as Physical to Logical Address Translation Table.

Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "Initial Bad Blocks". Bad blocks that are developed during the lifespan of the flash are named "Later Bad Blocks"

S.M.A.R.T. functionality

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Overprovision

Over provisioning is a technique used in the design of flash SSDs and flash media cards. By providing extra memory capacity (which the user can't access) the SSD controller can more easily create pre-erased blocks ready to be used in the virtual pool.

Overprovisioning improves:

- Write performance & IOPS
- Reliability & endurance

Thermal Throttling

Thermal Throttling is applied to reduce the risk of overheating of an SSD under high workload and in a high temperature environment. Thermal Throttling automatically adjusts the SSDs performance in defined temperature areas to ensure its reliable operation.

I'M's M.2 2280 PCIe SSDs feature flexible thermal throttling which can be set according to the individual application's requirements.

Security Features

Secure Erase

Crypto Erase

PSID (Optional for TCG OPAL 2.0)

Quick Erase (Optional)

Write Protection (Optional)

Lifetime & Endurance Management

Terabytes Written (TBW)

Media Wear Indicator

Read Only Mode at End of Life

When the SSD reaches its endurance limit, it will automatically go into read-only mode to protect the data stored on it and assure functionality while it is being replaced

4. Product Specification

4.1 Performance

We specify the performance of our NAND products in as below:

- "**Peak**" describes the measured performance when the product is new and unused. It is commonly used by vendors in their datasheets. However, SSDs by design reduce performance after a relatively short usage period, so peak values cannot be used to predict an application's longer-term performance.

We are specifying peak performance for easier comparison of I'M's products with other solutions but recommend considering sustained performance values when selecting the most suitable solution for an application. Further detail can also be found in our whitepaper on performance (hyperlink)

Table 2 – Peak Performance

Capacity	Sequential performance		Random Performance	
	Read (MB/s)	Write (MB/s)	4K Read (IOPS)	4K Write (IOPS)
120GB	1150	550	95K	125K
240GB	2300	1100	160K	240K
480GB	2400	1800	230K	400K
960GB	2450	1900	270K	420K
1,920GB	2450	1900	270K	420K

Notes:
1. Peak performance measured in **Fresh Out of the Box (FOB**) condition
2. Sequential performance is measured with 128KB transfer size; QD32 and 4KB align with IO Meter.
3. Random performance tested with IO Meter: 4KB random write with QD32.
4. Performance may differ depending on application and platform.

4.2 Endurance and Reliability

4.2.1 Endurance

The lifetime of our NAND products is specified in TBW, i.e. the total amount of data that the host can write to the NAND media in a defined pattern. In our case this pattern is based on the workload definitions set by JEDEC in JESD219A.

Same as for performance, endurance specification varies greatly depending on the underlying assumptions (especially also if the formula set by JEDEC, including the guard band is used) and I'M recommend assuring these assumptions are the same when comparing TBW values of different products.

Our endurance whitepaper is available here and also offers a simple calculator to validate and analyze different endurance values

Table 3 – Tera Bytes Written

Capacity	TBW	TBW with guard band
120GB	110	55
240GB	240	120
480GB	520	260
960GB	1120	560
1,920GB	2400	1200
Notes: 1. TBW values are specified based on JEDEC 218 client workload 2. Actual lifetime may vary depending on platform and application		
Note: JEDEC specifies to consider guard band of 2 for calculating the TBW as a wear levelling factor as industrial applications need more rigid working conditions.		

4.2.2 Reliability

Table 4 – Reliability

Parameter	Value
UBER	Uncorrectable Bit Error Rate (UBER) < 1 sector per 10^{16} bits read
MTBF	2,000,000 Hours

4.3 Power Supply

Table 5 – Supply Voltage

Supply Voltage	
Parameter	Rating
Operative Voltage	3.3V, +/-5%
Rise Time (Max/Min)	100ms/0.1ms
Fall Time (Max/Min)	5s/1ms
Min. Off Time*1	1s
Notes *1: Minimum time between power removed from SSD (Vcc < 100 mW) and power re-applied to the drive	

4.4 Power Consumption

Table 6 – Power Consumption

Capacity	Read	Write
	Avg.	Avg.
120GB	2000	1600
240GB	3000	2200
480GB	3100	3000
960GB	3300	3200
1,920GB	3500	3400

Unit: mW

5. Environmental Specifications

5.1 Temperature and Humidity

Table 7 – High Temperature Test Condition

High Temperature Test			
Test Item		Temperature Standard/Wide Temp	Humidity
High Temperature Test	Operation	70°C/85°C	0% RH
	Storage	85°C	0% RH
Low Temperature Test	Operation	0°C /-40°C	0% RH
	Storage	-40°C	0% RH
High Humidity Test	Operation	40°C	90% RH
	Storage	40°C	93% RH
Temperature Cycle Test	Operation	0°C-70°C/-40°C-85°C	—
	Storage	-40°C ~ 85°C	—
Notes: 1. Operation temperature is measured by device temperature sensor. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.			

5.2 Shock and Vibration

Table 8 – Mechanical Test Condition

Items			Condition
Shock	Operating	Acceleration Force	50G, (11ms duration, half sine wave)
	Non-operating		1500G, (0.5ms duration, half sine wave)
Vibration	Non-operating	Frequency/Acceleration	80Hz~2000Hz(peak)/20G

5.1 EMC

Table 9 – EMC Compliance

Items	Condition
ESD Compliance	EN 55024, CISPR 24 EN 61000-4-2 IEC 61000-4-2
EMI Compliance	EN 55032, CISPR 32(CE) AS/NZS CISPR 32(CE) ANSI C63.4 (FCC) VCCI-CISPR 32 (VCCI) CNS 13438 (BSMI)

6. Interface

6.1 Pin Assignment and Descriptions

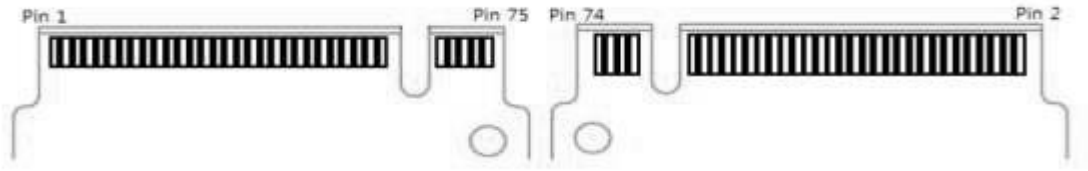


Figure 2 – Pin Locations

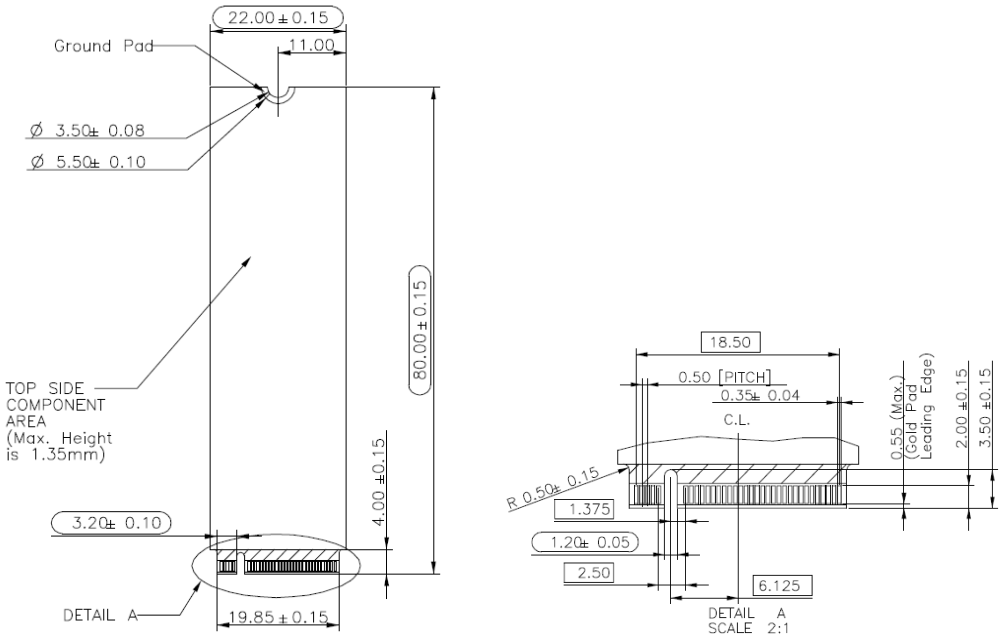
Table 10 – Signal Segment Pin Assignment and Descriptions

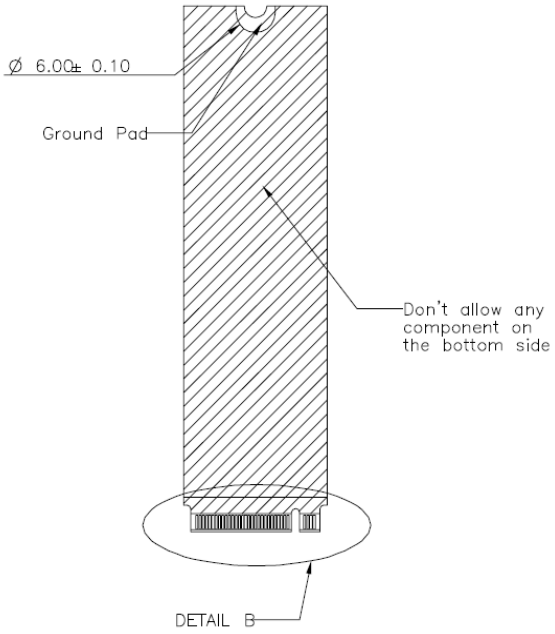
Signal and Power Pin Assignment and Description					
Pin #	Assignment	Description	Pin #	Assignment	Description
1	GND	Ground	2	3.3V	3.3V source
3	GND	Ground	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	N/C	N/C
9	GND	Ground	10	LED1#	Device Active Signal
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Ground	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Ground	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Ground	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Ground	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Ground	40	SMB_CLK	N/C
41	PETn0	PCIe TX	42	SMB_DATA	N/C
43	PETp0	PCIe TX	44	ALERT#	N/C
45	GND	Ground	46	N/C	N/C
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Ground	52	CLKREQ#	PCIe Device Clock Request

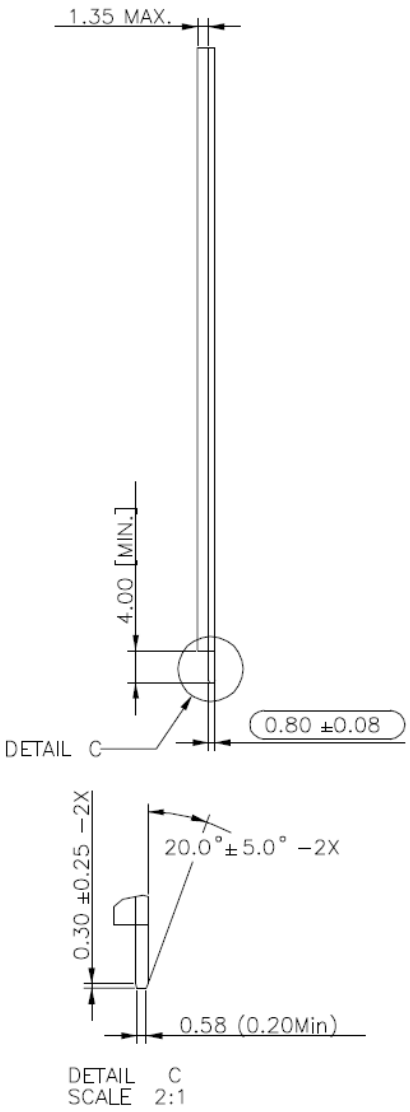
53	REFCLKN	PCIe Reference Clock	54	PEWAKE#	PCIe PME Wake
55	REFCLKP	PCIe Reference Clock	56	MFG DATA	Reserved for MFG DATA . Should left N/C in platform
57	GND	Ground	58	MFG CLOCK	Reserved for MFG CLOCK. Should left N/C in platform
59		Module Key	60		Module Key
61			62		
63			64		
65			66		
67	N/C	N/C	68	SUSCLK	32.768 kHz clk input by host
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Ground	72	3.3V	3.3V source
73	GND	Ground	74	3.3V	3.3V source
75	GND	Ground			

7. Physical Dimensions

80.00mm(L) x 22.00mm(W) x 3.50mm(H)







Notes: General Tolerance +/- 0.15mm

Figure 3 – Device Physical Dimension

8. Command Set

8.1 NVMe Admin Command List

Table 11 – Admin Commands

Identifier	O/M	Command Description
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Feature
0Ah	M	Get Feature
0Ch	M	Asynchronous Event Request
0Dh		Namespace Management
10h	O	Firmware Commit
11h	O	Firmware Image Download
14h	O	Device Self-Test
15h		Namespace Attachment
18h	O	Keep Alive
80h	O	Format NVM
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize

8.2 NVMe I/O Commands

Table 12 – I/O Commands

Identifier	O/M	Command Description
00h	O	Flush
01h	O	Write
02h	O	Read
04h	O	Write Uncorrectable
05h	O	Compare
08h	O	Write Zeroes
09h	O	Dataset Management

8.3 NVMe Set Feature Commands

Table 13 – Set Feature Commands

Set Feature Commands		
Identifier	O/M	Command Description
00h		Reserved
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number Of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Dh	O	Host Memory Buffer
0Eh	O	Timestamp
10h	O	Host Controlled Thermal Management
11h	O	Non-Operational Power State Config
0Eh-7Dh		Reserved
80h	O	Software Progress Marker

8.4 NVMe Get Log Page Commands

Table 14 – Get Log Page Commands

Get Log Page Commands		
Identifier	O/M	Command Description
00h		Reserved
01h	M	Error Information
02h	M	SMART / Health Information
03h	M	Firmware Slot Information
04h	O	Changed Namespace List
06h	O	Device Self-Test
09h-7Fh		Reserved
81h	O	Sanitize Status
82h-FFh		Reserved

8.5 Identify Device Command

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 15 – Identify Data Structure

Identify Data Structure			
Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	
03:02	M	PCI Subsystem Vendor ID (SSVID)	
23:04	M	Serial Number (SN)	
63:24:00	M	Model Number (MN)	Vendor Specify
71:64	M	Firmware Revision (FR)	TBD
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	Assigned by IEEE/RAC
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x06
79:78	M	Controller ID (CNTLID)	0x0001
83:80	M	Version (VER)	0x00010300
87:84	M	RTD3 Resume Latency (RTD3R)	0x00124F80
91:88	M	RTD3 Entry Latency (RTD3E)	0x002191C0
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000200
99:96	M	Controller Attributes (CTRATT)	0x0000
239:100	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x00
257:256	M	Optional Admin Command Support (OACS)	0x0017
258	M	Abort Command Limit (ACL)	0x00
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x0A
262	M	Error Log Page Entries (ELPE)	0x0F
263	M	Number of Power States Support (NPSS)	0x00
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x00
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x0166
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0170
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x64
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000
295:280	O	Total NVM Capacity (TNVMCAP)	**

Bytes	O/M	Description	Default Value
311:296	O	Unallocated NVM Capacity (UNVMCAP)	**
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x001F1F0002
317:316	O	Extended Device Self-test Time (EDSTT)	0x001E
318	O	Device Self-test Options (DSTO)	0x01
319	O	Firmware Update Granularity (FWUG)	0x04
321:320	O	Keep Alive Support (KAS)	0x0001
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x0001
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x0111
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x0166
331:328	O	Sanitize Capabilities (SANICAP)	0x00000007
511:332		Reserved	0x0
NVMe Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x0000
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0x005E
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x05
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	0x00FF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x0000
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
767:540	M	Reserved	0x00
I/O Command Set Attributes			
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	0x00
2047:1024	-	Reserved	0x00
2079:2048	M	Power State 0 Descriptor (PSD0)	0x0081031600401C52000000000000000258000002 5800000316
2111:2080	O	Power State 1 Descriptor (PSD1)	0x0081031600401C52010101010000000258000002 5800000316
2143:2112	O	Power State 2 Descriptor (PSD2)	0x0081031600401C52020202020000000258000002 5800000316
2175:2144	O	Power State 3 Descriptor (PSD3)	0x0081031600401C52030303030000003E8000003 E8030003E8
2207:2176	O	Power State 4 Descriptor (PSD4)	0x0081031600401C52240404040000186A0000013 8803000032

2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
Bytes	O/M	Description	Default Value
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State 26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00
Vendor Specific			
3278:3072	O	Vendor Specific (VS)	0x00
3279	O	Vendor Specific (VS)	0x00
4095:3080	O	Vendor Specific (VS)	Intelligent Memory Reserved

* The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html.
**Depends on the using of capacity

Table 16 – Identify Data Namespace Structure & NVMe Command Set Specific

Bytes	O/M	Description	Default Value
07:00	M	Namespace Size (NSZE)	TBD
15:08	M	Namespace Capacity (NCAP)	TBD

23:16	M	Namespace Capacity (NUSE)	TBD
24	M	Namespace Features (NSFEAT)	0x00
25	M	Number of LBA Formats (NLBAF)	0x01
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x00
28	M	End-to-end Data Protection Capabilities (DPC)	0x00
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x00
31	O	Reservation Capabilities (RESCAP)	0x00
32	O	Format Progress Indicator (FPI)	0x00
33		Reserved	0x09
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46		Reserved	
63:48	O	NVM Capacity (NVMCAP)	0x00
103:64		Reserved	
119:104	O	Namespace Globally Unique Identifier (NGUID)	
127:120	O	IEEE Extended Unique Identifier (EUI64)	
131:128	M	LBA Format 0 Support (LBAF0)	0x1090000
135:132	O	LBA Format 1 Support (LBAF1)	0xC000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000

383:192		Reserved	0x00

8.6 Identify Namespace Data Structure

Table 17 – List of Identify Namespace Data Structure for Each Capacity

Namespace Data Structure		
Capacity (GB)	Byte [7:0]: Namespace Size (NSZE)(Hex)	Byte [7:0]: Namespace Size (NSZE)(Dec)
120	DF94BB0h	234,441,648
240	1BF244B0h	468,862,128
480	37E436B0h	937,703,088
960	6FC81AB0h	1,875,385,008
1920	DF8FE2B0h	3,750,748,848

8.7 S.M.A.R.T. Attributes

Table 18 – S.M.A.R.T. Attributes (Log Identifier 02h)

S.M.A.R.T. Attributes		
Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power on Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)

[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved

9. Revision History

Revision	Descriptions	Release Date
0.1	Preliminary release	May, 2022
0.85	Performance, Endurance details added	May, 2022