XDPL8219 design guide

For high power factor flyback converter with constant voltage output

About this document

Scope and purpose

This document is a design guide using XDPL8219 as the control IC of the front-stage high power factor (HPF) flyback converter, which regulates the secondary output voltage supply to the second-stage constant current (CC) converter for LED lighting applications.

Intended audience

This design guide is intended for power supply design engineers and field application engineers.

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1 Introduction

XDPL8219 regulates the constant voltage (CV) output of a high power factor (HPF) flyback, according to its feedback (FB) pin voltage signal, which is controlled by the secondary side regulation (SSR) feedback circuit via an isolated optocoupler, as shown in **Figure 1**.

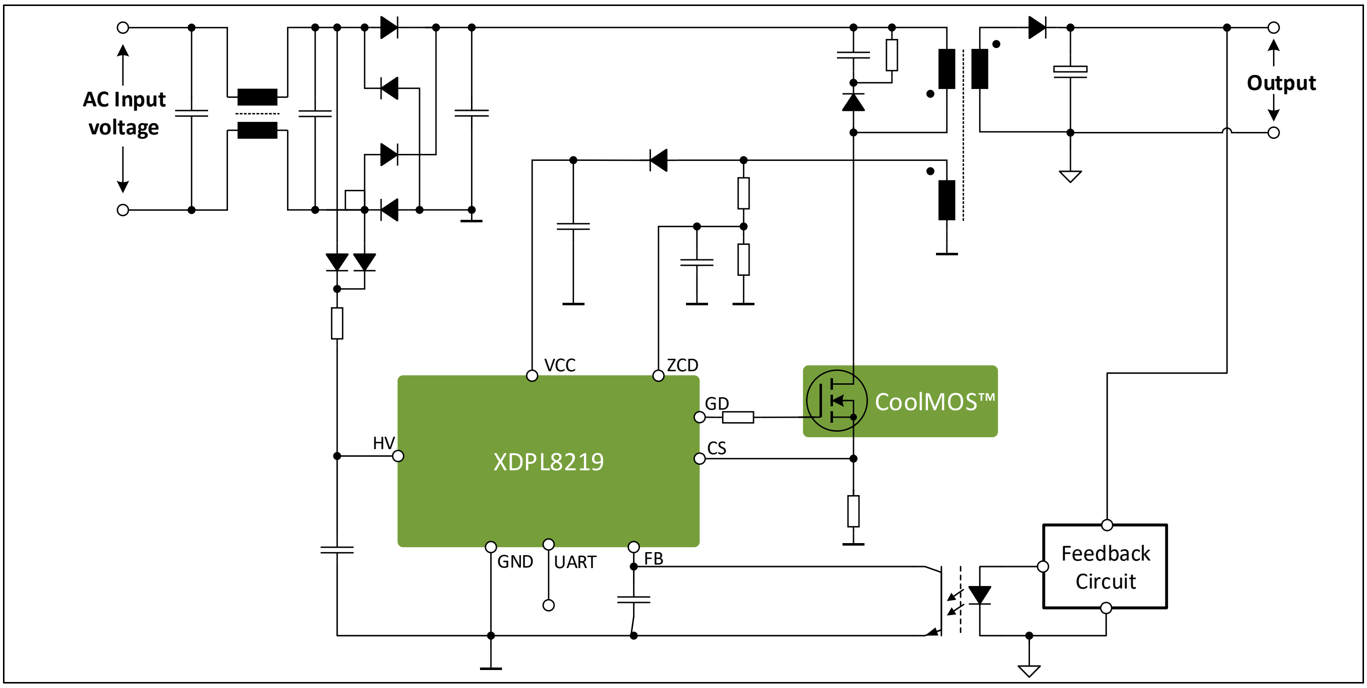


Figure 1 XDPL8219 flyback converter simplified circuitry with secondary-side regulated CV output

For LED lighting applications, XDPL8219 flyback CV output should be converted to a CC output by a second-stage DC-DC switching or linear regulator.

The device operates in quasi-resonant mode with multiple valley number switching (QRMn), to maximize the efficiency and minimize the EMI, across a wide load range. It enters active burst mode (ABM) at light load to prevent audible noise and at the same time achieving no-load standby power as low as < 100 mW. It also has a unique feature called UART reporting, which can be enabled to transmit data.

XDPL8219 comes in a PG-DSO-8 package. The main functions of each pin are shown in **Table 1**.

Table 1 XDPL8219 pin definitions and functions

Name	Pin	Type	Function(s)
ZCD	1	Input	Zero-crossing detection: The ZCD pin is connected to the transformer auxiliary winding via external resistors divider. It is used for zero-crossing detection, primary-side output voltage sensing and input voltage sensing.
FB	2	Input	Secondary side feedback: The FB pin is used as a feedback pin for secondary side regulation.
CS	3	Input	Current sensing: The CS pin is used for flyback MOSFET current sensing via external shunt resistor.

Name	Pin	Type	Function(s)
GD	4	Output	Gate driver: The GD pin is used for flyback MOSFET gate drive control via external series resistor.
HV	5	Input	High voltage: The HV pin is connected to the rectified input voltage via external series resistor. The HV pin is used to charge V_{CC} pin voltage during start-up and protection, via an internal 600 V start-up cell. In addition, it is also used for line synchronization.
UART	6	Input /Output	Universal asynchronous receiver transmitter (UART): The UART pin is used as the digital interface for IC parameter configuration. It can also be used for the information reporting based on the unidirectional UART communication (when UART reporting is enabled).
V_{CC}	7	Input	Operating voltage supply and sensing
GND	8	–	IC grounding

Note: By default, the configurable parameters of a new XDPL8219 chip from Infineon are empty, so it is necessary to configure them before any application testing.

Figure 2 shows the XDPL8219 design guide document sectioning for each step of the recommended design flow.

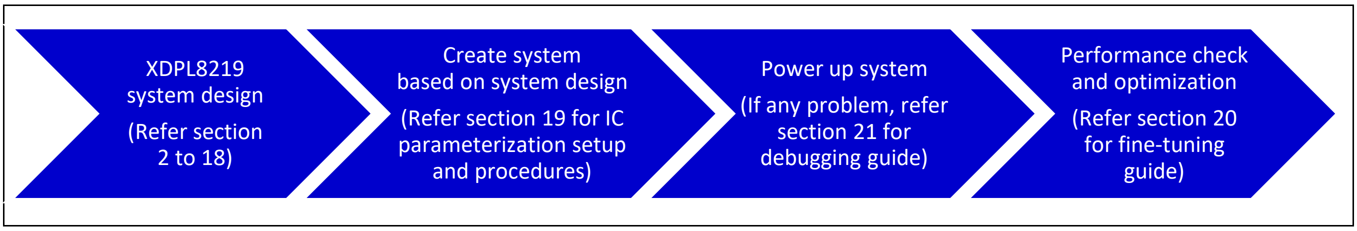


Figure 2 XDPL8219 design guide document sectioning for each step of the recommended design flow

2 Design specifications

A front-stage HPF flyback converter with CV output set-point $V_{out,setpoint}$ of 54 V (54 V/0.8 A) has been selected as a design example. The design specifications are shown in **Table 2**.

Table 2 Design specifications

Specification	Symbol	Value	Unit
Normal operational minimum AC input voltage	$V_{AC,min}$	90	V_{rms}
Normal operational maximum AC input voltage	$V_{AC,max}$	305	V_{rms}
Normal operational AC input frequency	F_{line}	47 ~ 63	Hz
Secondary-side regulated CV output set-point	$V_{out,setpoint}$	54	V
Steady-state output load current	I_{out}	0 ~ 800	mA
Steady-state full-load output power	$P_{out,full}$	43.2	W
Minimum efficiency at $P_{out,full}$	$\eta_{min,at,P,out,full}$	90	%
Target minimum switching frequency at $P_{out,full}$	$f_{sw,min,at,P,out,full}$	52	kHz

Note: *$P_{out,full}$ of 43.2 W is defined in this design example, to be able to supply a second-stage CC converter which has minimum efficiency of 93 percent (or maximum 3.2 W loss) at full load, for a 40 W LED driver design.*

Note: *The recommended $f_{sw,min,at,P,out,full}$ is between 45 kHz and 65 kHz. In general, higher $f_{sw,min,at,P,out,full}$ value would result in a smaller flyback transformer with lower efficiency, while lower $f_{sw,min,at,P,out,full}$ value would result in a larger flyback transformer with higher efficiency.*

3 Transformer design

To achieve both high efficiency and high power quality in the quasi-resonant valley switching operation, the flyback transformer primary main winding to secondary main winding turns ratio, N, should be high enough, but without exceeding the flyback MOSFET drain-source breakdown voltage $V_{(BR)DSS}$. Based on the $V_{AC,max}$ requirement of 305 V_{rms}, MOSFET **$V_{(BR)DSS}$ = 800 V** is selected for a good price to performance ratio.

To reduce transformer leakage inductance for low MOSFET voltage spike $V_{spike,FET}$, transformer design with sandwich construction as shown in **Figure 3** is recommended. Additionally, with the primary RCD snubber network deployed across the primary main winding (see **Figure 1**), $V_{spike,FET}$ can be estimated to be around 30 percent to 45 percent of $V_{AC,max}$ as a rule of thumb. In this design example, $V_{AC,max}$ is 305 V_{rms}, so we simply **assume $V_{spike,FET}$ = 100 V**, which is approximately 33 percent of $V_{AC,max}$.

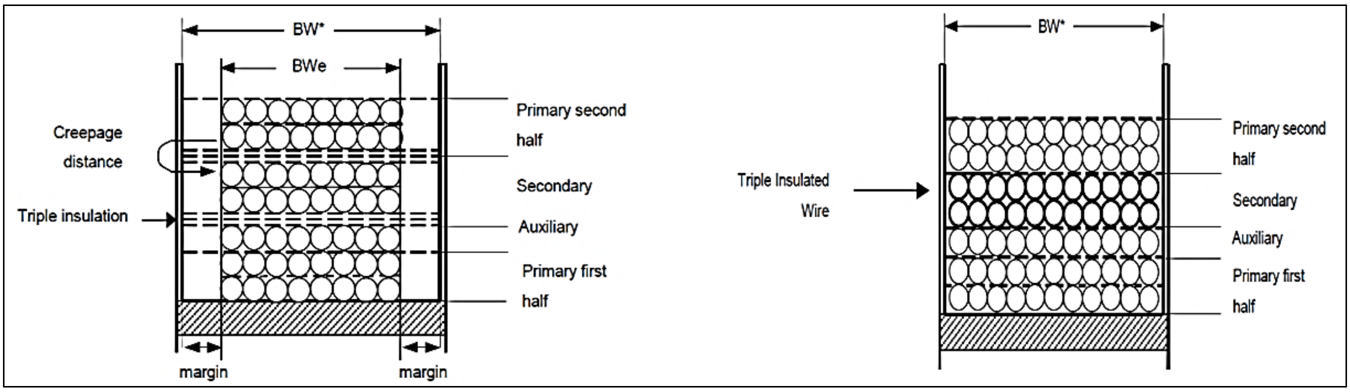


Figure 3 Transformer design with sandwich construction

For good reliability against input voltage surge, it is recommended to reserve a voltage margin $V_{margin,FET}$ of minimum 50 V from $V_{(BR)DSS}$. If XDPL8219 input overvoltage protection (OVP) would be enabled later in **Section 6**, as a rule of thumb, $V_{margin,FET}$ should be at least 25 percent of $V_{AC,max}$, which is equivalent to 76.25 V based on $V_{AC,max}$ of 305 V_{rms}. In this design example, **$V_{margin,FET}$ = 90 V** is selected.

Based on the above, N can be defined as:

$$N \leq \frac{V_{(BR)DSS} - V_{AC,max(pk)} - V_{spike,FET} - V_{margin,FET}}{V_{out,setpoint} + V_d} \tag{1}$$

Where $V_{AC,max(pk)}$ is √2 times $V_{AC,max}$, and V_d is the secondary main output diode forward voltage.

Taking V_d = 0.7 V, N can then be calculated as:

$$N \leq \frac{800 - \sqrt{2} \cdot 305 - 100 - 90}{54 + 0.7} = 3.27$$

Based on the above, **N = 3.2** is selected.

The maximum primary peak current $I_{pri(pk),max}$ can then be defined and calculated as:

$$I_{pri(pk),max} \approx \frac{4 \cdot P_{out,full}}{\eta_{min,at,P,out,full}} \cdot \left[\frac{1}{N \cdot (V_{out,setpoint} + V_d)} + \frac{1}{V_{AC,min(pk)}}\right] \tag{2}$$

Where $V_{AC,min(pk)}$ is √2 times $V_{AC,min}$.

$$I_{pri(pk),max} \approx \frac{4 \cdot 43.2}{90\%} \cdot \left[\frac{1}{3.2 \cdot (54 + 0.7)} + \frac{1}{\sqrt{2} \cdot 90}\right]$$

$$\boldsymbol{I_{pri(pk),max} \approx 2.606\ A}$$

As a result, the primary main winding inductance L_p can be defined and calculated as:

$$L_p = \frac{V_{AC,min(pk)} \cdot N \cdot (V_{out,setpoint} + V_d)}{I_{pri(pk),max} \cdot f_{sw,min,at,P,out,full} \cdot [V_{AC,min(pk)} + N \cdot (V_{out,setpoint} + V_d)]} \quad (3)$$

$$L_p = \frac{\sqrt{2} \cdot 90 \cdot 3.2 \cdot (54 + 0.7)}{2.606 \cdot 52 \cdot 10^3 \cdot [\sqrt{2} \cdot 90 + 3.2 \cdot (54 + 0.7)]}$$

$$\boldsymbol{L_p = 544\ \mu H}$$

Based on core cross-sectional area, A_e = 120.1 mm^2 and saturation flux density at 100°C, $B_{sat(T=100°C)}$ = 0.41 Tesla for TDG PQ26/20 core with TPW33 material, the transformer primary main winding turns N_p can be defined as:

$$N_p \geq \frac{L_p \cdot I_{pri(pk),max}}{A_e \cdot B_{sat(T=100°C)} \cdot D_{f,Bsat}} \quad (4)$$

Where $D_{f,Bsat}$ is the derating factor to ensure the designed transformer maximum flux density B_{max} is below $B_{sat(T=100°C)}$ by a margin of (100 percent - $D_{f,Bsat}$) from saturation, and it is typical to set $D_{f,Bsat}$ in the range of 85 percent to 95 percent for a margin of 5 percent to 15 percent from transformer core saturation.

Taking $D_{f,Bsat}$ = 90 percent, N_p can then be calculated as:

$$N_p \geq \frac{544 \cdot 10^{-6} \cdot 2.606}{120.1 \cdot 10^{-6} \cdot 0.41 \cdot 90\%} = 31.99$$

Based on the above, **N_p = 32** is selected.

The transformer secondary main winding turns N_s can then be calculated as:

$$N_s = \frac{N_p}{N} = \frac{32}{3.2}$$

$$\boldsymbol{N_s = 10}$$

To ensure fast V_{CC} supply takeover from the primary auxiliary winding for avoiding IC reset during start-up, and also to be able to deliver peak gate-drive voltage $V_{GD,peak}$ of 12 V with high enough primary auxiliary winding V_{CC} supply during steady-state, the minimum primary auxiliary winding demagnetization voltage **$V_{a,min}$ = 14 V** is therefore defined. As a result, the recommended minimum primary auxiliary winding turns $N_{a,min}$ can be defined and calculated as:

$$N_{a,min} = \frac{V_{a,min} \cdot N_s}{(V_{out,setpoint} + V_d)} = \frac{14 \cdot 10}{(54 + 0.7)} = 2.56 \quad (5)$$

To minimize the IC power consumption and, V_{CC} voltage should not exceed 19 V, the maximum auxiliary winding demagnetization voltage **$V_{a,max}$ = 19** is therefore defined. As a result, the recommended maximum primary auxiliary winding turns $N_{a,max}$ can be defined and calculated as:

$$N_{a,max} = \frac{V_{a,max} \cdot N_s}{(V_{out,setpoint} + V_d)} = \frac{19 \cdot 10}{(54 + 0.7)} = 3.47 \quad (6)$$

Based on the calculation results of equations (5) and (6), primary auxiliary winding turns **N_a = 3** is selected.

A secondary auxiliary winding is added to supply the operating voltage of the secondary side regulation (SSR) FB circuit, since its op-amp or shunt regulator's maximum operating voltage is less than $V_{out,setpoint}$ of 54 V. The recommended minimum secondary auxiliary winding turns $N_{a,sec,min}$ and recommended maximum secondary auxiliary winding turns $N_{a,sec,max}$ can be defined respectively as per $N_{a,min}$ and $N_{a,max}$, as shown below:

$$N_{a,sec,min} = N_{a,min} = 2.56 \quad (7)$$

$$N_{a,sec,max} = N_{a,max} = 3.47 \quad (8)$$

Based on the calculation results of equations (7) and (8), secondary auxiliary winding turns **$N_{a,sec}$ = 3** is selected.

4 Flyback MOSFET and secondary main output diode selection

The CoolMOS™ P7 MOSFET series is the latest CoolMOS™ product family and targets customers looking for high performance and at the same time being price sensitive. Through optimizing key parameters (C_{oss}, E_{oss}, Q_G, C_{iss} and $V_{GS(th)}$); integrating Zener diode for ESD protection and other measures, this product family fully addresses market concerns in performance, ease-of-use, and price/performance ratio, delivering best-in-class performance with exceptional ease-of-use, while still not compromising on price/performance ratio. The 700 V and 800 V types of the CoolMOS™ P7 series have been designed for flyback and could also be used in PFC topologies.

MOSFET drain-source breakdown voltage $\mathbf{V_{(BR)DSS} = 800\ V}$ is selected in this design example based on $V_{AC,max}$ of 305 V_{rms} and transformer design in **Section 3**.

Before selecting which MOSFET drain-source on-resistance at room temperature $R_{ds(on),25°C}$ is to be used, the maximum primary rms current $I_{pri(rms),max}$ has to be estimated based on:

$$I_{pri(rms),max} \approx I_{pri(pk),max} \cdot \sqrt{\frac{k}{3}} \qquad (9)$$

Where k is a number obtained from the function curve in **Figure 4**, based on the variable factor of $\frac{V_{AC,min(pk)}}{N \cdot (V_{out,setpoint} + V_d)}$.

In this design example, the variable factor of $\frac{V_{AC,min(pk)}}{N \cdot (V_{out,setpoint} + V_d)}$ can be calculated as:

$$\frac{V_{AC,min(pk)}}{N \cdot (V_{out,setpoint} + V_d)} = \frac{\sqrt{2} \cdot 90}{3.2 \cdot (54 + 0.7)} = 0.727$$

Referring to the function curve in **Figure 4**, k = 0.31 is obtained.

Based on equation (9), $I_{pri(rms),max}$ can then be calculated as:

$$I_{pri(rms),max} \approx 2.606 \cdot \sqrt{\frac{0.31}{3}}$$

$$\mathbf{I_{pri(rms),max} \approx 0.838\ A}$$

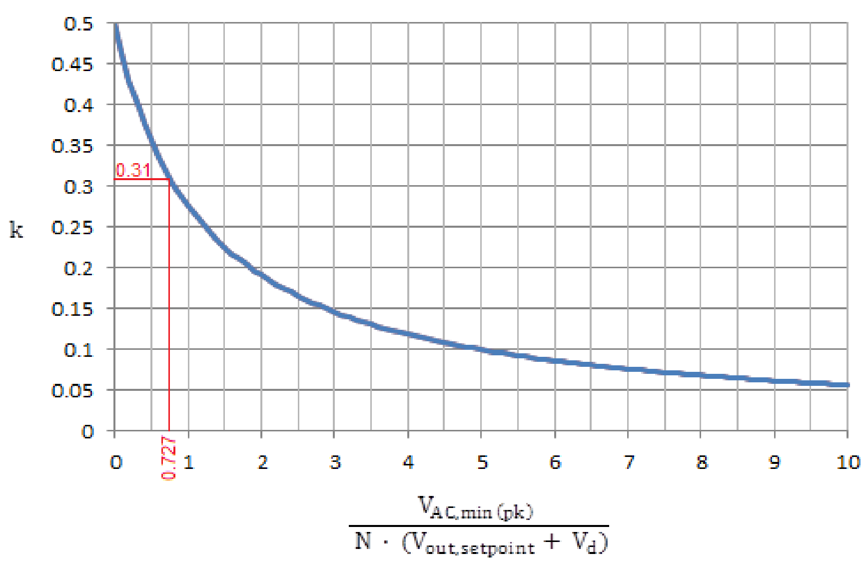


Figure 4 Function curve of k

The selectable MOSFET $R_{ds(on),25°C}$ can be defined as:

$$R_{ds(on),25°C} \leq \frac{m \cdot P_{out,full}}{I_{pri(rms),max}{}^2 \cdot \Delta R_{ds(on),100°C}} \quad (10)$$

Where m is the desired ratio of MOSFET conduction loss over $P_{out,full}$ and $\Delta R_{ds(on),100°C}$ is the ratio of $\frac{R_{ds(on),100°C}}{R_{ds(on),25°C}}$.

It is typical to select m in the range of 0.025 to 0.03 and $\Delta R_{ds(on),100°C}$ in the range of 1.75 to 1.85. Taking m = 0.0275 and $\Delta R_{ds(on),100°C}$ = 1.8, $R_{ds(on),25°C}$ can then be calculated as:

$$R_{ds(on),25°C} \leq \frac{0.0275 \cdot 43.2}{0.838^2 \cdot 1.8} = 0.94\ \Omega$$

Referring to the calculation results of equation (10) and **Table 3** below, **$R_{ds(on),25°C}$ = 900 mΩ** is selected.

To utilize the PCB as a heatsink for the MOSFET, **IPD80R900P7** with TO-252 (DPAK) package is selected.

Table 3 800 V CoolMOS™ P7 selection table

$R_{DS(on)}$ [mΩ]	TO-220 FullPAK	TO-220 FullPAK Narrow Lead	TO-252 DPAK	TO-220	TO-247	TO-251 IPAK	TO-251 IPAK SL	SOT-223
4500			IPD80R4K5P7			IPU80R4K5P7		IPN80R4K5P7
3300			IPD80R3K3P7			IPU80R3K3P7		IPN80R3K3P7
2400			IPD80R2K4P7			IPU80R2K4P7	IPS80R2K4P7	IPN80R2K4P7
2000			IPD80R2K0P7			IPU80R2K0P7	IPS80R2K0P7	IPN80R2K0P7
1400	IPA80R1K4P7		IPD80R1K4P7	IPP80R1K4P7		IPU80R1K4P7	IPS80R1K4P7	IPN80R1K4P7
1200	IPA80R1K2P7		IPD80R1K2P7	IPP80R1K2P7		IPU80R1K2P7	IPS80R1K2P7	IPN80R1K2P7
900	IPA80R900P7		IPD80R900P7	IPP80R900P7		IPU80R900P7	IPS80R900P7	IPN80R900P7
750	IPA80R750P7		IPD80R750P7	IPP80R750P7		IPU80R750P7	IPS80R750P7	IPN80R750P7
600	IPA80R600P7		IPD80R600P7	IPP80R600P7		IPU80R600P7	IPS80R600P7	IPN80R600P7
450	IPA80R450P7	IPAN80R450P7	IPD80R450P7	IPP80R450P7				
360	IPA80R360P7	IPAN80R360P7	IPD80R360P7	IPP80R360P7	IPW80R360P7			
280	IPA80R280P7	IPAN80R280P7	IPD80R280P7	IPP80R280P7	IPW80R280P7			

For the secondary main output diode selection, it is necessary to first estimate the maximum reverse voltage $V_{r(diode),max}$ and maximum secondary main winding peak current $I_{sec(pk),max}$, based on:

$$V_{r(diode),max} = V_{spike,diode} + V_{out,setpoint} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N} \quad (11)$$

Where $V_{spike,diode}$ is the diode reverse voltage spike.

Assuming $V_{spike,diode} \approx 35\% \cdot \left(V_{out,setpoint} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N}\right)$,

$$V_{r(diode),max} \approx 135\% \cdot \left(V_{out,setpoint} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N}\right) = 135\% \cdot \left(54 + \frac{\sqrt{2} \cdot 305 + 90}{3.2}\right)$$

$$V_{r(diode),max} \approx 292.81\ V$$

$$I_{sec(pk),max} \approx I_{pri(pk),max} \cdot \frac{N_p}{N_s} = 2.606 \cdot \frac{32}{10} \quad (12)$$

$$I_{sec(pk),max} \approx 8.34\ A$$

Based on the above, a secondary main output diode with repetitive reverse voltage rating **V_{RRM} = 300 V** is selected. To minimize its switching and conduction losses, the selected diode also has the properties of hyper-fast recovery speed and **low forward voltage drop at $I_{sec(pk),max}$.**

Additionally**, a RC secondary snubber network, e.g., 10 Ω resistor in series with 150 pF capacitor**, is deployed across the secondary main output diode, to suppress the diode reverse voltage spike and the EMI.

5 CS resistor and GD pin-related design

Figure 5 shows the connections of the current sense (CS) resistor R_{CS}, gate resistor R_G and gate source resistor R_{GS}.

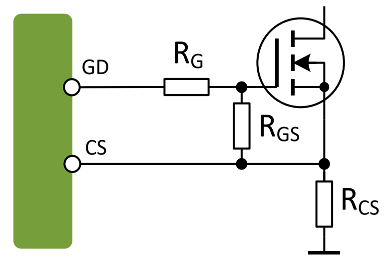


Figure 5 GD pin, CS pin, R_{CS}, R_G and R_{GS} connections

Based on the CS pin voltage across R_{CS}, the MOSFET current can be measured.

The recommended minimum CS resistor value $R_{CS,min}$ is defined and calculated as:

$$R_{CS,min} = \frac{0.45}{I_{pri(pk),max}} = \frac{0.45}{2.606} = 0.173\ \Omega \tag{13}$$

The recommended maximum CS resistor value $R_{CS,max}$ is defined and calculated as:

$$R_{CS,max} = \frac{0.54}{I_{pri(pk),max}} = \frac{0.54}{2.606} = 0.207\ \Omega \tag{14}$$

Based on the calculation results above, CS resistor **R_{CS} = 0.2 Ω** is selected in this design example.

R_G is to damp the gate-rise oscillation, and R_{GS} is to ensure the MOSFET gate has relatively low impedance to prevent it from being switched on undesirably. **R_G = 10 Ω** and **R_{GS} = 20 kΩ** are selected in this design example.

The gate-drive peak voltage $V_{GD,pk}$ is typically 12 V with sufficient V_{CC} voltage supply. To achieve a good balance of switching loss and EMI, the gate voltage rising slope can be controlled by configuring the gate driver peak source current parameter $I_{GD,pk}$ (configurable range: 30 mA to 118 mA). This saves two components (see $D_{fastoff}$, R_{slowon} in **Figure 6**), which are conventionally added for the same purpose.

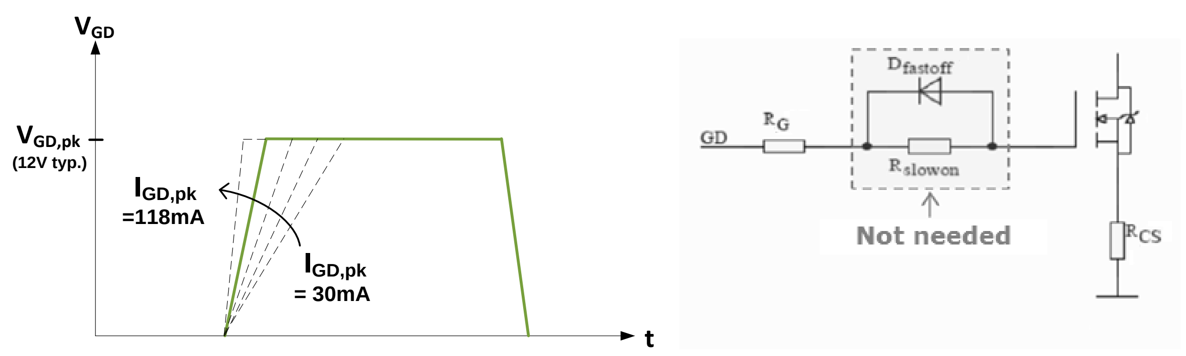


Figure 6 Gate-drive voltage rising slope control with $I_{GD,pk}$ parameterization for component saving

With the high-speed switching characteristics of CoolMOS™ P7 MOSFET, it is recommended to configure the $I_{GD,pk}$ parameter in the range of 30 mA to 49 mA.

As a result, **$I_{GD,pk}$ = 30 mA** is selected in this design example.

6 Input voltage parameters for operation, start-up and protection

The lowest operational input voltage parameter $V_{in,low}$ and the highest operational input voltage parameter $V_{in,high}$ can be defined and calculated as:

$$V_{in,low} = a \cdot V_{AC,min} \quad (15)$$

$$V_{in,high} = b \cdot V_{AC,max} \quad (16)$$

Where a is recommended to be between 0.9 and 0.95, and b is recommended to be between 1.05 and 1.10.

Taking a = 0.91 and b = 1.07,

$$\boldsymbol{V_{in,low} = 82\ V_{rms}}$$

$$\boldsymbol{V_{in,high} = 326\ V_{rms}}$$

$EN_{OVP,In}$ parameter refers to the enable switch for maximum input voltage start-up check and input OVP, based on $V_{in,start,max}$ and V_{inOV} levels, respectively. **$EN_{OVP,In}$ = Enabled** is selected in this design example.

$EN_{UVP,In}$ parameter refers to the enable switch for minimum input voltage start-up check and input UVP, based on $V_{in,start,min}$ and V_{inUV} levels, respectively. **$EN_{UVP,In}$ = Enabled** is selected in this design example.

$V_{in,start,max}$ parameter refers to the maximum input voltage level setting for start-up, which is recommended to be configured as $V_{in,high}$. Hence, **$V_{in,start,max}$ = 326 V_{rms}** is selected in this design example. V_{inOV} parameter refers to the input OVP level setting, which is recommended to be:

$$V_{inOV} \geq V_{in,start,max} \cdot 107\% = 349\ V_{rms} \quad (17)$$

$V_{in,start,min}$ parameter refers to the minimum input voltage level setting for start-up, which is recommended to be configured as $V_{in,low}$. Hence, **$V_{in,start,min}$ = 82 V_{rms}** is selected in this design example. V_{inUV} parameter refers to the input UV (brown-out) protection level setting, which is recommended as:

$$V_{inUV} \leq V_{in,start,min} \cdot 93\% = 76\ V_{rms} \quad (18)$$

Based on the above, **V_{inOV} = 350 V_{rms}** and **V_{inUV} = 70 V_{rms}** are selected in this design example.

The input voltage protections (based on V_{inOV} and V_{inUV}) in ABM can be optionally enabled with $EN_{VIN,ABM}$ parameter. If $EN_{VIN,ABM}$ is enabled, the enable switches for V_{inOV} and V_{inUV} protections in ABM are respectively based on $EN_{OVP,In}$ and $EN_{UVP,In}$. In this design example, **$EN_{VIN,ABM}$ = Enabled** is selected. The input OVP blanking period number parameter **$t_{VinOV,blank}$ = 1** is recommended and selected in this design example.

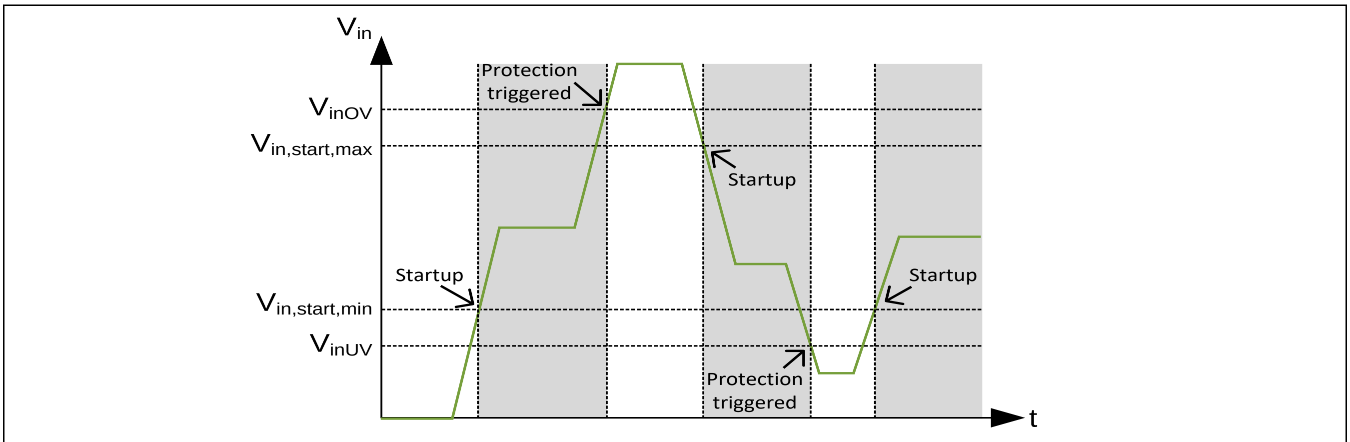


Figure 7 Input voltage levels for start-up and protection (with auto restart reaction)

7 HV pin-related design

As shown in **Figure 8**, HV series resistor R_{HV} is connected from the HV pin to the cathodes of HV diode D_{HV1} and D_{HV2}, while bridge rectifier AC input should be applied across the D_{HV1} anode and D_{HV2} anode.

A high voltage capacitor C_{HV} should also be connected between the HV pin and ground, to filter the switching noise for a robust HV pin line synchronization. In addition, C_{HV} also improves the input voltage surge and ESD capability of the HV pin.

The repetitive reverse voltage rating **V_{RRM} = 1000 V** for D_{HV1} and D_{HV2} is recommended and selected in this design example, to ensure good reliability of the diodes against input voltage surge.

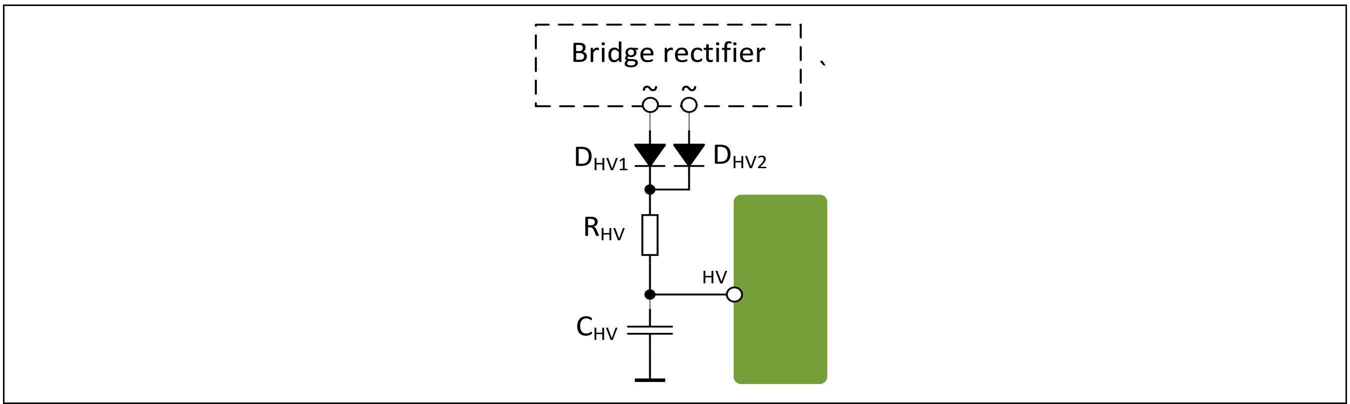


Figure 8 HV pin, R_{HV}, C_{HV}, D_{HV1} and D_{HV2} connections

The recommended minimum HV series resistor value $R_{HV,min}$ is defined and calculated as:

$$R_{HV,min} = \frac{V_{in,high(pk)}}{I_{HV,max}} \quad (19)$$

Where $I_{HV,max}$ is the HV pin maximum peak input current of 9.6 mA, and $V_{in,start,max(pk)}$ is √2 times $V_{in,high}$.

$$R_{HV,min} = \frac{\sqrt{2} \cdot 326}{9.6 \cdot 10^{-3}} = 48\ k\Omega$$

The recommended maximum HV series resistor value $R_{HV,max}$ is defined and calculated as:

$$R_{HV,max} = Min\left[10^5, \frac{V_{AC,min(rect,avg)} - V_{VCCON,max}}{I_{HV,min(avg)}} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{V_{VCCON,max}}{V_{AC,min(pk)}}\right)\right]\right] \quad (20)$$

Where $V_{AC,min(rect,avg)}$ is the average value of the rectified $V_{AC,min}$, while $V_{VCCON,max}$ is the maximum V_{CC} turn-on voltage threshold of 22 V, and $I_{HV,min(avg)}$ is the recommended HV pin minimum average input current of 1 mA.

$$R_{HV,max} = Min\left[10^5, \frac{0.9 \cdot 90 - 22}{1 \cdot 10^{-3}} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{22}{\sqrt{2} \cdot 90}\right)\right]\right]$$

$$R_{HV,max} = 52.5\ k\Omega$$

Based on the above, the HV resistor value and IC parameter setting of **R_{HV} = 52 kΩ** are selected in this design example.

The HV series resistor dielectric withstand voltage should be above the total of $V_{AC,max(pk)}$ and $V_{margin,FET}$ (from **Section 3**), which is equivalent to 521.3 V. As an example, the selected R_{HV} = 52 kΩ in this design example can be formed using a 36 kΩ 0.5 W resistor (dielectric withstand of 350 V) in series with a 16 kΩ 0.25 W resistor (dielectric withstand of 200 V).

C_{HV} = 1 nF is recommended and selected in this design example.

8 DC link filter and secondary output capacitance

$C_{DC,filter}$ denotes the DC link filter capacitor placed after the bridge rectifier. A higher $C_{DC,filter}$ value gives lower EMI but worse power quality, and vice versa.

Table 4 Recommended initial $C_{DC,filter}$ value

$V_{AC,min}$ (V)	Steady-state full-load output power $P_{out,full}$ (W)	Recommended initial $C_{DC,filter}$ (μF)
90 ~ 107	Less than 26	0.1
	26 ~ 35	0.15
	35 ~ 44	0.22
	Greater than 45	Greater than 0.22
Greater than or equal to 108	Less than 31	0.1
	31 ~ 40	0.15
	40 ~ 55	0.22
	Greater than 55	Greater than 0.22

Referring to **Table 4**, **initial $C_{DC,filter}$ = 0.22 μF** is selected in this design example. To improve the estimated input voltage V_{in} accuracy during pre-start-up check, it is also recommended to deploy DC link resistor **$R_{DC,filter}$ = 30 MΩ** in parallel with $C_{DC,filter}$, as shown in **Figure 9**.

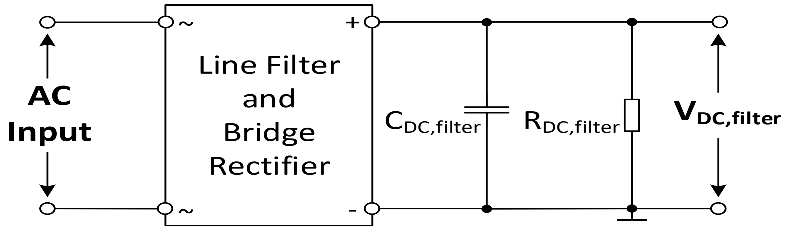


Figure 9 $C_{DC,filter}$ and $R_{DC,filter}$ across the DC link bus voltage

$V_{ripple,out(pk-pk),max}$ denotes the maximum allowable secondary main output voltage peak-to-peak ripple level. Assuming the flyback output in this design example is connected to a second-stage CC buck regulator, which has a maximum LED voltage load $V_{LED,max}$ of 48 V and maximum allowable duty cycle $D_{buck,max}$ of 95 percent, $V_{ripple,out(pk-pk),max}$ can be defined and calculated as:

$$V_{ripple,out(pk-pk),max} = 2 \cdot \left(V_{out,setpoint} - \frac{V_{LED,max}}{D_{buck,max}}\right) = 2 \cdot \left(54 - \frac{48}{0.95}\right) = 6.95\ V \quad (21)$$

The secondary main output capacitor $C_{out,main}$ value can then be defined and calculated as:

$$C_{out,main} \geq \frac{P_{out,full}}{2\pi \cdot F_{line,min} \cdot V_{ripple,out(pk-pk),max} \cdot V_{out,setpoint}} = \frac{43.2}{2\pi \cdot 47 \cdot 6.95 \cdot 54} = 390\ \mu F \quad (22)$$

Considering the electrolytic capacitor value tolerance, **$C_{out,main}$ = 470 μF** is selected in this design example.

For switching noise filtering, low-ESR ceramic capacitors **$C_{out,main,lowESR1}$ = 1 μF** and **$C_{out,main,lowESR2}$ = 0.1 μF** are also added in parallel with $C_{out,main}$.

The secondary auxiliary output capacitor $C_{out,aux,sec}$ is recommended to be at least 47 μF, to ensure stable operating voltage supply of the Secondary Side Regulation (SSR) FB circuit, during ABM.

$C_{out,aux,sec}$= 47 μF is selected in this design example.

9 V_{CC} capacitance and V_{CC} self-supply circuit

To fulfill the typical time-to-light requirement of 500 ms, the V_{CC} pin voltage maximum charging time for IC activation, $t_{VCCON,charge,max}$ should not exceed 350 ms. Therefore, the maximum V_{CC} capacitance $C_{VCC,max}$ can be defined and calculated as:

$$C_{VCC,max} = \frac{V_{AC,typ,low(rect,avg)} - V_{VCCON,max}}{R_{HV} \cdot V_{VCCON,max}} \cdot t_{VCCON,charge,max} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{V_{VCCON,max}}{V_{AC,typ,low(pk)}}\right)\right] \quad (23)$$

Where $V_{VCCON,max}$ is the maximum V_{CC} turn-on threshold of 22 V, $V_{AC,typ,low(rect,avg)}$ is the average value based on the rectified sine wave of the lowest typical input voltage, and $V_{AC,typ,low(pk)}$ is the peak of the lowest typical input voltage.

Take the lowest typical input voltage $V_{AC,typ,low}$ as 120 V_{rms} in this design example,

$$C_{VCC,max} = \frac{0.9 \cdot 120 - 22}{52 \cdot 10^3 \cdot 22} \cdot 350 \cdot 10^{-3} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{22}{\sqrt{2} \cdot 120}\right)\right] = 24.13\ \mu F$$

The V_{CC} capacitor value and IC parameter setting of **C_{VCC} = 22 μF** are selected. In addition, a noise decoupling ceramic capacitor of **$C_{VCCdecouple}$ = 0.1 μF** with low ESR is added in parallel to C_{VCC}.

Typically, the C_{VCC} and $C_{VCCdecouple}$ are the only capacitors needed to store the rectified auxiliary winding voltage for the V_{CC} voltage supply. An additional capacitor $C_{out,aux}$ and a blocking diode $D_{block,VCC}$ are however needed if the UART reporting feature is enabled, as shown in **Figure 10**, to increase the V_{CC} hold-up time for a proper UART reporting operation, while not increasing the $t_{VCCON,charge,max}$.

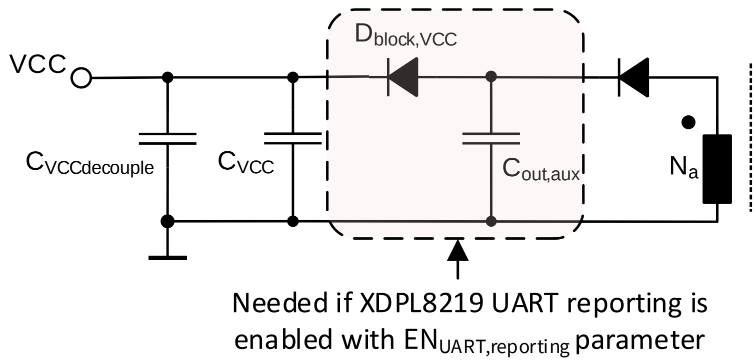


Figure 10 V_{CC} self-supply circuit

In this design example, the UART reporting is enabled, so **$D_{block,VCC}$** and **$C_{out,aux}$ = 220 μF** are added.

10 Pre-start-up check and start-up phase

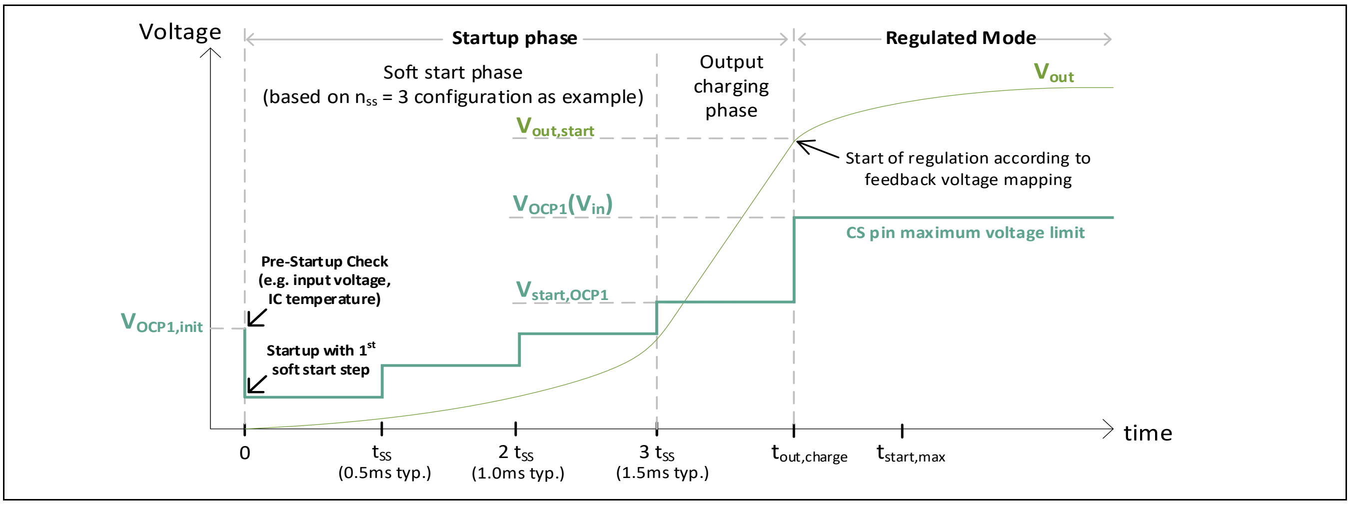


Figure 11 Pre-start-up check, start-up phase and regulated mode entering

Pre-start-up check ensures the estimated input voltage V_{in} and IC junction temperature T_j are within the configurable protection limits before start-up. During the pre-start-up check, the input voltage measurement switching pulse has an initial CS pin maximum voltage limit $V_{OCP1,init}$, which can be defined and calculated as:

$$V_{OCP1,init} = \frac{d \cdot R_{CS} \cdot V_{AC,max(pk)} \cdot t_{on,min,V,in,start,sense}}{L_p} \tag{24}$$

Where $t_{on,min,V,in,start,sense}$ is the minimum on-time for the MOSFET switching pulse to measure the input voltage during the pre-start-up check, and d is a ratio recommended to be between 1.3 and 1.4.

Take $t_{on,min,V,in,start,sense}$ = 1.38 µs, and d = 1.37,

$$V_{OCP1,init} = \frac{1.37 \cdot 0.2 \cdot \sqrt{2} \cdot 305 \cdot 1.38 \cdot 10^{-6}}{544 \cdot 10^{-6}}$$

$$\boldsymbol{V_{OCP1,init} = 0.3\ V}$$

During the start-up phase, the soft start phase is initiated and followed by the output charging phase. The soft start phase minimizes the component stress by limiting the CS pin maximum voltage for a number of steps based on n_{ss} parameter. **n_{SS} = 3** setting is recommended and selected. The output charging phase fast-charges the estimated output voltage V_{out} to the $V_{out,start}$ parameter value for fast V_{CC} self-supply from the primary auxiliary winding, with the MOSFET switching pulses based on either the CS pin maximum voltage limit of $V_{start,OCP1}$, or the maximum on-time of $t_{on,max}(V_{in})$, in QRMn operation.

$V_{start,OCP1}$ and $V_{out,start}$ parameters can be defined and calculated as:

$$V_{start,OCP1} = I_{pri(pk),max} \cdot R_{CS} = 2.606 \cdot 0.2 \tag{25}$$

$$\boldsymbol{V_{start,OCP1} = 0.52\ V}$$

$$V_{out,start} = \frac{V_{a,start} \cdot N_s}{N_a} - V_d \tag{26}$$

Where $V_{a,start}$ is the desired primary auxiliary winding demagnetization voltage when output voltage is $V_{out,start}$. $V_{a,start}$ is recommended to be between 9 V and 10.5 V. So, taking $V_{a,start}$ = 9.5 V,

$$V_{out,start} = \frac{9.5 \cdot 10}{3} - 0.7$$

$$\boldsymbol{V_{out,start} = 31\ V}$$

11 Output UVP-related design

In start-up phase, if the estimated output voltage V_{out} is lower than the $V_{out,start}$ parameter level over a time-out period of $t_{start,max}$ parameter, the start-up output UVP is triggered, as shown in **Figure 12 (right)**. $t_{start,max}$ parameter can be indirectly configured with V_{CC} capacitance parameter C_{VCC}, based on:

$$t_{start,max} = 967 \cdot C_{VCC} \quad (27)$$

Based on the earlier selected C_{VCC} = 22 µF and equation (27), **$t_{start,max}$ = 21.3 ms** is applied in this design example.

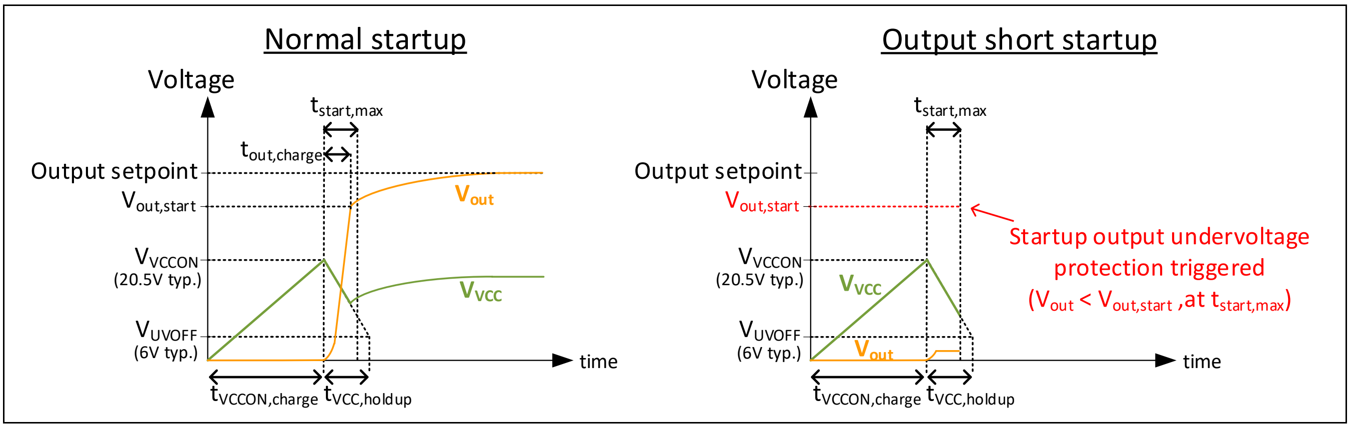


Figure 12 Normal start-up and start-up output UVP (short) waveforms

In regulated mode, **$EN_{UVP,Vout}$ = Enabled** parameter setting is selected, to enable the regulated mode output UVP, which can be triggered if the estimated output voltage V_{out} is below the regulated mode output UVP level V_{outUV} for longer than a blanking time of $t_{VoutUV,blank}$ parameter. V_{outUV} parameter can be defined and calculated as:

$$V_{outUV} = \frac{V_{a,UV} \cdot N_s}{N_a} - V_d \quad (28)$$

Where $V_{a,UV}$ is the desired primary auxiliary winding demagnetization voltage when output voltage is V_{outUV}.

$V_{a,UV}$ is recommended to be between 10 V and 11 V. So, taking $V_{a,UV}$ = 10.1 V,

$$V_{outUV} = \frac{10.1 \cdot 10}{3} - 0.7$$

$$\boldsymbol{V_{outUV} = 33\ V}$$

$t_{VoutUV,blank}$ is recommended to be at least 100 ms, so **$t_{VoutUV,blank}$ = 500 ms** is selected in this design example. The regulated mode output UVP reaction is configurable based on $Reaction_{UVP,Vout}$ parameter, so **$Reaction_{UVP,Vout}$ = Auto restart** is selected in this design example. The start-up output UVP reaction is fixed as auto restart.

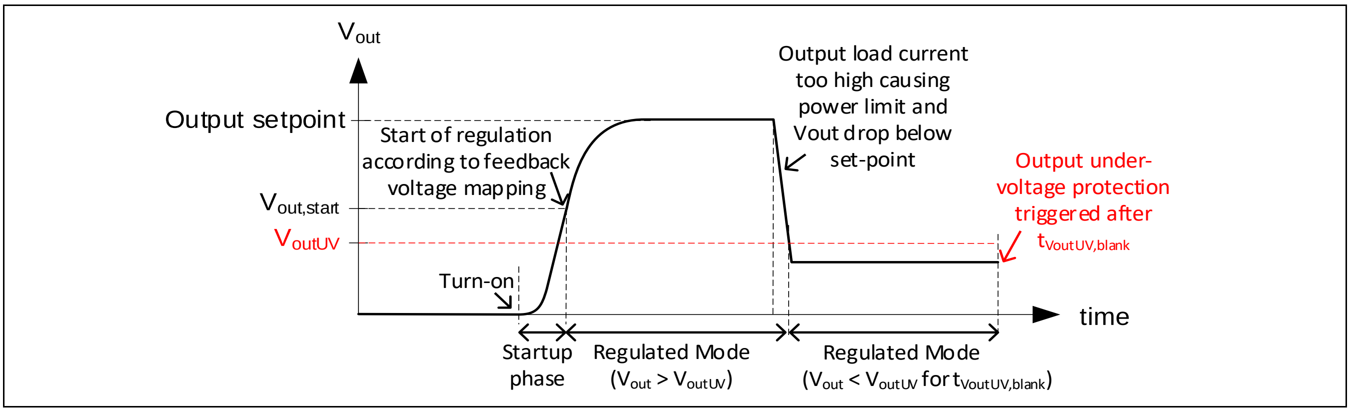


Figure 13 Regulated mode output UVP (not active in ABM)

12 Output OVP-related design

Under the single-fault condition of the FB pin open, the main output voltage could rise above the $V_{out,setpoint}$. As shown in **Figure 14**, the output OVP would be triggered when the estimated output voltage V_{out} is higher than the output OVP level V_{outOV} for longer than a blanking time.

To prevent the output OVP from being triggered by the output overshoot during line jump, e.g., from low to high input voltage, the output OVP level V_{outOV} should be configured well above $V_{out,setpoint}$. Therefore, the V_{outOV} parameter can be defined and calculated as:

$$V_{outOV} \geq 120\% \cdot V_{out,setpoint} = 120\% \cdot 54 = 64.8\,V \quad (29)$$

Based on the above, **V_{outov} = 65 V** is selected in this design example.

Considering the estimated output voltage protection accuracy is subjective to the the sampled signal accuracy, sampling delay, indirect sensing delay (e.g., output voltage cannot be estimated near AC input phase angle of 0 degrees and 180 degrees) and blanking time, the output capacitor voltage rating $V_{out,cap,rating}$ should be selected well above V_{outOV}. As a result, $V_{out,cap,rating}$ can be defined and calculated as:

$$V_{out,cap,rating} \geq \frac{V_{outOV}}{0.9} = \frac{65}{0.9} = 72.2\,V \quad (30)$$

Based on the above, **$V_{out,cap,rating}$ = 80 V** is selected in this design example.

Attention: ***It is mandatory to ensure that V_{outOV} is configured well below the actual output capacitor voltage rating $V_{out,cap,rating}$, while the $V_{out,cap,rating}$ is not exceeded in actual testing with all the necessary test conditions.***

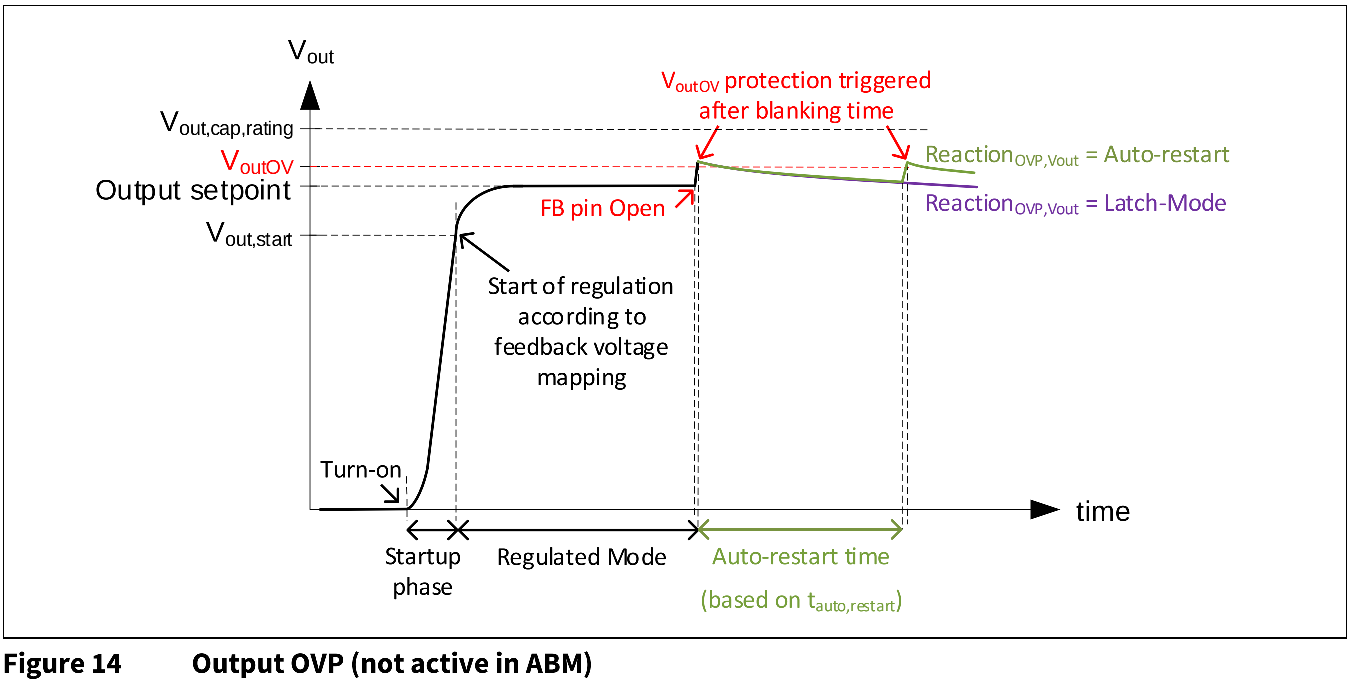


Figure 14 **Output OVP (not active in ABM)**

The reaction of output OVP is configurable to latch-mode or auto restart, based on the $Reaction_{OVP,Vout}$ parameter. **$Reaction_{OVP,Vout}$ = Auto Restart** is selected in this design example.

13 ZCD pin and input voltage sensing related design

ZCD pin filter capacitor C_{ZCD}, ZCD series resistor $R_{ZCD,1}$ and ZCD shunt resistor $R_{ZCD,2}$ are connected based on the connections shown in **Figure 15**.

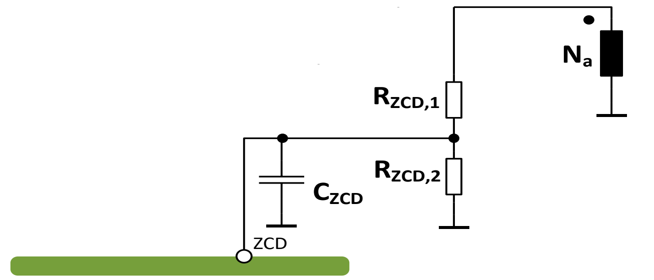


Figure 15 ZCD pin, C_{ZCD}, R_{ZCD1} and R_{ZCD2} connections

C_{ZCD} is mainly for ZCD pin noise-filtering, so a fixed value can generally be used for different designs. **C_{ZCD} = 47 pF** is selected in this design example. The quasi-resonant valley switching of the MOSFET drain voltage can be achieved with t_{ZCDPD} parameter fine-tuning based on **Section 20.2**. **Initial t_{ZCDPD} = 350 ns** can be used for powering-up of the system before the fine-tuning.

The recommended minimum ZCD series resistance $R_{ZCD,1,min}$ and maximum ZCD series resistance $R_{ZCD,1,max}$ are defined as:

$$R_{ZCD,1,min} = -\frac{N_a}{I_{IV,max,VinOV} \cdot N_p} \cdot \left[V_{inOV(pk)} + \frac{V_{INPCLN,min} \cdot N \cdot (V_{outOV} + V_d)}{V_{ZCDSH,max,VoutOV}} \right] \tag{31}$$

$$R_{ZCD,1,max} = -\frac{N_a}{I_{IV,min,VinUV} \cdot N_p} \cdot \left[V_{inUV(pk)} - \Delta V_{in,HF,ripple,est} + \frac{V_{INPCLN,max} \cdot N \cdot (V_{outOV} + V_d)}{V_{ZCDSH,min,VoutOV}} \right] \tag{32}$$

Where:

$V_{inOV(pk)}$ and $V_{inUV(pk)}$ are respectively √2 times V_{inOV} and √2 times V_{inUV}.

$I_{IV,max,VinOV}$ and $I_{IV,min,VinUV}$ are respectively the recommended maximum ZCD pin negative clamping current for V_{inOV} sensing and minimum ZCD pin negative clamping current for V_{inUV} sensing.

$V_{ZCDSH,max,VoutOV}$ and $V_{ZCDSH,min,VoutOV}$ are respectively the recommended maximum and minimum ZCD pin voltage sensing levels for V_{outOV} sensing.

$V_{INPCLN,max}$ and $V_{INPCLN,min}$ are respectively the maximum and minimum ZCD pin negative clamping voltages.

$\Delta V_{in,HF,ripple,est}$ is the estimated difference between the $V_{inUV(pk)}$ level and the high-frequency ripple minimum voltage level at the peak of AC input half sine wave. As a rule of thumb, it can be assumed to be between 25 V and 30 V.

Taking $I_{IV,max,VinOV}$ = -3.1 mA, $I_{IV,min,VinUV}$ = -0.15 mA, $V_{ZCDSH,max,VoutOV}$ = 2.6 V, $V_{ZCDSH,min,VoutOV}$ = 2.35 V, $V_{INPCLN,max}$ = -0.22 V, $V_{INPCLN,min}$ = -0.14 V, and $\Delta V_{in,HF,ripple,est}$ = 27.5 V,

$$R_{ZCD,1,min} = -\frac{3}{-3.1 \cdot 10^{-3} \cdot 32} \cdot \left[\sqrt{2} \cdot 350 + \frac{-0.14 \cdot 3.2 \cdot (65 + 0.7)}{2.6} \right] = 14.6\ k\Omega$$

$$R_{ZCD,1,max} = -\frac{3}{-0.15 \cdot 10^{-3} \cdot 32} \cdot \left[\sqrt{2} \cdot 70 - 27.5 + \frac{-0.22 \cdot 3.2 \cdot (65 + 0.7)}{2.35} \right] = 32.4\ k\Omega$$

In general, it is recommended to select $R_{ZCD,1}$ to be closer to $R_{ZCD,1,max}$, for lower power dissipation. If a higher input voltage sensing accuracy is desired for the UART reporting, a smaller $R_{ZCD,1}$ is however recommended. In this design example, **$R_{ZCD,1}$ = 27 kΩ** is selected.

The recommended minimum ZCD shunt resistance $R_{ZCD,2,min}$ and maximum ZCD shunt resistance $R_{ZCD,2,max}$ are defined and calculated as:

$$R_{ZCD,2,min} = \frac{R_{ZCD,1} \cdot N_s \cdot V_{ZCDSH,min,VoutOV}}{N_a \cdot (V_{outOV} + V_d) - N_s \cdot V_{ZCDSH,min,VoutOV}} = \frac{27 \cdot 10^3 \cdot 10 \cdot 2.35}{3 \cdot (65 + 0.7) - 10 \cdot 2.35} = 3.65\ k\Omega \quad (33)$$

$$R_{ZCD,2,max} = \frac{R_{ZCD,1} \cdot N_s \cdot V_{ZCDSH,max,VoutOV}}{N_a \cdot (V_{outOV} + V_d) - N_s \cdot V_{ZCDSH,max,VoutOV}} = \frac{27 \cdot 10^3 \cdot 10 \cdot 2.6}{3 \cdot (65 + 0.7) - 10 \cdot 2.6} = 4.1\ k\Omega \quad (34)$$

Based on the above, $\mathbf{R_{ZCD,2} = 3.9\ k\Omega}$ is selected in this design example.

When the AC input voltage decreases at full-load output, the DC link filter capacitor high-frequency peak-to-peak voltage ripple would increase, and this would also result in higher ripple on the ZCD pin negative clamping current, which is sensed for estimating input voltage V_{in}. Hence, for good V_{in} estimation via the ZCD pin, especially at input UVP level V_{inUV}, such a ripple effect should be minimized and compensated with proper configuration of $t_{on,max,at,V,in,low}$, $t_{on,max,at,V,in,UV}$ and R_{in} parameters, respectively.

$t_{on,max,at,V,in,low}$ and $t_{on,max,at,V,in,UV}$ parameter respectively denote the maximum on-time at the lowest operational input voltage $V_{in,low}$ and at the input UVP level.

$t_{on,max,at,V,in,low}$ should be configured not too high, while being able to deliver the steady-state full-load output power $P_{out,full}$ at $V_{in,low}$. Therefore, $t_{on,max,at,V,in,low}$ can be defined and calculated as:

$$t_{on,max,at,V,in,low} = \frac{e \cdot L_p \cdot I_{pri(pk),max}}{\sqrt{2} \cdot V_{in,low}} \quad (35)$$

Where e is the ratio for margin on the maximum on-time, which is recommended to be between 1.2 and 1.25.

Taking e = 1.23,

$$t_{on,max,at,V,in,low} = \frac{1.23 \cdot 544 \cdot 10^{-6} \cdot 2.606}{\sqrt{2} \cdot 82}$$

$$\boldsymbol{t_{on,max,at,V,in,low} = 15\ \mu s}$$

$t_{on,max,at,V,in,UV}$ is recommended to be configured lower than $t_{on,max,at,V,in,low}$, and can be calculated based on

$$t_{on,max,at,V,in,UV} = t_{on,max,at,V,in,low} \cdot \frac{V_{inUV}}{V_{in,low}} \quad (36)$$

$$t_{on,max,at,V,in,UV} = 15 \cdot 10^{-6} \cdot \frac{70}{82}$$

$$\boldsymbol{t_{on,max,at,V,in,UV} = 12.8\ \mu s}$$

R_{in} parameter is to compensate the DC link filter capacitor voltage ripple for accurate V_{in} measurement. As this parameter configuration is subjective to the line filter and the DC link filter capacitance design, parameter fine-tuning based on actual waveform measurement is required.

For powering up the board, the initial R_{in} parameter can be defined and calculated as:

$$Initial\ R_{in} = \frac{\Delta V_{in,HF,ripple,est}}{I_{pri(pk),max}} \quad (37)$$

$$Initial\ R_{in} = \frac{27.5}{2.606}$$

$$\boldsymbol{Initial\ R_{in} = 10.6\ \Omega}$$

Upon successful powering-up of the system, please refer to **Section 20.1** for the fine-tuning guide for the R_{in} parameter.

14 Secondary-side regulation FB circuit design

The FB pin filter capacitor C_{FB}, optocoupler and the SSR FB circuit are connected based on the connections shown in **Figure 16**.

The FB pin does not need any external pull-up as XDPL8219 has a fixed voltage reference V_{REF} of 2.428 V, which is internally connected to its FB pin via an internal pull-up resistor. The internal pull-up resistor value is configurable based on the $R_{FB,pull,up}$ parameter.

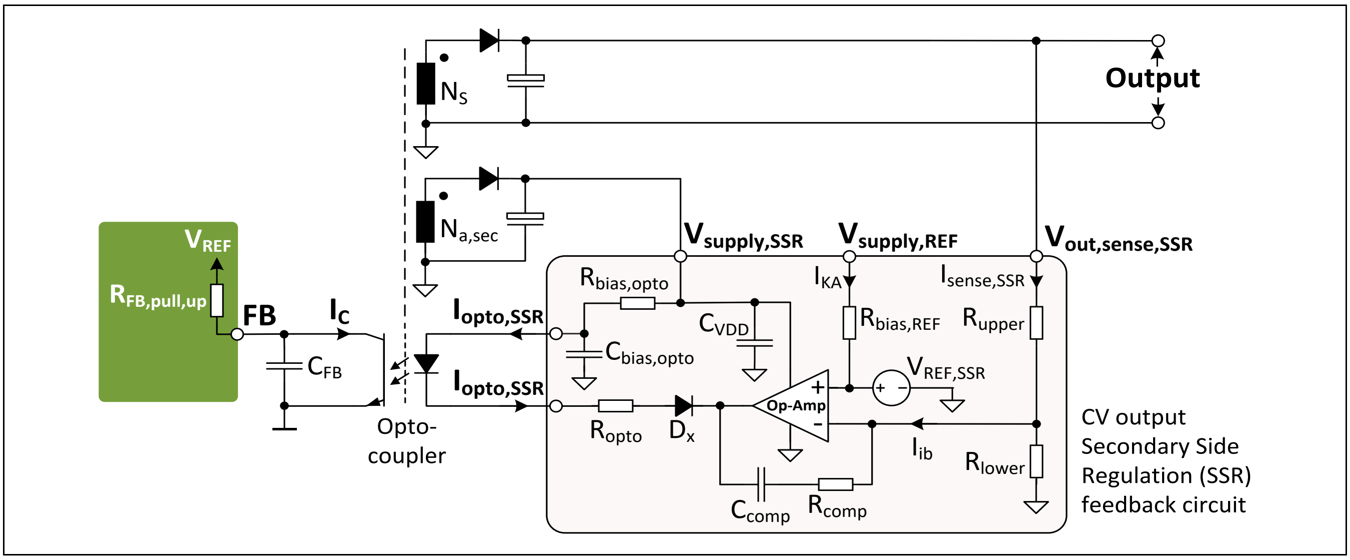


Figure 16 FB pin internal pull-up, C_{FB}, optocoupler and CV output SSR FB circuit connections

$V_{supply,SSR}$ from the secondary auxiliary winding rectified output is mainly used to supply the SSR circuit op-amp operational voltage V_{DD} and optocoupler LED current $I_{opto,SSR}$ via resistor $R_{bias,opto}$. For $V_{supply,SSR}$ noise decoupling, in this design example, a ceramic capacitor of **C_{VDD} = 100 nF** with low ESR is selected and placed near the op-amp V_{DD} pin.

As shown in **Figure 16**, the SSR op-amp non-inverting input should be connected to the SSR reference voltage $V_{REF,SSR}$, while the inverting input should be connected to a resistor/divider formed by R_{upper} and R_{lower} for output voltage sensing. In this design example, the selected op-amp part number is TSM103W, which has dual op-amps, and the non-inverting input of one op-amp is wired to a voltage reference $V_{REF,SSR}$ of 2.5 V internally.

$V_{supply,SSR}$ can be used as the SSR voltage reference supply $V_{supply,REF}$, to provide a minimum biasing current of $I_{KA,min}$ via voltage reference biasing resistor $R_{bias,REF}$, for generating the $V_{REF,SSR}$. However, in this design example, to minimize the standby loss, $V_{supply,REF}$ is not supplied by $V_{supply,SSR}$ based on $N_{a,sec}$ = 3, but by another rectified output with lower voltage, based on a partial secondary auxiliary winding turns number of **$N_{a,sec,partial}$ = 2**. Hence, the recommended maximum voltage reference biasing resistance $R_{bias,REF,max}$ can be defined and calculated as:

$$R_{bias,REF,max} = \frac{g}{I_{KA,min}} \cdot \left[(V_{out,setpoint} + V_d) \cdot \left(N_{a,sec,partial}/N_s\right) - V_{d,aux} - V_{REF,SSR}\right] \quad (38)$$

Where g is the ratio recommended to be between 0.75 and 0.85, and $V_{d,aux}$ is the auxiliary output diode forward voltage.

Taking g = 0.8, $V_{d,aux}$ = 0.5 V and $I_{KA,min}$ = 1 mA based on the selected op-amp datasheet,

$$R_{bias,REF,max} = \frac{0.8}{1 \cdot 10^{-3}} \cdot [(54 + 0.7) \cdot (2/10) - 0.5 - 2.5] = 6.35\ k\Omega$$

Based on the above, **$R_{bias,REF}$ = 6.2 kΩ** is selected in this design example.

To achieve accurate output voltage regulation based on $V_{out,setpoint}$, the op-amp input biasing current I_{ib} has to be much smaller than the output sensing upper resistor/divider current $I_{sense,SSR}$. As compared to using the conventional shunt regulator TL431, which has a maximum reference input current of 4 µA, the selected op-amp has a maximum input bias current of $I_{ib,max}$ = 0.2 µA, which results in much lower regulation offset error $ERR_{offset,ib}$ with the same level of $I_{sense,SSR}$.

Considering that $ERR_{offset,ib}$ is desired to be not more than 0.1 percent in this design example, the maximum output sensing upper divider resistance $R_{upper,max}$ can be de defined and calculated as:

$$R_{upper,max} = \frac{ERR_{offset,ib} \cdot (V_{out,setpoint} - V_{REF})}{I_{ib,max}} = \frac{0.1\% \cdot (54 - 2.5)}{0.2 \cdot 10^{-6}} = 257.5\ k\Omega \quad (39)$$

Since the ABM burst frequency is fixed based on the f_{burst} parameter for low audible noise, as a rule of thumb to achieve stable main output voltage at no-load, the R_{upper} selection should also ensure the output sensing resistor/divider power consumption is at least the power transfer of a single ABM pulse. Therefore, the $R_{upper,max}$ value can also be defined and calculated as:

$$R_{upper,max} = \frac{L_p \cdot V_{out,setpoint} \cdot (V_{out,setpoint} - V_{REF})}{{V_{inOV}}^2 \cdot {t_{on,min,ABM}}^2 \cdot f_{burst} \cdot \eta_{ABM}} \quad (40)$$

Where $t_{on,min,ABM}$ is the ABM minimum on-time parameter and η_{ABM} is the estimated power efficiency in ABM.

Take f_{burst} = 130 Hz, $t_{on,min,ABM}$ = 1 µs and assume η_{ABM} = 65 percent,

$$R_{upper,max} = \frac{544 \cdot 10^{-6} \cdot 54 \cdot (54 - 2.5)}{350^2 \cdot (1 \cdot 10^{-6})^2 \cdot 130 \cdot 65\%} = 146.15\ k\Omega$$

Based on the smaller $R_{upper,max}$ calculated from equation (39) and (40), the output sensing upper resistance R_{upper} should be selected near to $R_{upper,max}$ = 146.15 kΩ to achieve low standby power, so **R_{upper} = 127.5 kΩ** is selected in this design example.

The output sensing lower divider resistance R_{lower} can then be defined and calculated as:

$$R_{lower} = \frac{R_{upper} \cdot V_{REF}}{V_{out,setpoint} - V_{REF}} = \frac{127.5 \cdot 10^3 \cdot 2.5}{54 - 2.5} \quad (41)$$

$$\boldsymbol{R_{lower} \approx 6.2\ k\Omega}$$

For good control-loop stability, the FB pin internal pull-up resistance parameter $R_{FB,pull,up}$ should be configured not too high. On the other hand, for low standby power, $R_{FB,pull,up}$ should be configured not too low either. In a practical system, $R_{FB,pull,up}$ may be around 5 kΩ. Hence, **$R_{FB,pull,up}$ = 5.5 kΩ** is selected in this design example.

XDPL8219's internal ADC sampling point for the FB pin voltage signal is right after the GD pin signal becomes high for a period of $t_{CS,LEB}$ (480 ns typ.), to ensure a high signal to noise ratio (SNR). The FB pin capacitor C_{FB} is mainly used to filter the switching-on MOSFET current ringing noise, which might not be fully damped after $t_{CS,LEB}$. As the frequency of such ringing noise is normally at least a few MHz and the ADC sampling frequency $f_{sampling,ADC}$ is a few kHz, the RC filter frequency $f_{RC,FB}$ formed by C_{FB} and $R_{FB,pull,up}$ is recommended to be in the range of 40 kHz to 100 kHz. Therefore, C_{FB} can be defined and calculated as:

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot R_{FB,pull,up} \cdot f_{RC,FB}} \quad (42)$$

Taking $f_{RC,FB}$ = 60 kHz,

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot 5.5 \cdot 10^3 \cdot 60 \cdot 10^3} = 482\ pF$$

Based on the commonly used ceramic capacitor value which is near to the calculated C_{FB} above, **C_{FB} = 470 pF** is selected in this design example.

The minimum power transfer of the system is reached when the filtered FB voltage level $V_{FB,filtered}$ is the same as or less than the $V_{FB,min}$ parameter. It is recommended to configure the minimum FB voltage $V_{FB,min}$ the same as $V_{CE(sat)}$ based on the selected optocoupler datasheet. As a result, **$V_{FB,min}$ = 0.3 V** is selected in this design example.

Based on the minimum current transfer ratio CTR_{min} from the selected optocoupler datasheet, the total resistance of $R_{bias,opto}$ and R_{opto} can be defined as:

$$R_{bias,opto} + R_{opto} \leq h \cdot R_{FB,pull,up} \cdot CTR_{min} \cdot \left[\frac{(V_{out,setpoint}+V_d) \cdot N_{a,sec}/N_s - V_{d,aux} - V_{f,opto} - V_{dx}}{V_{REF}-V_{CE,sat}}\right] \quad (43)$$

Where h is the ratio recommended to be between 0.7 and 0.8 for compensating the secondary auxiliary winding rectified output voltage drop under no load at the main output, $V_{f,opto}$ is the optocoupler LED forward voltage, R_{opto} and V_{dx} are respectively the optocoupler series resistance and the forward voltage of D_x, as shown in **Figure 16**.

Taking CTR_{min} = 100 percent, h = 0.7, $V_{f,opto}$ = 1.1 V and V_{dx} = 0.5 V for the calculation,

$$R_{bias,opto} + R_{opto} \leq 0.7 \cdot 5.5 \cdot 10^3 \cdot 100\% \cdot \left[\frac{0.7 \cdot (54 + 0.7) \cdot 3/10 - 0.5 - 1.1 - 0.5}{2.428 - 0.3}\right]$$

$$R_{bias,opto} + R_{opto} \leq 16.98\ k\Omega$$

Based on the above, $R_{bias,opto}$ + R_{opto} = 16 kΩ is selected in this design example. $R_{bias,opto}$ is recommended to be at least 10 times lower than R_{opto}, so $R_{bias,opto,max}$, which denotes the maximum $R_{bias,opto}$ value, can then be defined and calculated as:

$$R_{bias,opto,max} = \frac{R_{bias,opto} + R_{opto}}{1.1} = 1.455\ k\Omega \quad (44)$$

The recommended maximum RC filter frequency $f_{RC,bias,opto,max}$ formed by $R_{bias,opto}$ and $C_{bias,opto}$ is $F_{line,min}$. Since $R_{bias,opto}$ with high resistance is generally cheaper than $C_{bias,opto}$ with high capacitance, $C_{bias,opto}$ nominal value is recommended not to exceed 4.7 µF. As a result, in this design example, **$C_{bias,opto}$ = 3.3 µF** is selected, while the minimum optocoupler biasing resistor value $R_{bias,opto,min}$ can be defined and calculated as:

$$R_{bias,opto,min} = \frac{1}{2 \cdot \pi \cdot C_{bias,opto} \cdot f_{RC,bias,opto,max}} = \frac{1}{2 \cdot \pi \cdot 3.3 \cdot 10^{-6} \cdot 47} \approx 1\ k\Omega \quad (45)$$

Based on the $R_{bias,opto,max}$ and $R_{bias,opto,min}$ calculation results, and also $R_{bias,opto}$ + R_{opto} selection above, **$R_{bias,opto}$ = 1** kΩ and **R_{opto} = 15** kΩ are selected in this design example.

A type II FB compensation network is used in this design example. It consists of a resistor R_{comp} in series with C_{comp}, as shown In **Figure 16**. As a rule of thumb, the initial frequency of the pole at origin $f_{pole,origin}$ can be around 2 Hz to 3 Hz, while the initial frequency of the zero f_{zero} is suggested to be around 5 Hz to 8 Hz. As a result, the initial value of C_{comp} and R_{comp} for system powering-up can be defined and calculated as:

$$Initial\ C_{comp} = \frac{1}{2 \cdot \pi \cdot R_{upper} \cdot f_{pole,origin}} \quad (46)$$

$$Initial\ R_{comp} = \frac{1}{2 \cdot \pi \cdot C_{comp} \cdot f_{zero}} \quad (47)$$

Taking $f_{pole,origin}$ = 2.65 Hz and f_{zero} = 5 Hz,

$$Initial\ C_{comp} = \frac{1}{2 \cdot \pi \cdot 127.5 \cdot 10^3 \cdot 2.65}$$

$$\boldsymbol{Initial\ C_{comp} = 470\ nF}$$

$$Initial\ R_{comp} = \frac{1}{2 \cdot \pi \cdot 470 \cdot 10^{-9} \cdot 5}$$

$$\boldsymbol{Initial\ R_{comp} = 68\ k\Omega}$$

15 Regulated mode parameters

In regulated mode, the FB pin voltage signal is periodically sampled and digitally filtered. Based on the filtered feedback voltage $V_{FB,filtered}$, the operating mode of QRMn, discontinuous conduction mode (DCM) or ABM, and the respective switching parameters (on-time t_{on}, valley number N_{valley}, minimum switching period $t_{sw,min}$, pulse number n_{ABM}) are periodically updated in each operation cycle.

Note: The period of every XDPL8219 operation cycle is 9.823 ms by default. When the HV pin line synchronization is enabled and properly in place with an AC input, it is approximately the half-sine-wave period of an AC input, else it follows the default value.

Note: The switching parameters can be modulated over every operation cycle to achieve the enhanced power quality for AC input, or the switching frequency dithering for constant DC input voltage.

15.1 Digital notch filter

In QRMn and DCM, when the HV pin line synchronization is properly in place with an AC input, or when a constant DC input voltage is detected by the controller, for a duration more than the $n_{notch,blank}$ parameter, a digital notch filter is enabled. Otherwise, the sampled feedback voltage is processed by a digital low pass filter, to reduce the high frequency component.

The digital notch filter with the quality factor of $N_{quality}$ suppresses either the double-line-frequency sine-wave component of an AC input, or the sine-wave component generated by the switching frequency dithering for constant DC input voltage, to stabilize the filtered feedback voltage $V_{FB,filtered}$. The recommended $N_{quality}$ and $n_{notch,blank}$ parameter configuration from **Table 5** is selected in this design example.

Table 5 Notch filter parameter configuration

Parameter name	Recommended value	Unit
$N_{quality}$	1.6	–
$n_{notch,blank}$	2	Number of operation cycle

15.2 Initial feedback voltage maximum limit

When the regulated mode is entered, the filtered feedback voltage maximum limit $V_{FB,filtered,max}$ is ramped up from $V_{FB,limit,start}$ (1.2 V typ.) to V_{REF} (2.428 V typ.), with an incremental voltage step of $V_{FB,limit,step}$ parameter after every $t_{FB,limit,step}$. .

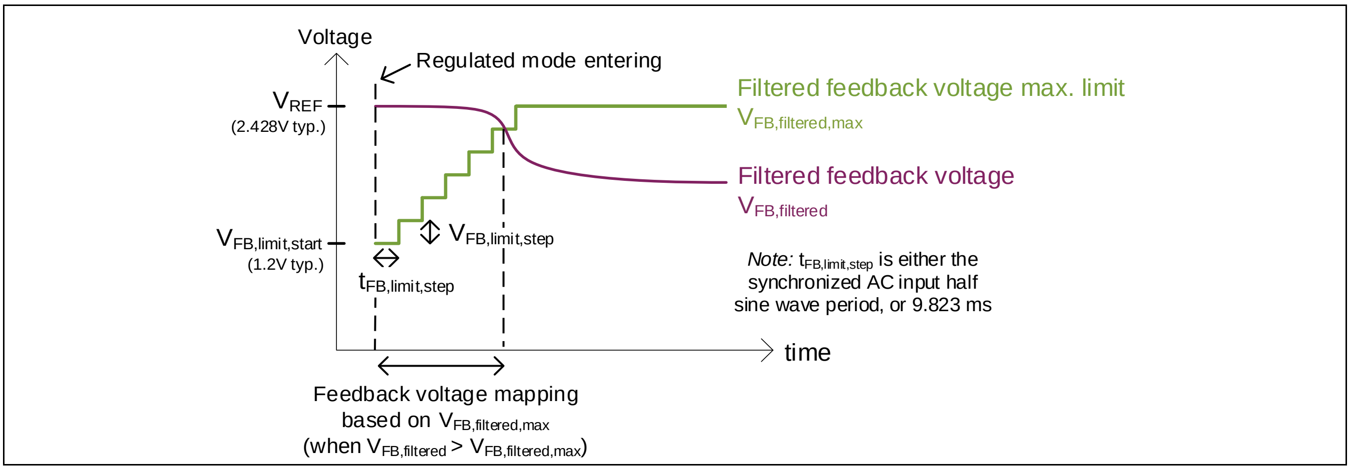


Figure 17 FB voltage maximum limit ramp when entering regulated mode

As shown in **Figure 17**, when $V_{FB,filtered}$ is higher than $V_{FB,filtered,max}$ initially in the regulated mode entering, the feedback voltage mapping is based on $V_{FB,filtered,max}$ ramp, to prevent the excessive output voltage overshoot during output rise. When $V_{FB,filtered}$ gets lower than $V_{FB,filtered,max}$, the feedback voltage mapping then follows $V_{FB,filtered}$, for the steady-state output regulation.

As a start, $\mathbf{V_{FB,limit,step}}$ **= 800 mV** is generally recommended. It can be reduced later after successful powering-up of the system, if there is excessive output rise overshoot found during the start-up test.

15.3 Regulated mode CS pin maximum voltage and minimum QRMn valley number limits

To better limit the flyback output power, especially at higher input voltage, XDPL8219 features the regulated mode CS pin maximum voltage $V_{OCP1}(V_{in})$ and minimum QRM valley number $N_{valley,min}(V_{in})$ limits, which are adaptive based on the estimated input voltage V_{in}, as shown in **Figure 18**.

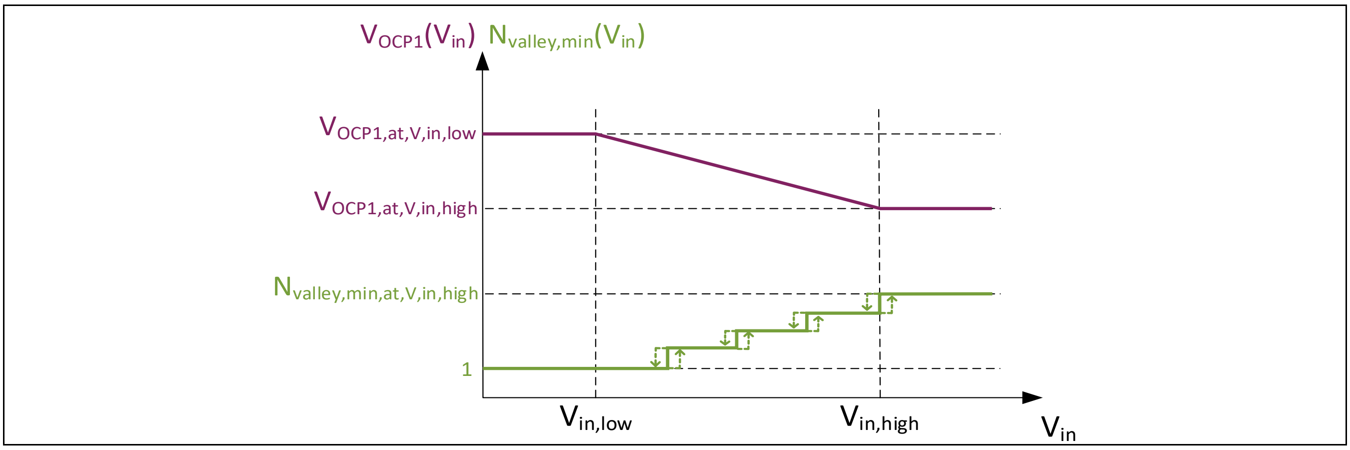


Figure 18 Regulated mode minimum valley number limit and CS pin maximum voltage limit adapation based on estimated input voltage V_{in}

As a rule of thumb, the $N_{valley,min,at,V,in,high}$ parameter in **Figure 18** can be configured as:

$$N_{\text{valley,min,at,V,in,high}} = \begin{cases} 1 \; or \; 2, & \frac{V_{AC,max}}{V_{AC,min}} < 2 \\ 4 \; or \; 5, & \frac{V_{AC,max}}{V_{AC,min}} \geq 2 \end{cases} \quad (48)$$

The $V_{AC,max}$ to $V_{AC,min}$ ratio is around 3.4 in this design example, so $N_{valley,min,at,V,in,high}$ = 5 is selected based on above.

The $V_{OCP1,at,V,in,low}$ and $V_{OCP1,at,V,in,high}$ parameters in **Figure 18** can be defined and calculated as:

$$V_{OCP1,at,V,in,low} = I_{pri(pk),max} \cdot R_{CS} \quad (49)$$

$$V_{OCP1,at,V,in,low} = 2.606 \cdot 0.2$$

$$\boldsymbol{V_{OCP1,at,V,in,low} = 0.52\ V}$$

$$V_{OCP1,at,V,in,high} = R_{CS} \cdot I_{pri(pk),max} \cdot \sqrt{\left[L_p \cdot I_{pri(pk),max} \cdot f_{sw,min,at,P,out,full} \cdot \left(\frac{1}{V_{\text{in,high(pk)}}} + \frac{1}{N \cdot (V_{out,setpoint} + V_d)}\right)\right]^2 + 2\pi \cdot (L_p \cdot C_{o,tr})^{0.5} \cdot (N_{valley,min,at,V,in,high} - 1) \cdot f_{sw,min,at,P,out,full}} \quad (50)$$

Where $V_{in,high(pk)}$ is √2 times of $V_{in,high}$, and $C_{o,tr}$ is the MOSFET time-related effective output capacitance.

Taking $C_{o,tr}$ = 135 pF from the selected MOSFET (IPD80R900P7) datasheet,

$$V_{OCP1,at,V,in,high} = 0.2 \cdot 2.606 \cdot \sqrt{\left[544 \cdot 10^{-6} \cdot 2.606 \cdot 52 \cdot 10^3 \cdot \left(\frac{1}{\sqrt{2} \cdot 326} + \frac{1}{3.2 \cdot (54 + 0.7)}\right)\right]^2 + 2\pi \cdot (544 \cdot 10^{-6} \cdot 135 \cdot 10^{-12})^{0.5} \cdot (5 - 1) \cdot 52 \cdot 10^3}$$

$$V_{OCP1,at,V,in,high} = 0.43\ V$$

Note: *$V_{OCP1,at,V,in,high}$ parameter is configurable between 0.34 V and $V_{OCP1,at,Vin,low}$ level only. If the calculated $V_{OCP1,at,V,in,high}$ is below 0.34 V, $V_{OCP1,at,Vin,high}$ = 0.34 V should be selected. If the calculated $V_{OCP1,at,V,in,high}$ is above the configured $V_{OCP1,at,Vin,low}$, then $V_{OCP1,at,Vin,high}$ should be configured as per $V_{OCP1,at,Vin,low}$.*

15.4 On-time limits

The maximum and minimum on-time limits in **Figure 19** are adaptive based on the estimated input voltage V_{in}.

- QRMn/DCM:

  To sense the output overvoltage level of V_{outOV} parameter, the device calculates a $t_{on,min,V,out,sense}(V_{in})$ variable, which is the estimated minimum on-time to achieve the desired minimum transformer demagnetization time of $t_{min,demag}$ parameter, at the peak of the estimated input voltage $V_{in,peak}$. The minimum on-time limit $t_{on,min}(V_{in})$ is based on the $t_{on,min}$ parameter or the $t_{on,min,V,out,sense}(V_{in})$ variable, whichever is higher, as shown in **Figure 19**.

  For V_{in} between the lowest operational input voltage parameter $V_{in,low}$ and the input overvoltage protection level parameter V_{inOV}, the maximum on-time limit $t_{on,max}(V_{in})$ is scaled to compensate the influence of input voltage on feedback gain.

  For V_{in} from $V_{in,low}$ to the input undervoltage protection level parameter $V_{in,UV,}$ $_{ton,max}(V_{in})$ can be linearly reduced from $t_{on,max,at,V,in,low}$ parameter to $t_{on,max,at,\ Vin,UV}$ parameter, to limit the maximum power during brown-out.

- ABM:

  For V_{in} decreased from $V_{in,high}$, the ABM minimum on-time limit $t_{on,min,ABM}(V_{in})$ is increased from $t_{on,min,ABM}$ parameter, to reduce the burst pulse number for a lower standby power at lower input voltage.

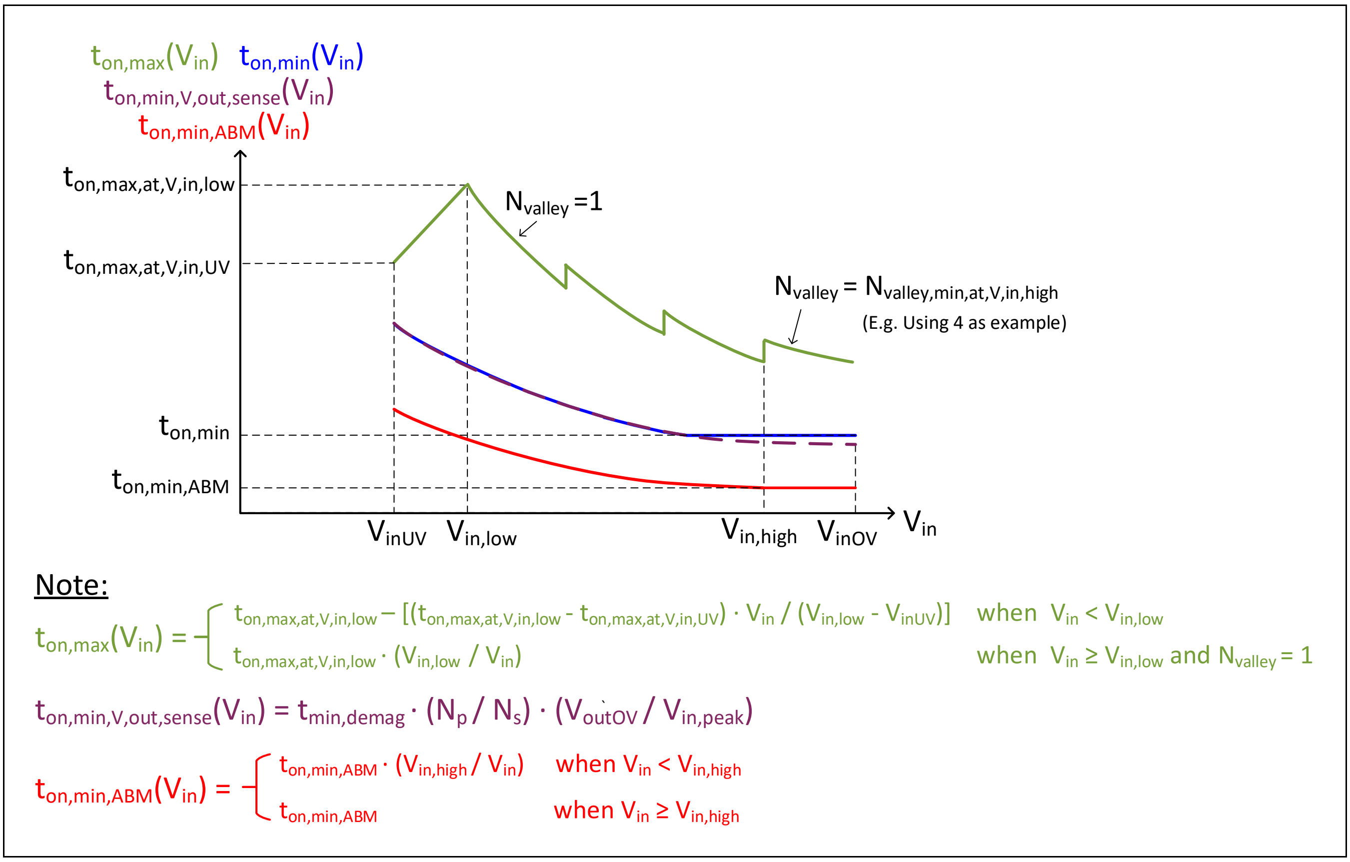


Figure 19 On-time limit adaptation based on estimated input voltage V_{in}

The recommended on-time limits related parameter configuration from **Table 6** is selected in this design example.

Table 6 On-time limits parameter configuration

Parameter name	Recommended value	Unit
$t_{on,max,at,V,in,low}$	Refer to calculation in **Section 13**	µs
$t_{on,max,at,V,in,UV}$	Refer to calculation in **Section 13**	µs
$t_{min,demag}$	2	µs
$t_{on,min}$	1.38	µs
$t_{on,min,ABM}$	1	µs

15.5 ABM FB voltage sensing and control

In ABM, the switching pulse on-time t_{on} and burst pulse number N_{ABM} are controlled based on $V_{FB,filtered}$ taken at the last pulse of the previous burst cycle, as shown in **Figure 20**. The ABM minimum on-time and minimum pulse number per burst are based on the $t_{on,min,ABM}(V_{in})$ and $n_{ABM,min}$ parameters, respectively.

During ABM burst pause, the controller enters sleep mode with the FB pin internal pull-up disabled, to reduce the power consumption. Before the next ABM burst pulse starts, the controller wakes up with the FB pin internal pull-up re-enabled. To avoid measuring the FB pin voltage spikes, which could present initially when the internal pull-up is re-enabled, the start of both ABM burst pulsing and FB pin voltage sampling is delayed upon the controller wake-up, based on the n_{wakeup} parameter.

Typically, the controller has a burst interval which is approximately the configured $1/f_{burst}$ and enters the sleep mode for power saving after completing the last pulse of each burst cycle, as shown in **Figure 20**.

However, if the UART reporting feature is enabled with $EN_{UART,reporting}$ parameter, either a longer than typical burst interval or a delayed sleep mode entry, or both can occur occasionally, for instance when the UART signal transmission can not be completed within the typical burst interval or before the last pulse of a burst cycle.

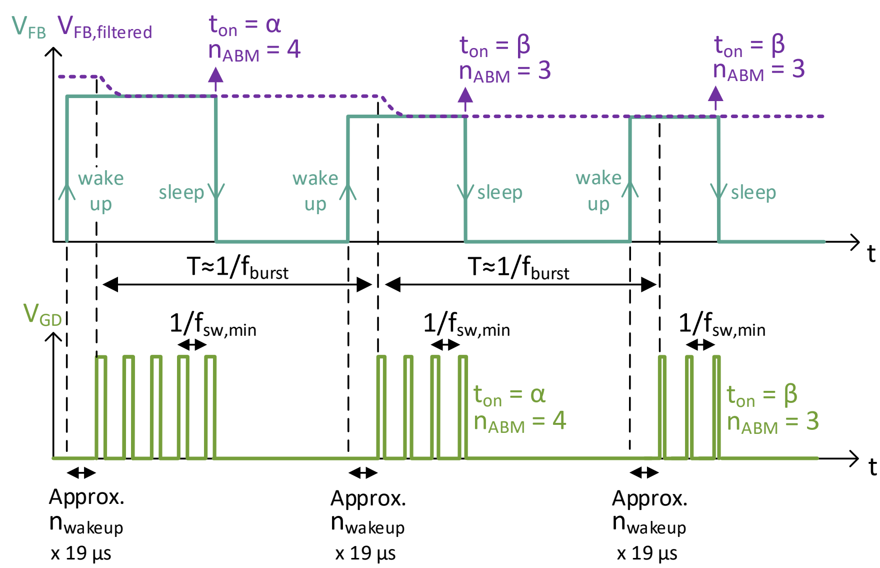


Figure 20 Typical ABM switching waveforms

Referring to **Table 7**, the recommended parameter configuration for ABM FB voltage sensing and control is selected in this design example.

Table 7 Parameter configuration related to ABM FB voltage sensing and control

Parameter name	Recommended value	Unit
f_{burst}	130	Hz
$n_{ABM,min}$	3	–
$t_{on,min,ABM}$	1.00	µs
n_{wakeup}	3	Interval (each interval is around 19 µs)

15.6 Filtered FB voltage mapping and mode transition

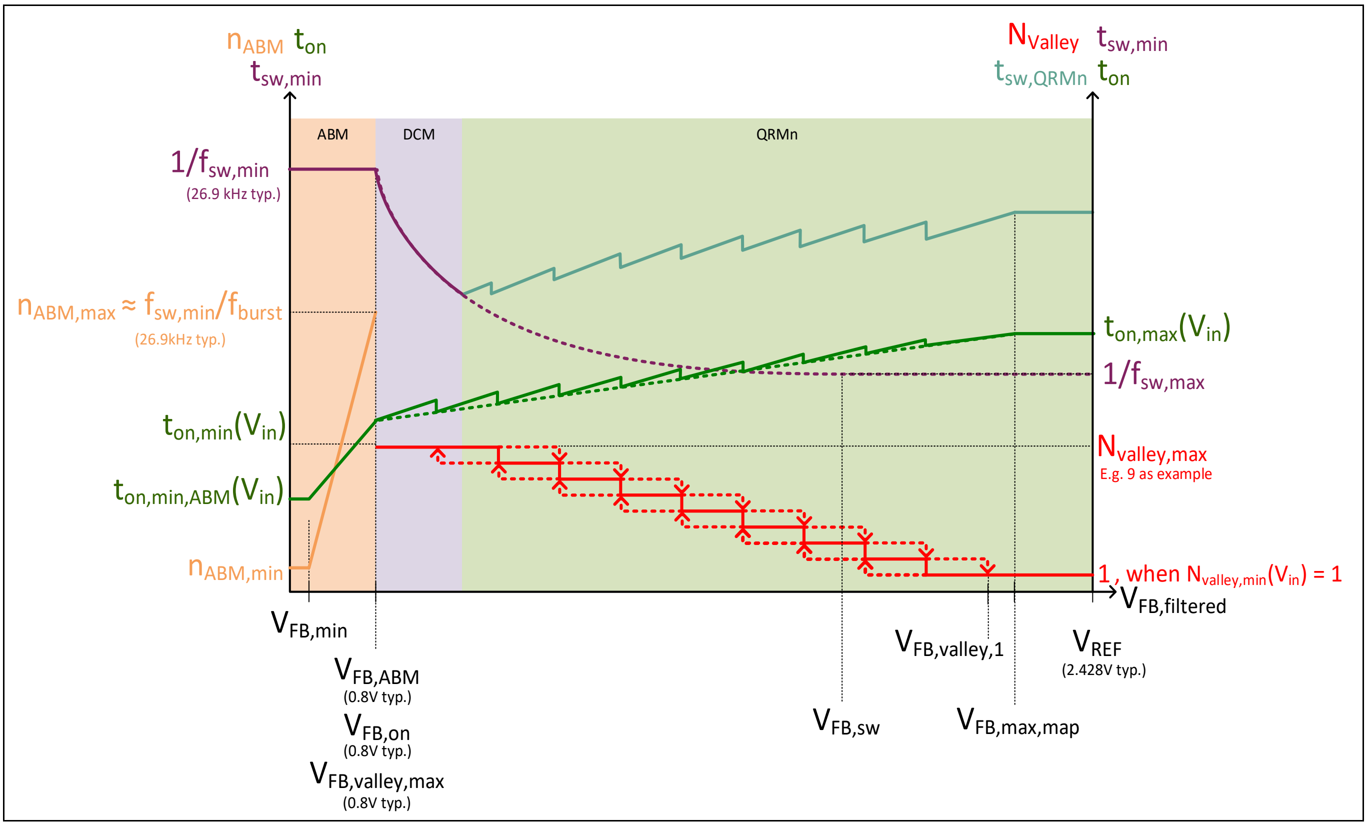


Figure 21 Filtered FB voltage mapping

- QRMn/DCM:

  The t_{on}, $t_{sw,min}$ and N_{valley} in **Figure 21** are mapped from the filtered feedback voltage $V_{FB,filtered}$.

  In QRMn, to switch on the MOSFET at the N_{valley} of the drain voltage, the system-dependent QRMn switching period $t_{sw,QRMn}$ has to be more than $t_{sw,min}$. If the drain voltage valley of N_{valley} happens before $t_{sw,min}$ is reached, the controller operates in DCM and the DCM switching period $t_{sw,DCM}$ follows $t_{sw,min}$.

  The minimum switching period $t_{sw,min}$ is decreased from $1/f_{sw,min}$ (37.2 µs typ.) to $1/f_{sw,max}$ when $V_{FB,filtered}$ is increased from $V_{FB,ABM}$ parameter (0.8 V typ.) to $V_{FB,sw}$ parameter or more. $f_{sw,min}$ and $f_{sw,max}$ are respectively the minimum and maximum switching frequency parameters.

  When $V_{FB,filtered}$ is $V_{FB,valley,max}$ parameter, N_{valley} is mapped to the maximum valley number parameter $N_{valley,max}$. The minimum N_{valley} value is however based on $N_{valley,min}(V_{in})$, as described in **Section 15.3** . When $N_{valley,min}(V_{in})$ is 1 and the $V_{FB,filtered}$ is the same as or higher than $V_{FB,valley,1}$ parameter,N_{valley} is mapped to 1.

  For a smoother transition when the N_{valley} changes, the device can compensate the t_{on} curve using $c_{valley,comp}$ parameter. To stabilize the N_{valley} in steady state operation, a hysteresis on N_{valley} change is applied, and the

N_{valley} is only updated once in each operation cycle. If the N_{valley} change is more than a $N_{valley,fast}$ parameter, the controller can speed up the N_{valley} update for a better dynamic load response.

When $V_{FB,filtered}$ increases from $V_{FB,on}$ parameter (0.8 V typ.), t_{on} increases from $t_{on,min}(V_{in})$. When $V_{FB,filtered}$ Is increased to $V_{FB,max,map}$ parameter or more, the power transfer is maximum, with the t_{on} based on $t_{on,max}(V_{in})$ or $V_{OCP1}(V_{in})$, and the switching period depending on either $1/f_{sw,max}$ or the minimum QRMn valley number limit $N_{valley,min}(V_{in})$.

- ABM:

t_{on} and n_{burst} are mapped from $V_{FB,filtered}$ taken at the last pulse of previous burst cycle.

$V_{FB,ABM}$ parameter (0.8 V typ.) is the $V_{FB,filtered}$ threshold for ABM entry and exit. To enter ABM, $V_{FB,filtered}$ needs to be below the $V_{FB,ABM}$ threshold, for a minimum time-out based on the $t_{ABM,blank}$ parameter. If $EN_{Burst,Exit,Filter,Feedback}$ parameter is enabled, ABM will be exited when $V_{FB,filtered}$ rises above the $V_{FB,ABM}$ threshold. If it is disabled, ABM will be exited when the sampled FB voltage rises above the $V_{FB,ABM}$ threshold.

When $V_{FB,filtered}$ decreases from $V_{FB,ABM}$ parameter (0.8 V typ.) to $V_{FB,min}$ parameter, t_{on} decreases from $t_{on,min}(V_{in})$ to $t_{on,min,ABM}(V_{in})$, while n_{burst} decreases from $n_{ABM,max}$ to $n_{ABM,min}$ parameter. $n_{ABM,max}$ is an integer which is approximately the ratio of $f_{sw,min}$ parameter over f_{burst} parameter.

When $V_{FB,filtered}$ is the same as or lower than the $V_{FB,min}$ parameter, the power transfer is minimum, with the t_{on} based on $t_{on,min,ABM}(V_{in})$ and pulse number n_{ABM} based on $n_{ABM,min}$.

Referring to **Table 8**, the recommended parameter configuration for FB voltage mapping and mode transition is selected in this design example.

Table 8 Parameter configuration related to FB voltage mapping and mode transition

Parameter name	Recommended value	Unit
$f_{sw,max}$	186.4	kHz
$EN_{Burst,Exit,Filter,Feedback}$	Enabled	
$t_{ABM,blank}$	6.5	ms
$N_{valley,max}$	14	
$N_{valley,fast}$	9	
$C_{valley,comp}$	3.0	
$V_{FB,valley,1}$	1.5	V
$V_{FB,max,map}$	2.0	V
$V_{FB,sw}$	1.5	V
$V_{FB,min}$	$V_{CE(sat)}$ (refer to optocoupler datasheet, as described in **Section 14**)	V

16 UART reporting

All UART reporting data packets are sent based on the unidirectional UART communication (XDPL8219 as master), with a fixed baud rate of 9600 bps.

When $EN_{UART,REPORTING}$ parameter is enabled, XDPL8219 UART pin transmits a regular data packet once every 14 operation cycles, which contains the following information:

- Last estimated input voltage rms value V_{in}
- Last detected line frequency or input voltage type based on $F_{line,UART}$
- Last measured IC junction temperature $T_{J,UART}$, based on its internal sensor

Note: In ABM, the $F_{line,UART}$ cannot be synchronized with the input voltage frequency, for power savings. It only shows the last detected values before entering ABM.

The regular data packet information are useful for the power monitoring, and also for the reliability improvement, such as to reduce the second-stage constant current regulator maximum output power, when the V_{in} drops too low or $T_{J,UART}$ rises too high.

When both $EN_{UART,REPORTING}$ and $EN_{SEND,V,IN,LOSS}$ parameters are enabled, XDPL8219 UART pin transmits one or more data packets which indicate the input voltage loss, if the consecutive number of too low ZCD pin clamping current $-I_{IV}$ sampling value has exceeded a limit.

When both $EN_{UART,REPORTING}$ and $EN_{SEND,LAST,ERROR,CODE}$ parameters are enabled, XDPL8219 transmits a data packet which contains the error code of the last triggered protection, right before every auto restart. If the triggered protection reaction is hardware restart, stop-mode or latch-mode, the error code will not be sent out.

Note: Upon protection triggering, XDPL8219 flyback converter without switching cannot deliver the operating voltage supply of the micro-controller, for receiving and decoding the error code.

When $UART_{polarity}$ parameter is configured as high, the UART reporting bus idle level is high (3.3 V typ.), with the data logic level based on high = 1 and low = 0. This parameter setting is recommended for the non-isolated unidirectional UART communication e.g., with a micro-controller on primary side.

When $UART_{polarity}$ parameter is configured as low, the UART reporting bus idle level is low, with the data logic level based on low = 1 and high = 0. This parameter setting is recommended for the isolated unidirectional UART communication e.g., with a micro-controller on secondary side, via an opto-coupler.

Figure 22 shows the recommended isolated UART circuit, when the $UART_{polarity}$ parameter is configured as low. This circuit is mounted on the isolated UART reporting evaluation plugin board, which is included in the XDPL8219 40 W reference design package, and it can be connected to the main board easily for evaluation.

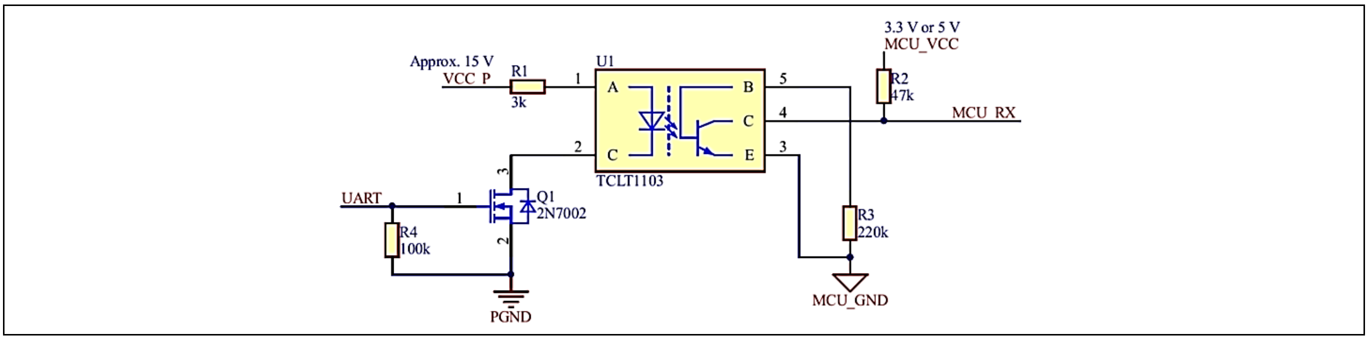


Figure 22 Isolated unidirectional UART circuit (when $UART_{polarity}$ parameter is configured as low)

*Note: In **Figure 22**, VCC_P net connects to the positive polarity of either C_{VCC} (if error code sending is needed), or $C_{out,aux}$, while the UART net connects to XDPL8219 UART pin, and PGND symbol connects to the primary ground.*

The UART reporting data packet decoding and interpretation are shown in **Table 9**, **Table 10** and Error! Reference source not found..

Table 9 UART reporting data packet format for decoding

Type of data packet	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Regular data packet	$7E_H$	Low byte of $V_{in,aux}$ data	High byte of $V_{in,aux}$ data	t_{in} data	T_{40} data	Checksum (XOR sum of Byte 1 to 5 before)
Typical loss of input voltage indication data packet	40_H	-	-	-	-	-
Loss of input voltage indication within the regular data packet	$7E_H$	ED_H or Low byte of $V_{in,aux}$ data	ED_H or High byte of $V_{in,aux}$ data	ED_H or t_{in} data	ED_H or T_{40} data	ED_H
Error code data packet	60_H	Low byte of Error code	High byte of Error code	Checksum (XOR sum of Byte 1 to 3 before)	-	-

Table 10 Interpretation of the decoded regular data

Regular data type	Decoded regular data minimum decimal value	Decoded regular data maximum decimal value	Data interpretation
t_{in}	0	255	If $t_{in} = FF_H$, the input voltage type has not been detected. If $t_{in} = 00_H$, the last detected input voltage type is constant DC. If $t_{in} \neq FF_H$ and $t_{in} \neq 00_H$, the last detected input voltage type is AC and the $F_{line,UART}$ (unit: Hz) can be calculated based on: $F_{line,UART} = \begin{cases} 5828/t_{in}, & T_{critical} > 119°C \\ 7726/t_{in}, & T_{critical} \leq 119°C \end{cases}$ Where $T_{critical}$ is the IC overtemperature protection level parameter setting.
$V_{in,aux}$	0	40960	$V_{in} = \begin{cases} 0.005460 \cdot V_{in,aux} \cdot N_p/N_a, & t_{in} \neq FF_H \text{ and } t_{in} \neq 00_H \\ 0.007722 \cdot V_{in,aux} \cdot N_p/N_a, & t_{in} = 00_H \end{cases}$
T_{40}	0	190	$T_{J,UART} = T_{40} - 40$

Note: The micro-controller receiving the regular data packet should do the averaging on the decoded V_{in} and $F_{line,UART}$ data samples, to obtain the more stable value.

Note: The microcontroller should store the necessary calibration data for its post-processing, to compensate the offset on V_{in},, which varies based on the IC and system tolerances of each board.

Table 11 Interpretation of the error code data

Error code data		Last triggered protection
$UART_{polarity}$ = High	**$UART_{polarity}$ = Low**	
0000_H	$FFFF_H$	None
0001_H	$FFFE_H$	Output OVP
0008_H	$FFF7_H$	Regulated mode output UVP
0010_H	$FFEF_H$	Start-up output UVP
0020_H	$FFDF_H$	Transformer demagnetization time shortage protection
0040_H	$FFBF_H$	Input UVP
0080_H	$FF7F_H$	Input OVP
0100_H	$FEFF_H$	IC overtemperature protection
0200_H	$FDFF_H$	V_{CC} OVP
0400_H	$FBFF_H$	Interrupt watchdog protection (may get triggered for input UVP)
0800_H	$F7FF_H$	MOSFET over-current protection
4000_H	$BFFF_H$	ADC watchdog protection (may get triggered for input UVP)
8000_H	$7FFF_H$	Regulated mode V_{CC} UVP

In this design example, **$EN_{UART,REPORTING}$ = Enabled**, **$EN_{SEND,V,IN,LOSS}$ = Enabled**, **$EN_{SEND,LAST,ERROR,CODE}$ = Enabled** and **$UART_{polarity}$ = Low** parameter settings are selected.

17 Other functions and protections

17.1 Enhanced power factor correction

To compensate for the input current displacement caused by the $C_{DC,filter}$ and line filter, the XDPL8219 enhanced power factor correction (EPFC) feature can be enabled by configuring the correction gain parameter named C_{EMI} above zero. As a start, it can be configured as per the $C_{DC,filter}$ value. Therefore, the **initial C_{EMI} = 0.22 μF** parameter setting is selected in this design example.

The EFPC gain is reduced from C_{EMI} parameter to zero for a smooth transition to ABM, when the $V_{FB,filtered}$ is decreased from $V_{EPFC,on}$ parameter to $V_{FB,ABM}$ parameter (0.8 V typ.). **$V_{EPFC,on}$ = 1 V** parameter setting is recommended and selected in this design example.

Upon successful powering-up of the system, refer to **Section 20.3** for the fine-tuning guide.

17.2 Enhanced THD correction

By enabling the EN_{ETHDC} parameter, the controller compensates the input current distortion caused by the changing QRMn duty cycle over the AC input half-sine-wave period. Such compensation can however increases the EMI at higher input voltage, caused by the higher switching peak current. Hence, it is only recommended to enable the EN_{ETHDC} parameter when the extremely low THD is required at full output power, where the QRM valley number is the lowest and such compensation effect would be the highest.

Using the XDPL8219 40 W reference design as an example, even with EN_{ETHDC} parameter disabled by default, THD less than 10 percent can be achieved over wide operating range. In this design example, **EN_{ETHDC} = Disabled** parameter setting is selected.

Upon successful powering-up of the system, refer to **Section 20.3** for the fine-tuning guide.

17.3 Switching frequency dithering for constant DC input

To lower the EMI while operating with a constant DC input voltage, the switching frequency dithering feature can be enabled by configuring the c_{dither} parameter above zero. Based on the modulation gain parameter c_{dither}, t_{on} and $t_{sw,min}$ are modulated in QRMn and DCM, while $t_{sw,min}$ is modulated in ABM, to dither the switching frequency.

c_{dither} = 10 percent parameter setting is recommended and selected in this design example.

17.4 Auto restart time

For all protections with the auto restart reaction, the auto restart time is common and configurable based on $t_{auto,restart}$ parameter.

$t_{auto,restart}$ = 1.2 sec parameter setting is recommended and selected in this design example.

17.5 V_{CC} OVP

The V_{CC} overvoltage protection (OVP) reaction is configurable to latch-mode or auto restart, based on the $Reaction_{VCC,OVP}$ parameter. In addition, the V_{CC} OVP level is also configurable based on the $V_{VCC,max}$ parameter.

$Reaction_{VCC,OVP}$ = Latch-Mode and **$V_{VCC,max}$ = 23 V** are recommended and selected in this design example.

17.6 Regulated mode V_{CC} UVP

$EN_{VCC,UVP}$ parameter refers to the enable switch for the regulated mode V_{CC} undervoltage protection (UVP). The protection reaction is fixed as auto restart and it is triggered when V_{CC} voltage is the same as or lower than regulated mode V_{CC} UVP level of $V_{VCC,min}$, for longer than a blanking time.

$EN_{VCC,UVP}$ = Enabled and **$V_{VCC,min}$ = 7.5 V** parameter settings are recommended and selected in this design example.

17.7 IC overtemperature protection

The IC overtemperature protection level is based on the $T_{critical}$ parameter. If $T_{critical}$ is configured above 119°C, the maximum switching frequency parameter $f_{sw,max}$ cannot be configured above 186.4 kHz. The protection reaction is fixed as auto restart, while the maximum junction temperature for start-up/restart is fixed as 4°C below $T_{critical}$.

$T_{critical}$ = 119°C is recommended and selected in this design example.

17.8 Primary MOSFET over-current protection

V_{OCP2} denotes the CS pin voltage level 2 for the primary MOSFET over-current protection. Under the single-fault condition of shorted primary main winding, the primary MOSFET over-current protection is triggered when the CS pin voltage exceeds V_{OCP2} for longer than a blanking time based on the t_{CSOCP2} parameter.

t_{CSOCP2} = 240 ns is recommended and selected in this design example.

V_{OCP2} level is automatically selected based on **Table 12**. In this design example, $V_{OCP1,at,V,in,low}$ = 0.52 V is selected, so **V_{OCP2} = 0.8 V** is applied automatically. The protection reaction is fixed as auto restart.

Table 12 V_{OCP2} level selection based on $V_{OCP1,at,V,in,low}$ parameter value

$V_{OCP1,at,V,in,low}$ (V)	V_{OCP2} (V)
0.34 to 0.36	0.6
0.37 to 0.54	0.8
0.55 to 0.72	1.2
0.73 to 1.08	1.6

17.9 Debug mode

When the $Debug_{Mode}$ parameter is enabled, the controller enters the stop mode, after a protection is triggered except for the V_{CC} undervoltage lockout. There is no GD pin switching in stop mode and the controller stays in this mode to allow the error code readout for identifying the triggered protection, as long as the V_{CC} stays above the V_{UVOFF} (6 V typ.).

The parameter setting of **$Debug_{Mode}$ = Disabled** is selected in this design example. The $Debug_{Mode}$ parameter should only be enabled for debugging purposes.

18 PCB layout guide

a) Minimize the circumference of the following high-current/high-frequency loop with traces which are short and wide (or with jumper wires which are short and thick).

- Power switch loop formed by DC link filter capacitor $C_{DC,filter}$, primary main winding, flyback MOSFET and CS resistor R_{CS}.
- Main output rectifier loop formed by secondary main winding, main output diode and main output capacitor.
- Auxiliary output rectifier loop formed by auxiliary winding, auxiliary output diode and auxiliary output capacitor.

b) Place each filter capacitor, V_{CC} noise decoupling capacitor $C_{VCCdecouple}$, ZCD pin filter capacitor C_{ZCD} and FB pin filter capacitor C_{FB} near to its designated pin and the GND pin of the controller.

c) Apply the following guide for star grounding.

- Connect ground signal traces of $C_{VCCdecouple}$, C_{ZCD}, $R_{ZCD,2}$, C_{FB}, the controller GND pin and the optocoupler emitter pin.
- Connect V_{CC} ground traces of the V_{CC} capacitor C_{VCC} and primary auxiliary winding.
- Connect the C_{HV} GND pin near to the ground pin of $C_{DC,filter}$.
- Connect the GND pin of each C_{VCC}, $C_{VCCdecouple}$, R_{CS} and bridge rectifier separately to a single point near $C_{DC,filter}$.

d) Ensure the high dv/dt traces from the MOSFET drain and GD pin are as far as possible from the FB pin and its connected trace.

e) Shield signal traces with ground traces or ground plane, which can help to reduce noise pick-up.

f) Always ensure appropriate safety clearances between the high voltage and low voltage nets.

19 Parameter configuration list, setup and procedures

19.1 Parameter configuration list

Figure 23 shows the XDPL8219 parameter configuration list, with selected values based on the design examples from **Section 2** to **Section 17**. For another system design, the values in the list can be different.

For the IC parameter configuration setup and procedures, please refer to **Section 19.2** and **Section 19.3**. For safety purposes, before powering up the board, it is important to ensure that the configured IC parameter values in the hardware configuration section in **Figure 23** are compatible with the actual system hardware dimensioning.

Parameter	Value	Unit
Hardware configuration		
N_p	32.000	
N_s	10.000	
N_a	3.000	
L_p	0.5440	mH
R_CS	0.200	ohm
R_ZCD_1	27.00	kohm
R_ZCD_2	3.90	kohm
C_VCC	22.00	uF
V_out_cap_rating	80	V
R_HV	52.00	kohm
I_GD_pk	30	mA
Startup		
n_ss	3	
V_out_start	31.0	V
V_start_OCP1	0.52	V
V_OCP1_init	0.300	V
Protections		
t_auto_restart	1.2	s
V_OCP1_at_V_in_low	0.52	V
V_OCP1_at_V_in_high	0.43	V
V_in_low	82.0	V
V_in_high	326.0	V
t_CSOCP2	240	ns
Reaction_OVP_Vout	Auto-Restart	
V_outOV	65.0	V
EN_UVP_Vout	Enabled	
Reaction_UVP_Vout	Auto-Restart	
V_outUV	33.0	V
t_VoutUV_blank	500.0	ms
EN_OVP_In	Enabled	
EN_UVP_In	Enabled	
EN_VIN_ABM	Enabled	
V_inOV	350.0	V
t_VinOV_blank	1	
V_in_start_max	326.0	V
V_in_start_min	82.0	V
V_inUV	70.0	V
t_on_max_at_V_in_UV	12.80	us
Reaction_VCC_OVP	Latch-Mode	
V_VCC_max	23.0	V
EN_VCC_UVP	Enabled	
V_VCC_min	7.5	V
T_critical	119	degreeC
Debug_Mode	Disabled	

Parameter	Value	Unit
Multimode		
R_FB_pull_up	5.5	kohm
N_quality	1.6	
n_notch_blank	2	
f_sw_max	186.4	kHz
t_on_min	1.38	us
t_min_demag	2.0	us
t_on_max_at_V_in_low	15.00	us
EN_Burst_Exit_Filter_Feedback	Enabled	
f_burst	130	Hz
n_ABM_min	3	
t_on_min_ABM	1.00	us
t_ABM_blank	6.50	ms
n_wakeup	3	
N_valley_max	14	
N_valley_fast	9	
N_valley_min_at_V_in_high	5	
c_valley_comp	3.00	
V_FB_valley_1	1.500	V
V_FB_max_map	2.000	V
V_FB_sw	1.50	V
V_FB_min	0.30	V
V_FB_limit_step	800.000	mV
Power factor correction		
C_EMI	0.2200	uF
V_EPFC_on	1.00	V
UART reporting		
EN_UART_REPORTING	Enabled	
EN_SEND_LAST_ERROR_CODE	Enabled	
EN_SEND_V_IN_LOSS	Enabled	
UART_POLARITY	Low	
Fine tuning		
t_ZCDPD	350	ns
R_in	10.60	ohm
EN_ETHDC	Disabled	
c_dither	10	%
User ID		
User_ID_A	0	

Figure 23 IC parameter configuration list with selected values based on design examples from Section 2 to Section 17

*Note: User$_{ID,A}$ parameter in **Figure 23** has no effect on the IC behavior and system performance. By default, the value of this parameter is set to zero. If necessary, it can be configured to store system information, such as parameter version, LED driver model, etc.*

19.2 Parameter configuration setup

The tools needed for on-board XDPL8219 parameter configuration are listed in **Table 13**.

Table 13 Tools needed for XDPL8219 parameter configuration

Tool type	Tool name	Description	Ordering/Download link	Ordering/Download content
Hardware	.dp Interface Gen2	.dp Interface board	IF-BOARD.DP-GEN2	.dp Interface Gen2 x 1 USB cable x 1
Software	.dp Vision	GUI for parameter configuration of all .dp products	.dp Vision *Note:* *Please install .dp Vision before running the XDPL8219 .dp Vision folder setup file shown below.*	Latest version of the .dp Vision installer (*.exe)
	XDPL8219 parameter csv file	XDPL8219 parameter configuration file	XDPL8219 40W reference board homepage *Note:* *Please download the zipped package which contains the .dp Vision folder setup file (*.msi)*	Latest version of .dp Vision folder setup file (*.msi), which installs the following XDPL8219 40 W reference design engineering report (*.pdf) and parameter configuration file (*.csv), including images for the configuration file. XDPL8219 design guide (*.pdf)

Figure 24 shows the hardware setup needed for the on-board XDPL8219 parameter configuration.

Note: Please ensure the board is not supplied with any voltage before connecting the programmable cable to the target XDPL8219 board. For parameter configuration on the XDPL8219 40 W reference design, please connect the programming cable to its configuration connector X2.

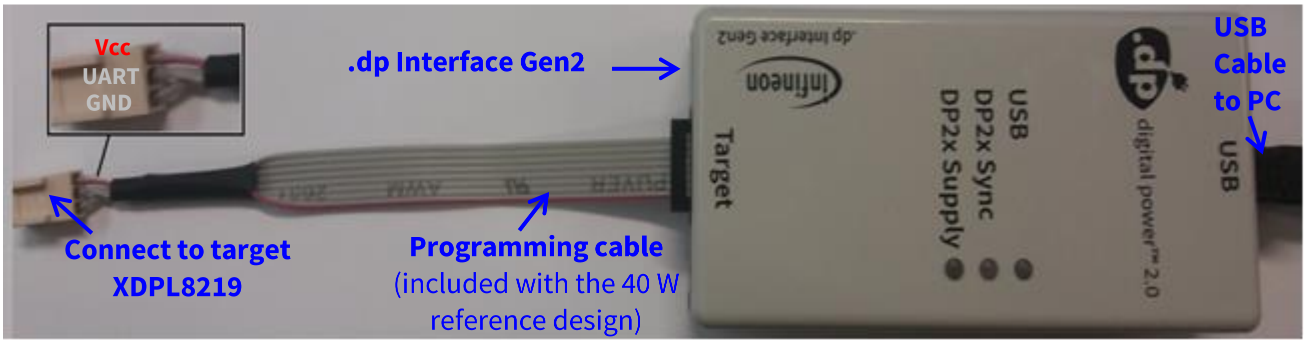


Figure 24 Hardware setup for on-board XDPL8219 parameter configuration

19.3 Parameter configuration procedures

After the hardware connections for XDPL8219 configuration (see **Figure 24**) are done, please start the program by clicking the shortcut ".dp Vision" on the desktop.

Note: *During the program start-up, if the system shows there is a newer version of .dp Vision, please follow the procedure and update accordingly. As the screenshots were taken based on .dp Vision version 2.0.9.4, it might look different for newer versions of .dp Vision.*

A .dp Vision user manual is available by clicking [Help] >> [Help contents], to provide the detailed instructions on how to use this GUI for parameter configuration. Alternatively, the following simple guide is also available for quick and easy reference.

Open the XDPL8219 parameter configuration file (*.csv) from the default installation folder at ***C:\Users\<Username>\Infineon Technologies AG\.dp vision\Parameters***, as shown in **Figure 25**.

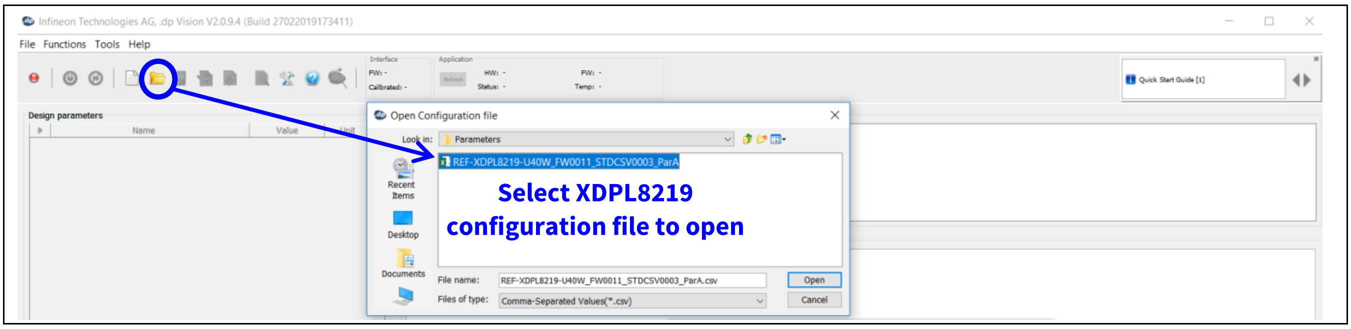


Figure 25 Opening the XDPL8219 parameter configuration file (*.csv) in .dp Vision

After opening the parameter csv file, a list of configurable parameters with default values based on the reference board design will be shown (see the box on the left in **Figure 26**). These default values can be changed for another board design, by referring to the design guide from **Section 2** to **Section 18** and the fine-tuning guide in **Section 20**.

If a parameter value is changed and no limit violation is found, the changed value itself will turn blue, like the example in **Figure 26** which the R_{CS} parameter in the hardware configuration section has been changed from 0.2 Ω to 0.18 Ω. Otherwise, if an error is detected (e.g., exceeded min./max. value), the parameter value which caused the error will turn red and the message bar of .dp Vision (see the top right in **Figure 26**) will show an error message. If any error is not resolved, the user is not allowed to configure the IC with the changed value.

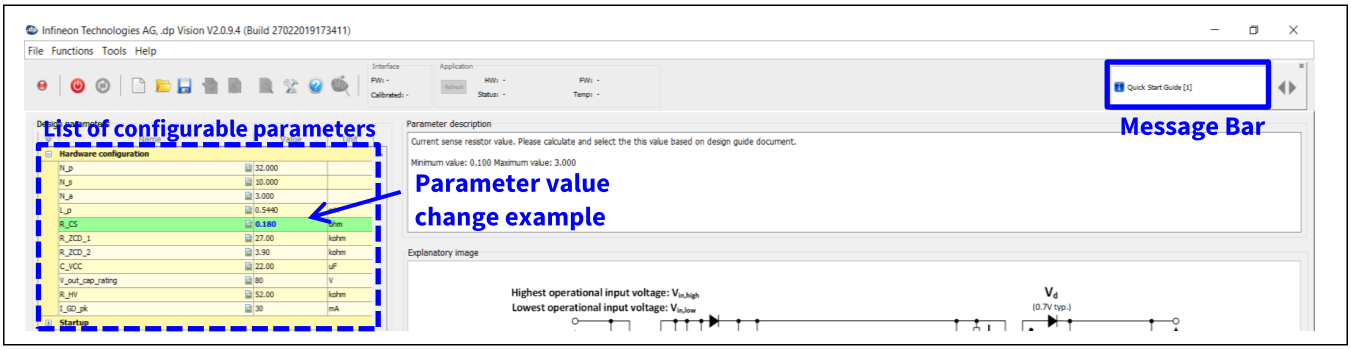


Figure 26 Changing parameter values of XDPL8219 configuration file in .dp Vision

Note: *For safety and proper system functioning, it is important to ensure the hardware configuration section parameter values are compatible with the actual system hardware dimensioning.*

There are two options available to configure the IC based on the list of parameter values shown in .dp Vision.

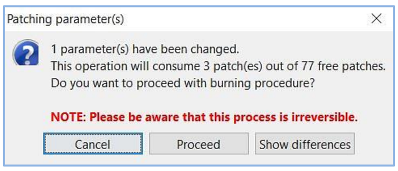
- Burn configuration

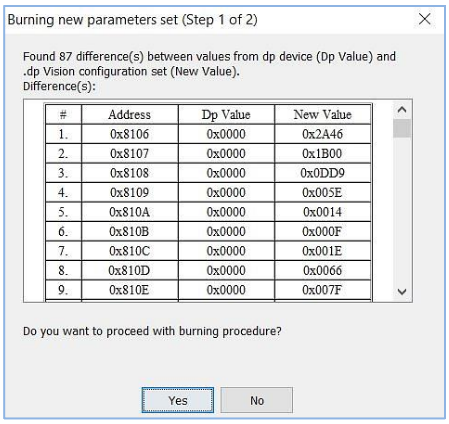
  The new XDPL8219 chip from Infineon does not contain any parameter configuration by default, so the user should first burn a full set of parameters on the new chip using this function, before any application testing. If the XDPL8219 chip on board has already been burned with a first full set of parameters in its one-time programmable (OTP) memory space, such as the XDPL8219 40 W reference board, any IC parameter value change on it with this option is considered as parameter patching. There are total 77 patchable OTP memory spaces.

  Each time the burn configuration function is executed, .dp Vision will detect if there is parameter value difference between the saved configuration file and the target XDPL8219. If a difference is detected, each burn configuration will consume a minimum of three patchable memory spaces. However, the process will be aborted if it requires more memory space than what is available on the target IC. In that case, the user will have to replace the XDPL8219 chip with a new one in order to burn the configuration.

  Table 14 shows the recommended procedures for using the burn configuration function in .dp Vision to burn a first full set of parameters or patch the parameters into the OTP memory.

Table 14 Burn configuration procedures

<table>
<tr><th>Step</th><th>Instruction</th></tr>
<tr><td>I</td><td>Open configuration file using .dp Vision (see example in Figure 25).</td></tr>
<tr><td>II</td><td>If necessary, change any parameter value (see example in Figure 26), then click [File] >> [Save] or [File] >> [Save as] to save the configuration file. Otherwise, proceed to step III.</td></tr>
<tr><td>III</td><td>Ensure that the primary supply voltages (e.g., AC input) to the board are switched off or disconnected, and the hardware connection for configuration is OK based on Figure 24.</td></tr>
<tr><td>IV</td><td>Click to supply power and establish a connection to the target XDPL8219. After this step, XDPL8219 will be in configuration mode (with V_{CC} voltage for OTP programming at 7.5 V ± 0.15 V) and the device status should change to .</td></tr>
<tr><td>V</td><td>Click to burn the configuration to the target XDPL8219.
After this step, you should see a pop-up window, which is similar to one of those below.


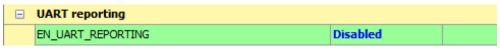
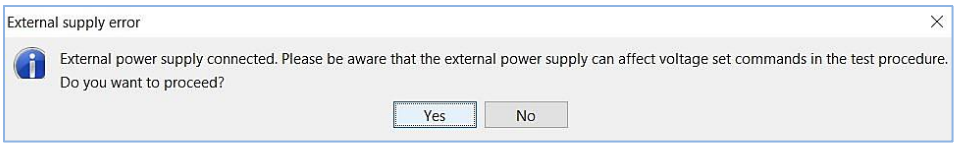
or

</td></tr>
<tr><td>VI</td><td>Click “Proceed” or “Yes” to burn/patch the configuration.
After this step, a pop-up window should show that the burning/patching is successful.</td></tr>
<tr><td>VII</td><td>Click “OK” on the pop-up window, then disconnect the programming cable from the XDPL8219 configuration connector.</td></tr>
</table>

– Test configuration

This function will download the parameter values from the list in .dp Vision into the XDPL8219 RAM, followed by an automatic IC start-up, for application testing with the new configuration (See the recommended procedures in **Table 15**).

Unlike using the burn configuration, parameter configuration with this option is not permanent because the loaded RAM contents will be lost once the IC supply voltage is turned off, but the advantage of using this option is that it does not consume OTP memory space, thus there is no limit on the number of parameter value changes.

Table 15 Test configuration procedures

Step	Instruction
I	Open the configuration file using .dp Vision (see example in **Figure 25**).
II	Ensure that the primary supply voltages (e.g., AC input) to the board are switched off and the hardware connection for configuration is OK based on **Figure 24**, plus a low-ESR ceramic capacitor of 1 nF soldered across the UART pin and ground for noise decoupling.
III	Ensure $EN_{UART,REPORTING}$ parameter is disabled and change the desired parameter value (see example in **Figure 26**).  *Note: If the $EN_{UART,REPORTING}$ parameter is enabled, the success of test configuration cannot be guaranteed, since .dp Vision will show an error due to unable to get the status from XDPL8219 with UART reporting, after the automatic IC start-up with the new configuration in RAM.*
IV	Click [power icon] to supply power and establish a connection to the target XDPL8219. After this step, XDPL8219 will be in configuration mode and the device status [red icon] should change to [green icon].
V	Ensure the board test setup (e.g., output load) is OK, then apply the AC input to the board. After this step, the board does not start-up because XDPL8219 is still in configuration mode.
VI	Click [test icon] to test the new configuration with the target XDPL8219.
VII	If the IC automatically starts up with the new configuration, you should see a pop-up window like the one shown below. Click "OK" to proceed.  *Note: If there is any protection being triggered after step VI, the pop-up window would show that the test configuration is unsuccessful; Please refer **Section 21** for the debugging guide.*
VIII	To test another configuration change, repeat steps II to VII. If the following message box appears in between the steps, click "Yes" to proceed.  Otherwise, turn-off the AC input and disconnect the programming cable from the XDPL8219 configuration connector.

Note: If any error occurs during the parameter configuration procedures, please refer to the message bar of .dp Vision for the error description. For more details, please refer to the .dp Vision user manual.

20 Fine-tuning guide

This section presents guidelines for how to fine-tune the value of a few essential XDPL8219 parameters, based on the actual measurement waveform or data.

20.1 Input voltage-sensing parameter fine-tuning

When the primary MOSFET is switched on, the XDPL8219 measures the current flowing out of the ZCD pin $-I_{IV}$, to estimate the DC link filter capacitor voltage $V_{DC,filter}$.

Ideally, $V_{DC,filter}$ should be a low-frequency (e.g., typically 100 Hz ~ 120 Hz) rectified sinusoidal waveform, as shown in **Figure 27**, where the peak value of $V_{DC,filter}$ is equal to AC input peak value $V_{in,peak}$, and the estimated input voltage V_{in} in rms value is assumed to be 0.707 times $V_{in,peak}$. However, due to the input line filter impedance and the filter capacitor ESR, the actual $V_{DC,filter}$ has high switching frequency ripple (in the kHz range) over the low-frequency sinusoidal waveform, whose ripple peak-to-peak voltage level varies based on the peak current being drawn by the transformer primary main winding. Step III of **Table 16** shows an example of the actual $V_{DC,filter}$ waveform.

To improve the input voltage estimation accuracy, R_{in} parameter fine-tuning is important for the IC to estimate the correct $V_{in,peak}$ by compensating such switching frequency ripples, which appears in $-I_{IV}$ measurements as well.

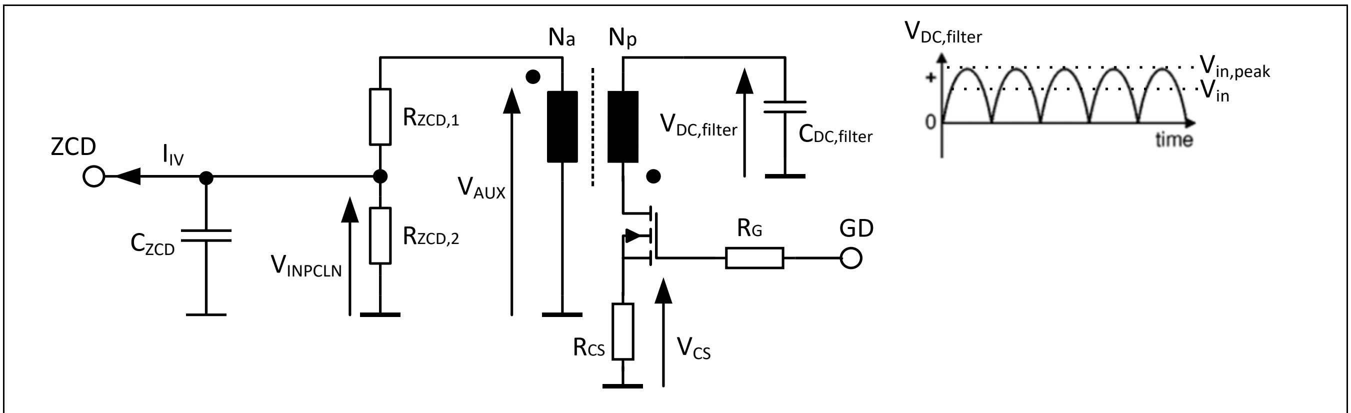
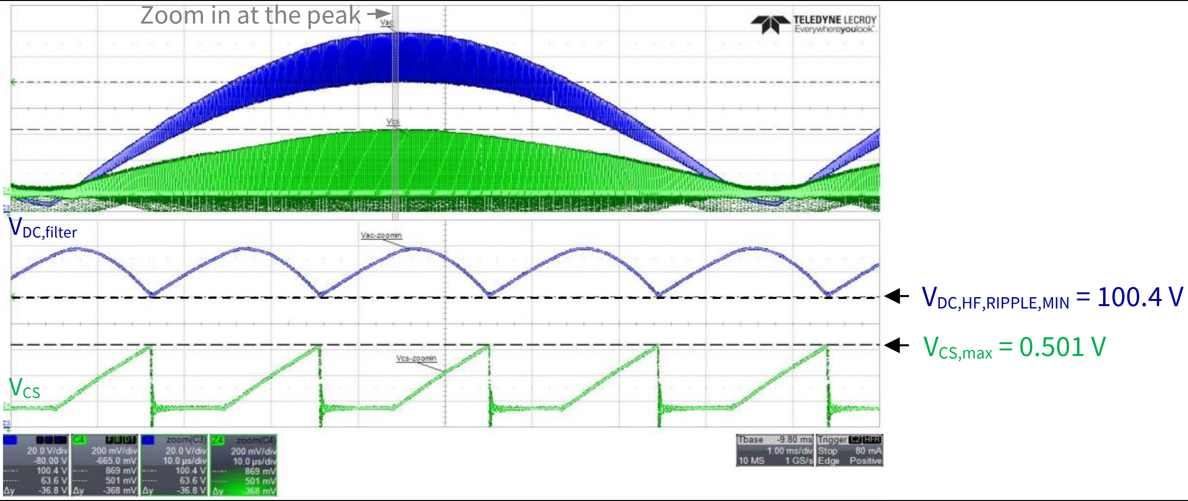


Figure 27 –I_{IV} measurement for input voltage sensing

Table 16 shows the recommended procedures for R_{in} parameter fine-tuning.

Table 16 Recommended procedures for R_{in} parameter fine-tuning

Step	Instruction
I	Apply two voltage probes on the board, which respectively measure the waveform of the DC link filter capacitor voltage $V_{DC,filter}$ and CS pin voltage V_{CS}.
II	Ensure the target XDPL8219 has already been burned with at least a first full set of parameters. Power up the board with normal operational minimum AC input voltage $V_{AC,min}$ and full load output. If it cannot be powered up, retry by burning the input UVP to enable switch parameter $EN_{UVP,In}$ as "Disabled" (if it was not before) or refer **Section 21** for the debugging guide.
III	Capture the voltage waveform with a time base of 1 ms and zoom into the peak voltage for measuring the minimum level of the $V_{DC,filter}$ high-frequency voltage ripple ($V_{DC,HF,RIPPLE,MIN}$) and the maximum level of V_{CS} ($V_{CS,max}$). Below is an example of a waveform captured on the 40 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and full-load output (I_{out} = 0.8 A).

	
IV	Turn-off the AC input. Calculate R1 with the equation below and voltage measurements from step III: $R1 = R_{CS} \cdot \left(\frac{\sqrt{2} \cdot V_{AC,min} - V_{DC,HF,RIPPLE,MIN}}{V_{CS,max}} \right)$, based on full load output Calculation example based on 40 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and full-load output (I_{out} = 0.8 A): $R1 = 0.2 \cdot \left(\frac{\sqrt{2} \cdot 90 - 100.4}{0.501} \right) = 10.73\,\Omega$
V	Repeat step III to obtain another measurement of $V_{DC,HF,RIPPLE,MIN}$ and $V_{CS,max}$ based on 33 percent load.
VI	Turn-off the AC input. Calculate R2 with the equation below and voltage measurements from step V: $R2 = R_{CS} \cdot \left(\frac{\sqrt{2} \cdot V_{AC,min} - V_{DC,HF,RIPPLE,MIN}}{V_{CS,max}} \right)$, based on 33 percent load output Calculation example based on 40 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and 33 percent load output (I_{out} = 0.265 A): $R2 = 0.2 \cdot \left(\frac{\sqrt{2} \cdot 90 - 116.6}{0.281} \right) = 7.59\,\Omega$
VII	Calculate the fine-tuned R_{in} parameter value with the following equation: $Fine\ tuned\ R_{in} = 0.5 \cdot (R1 + R2) + R_{ds(on),25°C} + R_{dc,pri,winding} + R_{CS}$ Where $R_{ds(on),25°C}$ is the MOSFET drain-source on-resistance at 25°C, and $R_{dc,pri,winding}$ is the primary main winding DC resistance. Calculation example based on 40 W reference design: $Fine\ tuned\ R_{in} = 0.5 \cdot (10.73 + 7.59) + 0.9 + 0.265 + 0.2$ $\boldsymbol{Fine\ tuned\ R_{in} \approx 10.5\,\Omega}$
VIII	Use the burn configuration in .dp Vision to patch the R_{in} parameter with the value from step VII and also enable the $EN_{UVP,In}$ parameter (if it was set to “Disabled” before). Then, verify the AC input UVP accuracy at full load and low load.

20.2 QR valley switching parameter fine-tuning

Unlike conventional analog solutions which achieve QR valley switching by introducing an external hardware delay on the zero-crossing signal with the ZCD pin capacitor, the XDPL8219 ZCD pin capacitor is mainly used for noise filtering only. Therefore, a fixed capacitor value, e.g., 47 pF, can be used across designs of different power classes. To achieve QRMn, the XDPL8219 dynamically measures the resonant period and delays the MOSFET switch-on by a quarter of the resonant period after zero-crossing of the primary auxiliary winding voltage.

t_{ZCDPD} parameter fine-tuning is, however, necessary to compensate for XDPL8219 internal propagation delay in ZCD and also external delay caused by the noise-filtering capacitor at the ZCD pin. **Table 17** shows the recommended procedures for t_{ZCDPD} parameter fine-tuning.

Table 17 Recommended procedures for t_{ZCDPD} parameter fine-tuning

Step	Instruction
I	Apply a differential probe on the board to measure the flyback MOSFET drain voltage waveform.
II	Set the t_{ZCDPD} parameter to 0 and use the test configuration function in .dp Vision to power up the board with lowest typical AC input voltage, e.g., 120 V_{rms}, and full-load output. If the board cannot be powered up, please refer to **Section 21** for the debugging guide.
III	Capture the waveform with a 1 ms time base and zoom into the voltage peak with a 1 µs time base.
IV	Place a horizontal cursor at the highest possible level which crosses two points on the resonance part of the waveform (see a and b below), and measure the time between them ($t_{a\text{-}b}$). In the example below, which is based on the 40 W reference design, $t_{a\text{-}b}$ is measured to be approximately 744 ns. 
V	Set the t_{ZCDPD} parameter as approximately half of $t_{a\text{-}b}$ and burn the configuration with .dp Vision.
VI	Disconnect the programming cable after burning, then power up the board and the flyback MOSFET drain voltage waveform should be switching at the QRM1 (see example below based on the 40 W reference design with **fine-tuned t_{ZCDPD} = 370 ns**). 

20.3 Power factor related parameter fine-tuning

The enhanced PFC feature can be enabled by configuring the C_{EMI} parameter above zero and fine-tuning the value to compensate for the current displacement effect, which is mainly caused by the DC link filter capacitor and the line filter. A higher C_{EMI} parameter value gives higher compensation and vice versa.

The recommended starting value of the C_{EMI} parameter is the value of the DC link filter capacitor $C_{DC,filter}$ placed after the bridge rectifier. If necessary, fine-tune the C_{EMI} parameter using the test configuration function in .dp Vision, to achieve the optimized power factor and THD. For example with the XDPL8219 40W reference design, the initial C_{EMI} based on $C_{DC,filter}$ is 0.22 μF for powering up of the board, and the **fine-tuned C_{EMI} = 0.16 μF** parameter is then selected for performance optimization.

20.4 THD related parameter fine-tuning

To achieve low THD in QRMn and DCM, it is important to stabilize the $V_{FB,filtered}$ which is based on the digital notch filter output, by ensuring the a.c. component of the FB pin voltage signal to be a sinusoidal wave with double-line frequency.

Figure 28 (left) shows an input current distortion near the peak due to the FB pin non-sinusoidal a.c. wave, which has its peak clamped at FB pin pull-up voltage V_{REF} (2.428 V typ.). To avoid the voltage clamp for a more sinusoidal a.c. wave signal on the FB pin, the SSR feedback compensation network, consisting of R_{comp} and C_{comp} (see **Figure 16**), can be fine-tuned to reduce the FB pin voltage ripple. In this design example, such distortion can be seen when using the initial R_{comp} = 68 kΩ and initial C_{comp} = 470 nF (calculated from **Section 14**) for powering up of the board. Therefore, the **fine-tuned R_{comp} = 47 kΩ, fine-tuned C_{comp} = 470 nF** are then chosen, to overcome such distortion, as shown in **Figure 28 (right)**.

If the EN_{ETHDC} parameter is enabled to further enhance the THD correction, it is important to ensure the output and FB pin voltage ripple increase would not cause the peak clamped to V_{REF} similarly as **Figure 28 (left)**.

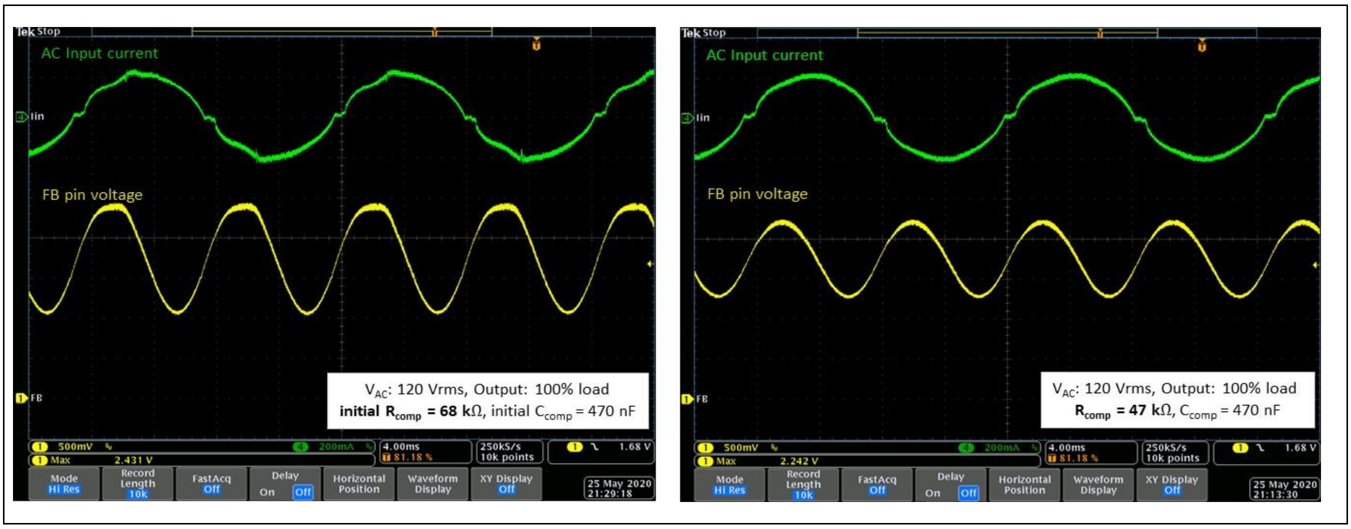


Figure 28 Input current distortion near the peak due to the FB pin non-sinusoidal a.c. waveform, and fine-tuning

When $f_{sw,max}$ parameter is configured too low, there can be input current glitches (distortion) caused by the non-valley switching, as shown in **Figure 29 (left)**. Therefore, a higher $f_{sw,max}$ value (e.g., 186.4 kHz) is recommended and selected in this design example, to minimize the fine-tuning effort, while ensuring a good power quality, as shown in **Figure 29 (right)**.

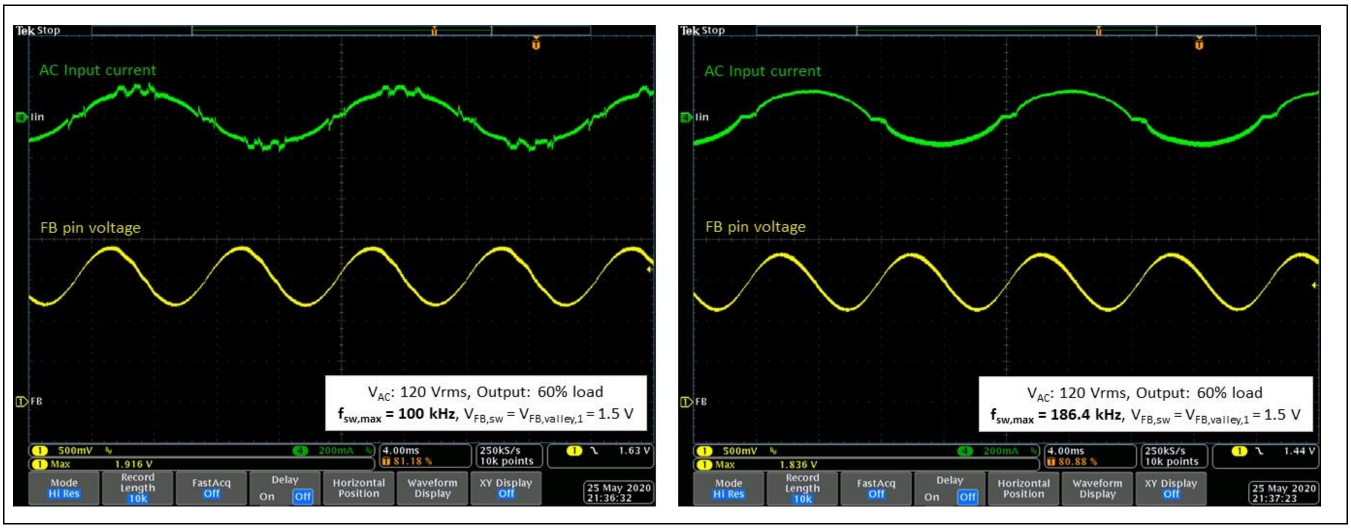


Figure 29 Input current glitches (distortion), when $f_{sw,max}$ is too low

When $N_{valley,min,at,V,in,high}$ parameter is configured too low for an universal input design, there can be input current glitches (distortion) at higher input voltage, which are caused by the non-valley switching and changing quasi-resonant duty cycle over the half-sine wave period, as shown in **Figure 30 (left)**. Therefore, a higher $N_{valley,min,at,V,in,high}$ value (e.g., 4 or 5) is recommended for an universal input design and selected in this design example, to minimize the fine-tuning effort, while ensuring a good power quality, as shown in **Figure 30 (right)**.

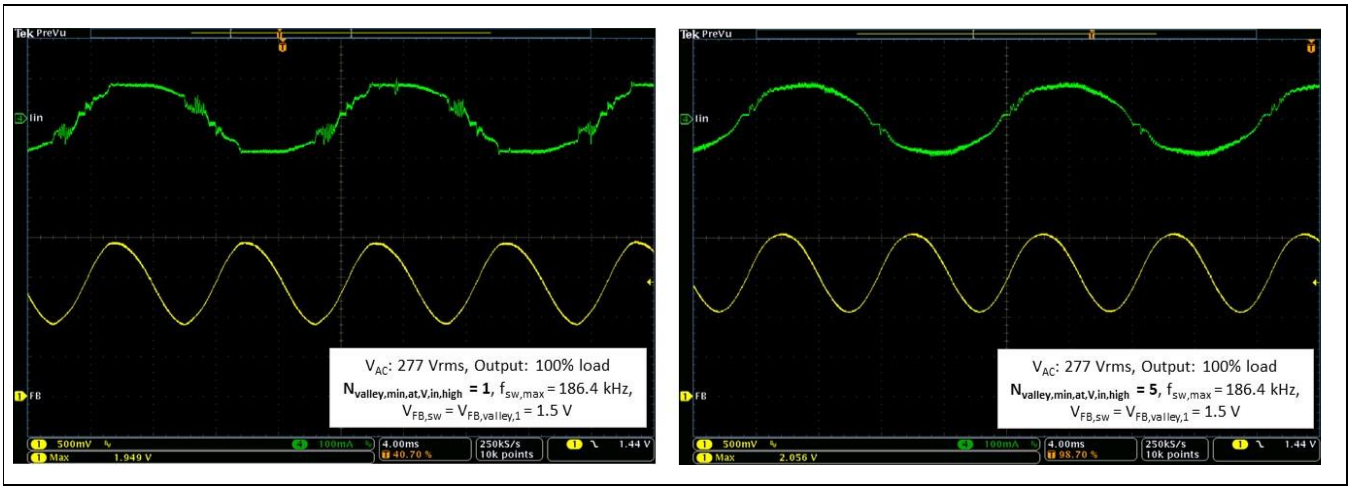


Figure 30 Input current glitches (distortion) at higher input voltage, when $N_{valley,min,at,V,in,high}$ is too low for an universal input design

21 Debugging guide

This section presents the guidelines for system debugging, if the board has any problem with powering up or shutting down during testing.

With XDPL8219, there are 3 debugging options, to identify the triggered protection for the powering up or shutting down problem:

i) UART reporting error code readout (Refer the procedures in **Section 21.1**)

ii) Debug mode error code readout by test configuration (Refer the procedures in **Section 21.2**)

iii) Debug mode error code readout by burn configuration (Refer the procedures in **Section21.3**)

Figure 31 presents the flowchart to systematically choose the suitable debugging option for the problem, depending on the following checkpoints:

- Does V_{CC} drop to V_{UVOFF} (6 V typ.) when the powering up or shutting down problem takes place? (Yes/No)
- Is the UART reporting feature enabled for the target application? (Yes/No)
- Is there any ABM operation, ABM entering or exiting, needed to trigger the powering up or shutting down problem? (Yes/No/Not sure)

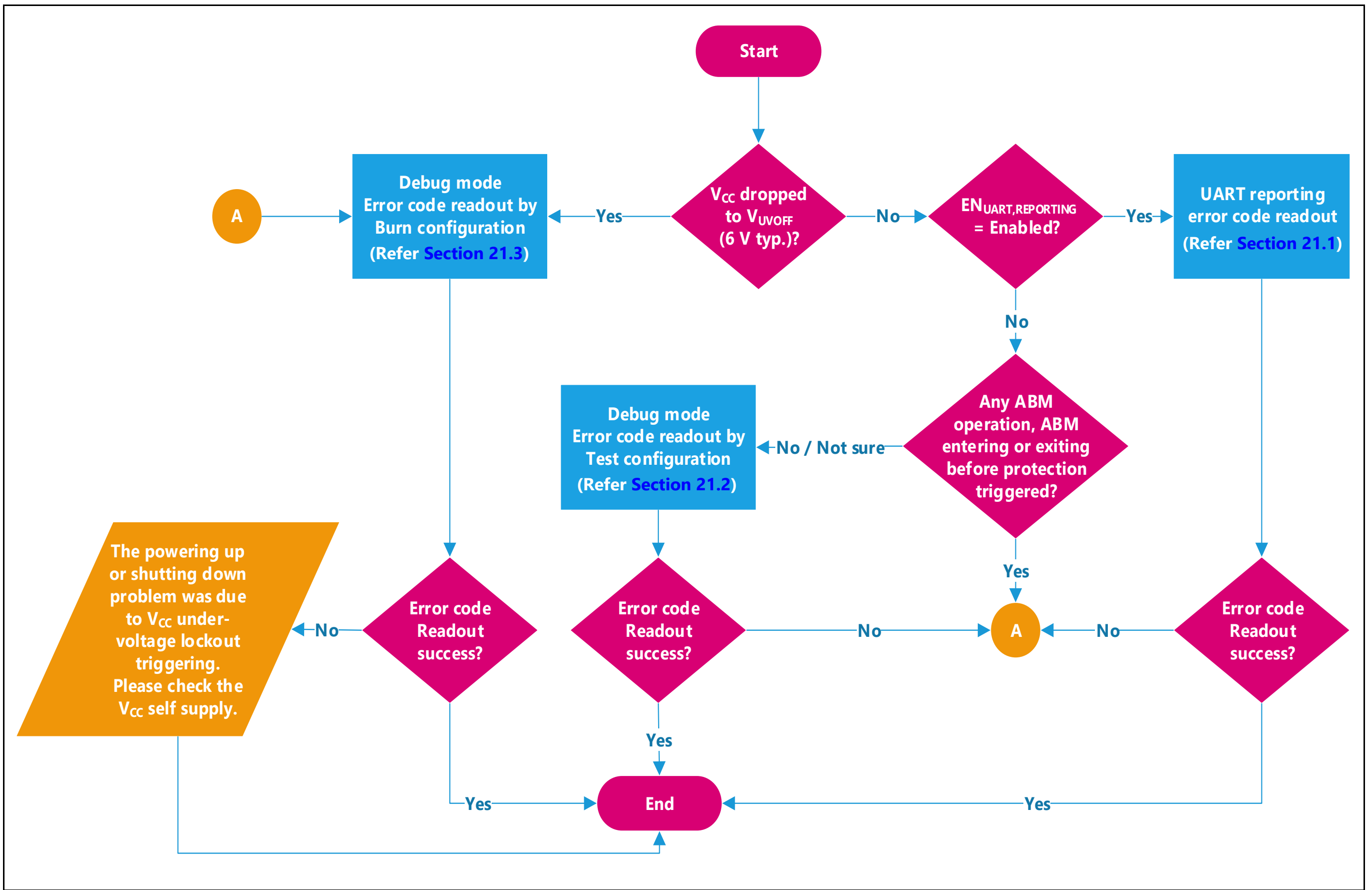
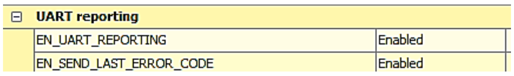
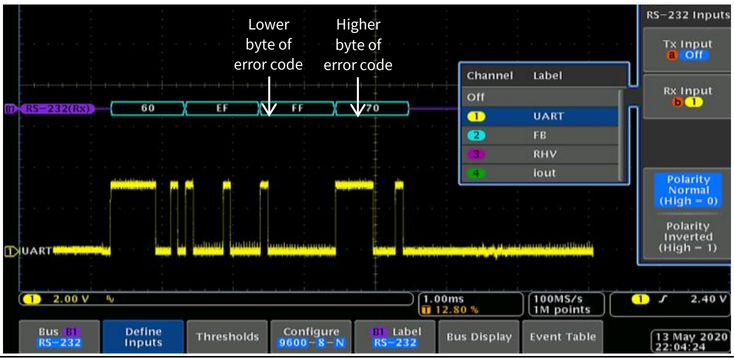


Figure 31 Flowchart to choose the debugging option (for powering up or shutting down problem)

Depending the error code readout success of the first debugging option recommended by the flowchart, a second debugging option might be recommended by the flowchart, to read out the error code or to identify the triggered protection.

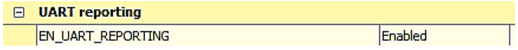
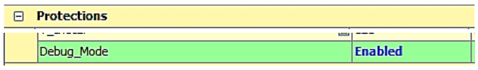
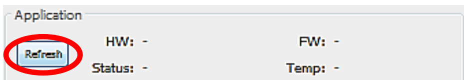
21.1 UART reporting error code readout

Table 18 Procedures for UART reporting error code readout

Step	Instruction
I	**Open the configuration file** (see the example in **Figure 25**) used in the system which has the powering up or shutting down problem.
II	**If both $UART_{REPORTING}$ and $EN_{SEND,LAST,ERROR,CODE}$ parameters have already been "Enabled", proceed to next step. Otherwise, save the configuration file with both parameters being "Enabled" and burn the configuration** (follow the burn configuration procedures in **Table 14**). 
III	**Ensure the primary supply voltage (e.g., AC input) to the board is switched off and the programming cable is disconnected** from the board.
IV	**Apply 2 voltage probes, to measure the GD pin and UART pin signals.** Set the oscilloscope on roll mode with 500 ms time base and the sampling rate of at least 200k samples per second.
V	**Supply the board with the initial primary supply voltage (e.g., AC input) and output load**, which can trigger the powering up problem, or the shutting down problem afterwards. **Proceed to Step VII, if a protection has been triggered**.
VI	To debug the desired shutting down problem, after the powering up, **apply the necessary input/output condition change to trigger the protection for the shutting down**.
VII	**Capture the oscilloscope waveform** upon triggering the protection in step V or VI, and **zoom into the UART signal** at auto restart, which is approximately the fast auto restart time of 0.4 sec, or the configured auto restart time $t_{auto,restart}$, after the IC's GD pin stops switching. *Note: If the triggered protection reaction is not auto restart, with the auto restart time of approximately 0.4 sec or $t_{auto,restart}$, the error code data readout will not be successful, so please refer **Figure 31** for the next debugging step.*
VIII	**Decode the UART data packet** based on the configured $UART_{POLARITY}$ parameter setting (Low or High) and the baud rate of 9.6 kbps (without parity). **Ensure that an error code data packet with the first byte value of 60_H has been found**, before proceed to next step.
IX	**Read out the lower byte and higher byte of error code** (second byte and third byte of the error code data packet) and identify the triggered protection based on Error! Reference source not found.. Below is an example of a captured error code data packet based on $UART_{POLARITY}$ parameter = "Low". The error code readout is $FFEF_H$. Based on Error! Reference source not found.**,** the start-up output UVP has been triggered. 
X	To abort the error code readout, switch off the primary supply voltage (e.g., AC input), and if necessary, revert the step II parameter change by burn configuration.

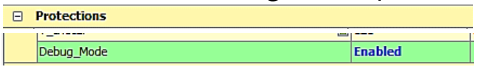
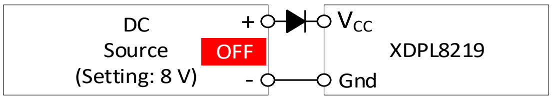
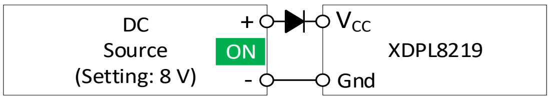
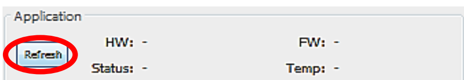
21.2 Debug mode error code readout by test configuration

Table 19 Procedures for debug mode error code readout by test configuration

Step	Instruction
I	**Open the configuration file** (see the example in **Figure 25**) used in the system which has the powering up or shutting down problem, then set **$\text{Debug}_{\text{Mode}}$ parameter to "Enabled"** and ensure **$\text{EN}_{\text{UART,REPORTING}}$ parameter is "Disabled"**.  
II	**Ensure the primary supply voltage (e.g., AC input) to the board is switched off and the hardware connection for configuration is OK** based on **Figure 24**, plus a low-ESR ceramic capacitor of 1 nF soldered across the UART pin and ground for noise decoupling.
III	**Click to supply power and establish connection** to the target XDPL8219. After this step, the XDPL8219 will be in configuration mode and the device status should change to .
IV	**Supply the board with the initial primary supply voltage (e.g., AC input) and output load**, which can trigger the powering up problem, or the shutting down problem afterwards. After this step, the board does not start-up yet because XDPL8219 is still in configuration mode.
V	**Click to test the configuration with the target XDPL8219.** After this step, the IC will automatically start-up in debug mode. **If a protection is triggered when powering up, the IC's GD pin stops switching and the output will stay low.** *Note: If the desired powering up problem cannot be reproduced, please repeat the steps above to debug again or refer **Figure 31** for the next debugging step.*
VI	There should be a pop-up window like the one shown below. **Click "OK" in the pop-up window**. **Proceed to Step VIII, if a protection has been triggered after step V**.  *Note: If there is an error pop-up instead, please repeat the steps above to debug again or refer **Figure 31** for the next debugging step.*
VII	To debug the desired shutting down problem, after the powering up, **apply the necessary input/output condition change to trigger the protection for the shutting down**. If a protection is triggered, the IC's GD pin stops switching and the output will stay low. *Note: If the desired shutting down problem cannot be reproduced, please repeat the steps above to debug again or refer **Figure 31** for the next debugging step.*
VIII	**Switch off the primary supply voltages (e.g., AC input)** and **click the "Refresh" button** in the .dp Vision application section. Proceed to next step if there is a status code readout.  *Note: If there is device status change to or any error pop-up before this step, the "Refresh" button will not be available for error code readout. Please repeat the steps above to debug again or refer **Figure 31** for the next debugging step.*
IX	**Hover the mouse over the status code** and the description of the status code will be shown. For example, 0x0040 means input UVP has been triggered.
X	**To repeat the error code readout, start from step II again**. To abort this, ensure the primary supply voltage (e.g., AC input) is off, then disconnect the programming cable from the board.

21.3 Debug mode error code readout by burn configuration

Table 20 Procedures for debug mode error code readout by burn configuration

Step	Instruction
I	**Open the configuration file** (see the example in **Figure 25**) used in the system which has the powering up or shutting down problem.
II	**Save the configuration file with $\text{Debug}_{\text{Mode}}$ parameter = "Enabled", and burn the configuration** (follow the burn configuration procedures in **Table 14**). 
III	**Ensure the primary supply voltage (e.g., AC input) to the board is switched off**, then **disconnect the programming cable** from the .dp Interface Gen2's 8 pins connector.
IV	**Ensure DC source output is off**, then **connect DC source** (Setting: 8 V) to XDPL8219 V_{CC} **via a diode**. 
V	**Switch on the DC source output.** 
VI	**Supply the board with the initial primary supply voltage (e.g., AC input) and output load**, which can trigger the powering up problem, or the shutting down problem afterwards. After that, **if a protection is triggered when powering up, the IC's GD pin stops switching and the output will stay low. Proceed to Step VIII, if a protection has been triggered.** *Note: If the desired powering up problem cannot be reproduced, please repeat the steps above to debug again or refer* ***Figure 31*** *for the next debugging step.*
VII	To debug the desired shutting down problem, after the powering up, **apply the necessary input/output condition change to trigger the protection for the shutting down**. If a protection is triggered, where the IC's GD pin stops switching and the output will stay low. *Note: If the desired shutting down problem cannot be reproduced, please repeat the steps above to debug again or refer* ***Figure 31*** *for the next debugging step.*
VIII	**Turn-off the primary supply voltage (e.g., AC input)**.
IX	**Ensure again the primary supply voltage is off, then reconnect the programming cable to the .dp Interface Gen2.** Ensure the hardware connection for configuration is OK based on **Figure 24**.
X	**Click** **to supply power and establish connection** to the target XDPL8219. After this step, the XDPL8219 will be in configuration mode and the device status should change to .
XI	**Click the "Refresh" button** in the .dp Vision application section. Proceed to next step if there is a status code readout. 
XII	**Hover the mouse over the status code** and the description of the status code will be shown. For example, 0x0040 means input UVP has been triggered.
XIII	**To repeat the error code readout, turn-off the DC source before starting from step III again**. **To abort this, burn the configuration with $\text{Debug}_{\text{Mode}}$ parameter = "Disabled"**, and disconnect the programming cable from the board.

22 References

[1] XDPL8219 datasheet

[2] REF-XDPL8219-U40W engineering report

23 Revision history

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V 1.0	17-06-2020	First release

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