3300 W continuous conduction mode totem pole PFC with 600 V CoolMOS™ CFD7 and XMC™

EVAL_3K3W_TP_PFC_CC

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About this document

Scope and purpose

This document presents a system solution based on Infineon CoolMOS™ CFD7 silicon superjunction power semiconductors, drivers and microcontroller for a bridgeless totem pole power factor correction (PFC) converter operated in continuous conduction mode (CCM). In order to use the CoolMOS™ CFD7 in CCM operation a pre-charge circuit is added to the traditional totem pole topology. This document shows the operation of such a circuit and the design procedure. The **EVAL_3K3W_TP_PFC_CC** is intended for those applications which require the highest efficiency (99 percent) and high power density (92 W/in^3), such as high-end server and telecom.

Furthermore, the implementation of the totem pole PFC with CoolMOS™ CFD7 provides an attractive price–performance ratio. The totem pole implemented in the EVAL_3K3W_TP_PFC_CC board operates at 65 kHz with full digital control implementation on an Infineon XMC1000 series microcontroller.

The Infineon components used in this 330 W bridgeless CCM totem pole PFC board are:

- **600 V CoolMOS™ S7** and **CFD7** superjunction MOSFET
- **EiceDRIVER™ 2EDF7275F** safety isolated gate drivers
- **XMC1402** microcontroller
- **ICE5QSAG** CoolSET™ quasi-resonant (QR) flyback controller
- **950 V CoolMOS™ P7** superjunction MOSFET
- **OptiMOS™ 100 V MOSFET** and **CoolSiC™ 650 V** Schottky diode

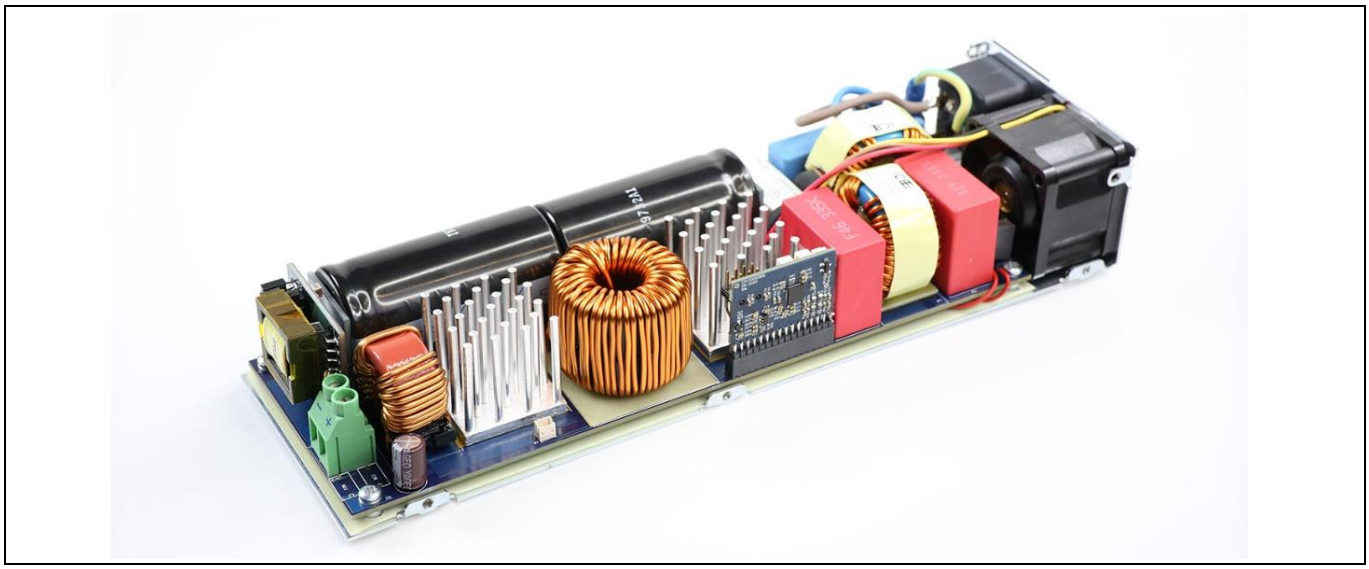

Figure 1 **3300 W bridgeless totem pole PFC with CoolMOS™ and XMC™ control. The plastic enclosure has been removed for a better view.**

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1 System description

The **EVAL_3K3W_TP_PFC_CC board** is a system solution enabled by Infineon as well as drivers and a microcontroller. The evaluation board consists of a bridgeless totem pole PFC rectifier and it is intended for high-end applications in which the highest efficiency is required. Totem pole PFC topology is simple and offers a reduced part count and full utilization of the PFC inductor and switches [1]. For these reasons, totem pole PFC achieves high power density at a reduced system cost for high-performance systems.

The EVAL_3K3W_TP_PFC_CC board operates in CCM exclusively at high-line (176 Vrms minimum, 230 Vrms nominal), with a fixed switching frequency of 65 kHz. It implements the surface-mount device (SMD) 600 V CoolMOS™ CFD7 silicon (Si) superjunction MOSFETs to enable a high power density (80 W/in^3, including fan and connectors) totem pole implementation with an attractive performance–price ratio. As shown in **Figure 2**, with the CoolMOS™ CFD7 CCM totem pole solution, the next level of silicon-based efficiency (close to 99 percent for nominal AC voltage) can be reached. Therefore, EVAL_3K3W_TP_PFC_CC board is a cost attractive alternative complementing the powerful offering of wide bandgap solutions from infineon technologies.

Note: Due to production tolerances and differences between measurement setups, efficiency variations of up to ±0.2 percent may be observed in the results.

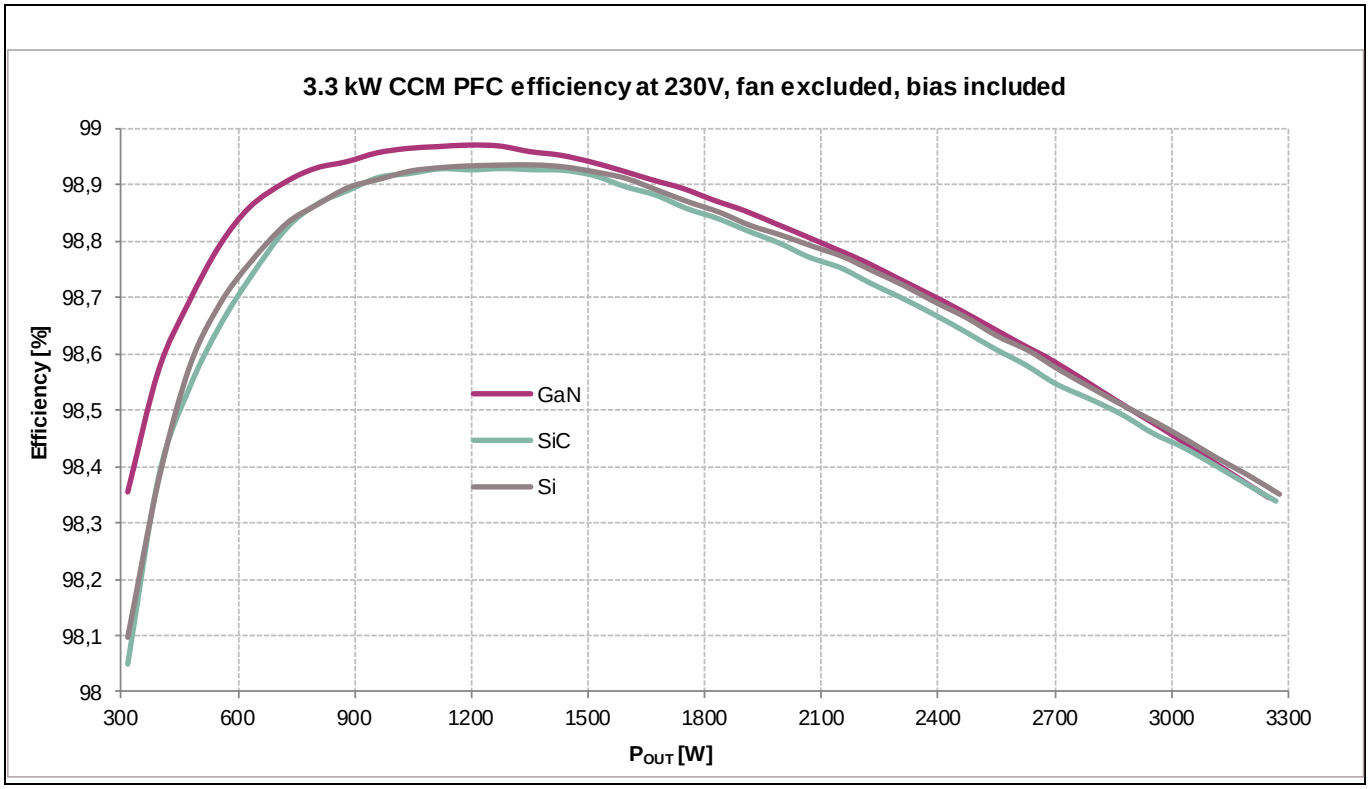


Figure 2 Measured efficiency at 230 V of the 3300 W totem pole PFC with 90 mΩ CoolMOS™ CFD7 and 22 mΩ CoolMOS™ S7

The PFC function, to achieve bulk voltage regulation while demanding high-quality current from the grid, is implemented with an Infineon XMC1402 microcontroller [2]. Further detail on PFC control implementation in the XMC1000 family can be found in the application notes of other Infineon PSU and PFC evaluation boards with classic-boost, dual-boost or totem pole topologies [3] to [6].

System description

The 3300 W CCM bridgeless totem pole PFC with 600 V CoolMOS™ CFD7 presented in this application note is a system solution developed with Infineon power semiconductors, all of them in SMD packages, as well as Infineon drivers and controllers.

The Infineon devices used in the implementation of the EVAL_3K3W_TP_PFC_CC board are listed below:

- 90 mΩ 600 V CoolMOS™ CFD7 (**IPT60R090CFD7**) in TO-Leadless (TOLL) package, as totem pole PFC high-frequency switches
- 22 mΩ 600 V CoolMOS™ S7 (**IPT60R022S7**) in TOLL package, for the totem pole PFC return path (low-frequency half-bridge)
- **BSZ440N10NS3** and **IDDD08G65C6** Double DPAK (DDPAK), for a required pre-charge circuit to enable CCM totem pole operation with CoolMOS™ CFD7
- **2EDF7275F** isolated and **1EDN8511B** non-isolated gate drivers (EiceDRIVER™)
- **ICE5QSAG** QR flyback controller and 950 V CoolMOS™ P7 (**IPU95R3K7P7**) for the bias auxiliary supply.
- **XMC1402** microcontroller for PFC control implementation

A simplified block diagram of the bridgeless topology with the devices mentioned from the Infineon portfolio is shown in **Figure 3**. It can be seen in the simplified block diagram that a low-voltage (LV) OptiMOS™ and a CoolSiC™ silicon-carbide (SiC) diode are enclosed together with the driver for the high-frequency half-bridge. This circuit is required to enable hard-commutation operation of the CoolMOS™ CFD7, and it will be shown in more detail in section 2.

Note: *The diode bridge in front of the totem pole PFC converter is meant to be a current path for start-up or surge conditions, and it is not part of the current path during the steady-state converter operation.*

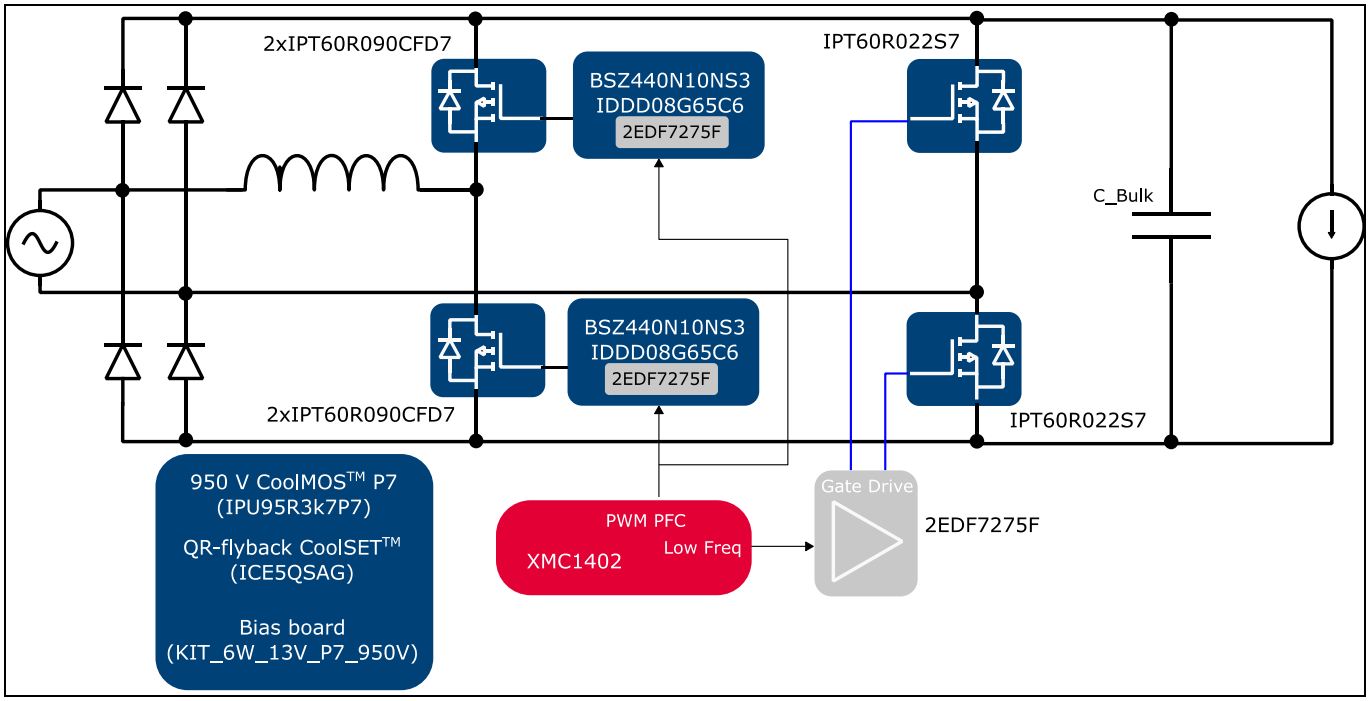


Figure 3 **3300 W bridgeless totem pole PFC board with CoolMOS™ CFD7 (EVAL_3K3W_TP_PFC_CC) – simplified diagram showing the topology and the Infineon semiconductors used**

This document will describe the EVAL_3K3W_TP_PFC_CC board implementation, as well as the specifications and main test results. For further information on Infineon semiconductors visit the **Infineon** website, the Infineon **evaluation board** search, and the different websites for the different implemented components:

- **CoolMOS™** power MOSFET
- **Gate driver ICs**
- QR **CoolSET™**
- **XMC™** microcontrollers
- **OptiMOS™** power MOSFET
- **CoolSiC™** Schottky diodes

1.1 Board description

The evaluation board EVAL_3K3W_TP_PFC_CC is mounted over a metallic chassis and covered by a plastic enclosure to suit the fan. **Figure 4** shows placement of the different sections of the bridgeless totem pole PFC with Infineon 600 V CoolMOS™. The board is 240 mm long, with a width of 70 mm and a height of 40 mm (1U), for a power density of 80 W/in^3. The dimensions shown include the fan as well as the input and output connectors.

Immediately after the AC input connector, a two-stage EMI (electromagnetic interference) filter is placed, as well as a fuse and NTC inrush current limiter, together with the input relay. The fan is placed at the side of the AC connector and blows air out of the evaluation board. The DC output connector is placed on the other side of the board than the AC connector. Close to the output connector, a common-mode choke is placed to guarantee proper acquisition of the output variables in efficiency measurements.

Two daughter cards are introduced: the bias board and the control card. The bias board (**KIT_6W_13V_P7_950V**) uses a QR CoolSET™ controller and 950 V CoolMOS™ P7 switch to generate the required voltages for the control card, driving, relay, fan supply and pre-charge voltage supply. The control card implements the required current, voltage and polarity sensing. The full digital control is implemented in the Infineon XMC™ microcontroller, which is in charge of the proper operation of the bridgeless totem pole topology.

The rest of the board is occupied by the bridgeless totem pole itself, which comprises the PFC choke, the bulk capacitor and a bridge with 600 V CoolMOS™ CFD7 and 600 V CoolMOS™ S7. The bulk capacitance is designed to comply with the hold-up time shown in Table 2. The semiconductors in SMD package (TOLL and DDPAK) are mounted on the bottom side of the board (**Figure 5**). Two heatsinks, at both sides of the PFC choke, help to remove the heat dissipation of the SMD semiconductors mounted in the bottom side. The choke is designed with high-flux GT material in order to comply with the height requirement, high efficiency performance and high power density.

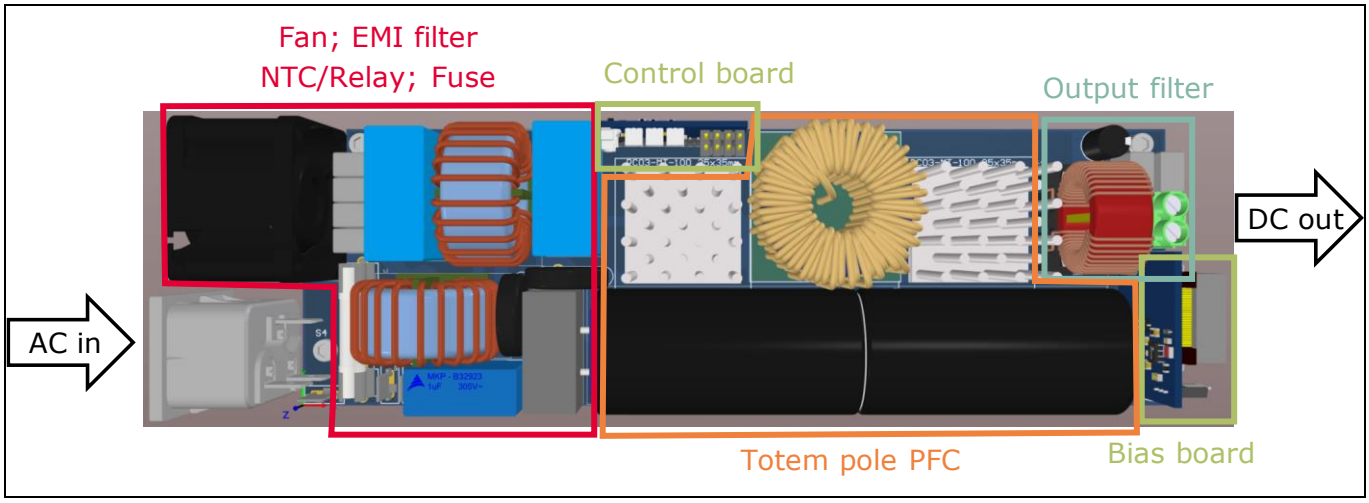


Figure 4 **Placement of the different sections in the 3300 W bridgeless totem pole PFC with Infineon 600 V CDF7 and CoolMOS™ S7 MOSFETs and XMC™ control**

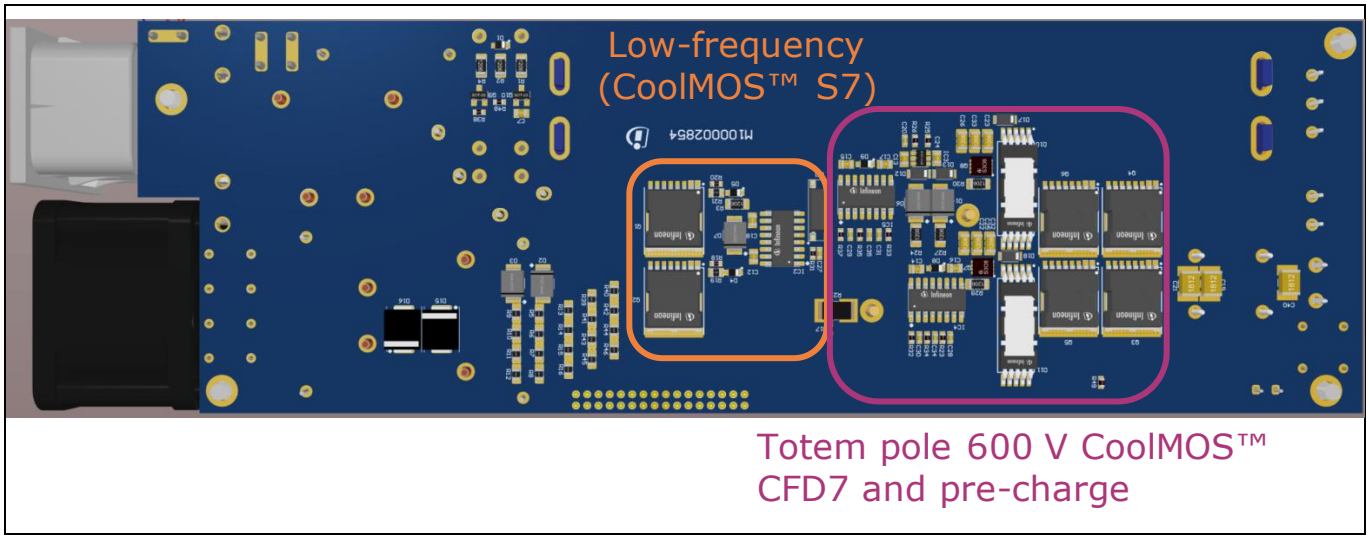


Figure 5 **SMD power semiconductors mounted on the bottom side of the PCB**

2 Lossless hard-commutated operation of CoolMOS™ in CCM totem pole PFC

The use of Si superjunction MOSFETs and CoolMOS™ in a half-bridge configuration does not enable high performance of the totem pole PFC in CCM operation. The reasons are the very high charge (Q_{oss}) required to charge and discharge the highly non-linear C_{oss} of the devices together with the significantly high reverse-recovery losses of the intrinsic body diode of the Si superjunction MOSFETs (**Figure 6**).

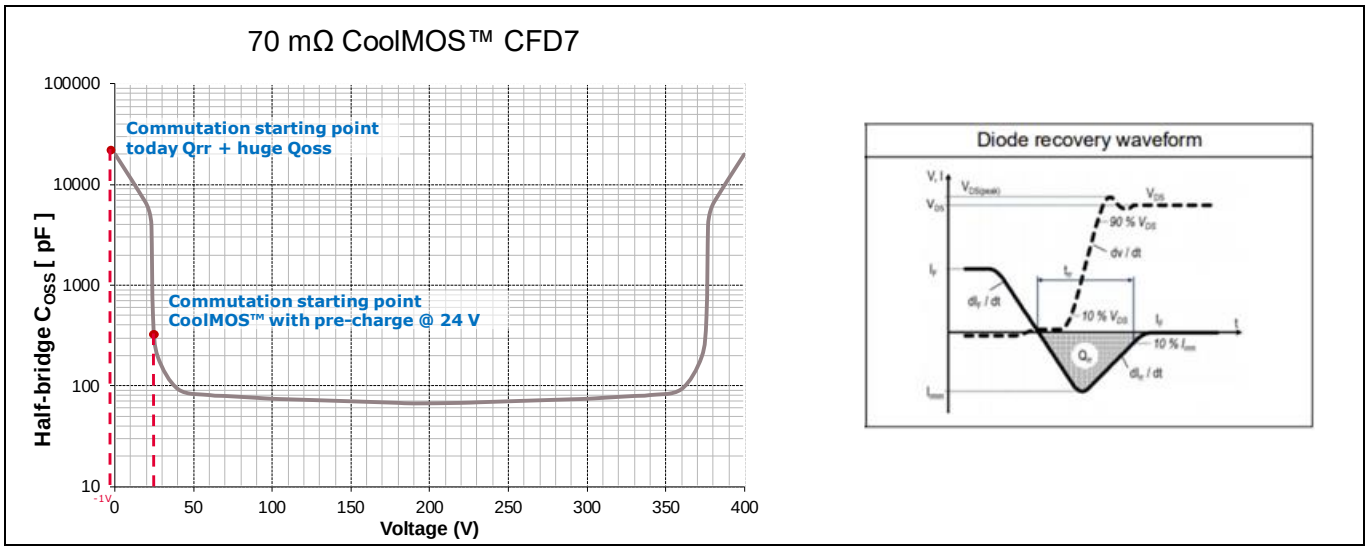


Figure 6 C_{oss} behavior in a half-bridge (left), and reverse recovery charge (right) of CoolMOS™ CFD7

In order to use CoolMOS™ in a hard-commutated half-bridge, e.g., in CCM PFC, a solution based on a pre-charge circuit is implemented in EVAL_3K3W_TP_PFC_CC. The implementation is presented in **Figure 7** as a typical double-pulse test configuration, which reflects the hard-commutation event at the diode-to-switch transition in the totem pole PFC operating in CCM. In that topology, hard-commutation of the diode-mode switch occurs every switching cycle.

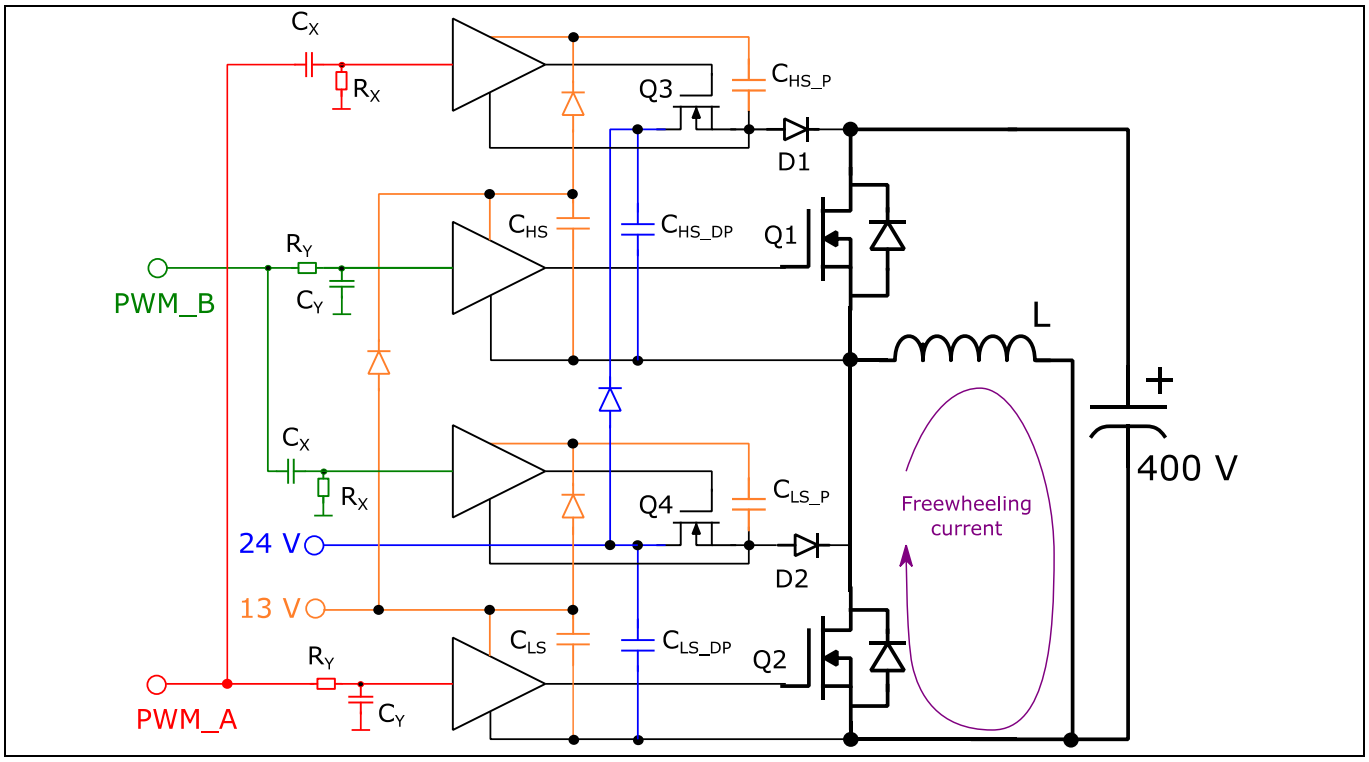


Figure 7 **Circuit diagram for operation of CoolMOS™ superjunction MOSFETs in a hard-commutated half-bridge**

In the half-bridge of **Figure 7**, Q2 typically turns on with soft-switching, after Q1 turns off, given the energy accumulated in the inductor connected to the switching node. However, when Q2 is turned off, the inductor current keeps flowing through its body diode (freewheeling current) and a hard-commutation of Q2 body diode current occurs when Q1 is turned on.

With the added pre-charge circuit, the Si superjunction MOSFET operating in freewheeling or “diode mode” (Q2 in **Figure 7**) can be depleted to a certain level, e.g., 24 V, before its channel is switched on. This drastically reduces the losses associated with its output capacitance charge (Q_{oss}), and the reverse recovery charge (Q_{rr}) of its body diode during the turn-off transition, since those charges are provided from a LV source. As a result, the commutation losses in the Si superjunction MOSFETs are greatly reduced, and continuous hard-commutation in the CCM operation of the totem pole PFC is feasible.

The proposed “pre-charge” solution requires extra parts for each of the CoolMOS™ devices in the half-bridge: a single high-voltage Schottky diode (D1 and D2 in **Figure 2**) and a LV MOSFET (Q3 and Q4 in **Figure 2**). It also requires two supply voltages for driving the half-bridge and the LV MOSFETs (13 V) and for providing the pre-charge or depletion voltage (24 V). The proposed solution implements the level-shifting (bootstrap capacitors) technique with traditional drivers, for both the driver supply and the depletion voltage. These two voltage domains are highlighted in orange (13 V) and blue (24 V) in **Figure 7**.

Furthermore, the included R_x to C_x and R_y to C_y filter networks at the driver inputs allow the proper timing of the PWM (pulse width modulation) signals to the half-bridge devices as well as to the added LV switches; thus, no extra PWM signals from the controller are required.

2.1 Half-bridge hard-commutation transition with the pre-charge circuit

This section presents the operation of a hard-commutated half-bridge with CoolMOS™ and the added pre-charge circuit. The double-pulse test configuration as in **Figure 7** is used for explanation. The main waveforms are presented in **Figure 8**, where the transitions at the different PWM events are not shown to scale for a more adequate display.

In a state prior to t_0, the inductor was energized through Q1, which would implement the switch function in a totem pole PFC. Once Q1 is turned off, the inductor current flows through Q2, first through its body diode and then through the channel of the device, once Q2 is turned on. Therefore Q2, which implements the diode function in a totem pole PFC, is turned on with zero voltage switching (ZVS).

At a given moment in time (t_0 in **Figure 8**), Q2 must be switched off so the current will flow again through Q1 when turned on. After a certain delay time (due to the R_y to C_y network at the input of the gate driver of Q2), the gate-to-source voltage signal of Q2 also changes its state to off at t_1. During the mandatory dead-time in any half-bridge (t_1 to t_2), the inductor current freewheels through the body diode of Q2. Until t_2, the switching node is clamped to the ground and all the bootstrap capacitors, with the exception of C_{HS_P}, for both driving and depletion voltages are charged (**Figure 9.a** and **Figure 9.b**).

Then, after the corresponding dead-time, PWM B is applied, and the C_x to R_x network at the input of the Q4 gate driver generates a pulse of a certain duration. Therefore, the pre-charging MOSFET Q4 is turned on at t_2 (**Figure 9.c**) and a pre-charge current (pre-charge I "diode") circulates in the C_{LS_DP} to Q4 to D2 to Q2 network. The effective circulation of this current depends on the fact that the magnitude of such a pre-charging current must be higher than the freewheeling load current flowing through the body diode of the Si superjunction MOSFET Q2. At the end of the pre-charge current (t_3), the intrinsic body diode of Q2 is deactivated and the drain-to-source voltage ($V_{DS,Q2}$) is pre-charged to 24 V.

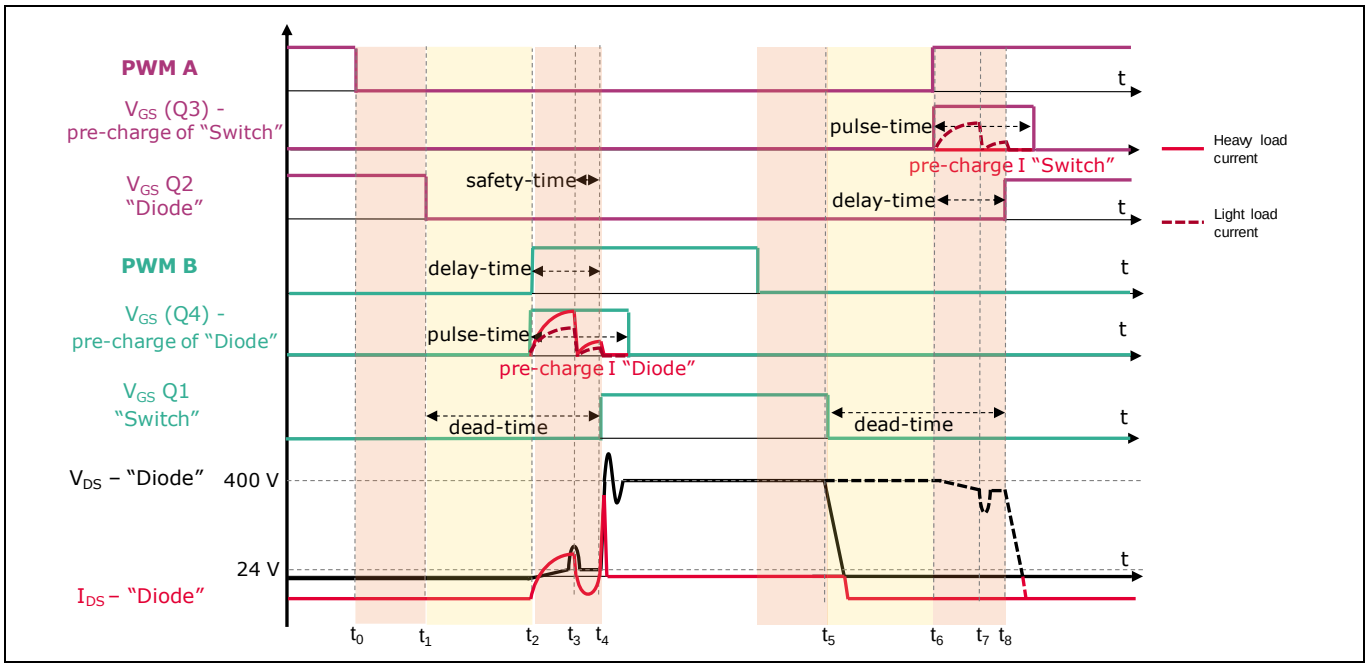


Figure 8 Commutation waveforms of the half-bridge shown in Figure 7

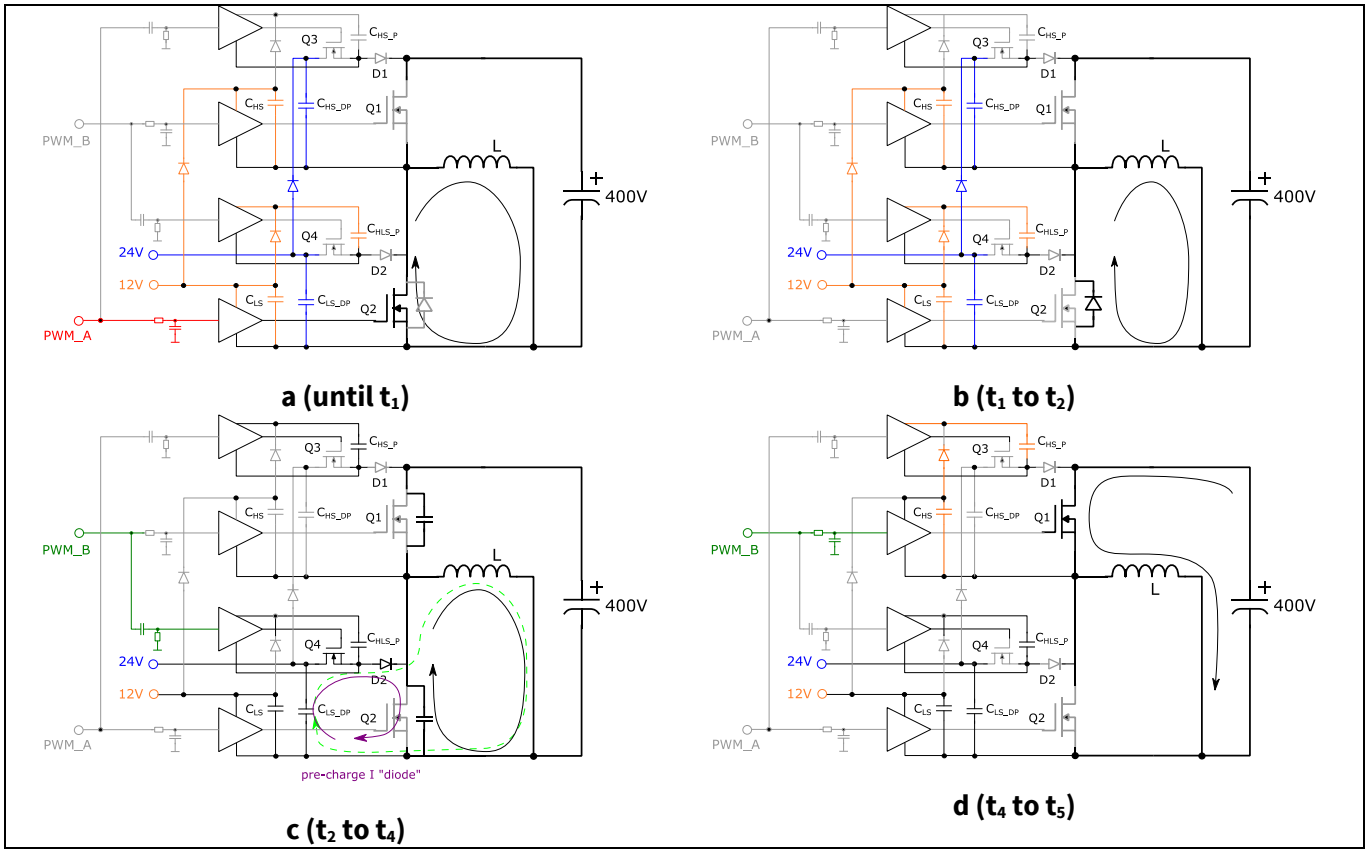


Figure 9 **Hard-commutation transition in a half-bridge operation with CoolMOS™ and the added pre-charge circuit**

As shown in **Figure 8**, the pre-charge current waveform has two peak pulses; the first one, between t_2 and t_3, is related to the charging of the Q2 C_{oss} and the second one, with a lower magnitude between t_3 and t_4, is due to the resonance with the stray inductances of the pre-charge loop.

When the delayed PWM B signal finally reaches the gate of Q1 at t_4, the C_{oss} of Q2 is already depleted with 24 V, which sets the stage for a smooth diode-to-switch transition. As shown in **Figure 9.d**, when Q1 is turned on the bootstrap capacitor for the driving of Q3 (C_{HS_P}) is charged from the bootstrap capacitor of Q1 (C_{HS}).

As can be seen in **Figure 8**, the duration of the pulse applied to the pre-charge MOSFET Q4 goes beyond t_4 when commutation and transient events happen in both Q1 and Q2. This is done intentionally in order to guarantee the proper losses of the Si SJ MOSFET Q1 during turn-on. If this pulse falls short, the possibility of severe hard-commutation is high in the Si superjunction MOSFET, which would produce destructive results if it were to occur during multiple successive events.

When the PWM B signal goes low, similar to before, due to the R_y to C_y network at the input of the gate driver of Q1, there is a certain delay before the device fully turns off at t_5. Due to the load or inductor current, immediately after the channel is completely closed, the C_{oss} of Q1 will be charged to 400 V and the C_{oss} of Q2 will be discharged to 0 V, producing a ZVS transition for Q2. This is the case in the switch-to-diode transition in a PFC application. In this situation, the pre-charge circuit of the high-side switch (C_{HS_DP} to Q3 to D1) will not have any influence on the operation of the half-bridge with Si superjunction MOSFETs.

This ZVS turn-on transition of the diode is possible when the load or inductor current is high enough to enable charge and discharge of the corresponding C_{oss}. However, if the inductor current at this transition is not enough to charge and discharge the C_{oss} of the half-bridge devices, a hard-switching transition will happen. This situation is shown in **Figure 8** as a dotted line after t_6. In this case, the pulse applied to the pre-charge MOSFET

Q3 becomes effective and causes the charge of Q1 C_{OSS} to the depletion voltage by the C_{HS_P} to Q3 to D1 to Q1 network. Once Q2 is turned on, its drain-to-source voltage will drop again close to zero and a smooth switch-to-diode transition is achieved without severe hard-switching.

2.2 Pre-charge circuit design

The circuit shown in **Figure 7** has been simulated for different inductor current levels and the results are shown in **Figure 10**. As it can be seen in **Figure 10**, there are different responses of the V_{DS} of the Si superjunction MOSFET working as a diode (freewheeling the inductor current) in **Figure 7**. Once the C_{OSS} reaches the same voltage as the C_{LS_DP}, then the pre-charge currents stops circulating and abruptly falls to zero. The slope of this falling edge provokes a voltage drop across the stray inductance in the loop, which is reflected as a voltage spike in V_{DS}. Once the V_{DS} falls back toward the depletion voltage, it is possible to start the hard-commutation transition against the other Si superjunction MOSFET in the half-bridge. During the turn-on transition of Q1, the losses associated with the Q_{OSS} and Q_{rr} of Q2 are calculated as in (1).

$$P = \frac{1}{2} \cdot \left(Q_{oss\_Q2@24V} + Q_{rr\_Q2\_BD@24V}\right) \cdot V_{depletion} \cdot f_{sw} \tag{1}$$

For a given CoolMOS™ to be used in the half-bridge (Q1 and Q2), there is a charge that needs to be removed from its body diode and output capacitance. This is the red triangle area in **Figure 10**, when there is a very low freewheeling current in the inductor, or the blue area when the freewheeling current is 20 A. Therefore, the maximum current in the pre-charge circuit can be approximated as (2), where I_{FW_max} is the maximum inductor current to be commutated, Q_{rr} is the device reverse-recovery charge stated in the datasheet [7], and n is the number of devices in parallel per position in the half-bridge.

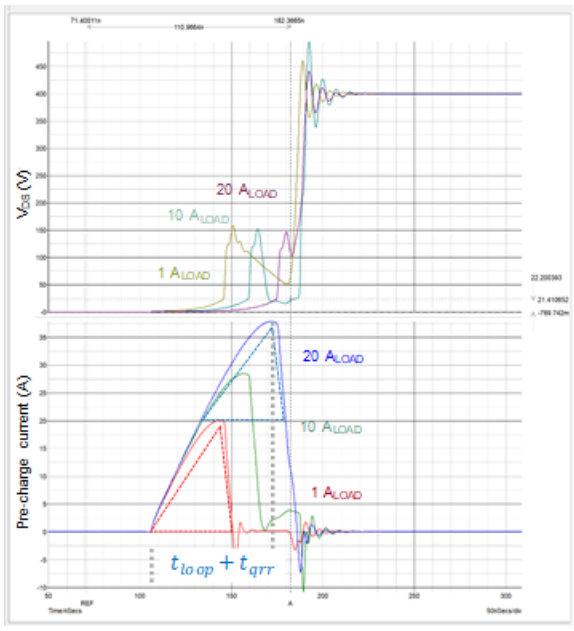


Figure 10 Simulated drain-source voltage of Q2 (top) and pre-charge current (bottom) for different freewheeling currents

$$I_{PreCharge\_pk} \approx I_{FW\_max} + \frac{\mathrm{n} \cdot \mathrm{Q}_{rr}}{t_{qrr}} \tag{2}$$

The time t_{qrr} is the part of the conduction time of the pre-charge circuit due to the removal of the reverse-recovery charge and it is calculated as in (3), where L_{PCloop} is the stray inductance of the pre-charge loop and V_{DP} is the provided depletion voltage (24 V as introduced in the previous section). This voltage can be modified according to the C_{OSS} variation of the SJ MOSFET (**Figure 6**).

$$t_{qrr} = \sqrt{\frac{L_{PCloop} \cdot \mathrm{n} \cdot \mathrm{Q}_{rr}}{V_{DP}}} \tag{3}$$

A second component of the conduction time of the pre-charging circuit is t_{loop}. This is related to the required time to reach the freewheeling current due to the stray inductance of the pre-charge loop, and the longest time in the application happens at the maximum current to be commutated by the half-bridge (4).

$$t_{loop} = \frac{L_{PCloop} \cdot \mathrm{I}_{FW\_max}}{V_{DP}} \tag{4}$$

The total conduction time ($t_{PreCharge}$) is the addition of the times calculated in (3) and (4). This time is required to calculate the filter to be applied to the half-bridge switches: C_y and R_y. For a selected capacitance C_y, the resistor R_y can be calculated as shown in (5), where $V_{on\_th\_driver\_in}$ and $V_{cc\_driver\_in}$ are the on-threshold and the supply voltages of the input section of the driver, respectively.

$$R_y = \frac{1.35 \cdot \mathrm{t}_{PreCharge}}{C_y \cdot ln\left(\frac{1}{1 - \frac{V_{on\_th\_driver\_in}}{V_{cc\_driver\_in}}}\right)} \tag{5}$$

Once the R_y and C_y values have been calculated, the actual delay of the half-bridge pulses can be calculated by considering the delay introduced to the input of the driver (R_y to C_y network) and the turn-on delay motivated by the $R_{g(on)}$ to C_{ISS} of the CoolMOS™ mounted in the totem pole (6). Both the internal R_g of the device (if applicable) and the external one have to be considered in the calculation, as well as the plateau voltage of the CoolMOS™ implemented in the totem pole.

$$t_{delay} = \left(R_{g_{ext}} + R_{g_{int}}\right) \cdot C_{iss} \cdot ln\left(\frac{1}{1 - \frac{V_{plateau}}{V_{cc_{driver_{in}}}}}\right) + R_y \cdot C_y \cdot ln\left(\frac{1}{1 - \frac{V_{on\_th\_driver\_in}}{V_{cc\_driver\_in}}}\right) \tag{6}$$

With this delay, the high-pass filter to generate the pulse which activates the pre-charging loop can be calculated. As already mentioned, the duration of this pulse should be longer than the calculated delay for proper operation of the pre-charge circuit, which avoids hard-commutation of the half-bridge CoolMOS™ MOSFETs. With these considerations, R_x is calculated as in (7) by selecting first a capacitance C_x and introducing the supply voltage and the off-threshold ($V_{off\_th\_driver\_in}$) of the input section of the driver.

$$R_x = \frac{2 \cdot \mathrm{t}_{delay}}{C_x \cdot ln\left(\frac{V_{cc\_driver\_in}}{V_{off\_th\_driver\_in}}\right)} \tag{7}$$

The SiC Schottky diode of the pre-charge loop (D1/D2 in **Figure 7**) is selected to cope with the maximum current in the loop (2) at a given temperature, which is usually 100°C or 150°C as maximum junction temperature from the datasheet.

The selection of the LV MOSFET in the pre-charge circuit must consider the charge balance between its output capacitance and the one of the Schottky diode in series in order to avoid avalanche issues when both devices go into the blocking state. In practical terms, the output capacitance of the LV MOSFET must be considerably higher than the capacitance of the Schottky diode. A clamping diode can be used as well, with an anode in the source of the CoolMOS™ CFD7 of the half-bridge and the cathode in the source of its corresponding LV MOSFET. This clamping diode avoids the possibility of the LV MOSFET falling into avalanche.

2.2.1 Design tool for the pre-charge circuit

The design procedure presented above has been implemented in a calculation tool to automate the design for different $R_{DS(on)}$ values of the CoolMOS™ CFD7 series. A capture of the tool, which is embedded at the end of this section, is shown in **Figure 11**. On the left side, the green cells are the inputs for the design procedure and include parameters of the pre-charge loop as the depletion voltage and the loop inductance, as well as the maximum current to be commutated and the number of parallel CFD7 devices in the totem pole. Other inputs are related to the driver voltages and supply, and the external R_g used as well as the capacitance to be used in the R_x to C_x and R_y to C_y filters.

Regarding the outputs of the design tool, the total Q_{rr} involved in the hard-commutation as well as the required pre-charge time and the pre-charge peak current are shown for different $R_{DS(on)}$ devices of CoolMOS™ CFD7 in TOLL package, from 35 mΩ up to 145 mΩ. With the time and current, the R_x and R_y values are calculated as well as the required diode to be used when 100°C or 150°C are considered as maximum junction temperatures.

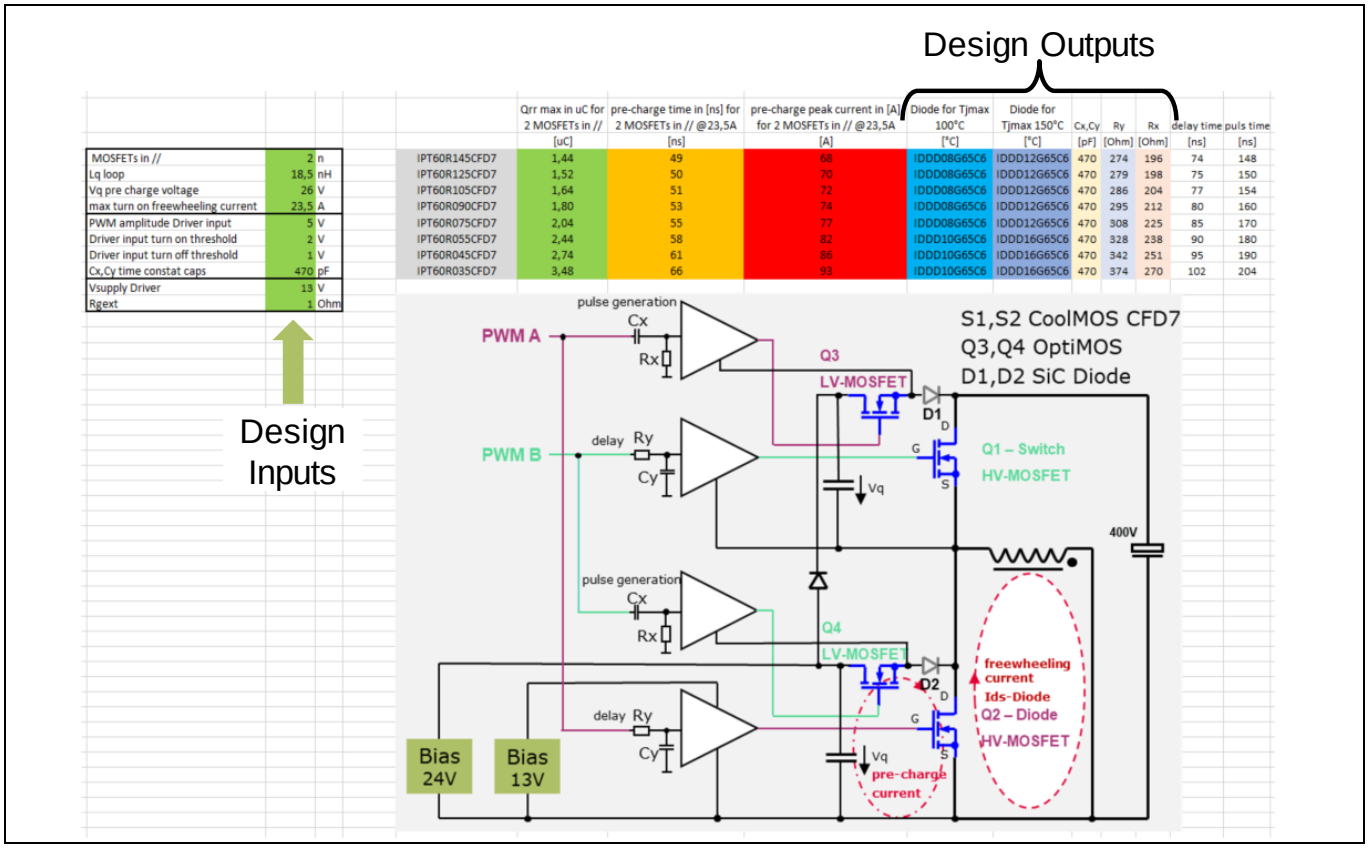


Figure 11 Capture of the design tool for implementing CoolMOS™ CFD7 in CCM totem pole PFC according to the design procedure presented in this section

Table 1 shows the estimated timing and current for a half-bridge design using two 90 mΩ 600 V CoolMOS™ CFD7 in parallel per position in the half-bridge, as well as the design of the RC filter values and the chosen semiconductors according to the presented design procedure implemented in the design tool.

Table 1 Pre-charge loop parameters when two IPT60R090CFD7 CoolMOS™ are used in parallel in the half-bridge

Parameter	Value
L_{loop}	18.5 nH
$V_{CC}/V_{on}/V_{off}$ driver input	5 V/2 V/1 V
Q_{rr}	0.9 µC
T_{qrr}	36 ns
T_{loop}	17 ns
$I_{preCharge\_pk}$	74 A
Diode at 100°C	IDDD08G65C6
Diode at 150°C	IDDD12G65C6
LV MOSFET	BSZ440N10NS3
R_x/R_y ($C_x = C_y = 470$ pF)	187 Ω/294 Ω

Note: The design tool presented in this section can be downloaded in the product registration page (www.infineon.com/productregistration) using the serial number of your evaluation board.

2.3 Schematic implementation of the CCM totem pole with CoolMOS™ CFD7

This section will present the actual implementation, at a schematic level, of the previously presented solution. The totem pole with Si superjunction MOSFET and the required pre-charge circuit is shown in **Figure 12**. Apart from the low-frequency CoolMOS™ S7 (highlighted in black) and the totem pole with paralleled CoolMOS™ CFD7 (marked in red), the pre-charge circuit is shown inside the orange frame together with the bootstrap implementation for the depletion voltage of the high-side CoolMOS™ CFD7.

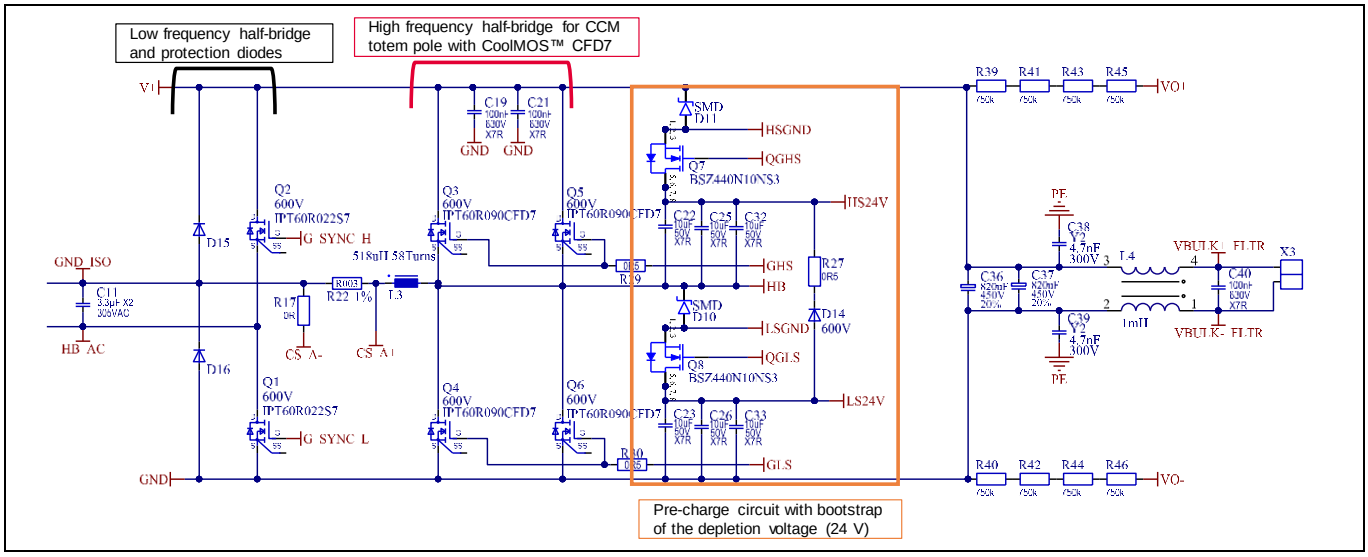


Figure 12 **Schematic of the totem pole implementation with CoolMOS™ CFD7 and the pre-charge circuit**

The driving scheme applied to the previously introduced totem pole with pre-charge circuit is shown in **Figure 13**. Two dual-channel isolated drivers from Infineon (2EDF7275F) are used. The RC and CR networks for pulse generation are inside the orange frame, and the bootstrap implementation for both HV and LV MOSFETs can be found in the green box.

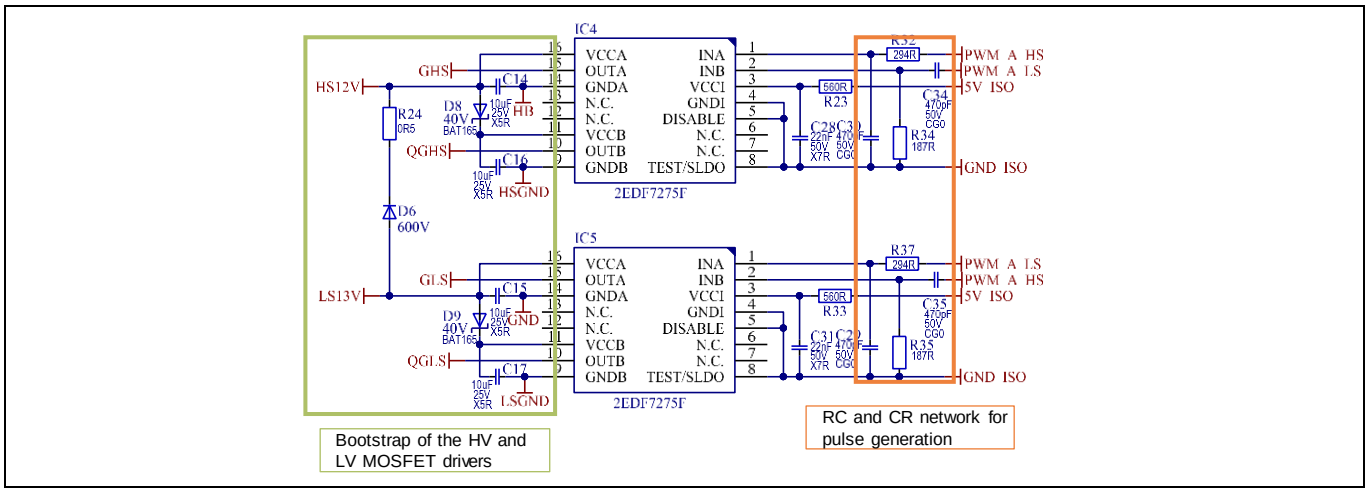


Figure 13 **Schematic of the drivers for the high-frequency half-bridge and the pre-charging circuit**

The low-frequency half-bridge is also driven using the 2EDF7275F dual-channel isolated driver with bootstrap, as shown in the bottom part of **Figure 14**. The same figure presents a charge pump implemented with the driver 1EDN8511B from Infineon. This charge pump is used as a voltage doubler and enables generation of the depletion voltage (24 V domain in the previous explanation) directly from the 13 V (driving voltage) provided by the bias board.

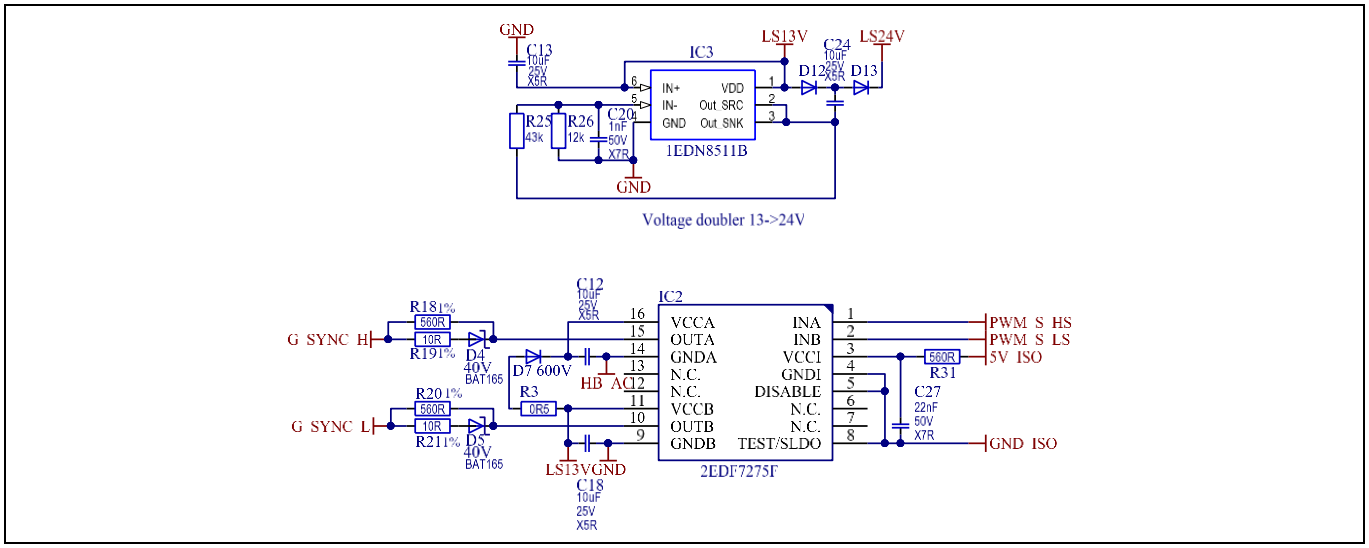


Figure 14 Schematic of the low-frequency half-bridge driver (bottom) and voltage doubler to generate the depletion voltage (top)

The only part left of the EVAL_3K3W_TP_PFC_CC board schematic is the input filter. **Figure 15** introduces the EMI filter schematic with the input current fuse and the inrush current limitation (NTC and relay). The AC voltage is sensed before the NTC. Another NTC for temperature sensing (SMD) is included as well as the input connector, the screws to connect to the chassis, and the bias board connector and decoupling capacitor for the fan supply.

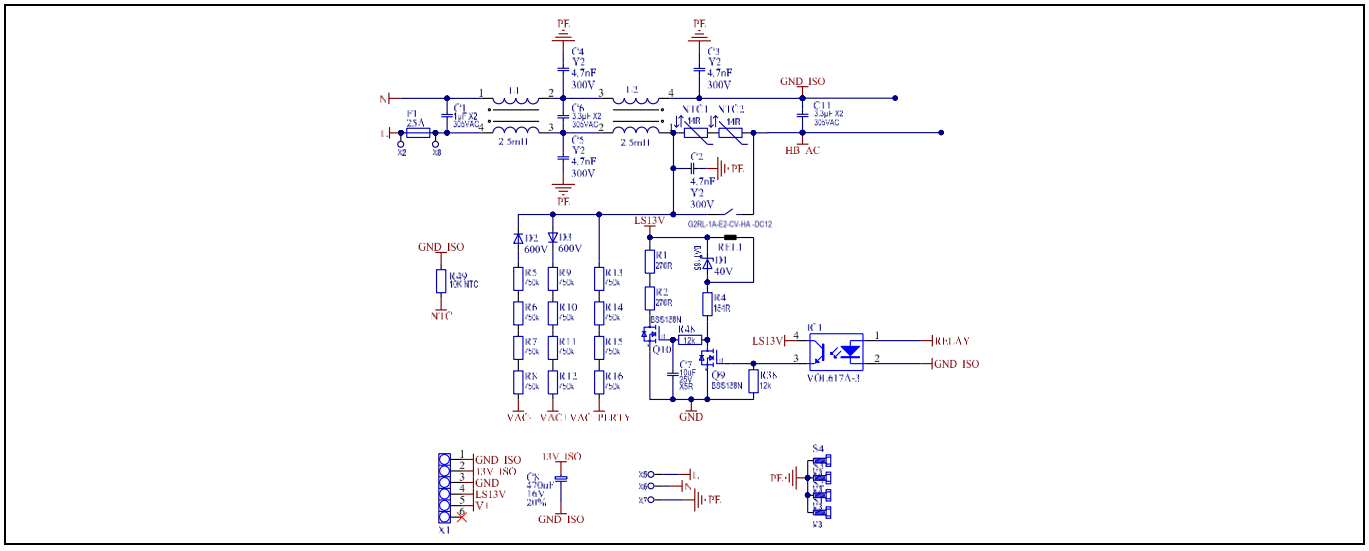


Figure 15 Schematic of the EMI filter, fuse, NTC and relay together with AC and polarity sensing

2.4 Control implementation

The evaluation board EVAL_3K3W_TP_PFC_CC implements CCM average current mode control with duty feed-forward (DFF). For the digital implementation of a CCM average current mode control, the inductor current, the AC input voltage and the DC output voltage are required. **Figure 16** shows a simplified block diagram of the totem pole topology with the required sensing. In addition, the pre-charge block has been added. It can be noted that due to the RC and CR filters, it is not required to provide more control signals than the ones for the half-bridge operation of the totem pole PFC. Furthermore, due to the bootstrap concept, shown in the figure by

the orange and blue diodes connecting the pre-charge and driver blocks, only 13 V and 24 V referenced to the low-side source are required.

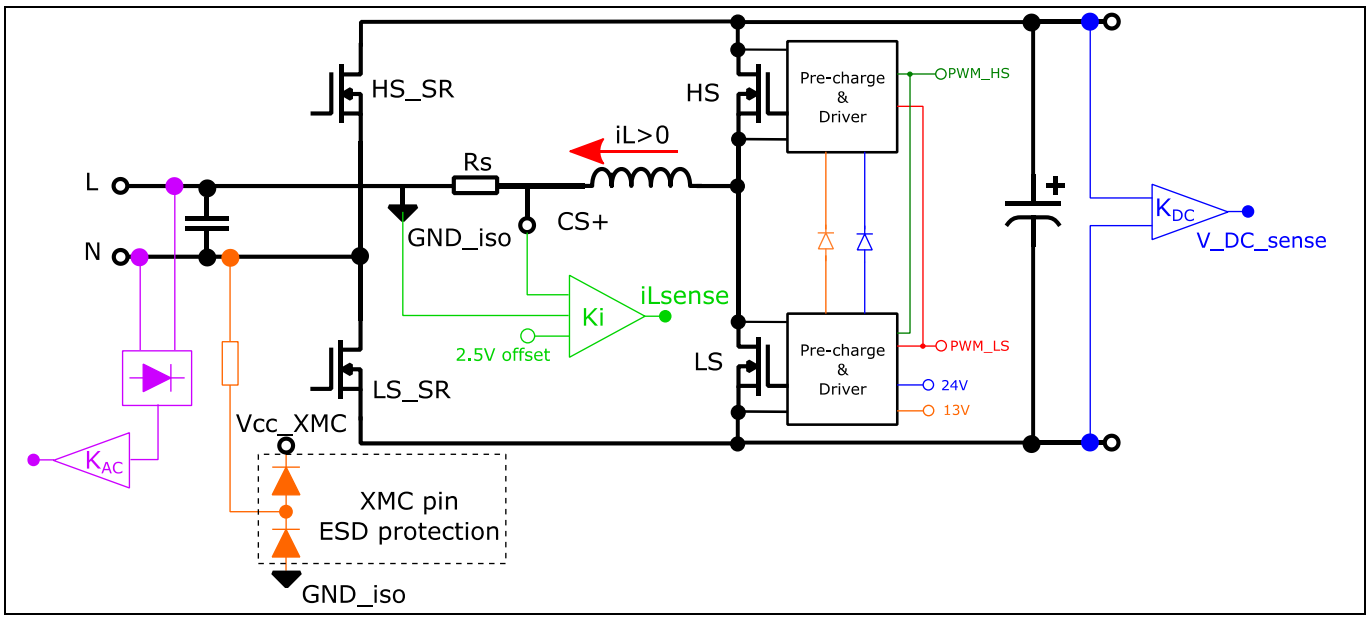


Figure 16 Block diagram of the sensing circuitry required for totem pole control with XMC™ and control reference in the AC rail in series with the PFC choke

2.4.1 Signal conditioning for digital control of totem pole CCM PFC

Unlike the classic PFC in which the AC voltage is rectified by the diode bridge, in the bridgeless totem pole PFC the inductor current is both positive and negative. The most simple and cost effective way to sense this current is to use a shunt resistor in series with the inductor, as shown in **Figure 16**. In addition, in the EVAL_3K3W_TP_PFC_CC board, the control reference (GND_iso in **Figure 16**) is placed in the AC-line after the shunt resistor. Therefore, the current sense voltage (CS+) is positive and negative according to the positive reference current shown by the red arrow of **Figure 16**.

Since the ADC of the microcontroller used for the control implementation (XMC1402 from Infineon Technologies [2]) only allows input voltages between zero and the supply voltage (Vcc_XMC in **Figure 16**), an offset is included together with the current sense gain in order to properly use the input span of the ADC. In this case the offset is 2.5 V, which corresponds to half of the supply voltage for the XMC™ controller used. The differential gain (K_i) is adjusted to consider not only inductor average current but also the switching frequency ripple, since this signal is used for CCM average current control and peak current limitation (PCL).

In the totem pole operation the return path transistors (HS_SR and LS_SR on **Figure 16**) are switched at the AC zero crossing according to the AC polarity: HS_SR for positive AC and LS_SR for negative AC cycle. The polarity of the input voltage is set according to the control reference GND_iso. Since the control reference is in one of the AC input rails, the polarity detection is significantly simplified and the internal ESD (electrostatic discharge) diode protection of the XMC™ controller is used to transform the input capacitor voltage into a digital signal.

Due to the control reference location, the bulk voltage sense requires a differential amplifier with gain K_{DC}, as shown in **Figure 16**. In the case of the of AC voltage sense, the control reference location allows a simple sense. In this case, the voltage has been rectified (positive ADC input is required) and adapted to the ADC input range with a differential gain K_{AC}.

Since the AC voltage is used for the current reference generation in the selected average current mode structure (**Figure 17**), the current reference is a full-wave rectified sinusoidal sequence. However, the current

sense after the ADC is a sinusoidal sequence with offset at half of the ADC span. Therefore, the ADC result from the current sense requires modification. First the offset is removed and the resulting value is rectified according to the AC polarity signal. These two steps, together with extra gain, are implemented by software in the XMC™ controller.

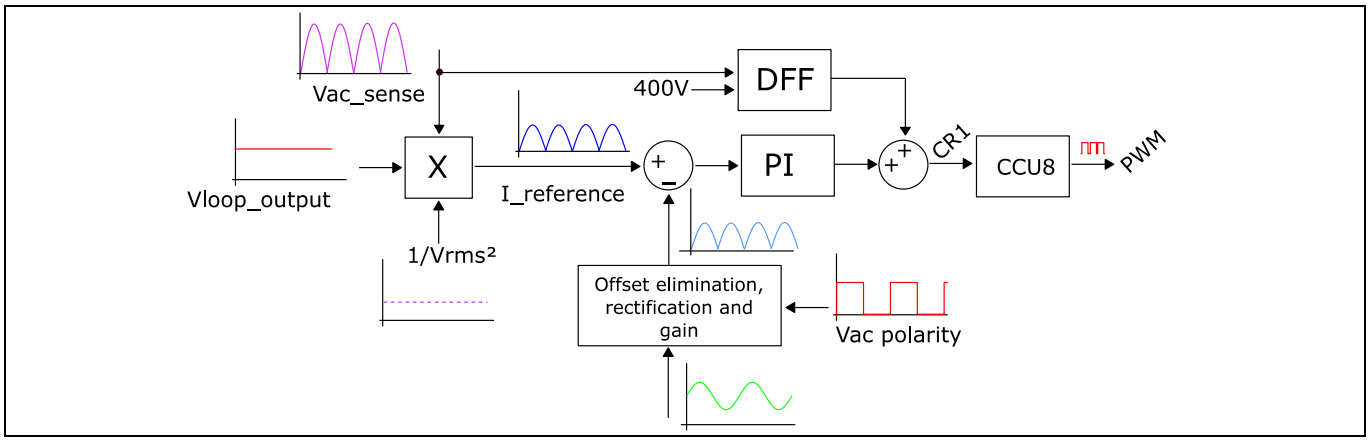


Figure 17 Current loop structure with DFF and the required current manipulation

2.4.2 PWM sequence for bootstrapping

Due to the bootstrap concept implemented, it is important to properly start the PFC PWM at start-up or after a long time without operation, i.e., after a fault has stopped the PWM. This is important not only for the high-frequency half-bridge, in which a proper PWM sequence guarantees the bootstrap to be charged, and thus the proper operation of the pre-charge circuit. It is also important for the low-frequency half-bridge, in which bootstrap capacitors are dimensioned to comply with 20 ms hold-up time (at 50 percent of the load).

Due to the selected control ground, in the AC-line with the shunt resistor, the low-side low-frequency switch (LS_SR in **Figure 16**) is enabled when the potential in node “N” is higher than the one in node “L”. Therefore, at start-up or after a long time with no PFC operation, LS_SR must be switched on first. Then the bootstrap for HS_SR can be charged and the high-side low-frequency transistor can be switched on when the AC polarity changes. The implemented SW considers this circumstance, as shown in **Figure 18**, where the PFC resumes operation after a fault. As can be seen, the PFC resumes operation with soft-start (as in start-up) at the AC zero crossing with the mentioned polarity, because the AC voltage probe has node “N” as reference.

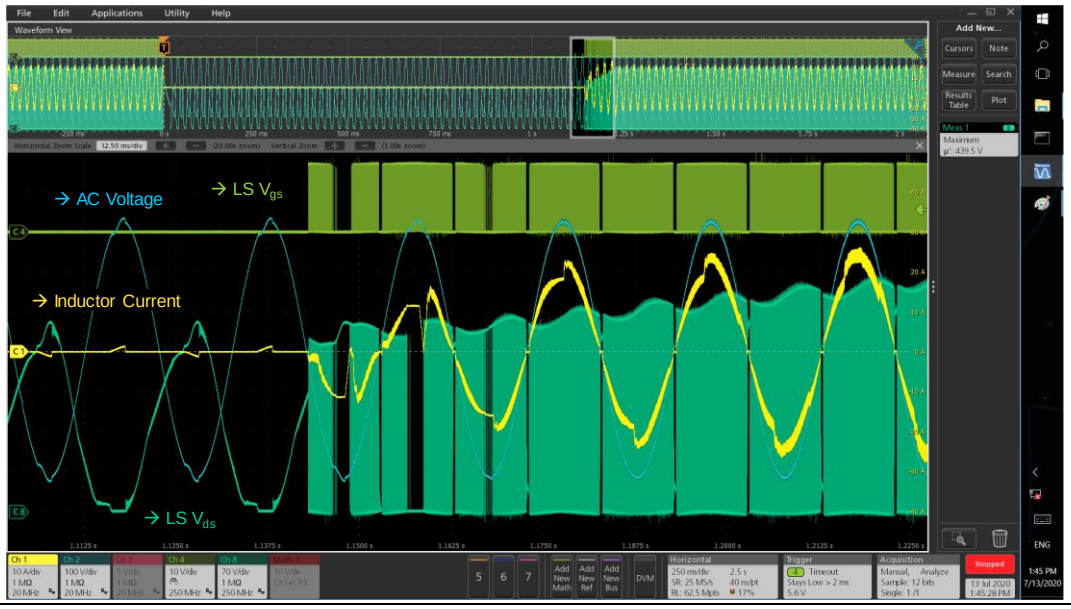


Figure 18 Resume operation after a fault is detected with the low-side low-frequency switch

As mentioned above, the bootstrap of the low-frequency half-bridge is designed for a 20 ms hold-up time at half-load. This allows the totem pole to resume operation after that time if the high-side switch in the low-frequency half-bridge needs to be switched on, as shown in **Figure 19**. This capture also shows how the low-side switch in the high-frequency half-bridge is switched on first in the sequence, even if it is acting as the boost diode for such polarity of the AC voltage. This guarantees that the different bootstrap capacitors will be charged and the concept presented in the previous sections would perform as expected.

The low-side switch in the half-bridge is therefore switched on first for every circumstance in which the PWM has been previously stopped (start-up, AC zero crossing, AC lost or after a fault is detected) and it complements the previously presented strategy for the low-frequency half-bridge.

Figure 19 Low-side in the boost half-bridge is switched on first after the PWM is stopped

3 Bridgeless PFC specification and test results

This chapter shows the specifications, performance and behavior of the 3300 W bridgeless totem pole CCM PFC evaluation board implementing the 600 V CoolMOS™ CFD7 presented in this application note. The evaluation board EVAL_3K3W_TP_PFC_CC design follows the pre-charge circuit design procedure described in section 2.2. Table 1 presents the pre-charge circuit design when two IPT60R090CFD7 CoolMOS™ are used in parallel at thePFC totem pole. Table 2 shows the evaluation board performance and specifications under several steady-state and dynamic conditions. The converter operates at 65 kHz switching frequency and only for high-line AC input (176 V minimum RMS voltage).

Table 2 Summary of specifications and test conditions for the 3300 W totem pole in CCM with CoolMOS™ CFD7

Test		Conditions	Specification	
Efficiency test		230 Vrms, 50 Hz/60 Hz	η_{pk} ≈ 99% at 1650 W (50% load)	
Current THD		230 Vrms, 50 Hz/60 Hz	THDi less than 10% from 10% load	
Power factor		230 Vrms, 50 Hz/60 Hz	PF more than 0.95 from 20% load	
Rated DC voltage			400 V	
Steady-state V_{out} ripple		230 Vrms, 50 Hz/60 Hz, 100% load	$\lvert\Delta V_{out}\rvert$ less than 20 $V_{pk\text{-}pk}$	
Inrush current		230 Vrms, 50 Hz/60 Hz, measured on the first AC cycle	I_{in_peak} less than 30 A	
Power line disturbance	AC lost (hold-up time)	230 Vrms, 50 Hz, 10 ms at 100% load, 20 ms at 50% load	V_{out_min} = 300 V (UVP)	No damage: * PFC soft-start if bulk voltage under 300 V * PFC soft-start if AC out of range for certain time
	Voltage sag	200 Vrms, 50 Hz/60 Hz, different sag conditions, 100% load		
Brown-out	AC voltage		174 V on; 168 V off	
Load transient		8.2 A (100%) ↔ 0 A (0%), 0.2 A/µs	V_{out_min} = 300 V (UVP) V_{out_max} = 450 V (OVP)	
Overcurrent protection (OCP)			Peak current limit 40 A	
			AVG current limit 28 A	

3.1 Steady-state performance

Figure 20 shows the efficiency measurements for PFC operation at different AC voltages. The efficiency measurements have been obtained with a WT3000 power analyzer and include the bias consumption as well as the fan, which is supplied through the 6 W bias converter.

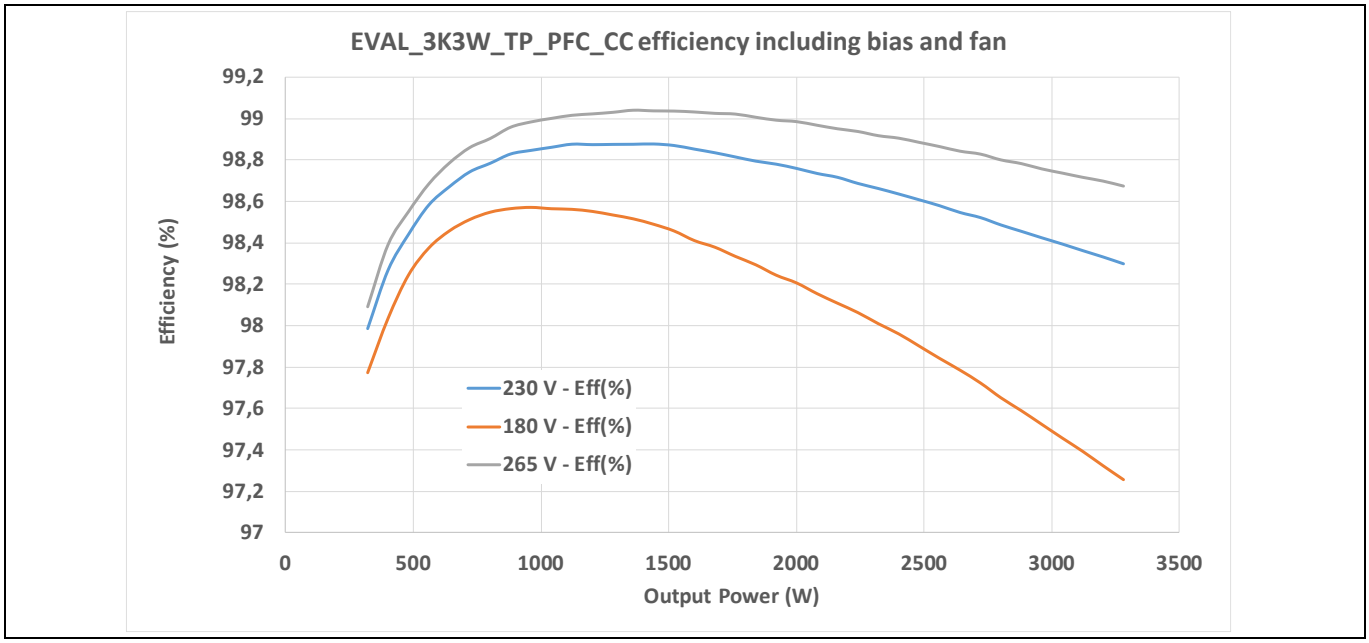


Figure 20 Measured efficiency at different RMS voltages. The measurements include bias and fan consumption.

Figure 21 depicts the total harmonic distortion (THD) and power factor measured at different AC voltages at 50 Hz. Only 50 Hz results are shown because the high-line AC voltage typically operates at such a frequency. However, the EVAL_3K3W_TP_PFC_CC board is prepared to operate at 60 Hz, and similar results can be expected.

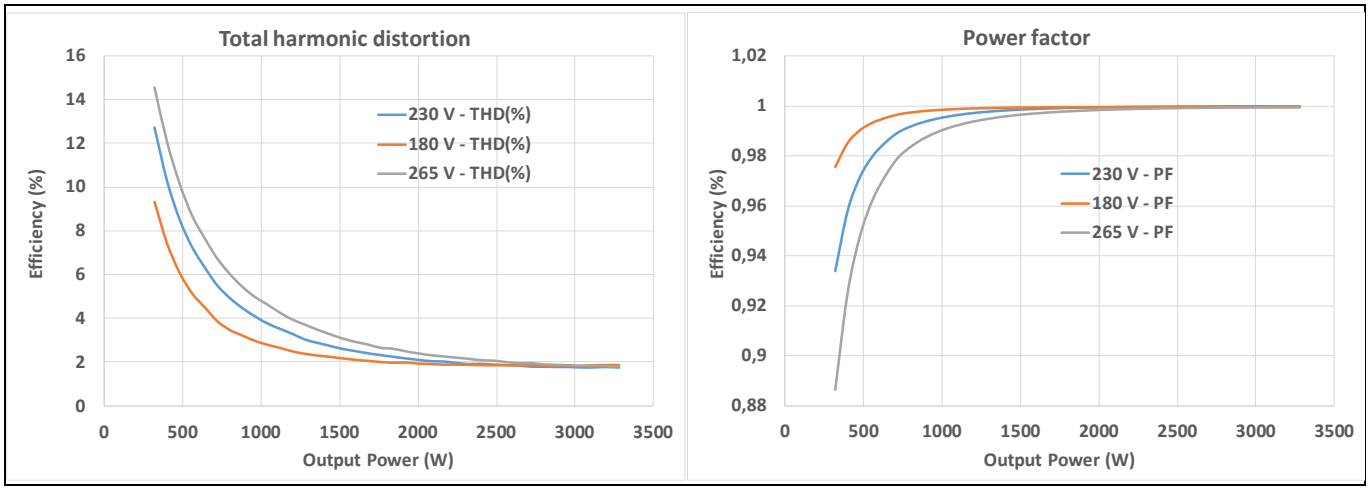


Figure 21 Measured THD (left) and power factor (right) at different RMS voltages for 50 Hz high-line AC voltage

3.2 Totem pole commutation with CoolMOS™ and the pre-charge circuit

The steady-state operation of the main totem pole PFC with 600 V CoolMOS™ CF7 is shown in **Figure 22**, which also includes the main pre-charging waveforms. As can be seen, there are neither overshoots in the LV switch for the pre-charge, nor in the CoolMOS™ CFD7 implemented in the totem pole PFC half-bridge. The pre-charging voltage, with its bootstrap concept, remains almost constant and allows the implementation shown in this document. It must be noted that the pre-charge current appears only in that AC cycle in which the

corresponding half-bridge switch is acting as boost diode, and it has no impact on the switching for the opposite AC cycle in which the MOSFET implements the boost switch function. The same waveforms are shown in **Figure 23** for one switching cycle at the peak of the AC voltage.

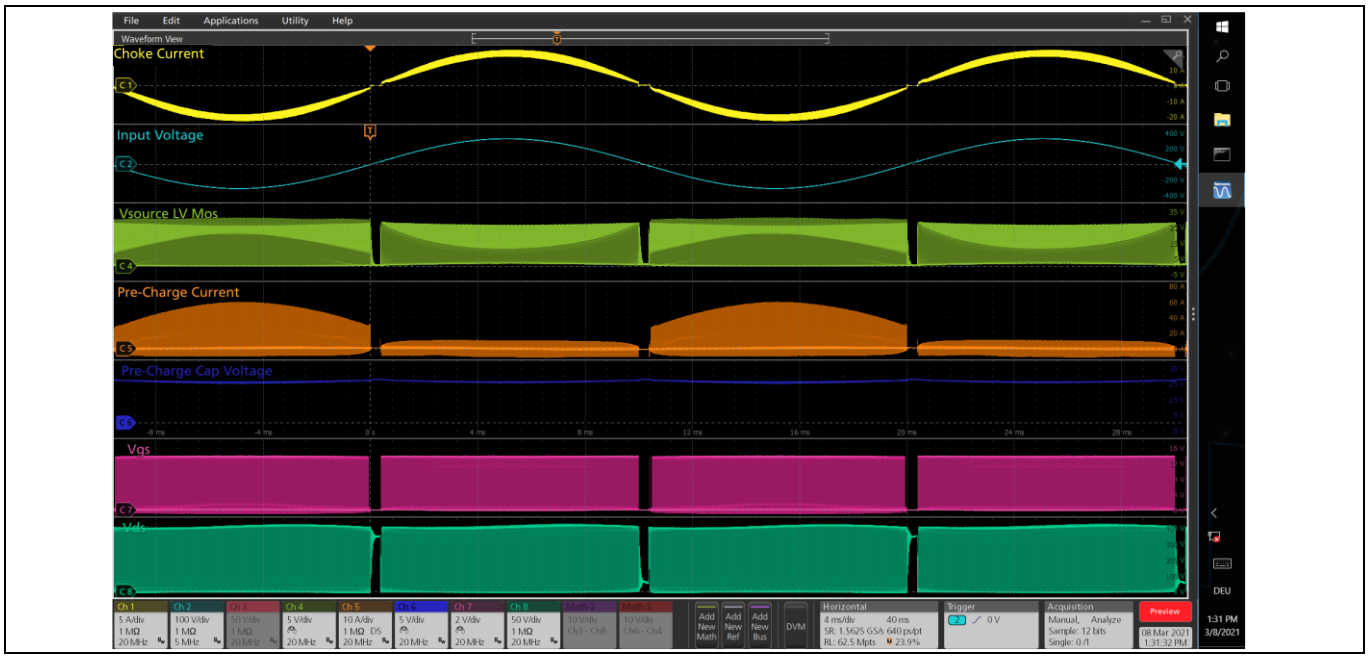


Figure 22 Steady-state waveforms, including pre-charging, for EVAL_3K3W_TP_PFC_CC at 230 V/50 Hz AC voltage and full load

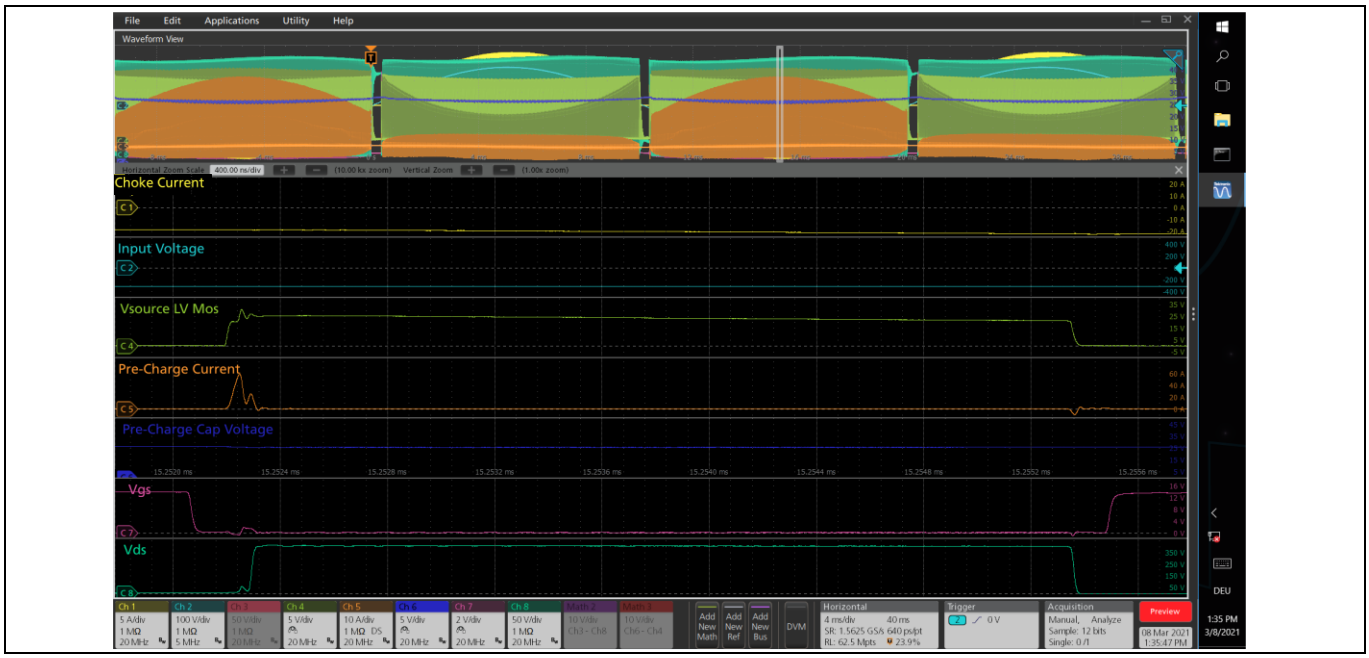


Figure 23 Switching cycle detail of the steady-state waveforms, including the pre-charging, for EVAL_3K3W_TP_PFC_CC at 230 V/50 Hz AC voltage and full load

The drain-source voltage is shown in **Figure 24** and **Figure 25** for 0 A and 23 A inductor current respectively. The waveforms are captured during PFC steady-state operation at nominal AC voltage and full load, and also include the necessary pre-charge current from the LV AC source in order to deplete the 600 V CoolMOS™ CFD7 in the totem pole half-bridge. The waveforms shown are in good agreement with the simulation presented in

section 2.2, and it is clear that there is no overshoot in the V_{ds} motivated by hard-commutation due to the pre-charge circuit implemented, which enables hard-commutation operation of CoolMOS™ at switching frequency.

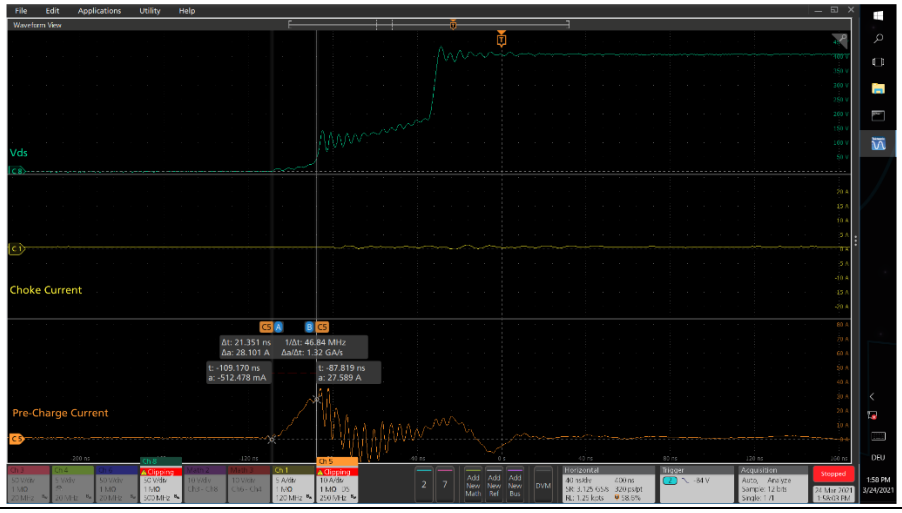


Figure 24 Pre-charge current and drain-source voltage of the CoolMOS™ CFD7 operating as a diode during totem pole operation and 0 A choke current

Figure 25 Pre-charge current and drain-source voltage of the CoolMOS™ CFD7 operating as a diode during totem pole operation and 23 A inductor current

3.3 Power line disturbance

Two main line disturbance conditions can occur when connected to the grid. On one side the AC can be lost during a certain time – line cycle drop-out (LCDO) – and, on the other side, the AC voltage can suddenly decrease to an abnormal value – voltage sag. This section introduces the test conditions for both disturbances as well as the EVAL_3K3W_TP_PFC_CC bridgeless evaluation board performance when those conditions are applied.

3.3.1 Line cycle drop-out

The 3300 W totem pole CCM PFC with 600 V CoolMOS™ CFD7 operates exclusively in high-line. Therefore, the AC LCDO capability is tested from 230 V to 0 V. Different timing, related to the specified hold-up time and the line frequency, is applied as shown in Table 3. The output voltage is within the specified dynamic variation regardless of the start angle of the voltage drop-out. **Figure 26** shows an example of LCDO operation at full load starting at an AC angle of 45 degrees, which corresponds to the point of lowest DC voltage in steady-state conditions. In case the drop-out is longer than specified, output undervoltage (300 V) can be triggered and a turn-off and restart of the unit will occur.

Note: The electronic load used during the test is configured in such a way that it demands current only when the voltage applied to the load is over 300 V, which is the undervoltage setting of the bridgeless PFC and emulates the typical behavior of a back-end DC-DC converter.

Table 3 Applied voltage cycles for LCDO test at different loads with 50 Hz AC input voltage

		First to tenth time	
Applied voltage	230 V AC	0 V AC	230 V AC
Timing at different load conditions	50% load	20 ms	100 ms
	100% load	10 ms	100 ms

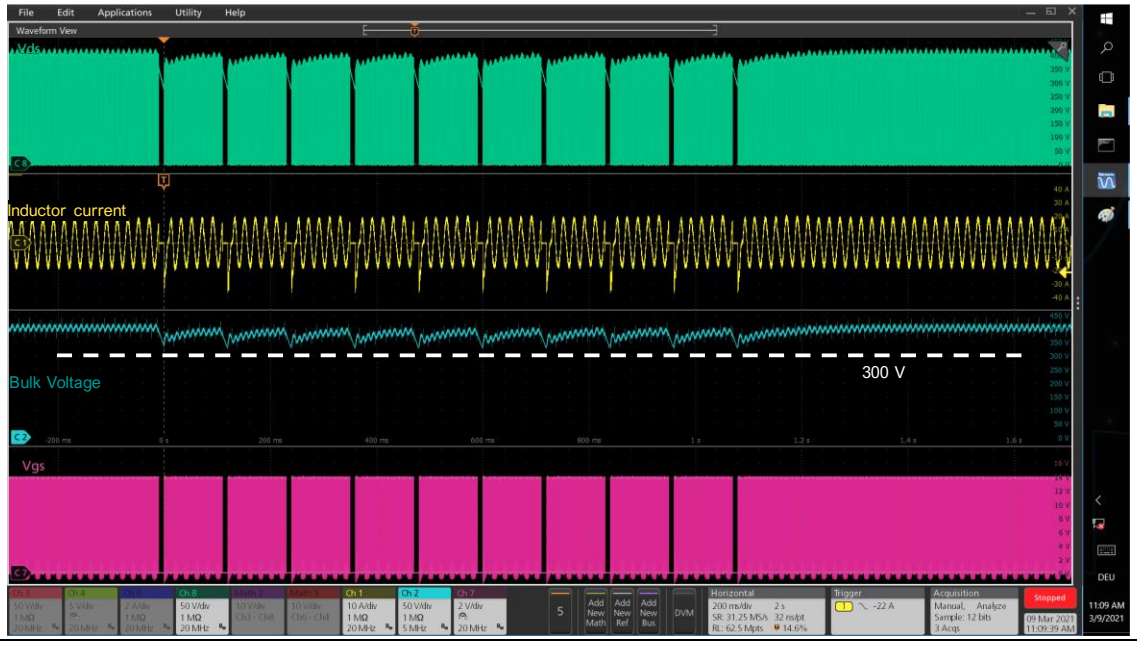


Figure 26 10 ms LCDO test at 230 V AC/50 Hz, and 100 percent load with a starting angle of 45 degrees

More detailed waveforms of a full-load 10 ms LCDO are presented in **Figure 27**. It shows the PCL when the AC returns, set to 40 A, as well as the initial and final bulk voltages during the hold-up time. This high current is demanded by the voltage loop in order to quickly increase the bulk voltage to its target value.

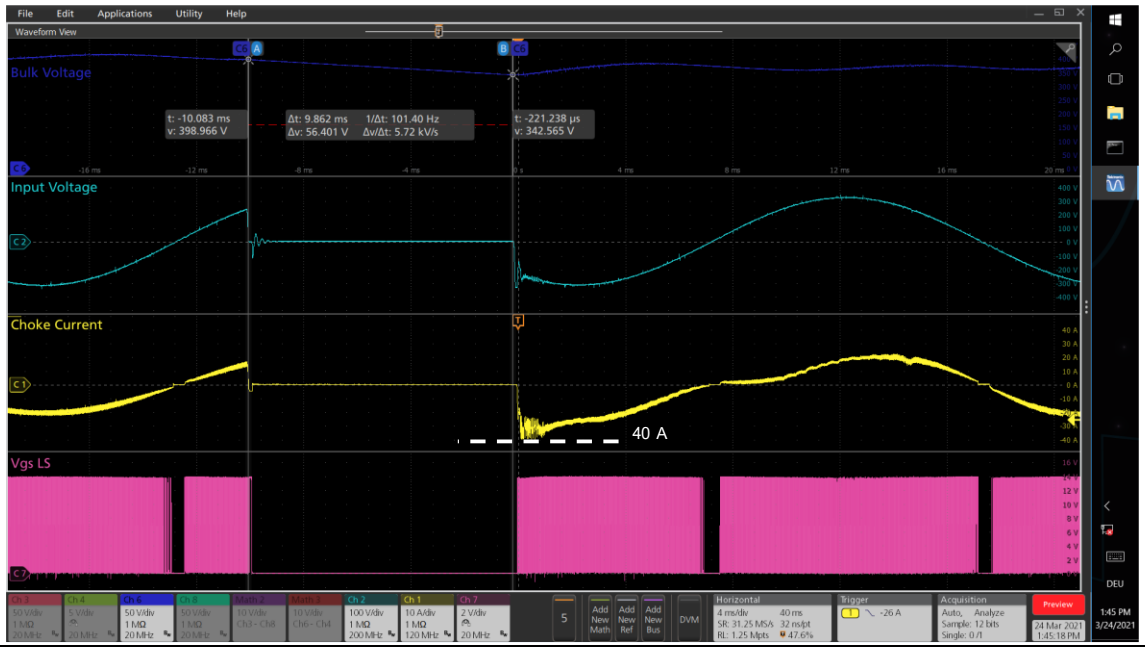


Figure 27 Detail of a 10 ms LCDO test at 230 V/50 Hz and full-load with a starting angle of 45 degrees

3.3.2 Voltage sag

For high-line, two different voltage sag conditions are considered and tested, as shown in Table 4.

Table 4 Voltage sag conditions for high-line applied to the EVAL_3K3W_TP_PFC_CC board

		First to tenth time	
	Steady AC input	Voltage sag (time)	Period
AC input	200 V AC	130 V AC (0.5 s)	5 s
	200 V AC	150 V AC (2 s)	20 s

The EVAL_3K3W_TP_PFC_CC board includes not only PCL, which in this case is motivated by a sudden change in the AC voltage, but also average current limitation. This effect can be clearly seen in the voltage sag test shown in **Figure 28**, which shows the totem pole PFC behavior with 130 V voltage sag during 500 ms. Since the input current (inductor average current) is limited to 28 A, the output voltage cannot be regulated to 400 V during the voltage sag. If the voltage is under the nominal range for longer than specified in the previous table, the PFC turns off and restarts with soft-start after an idle time.

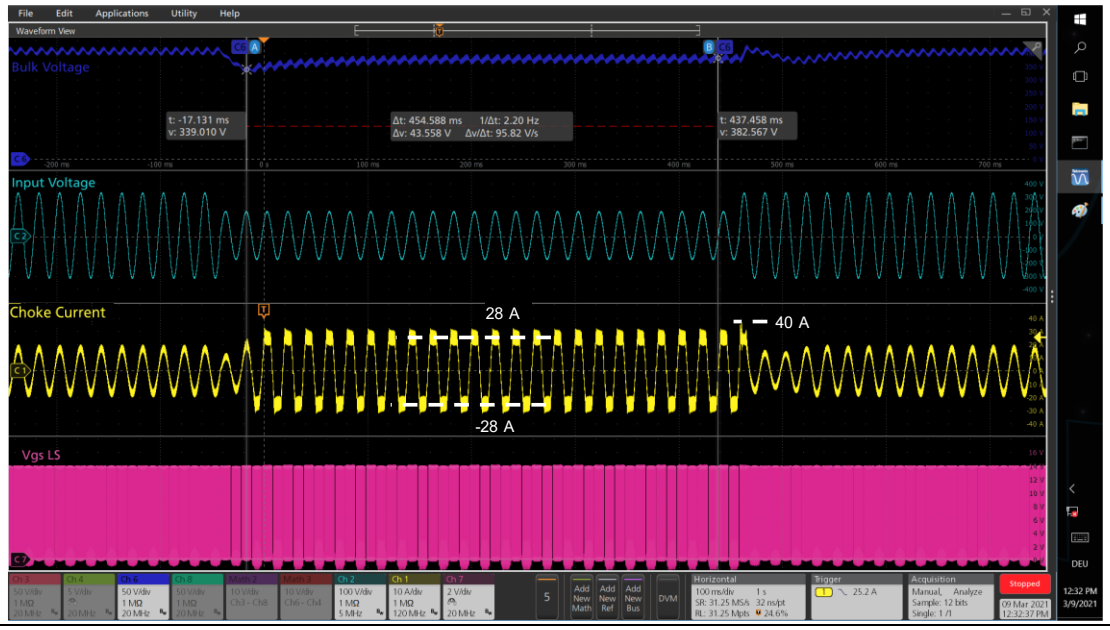


Figure 28 Main waveforms during a 500 ms and 130 Vrms voltage sag at full load

3.4 Output voltage dynamic behavior

In addition to power line disturbance, two other dynamic perturbances can affect the performance of the bridgeless totem pole PFC: load steps and input voltage variation.

3.4.1 Load-transient response

As specified in Table 2, no-load (0 A) to full-load (8.2 A) steps (and vice-versa) with 0.2 A/µs slope are considered for the PFC load variation. **Figure 29** shows the EVAL_3K3W_TP_PFC_CC board behavior under these conditions, at nominal AC voltage (230 V).

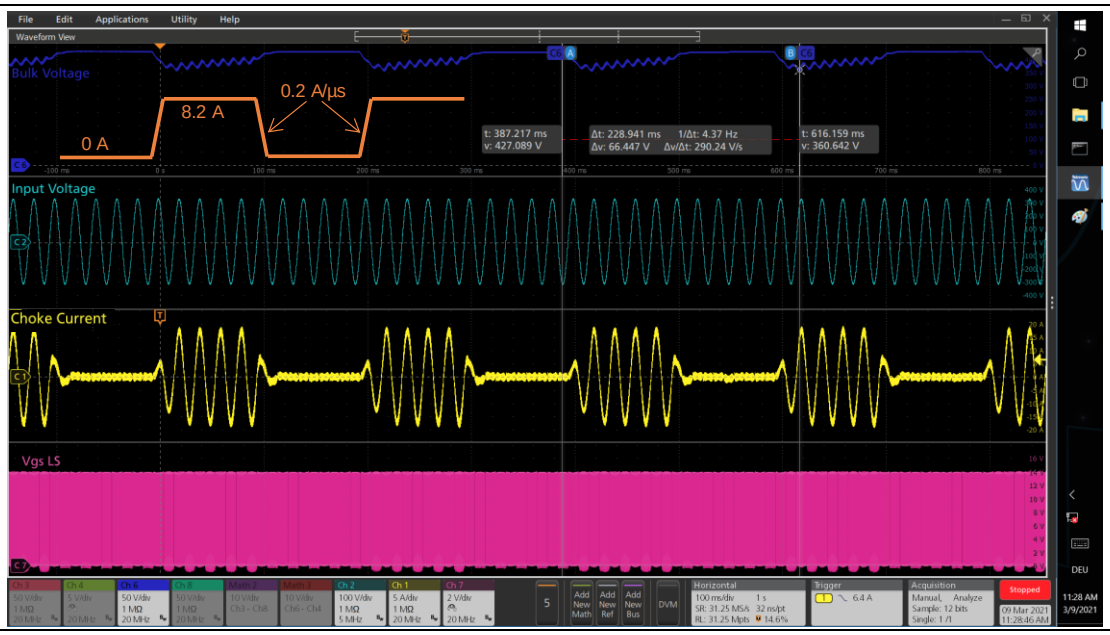


Figure 29 3.3 kW totem pole CCM PFC with CoolMOS™ CFD7 response for full-load to no-load load steps every 100 ms with 0.2 A/µs current slope

The output voltage dynamic range for the specified load variation is between 360 V and 430 V. When the load is removed the overshoot is under the overvoltage setting (450 V), and the converter attempts to regulate the output voltage under no-load conditions by making the average inductor current close to zero. This is possible because negative inductor current is allowed in a totem pole configuration with complementary PWM signals.

3.4.2 AC voltage variation

Input voltage variations, as seen in the power line disturbance section, can modify the bulk voltage. This can also occur when the input voltage varies even within the normal operation range, as shown in **Figure 30**. In this condition, the bulk voltage is in the range 330 V to 440 V, as shown by the test result.

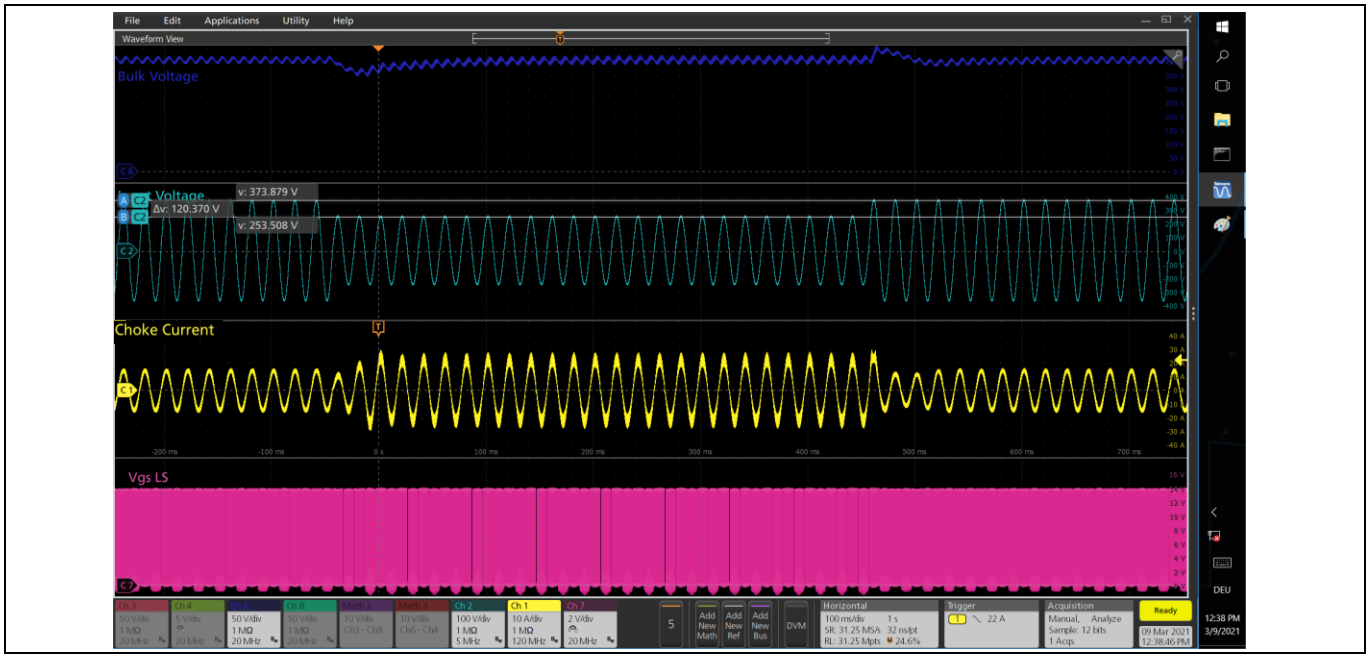


Figure 30 265 V to 180 V line voltage variation at full-load operation

A sudden increase in the input voltage leads to an immediate increase in the inductor current until the voltage loop and the LFF reduce the current demand. Therefore, a sudden change of the AC voltage might lead to PCL, as already shown in sections 3.3.1 and 3.3.2.

3.5 Inrush current and PFC start-up

Figure 31 shows the start-up of the bridgeless CCM totem pole PFC with CoolMOS™ CFD7 for full-load operation. The test has been performed with programmable AC source and HV electronic load. The load is configured with a 350 V threshold to start sinking current. This threshold emulates the behavior of the DC-DC converter, which would be the load for the PFC.

The inrush current when connecting to the AC source is limited by an NTC. This resistor is bypassed by a parallel relay before start-up if the input and output voltage conditions to start the bridgeless PFC are met. The inrush current is measured at the first AC cycle and it is independent of the output load. As shown in **Figure 31**, the inrush current is significantly under the 30 A specified in Table 2.

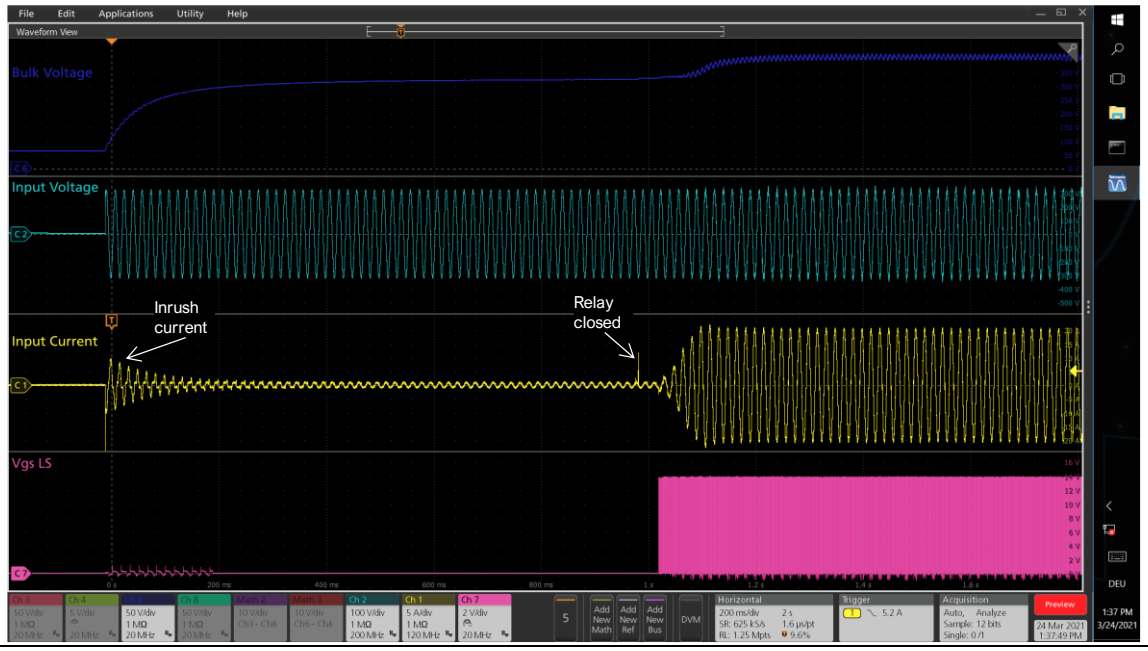


Figure 31 EVAL_3K3W_TP_PFC_CC start-up at full load for 230 V, 50 Hz input voltage

4 Summary

This document has introduced an Infineon system solution for bridgeless totem pole PFC, which achieves a peak efficiency of 99 percent with a 1U form factor and a power density of 80 W/in^3. The EVAL_3K3W_TP_PFC_CC evaluation board implements Infineon 600 V CoolMOS™ CFD7 MOSFETs and a pre-charge circuit to enable continuous hard-commutation in CCM operation. This pre-charge circuit significantly reduces the losses associated with Q_{oss} and Q_{rr} by providing these charges from a LV source.

The combination of CoolMOS™ CFD7 and the pre-charge circuit, together with the 600 V CoolMOS™ S7 selected for the low-frequency half-bridge, enables high performance (efficiency close to 99 percent) with a very attractive price–performance ratio. Furthermore, despite the increase in the number of semiconductors due to the pre-charge circuit, the use of SMD packages for all the power semiconductors allows a compact form factor (92 W/in^3 power density) with proper thermal management. The bridgeless topology implements full digital control on the XMC1000 series Infineon microcontroller and does not require extra PWM signals for the pre-charge circuit.

This document has shown the design procedure and component selection for the pre-charge circuit, and a design tool is embedded to offer the design values for different $R_{DS(on)}$ of the 600 V CoolMOS™ CFD7. This design prodecure has been followed for the design of the presented evaluation board, and the experimental results and capabilities are shown in this document.

The performance of the board in PFC operation is not only outstanding in steady-state conditions, offering high efficiency and high-quality input current (power factor over 0.95 and THD under 10 percent from 20 percent of the load), but it also complies with power line disturbance and hold-up time requirements.

5 Bill of materials

Table 5 Main board components in EVAL_3K3W_TP_PFC_CC

Designator	Value	Tolerance	Voltage	Description
Q1, Q2	IPT60R022S7		600 V	N-channel MOSFET
Q3, Q4, Q5, Q6	IPT60R090CFD7		600 V	N-channel MOSFET
Q7, Q8	BSZ440N10NS3		100 V	N-channel MOSFET
Q9, Q10	BSS138N		60 V	MOSFET
D10, D11	IDDD08G65C6		650 V	Schottky diode
IC2, IC4, IC5	2EDF7275F			Integrated circuit
IC3	1EDN8511B			Gate driver IC
D1, D4, D5, D8, D9	BAT165		40 V	Schottky diode
C1	1 µF X2	20%	305 V AC	Foil capacitor
C4, C5	4.7 nF	Y2	300 V	Ceramic capacitor
C6, C11	3.3 µF X2	10%	305 V AC	Foil capacitor
C8	470 µF	20%	16 V	Polarized capacitor
C12, C13, C14, C15, C16, C17, C18, C24	10 µF	X5R	25 V	Ceramic capacitor
C19, C21, C40	100 nF	X7R	630 V	Ceramic capacitor
C20	1 nF	X7R	50 V	Ceramic capacitor
C22, C23, C25, C26, C32, C33	10 µF	X7R	50 V	Ceramic capacitor
C27, C28, C31	22 nF	X7R	50 V	Ceramic capacitor
C29, C30, C34, C35	470 pF	CG0	50 V	Ceramic capacitor
C36, C37	820 µF	20%	450 V	Electrolytic capacitor
D2, D3, D6, D7, D14	MURS160BT3G		600 V	Standard diode
D12, D13	DFLS130L-7		30 V	Standard diode
D15, D16	S8KCDICT		800 V	Standard diode
F1	25 A			Fuse
IC1	VOL617A-3			Integrated circuit
L1, L2	ICE MG10000842			Common mode choke
L3	ICE MG30002800			PFC inductor
L4	Würth 744824101			Common mode choke
NTC1, NTC2	14 R	25%		NTC inrush resistor
R1, R2	270 R	1%		Resistor
R3, R24, R27, R29, R30	0R5	1%		Resistor
R4	154 R	1%		Resistor
R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R39, R40, R41, R42, R43, R44, R45, R46	750 k	0.10%		Resistor
R17	0 R	1%		Resistor

Designator	Value	Tolerance	Voltage	Description
R18, R20, R23, R31, R33	560 R	1%		Resistor
R19, R21	10 R	1%		Resistor
R22	R003	1%		Shunt resistor
R25	43 k	1%		Resistor
R26, R38, R48	12 k	1%		Resistor
R32, R37	294 R	1%		Resistor
R34, R35	187 R	1%		Resistor
R49	10 k	3%		NTC SMD resistor
REL1	G2RL-1A-E2-CV-HA - DC12		12 V	Relay
X1	MOD100002740 KIT_6W_13V_P7_950V		13 V	Female header, six contacts
X2, X8	Fuse clip			Connector
X3	MKDS 5/ 3-6,35 - 1714955			Connector
X4	SQW-116-01-L-D			Pin header, 2x16
X5, X6, X7	1217169			TE Connectivity AMP connectors

Table 6 Control board components in EVAL_3K3W_TP_PFC_CC

Designator	Value	Tolerance	Voltage	Description
IC3	XMC1402Q040X0064AAXUMA1			XMC™ microcontroller
C1, C2, C20	330 pF	X7R	50 V	Ceramic capacitor
C3, C4, C16, C17, C23	100 pF	X7R	50 V	Ceramic capacitor
C5, C6, C7, C11	1 nF	X7R	25 V	Ceramic capacitor
C8, C9	1 µF	X7R	25 V	Ceramic capacitor
C10, C13, C15, C18, C19, C22, C24	100 nF	X7R	25 V	Ceramic capacitor
C12, C14, C21	10 µF	X5R	6.3 V	Ceramic capacitor
D1	Orange LED			LED
D2	Green LED			LED
D3	Bat54S			Diode
D4	Red LED			LED
IC1	OPA2376AIDR			Integrated circuit
IC2	L78L05ACUTR			Integrated circuit
IC4	TL431B	0.50%		Integrated circuit
IC5	LMH6642MF			Integrated circuit
IC6	SN74LVC2G34DBVR			Integrated circuit

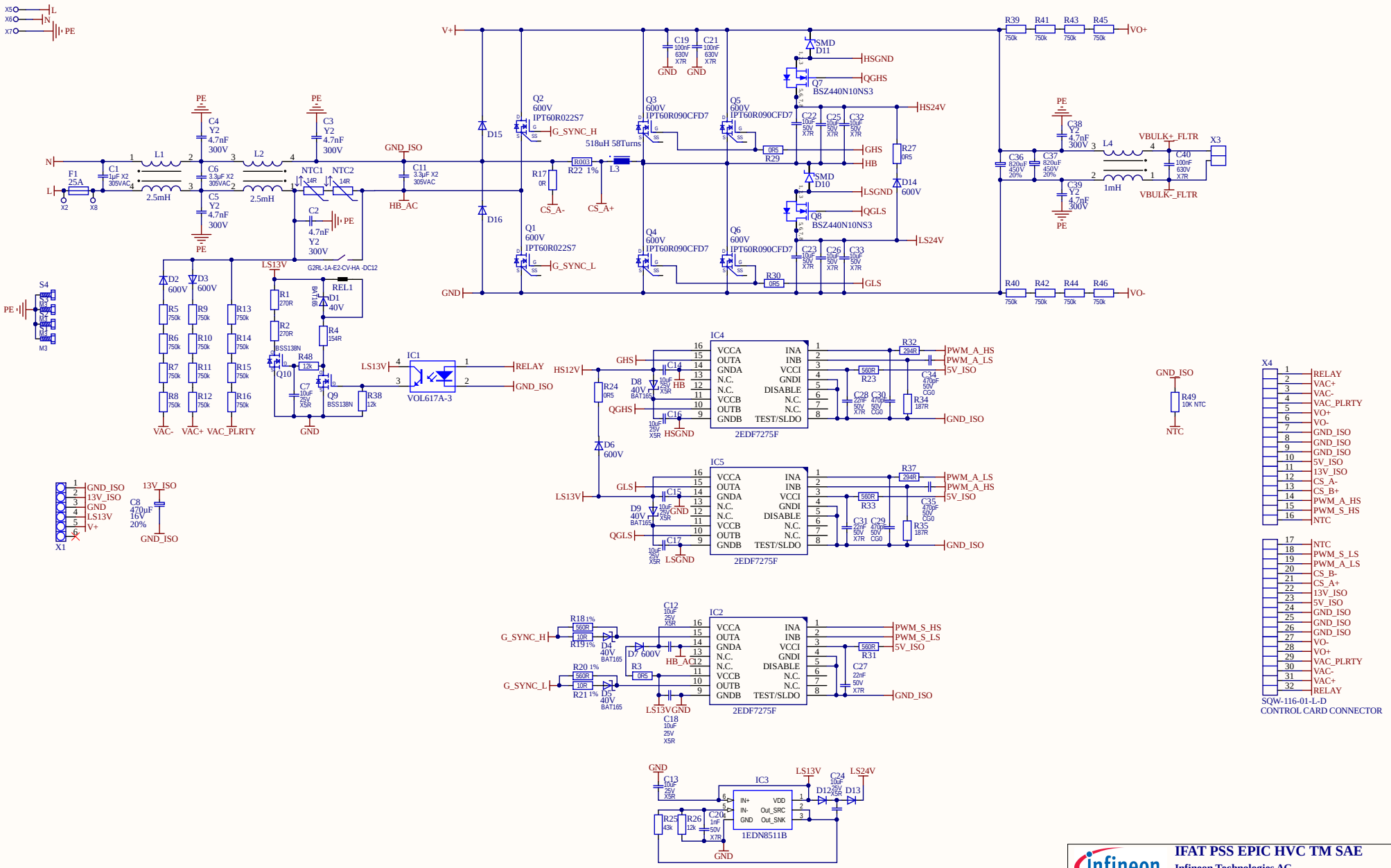
Bill of materials

Designator	Value	Tolerance	Voltage	Description
R1, R2, R17, R19, R25	510 R	1%		Resistor
R3, R4, R9, R11	37k4	0.10%		Resistor
R5, R6, R7, R10	750 k	0.10%		Resistor
R8, R13, R15	1k4	1%		Resistor
R12, R16, R20, R24	1 k	1%		Resistor
R14	10 R	1%		Resistor
R18, R21	750 R	0.10%		Resistor
R22, R23	47 R	0.10%		Resistor
R26	22 k	1%		Resistor
X1	TSM-104-01-F-DH-A			Female header, eight contacts
X2	TMM-116-03-L-D			Pin header, 2x16 contacts
X3	PicoBlade four-pin SMD			Pin header, five contacts

6 Schematics

The next pages shows the schematics for the EVAL_3K3W_TP_PFC_CC board.

M100002853 PCB.SchDoc



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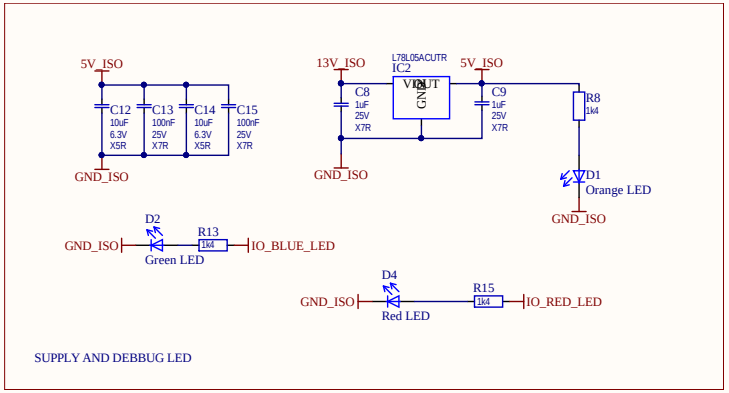
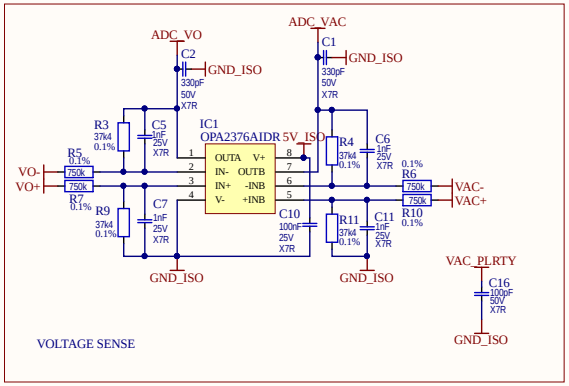
Title	EVAL_3K3W_TP_PFC_CC Main Board
Variant	[No Variations]
Approved	<Appr.>
Size	A3
Document Name	M100002853 PCB.SchDoc
Rel.	
Rev.	<Rev.>
Author	Matteo-Alessandro Kutschak
Date	31.05.2021 Time: 13:49:24
SVN Revision	1174 [Locally Modified]

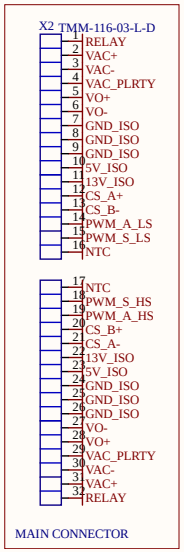
Sheet 1 of 1

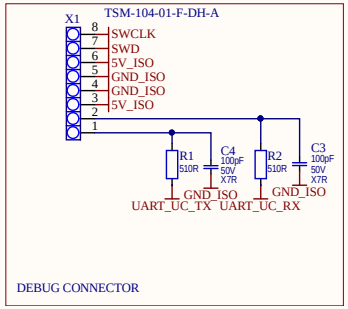
CD100002854 PCB.SchDoc

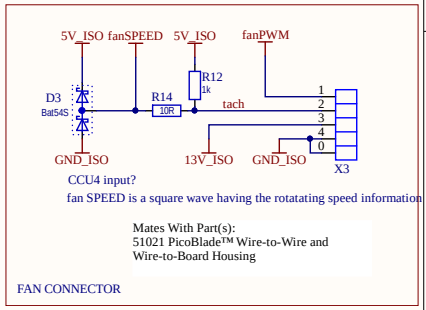
FID1 Fiducial — Fiducials
FID2 Fiducial — Fiducials
FID3 Fiducial — Fiducials
FID4 Fiducial — Fiducials

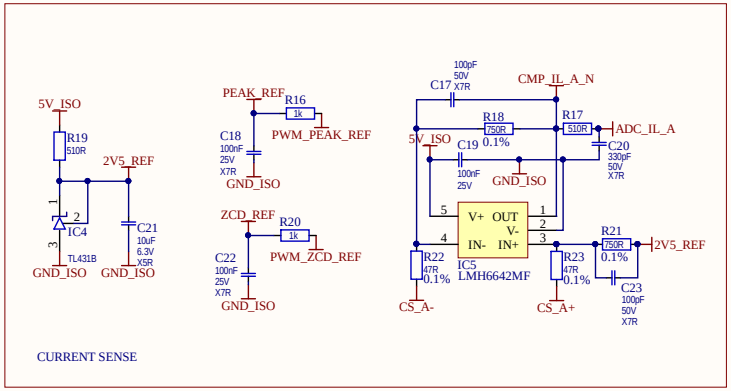


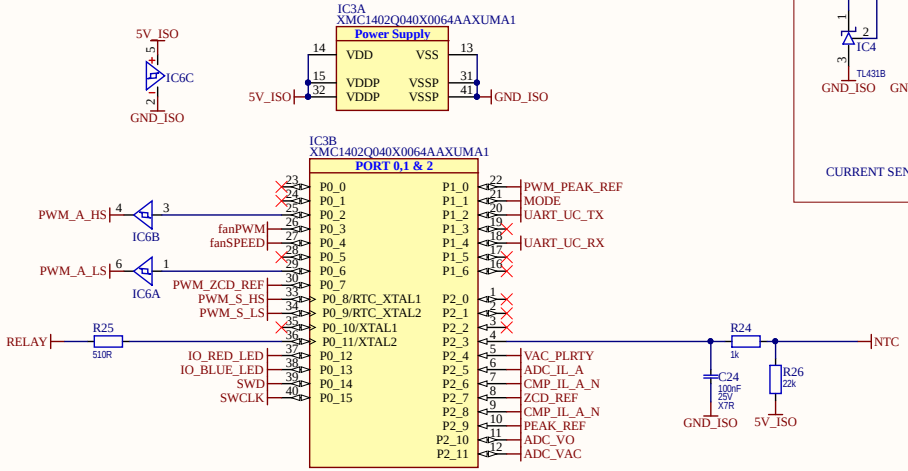












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Variant	[No Variations]
Author:	Matteo-Alessandro Kutschak; David Meneses
Date:	31.05.2021 Time: 13:59:55
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Sheet	1 of 1

7 References

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[7] “600 V CoolMOS™ CFD7 Power Transistor IPT60R090CFD7 Datasheet”. **Available online**.

8 Revision history

Document version	Date of release	Description of changes
V 1.0	31-03-2021	First release

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