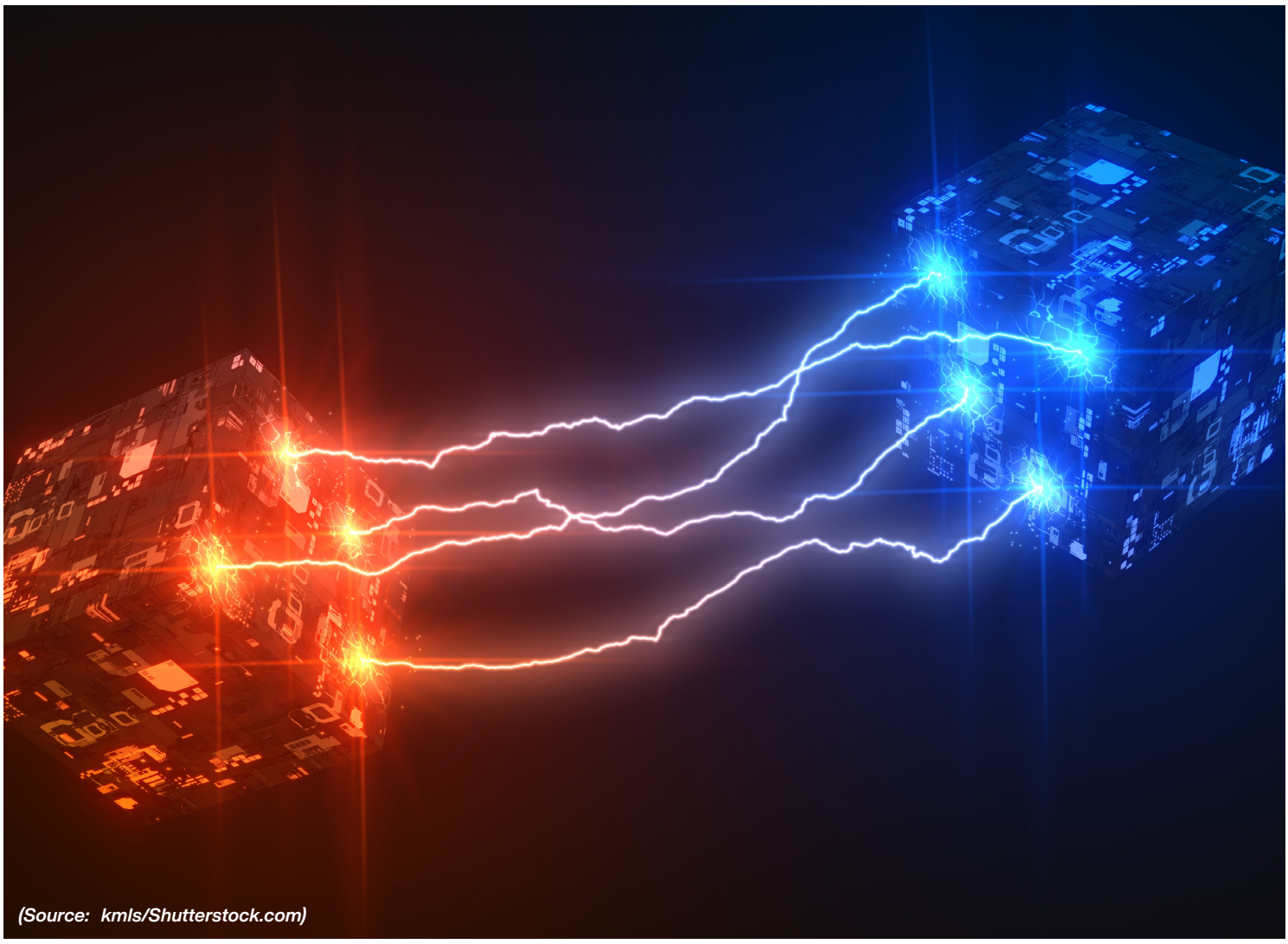
A Solution for High-Density AC/DC Conversion

By Jim Harrison for Mouser Electronics



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MOUSER ELECTRONICS | Infineon

Power converter design engineers are some of the elites of the electronics design community. These designers must possess analog technical skills and intimate knowledge of many components to design modern switch-mode power converters.

Successful designs must be super-efficient across a broad load range, very reliable, and—more than ever—be in a tiny package. Modern MOSFET transistors, when properly integrated, can yield efficiencies that were merely a dream two decades ago. Today, 95% efficiency is well within sight, including power factor correction (PFC) and AC rectification. The design engineer must do all this while keeping costs down. The key to success is knowing the latest and best semiconductors and optimizing tradeoffs between various circuit areas.

Power factor correction (PFC) is a must for modern off-line power conversion. PFC reduces the load on the electrical grid, increases power quality, and reduces electricity system costs. PFC is added to a unit to meet the specifications of IEC 61000-3-2, which sets limits to the harmonic currents drawn by an electrical apparatus.

The engineer can use this as a design tradeoff. For example, if the designer can increase PFC performance, they may relax the requirements of the DC-DC converter and vice versa.

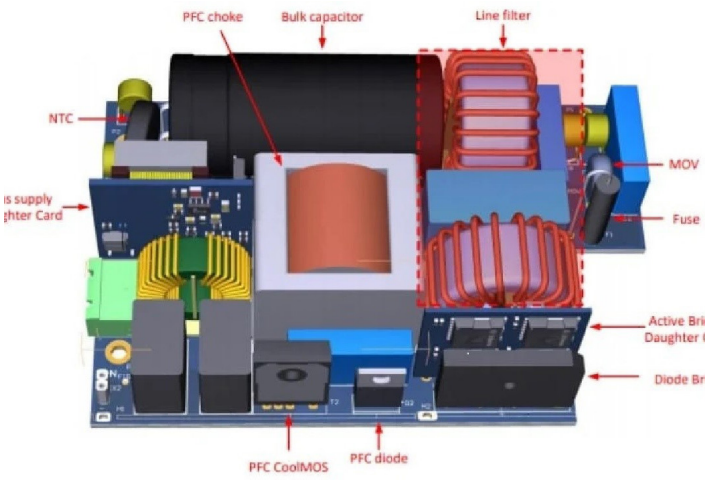

Figure 1: *The EVAL_2K4W_ACT_BRD_S7 Continuous Conduction Mode (CCM) Power Factor Correction (PFC) converter demo board with 600V CoolMOS™ S7 for active-line rectification and inrush current control from Infineon Technologies. (Image Source: Mouser Electronics)*

Making the Converter Design Effort Trouble-Free

The power MOSFET is an excellent place to start dividing the task into critical elements makes this design a lot easier. The CoolMOS™ S7 from Infineon is a 600V device that uses the superjunction (SJ) principle. This family of MOSFETs enables the excellent price-performance for low-frequency switching applications while also allowing for fast switching that increases the associated efficiency. The device uses a 4-pin kelvin source package design to complement its best-in-class R_{ds} specification.

The EVAL2K4WACTBRDS7TOBO1 evaluation board exposes this device to a continuous conduction mode (CCM) 2.4kW power supply operating from a 90–265Vrms 50/60Hz with a nominal output voltage of 390V. This design will yield more than 98.6% efficiency with a 230VAC input and 6A output.

Four Key Devices Used on The Evaluation Board

The evaluation board is 127mm long, with a width of 85mm and a height of 44mm. Located at the input to the board is a fuse and a Metal-Oxide Varistor (MOV) surge protector, followed by a two-stage electromagnetic interference (EMI) line filter. After that comes the bridge rectifier and the PFC/main converter. The primary inductor is located in the center of the board (**Figure 1**).

The Active Bridge Rectifier

In a typical modern supply design, the input bridge rectifier's power dissipation dominates losses with about 35% of the total. The active bridge design uses four IPT60R022S7 FETs that parallel a standard diode bridge. On the evaluation board, these FETs are on a plug-in daughter card along with two gate drivers. It is essential to ensure that the FETs are properly driven to prevent false triggering.

A secondary-side high-speed synchronous rectification controller for resonant half-bridge converters directly senses the drain-to-source voltage of each MOSFET to determine the drain current. This sensing enables it to rapidly turn on each gate at the start of each conduction cycle and off near the zero current transitions. Ruggedness and noise immunity is accomplished using an advanced blanking scheme and double-pulse suppression. In addition, the chip's cycle-by-cycle minimum on time (MOT) protection can automatically detect light or no-load conditions so that the gate drives may be disabled to avoid unwanted reverse currents.

The 2EDF7275F high side driver IC is internally galvanically isolated and has 150V/ns common-mode transient immunity. Its PWM inputs have 18ns noise filters, and it has an under-voltage lockout. The IC can source/sink 4A/8A and provides full isolation in a small 10mm x 6mm package (**Figure 2**).

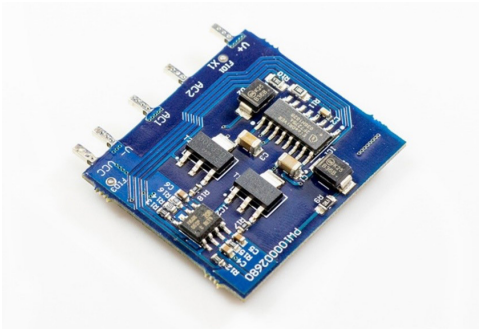

Figure 2: *Infineon Technologies KIT_ACT_BRD_60R040S7 is an extremely compact daughter card that aims to replace standard diode bridge rectifiers with an active full-bridge for line rectification in standard Continuous Conduction Mode (CCM) Power Factor Correction (PFC) Converters. (Image Source: Mouser Electronics)*

With a 1200W load, this active bridge circuit gains about a one-half of one percent (0.5%) efficiency increase over the standard bridge. A peak efficiency improvement of 1.3 percent (1.3%) is reached at low-line with an active-bridge line rectification of 22mΩ MOSFET. At high-line the delta efficiency peak is around 0.7 percent (0.7%).

The Conversion and PFC Controller

An Infineon ICE3PCS01G controller IC provides voltage regulation and power factor correction (PFC) in a boost topology in continuous conduction mode (CCM). In a CCM design, there is always a current flow in the inductor. The voltage across the inductor reverses as the inductor current rises and falls, and the current flow is continuous. The chip provides voltage loop compensation and fast output dynamic response during load jump and external current loop compensation. The switching frequency is set at 65kHz on this evaluation board, but it can go as high as 250kHz.

The IC operates with a cascaded control, an inner current loop, and an outer voltage loop. The inner loop controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage if the device operates in CCM—and since the voltage and current are in-phase, it has power factor correction.

The outer voltage loop controls the output bulk voltage and is digitally processed within the IC. The pin VSENSE is the input of a sigma-delta A/D followed by digital loop compensation and converted to an appropriate DC voltage which controls the amplitude of the average input current. The nonlinear gain block manages the amplitude of the regulated inductor current.

In steady-state operation, the converter fundamentally keeps the volt-seconds (V*s) across the inductor during the on-time of the switch equal to the V*s across the inductor during the off-time of the switch. Under light load conditions, depending on the choke inductance, the system may enter discontinuous conduction mode resulting in higher harmonics but still meeting the class D requirement for harmonic currents drawn. In steady-state operation, the ampere-seconds (A*s) charging the output capacitor during the on-time of the switch must be equal to the A*s discharging of the capacitor during the switch-off time. If not, then it is not operating in regulation.

The controller, via a gate driver, switches a single CoolMOS™ FET. Its low gate-to-source and gate-to-drain charge enhance the fast-switching ability of the IPZ60R040C7 CoolMOS™ superjunction FET. Turn-on delay time is 18ns and rise time of just 8ns. The gate driver IC features a differential input providing very high common-mode rejection, which reduces false triggering vulnerability. Peak common-mode voltages of up to ±150V between driver reference and system ground are tolerable. The input signal to the driver is filtered and then applied to a differential Schmitt-trigger. Input-to-output propagation delay is around 45ns.

Having a very low reverse recovery time PFC diode is an essential factor in this regulator circuit design. The 650V G6 CoolSiC™ Schottky barrier diode (IDH12G65C6) from Infineon employs leading-edge technology, fully leveraging all advantages of silicon carbide over silicon. A proprietary soldering process is combined with thin-wafer technology and a novel Schottky metal system. The result is a diode with VF of 1.25V at 12A and total capacitive charge (QC) of 17.1nC, typical.

Startup Inrush Limiting

All power converters must deal with a large input current inrush when AC power is first switched on. A typical design method to limit this surge is to have a power resistor just after the bridge rectifier. That resistor, or often a negative temperature coefficient thermistor, is then bypassed with a mechanical relay after a time delay to save power. This reference design is clever and removes bulky components to improve power density significantly.

First, we move protection from near the bridge rectifier to be in series with the DC side filter capacitor. This is where almost all the inrush occurs. Being on the DC side of things makes driving things easier. We can then replace the bulky mechanical relay with an IPT60R022S7 SMT MOSFET. This 22mΩ on-resistance device handles the total peak current of the circuit. The relay volume of 3.1cm^3 is replaced with the 0.27cm^3 of a MOSFET. Once the bias supply is up, and the main PWM is operating, the ICE3PCS01G controller IC enables the VB_OK signal and turns on the MOSFET shunt.

System Bias Supply

A second plug-in module on the evaluation board (**Figure 3**) provides the critical bias supply voltage directly from the AC input. The circuit employs an Infineon Quasi-Resonant CoolSET™ Power IC optimized for off-line switch power supplies in cascade configurations. The chip's digital switching frequency control offers lower EMI and higher efficiency over wide AC input and load ranges. In addition, the IC's enhanced active burst mode enables flexibility in standby power range selection. The Start-up current is only 0.19mA, and the normal operation takes just 0.9mA. The numerous protection functions include both input OVP and brownout.

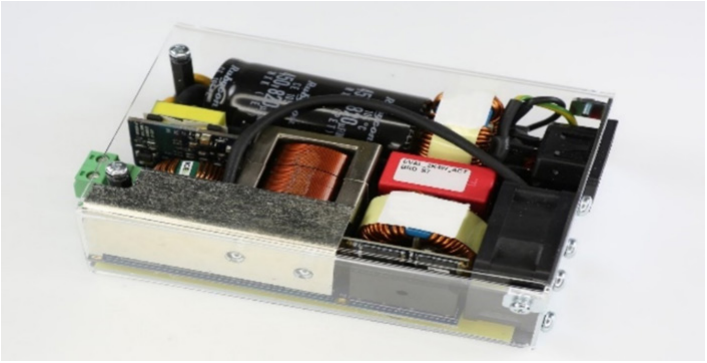

Figure 3: *The eval kit package. (Image Source: Mouser Electronics)*

Power Conversion at Its Best

Various power conversion efficiency requirements, such as 80 PLUS or EuP, are defined for multiple power conversion applications. Meeting the best-in-class 80 PLUS Titanium requirement is no easy task. In the Platinum class, the PSU must have a peak efficiency above 94% at high-line and 92% at low-line, while for a Titanium design, these values increase to 96% and 94%, respectively.

The addition of the active-bridge solution in this reference design puts it solidly into the Platinum class, and the outstanding packaging solutions of the entire scheme make it a power density champion and a sure-to-be industry favorite.