Increasing output power in motor drives with OptiMOS™ 6 150 V

About this document

Scope and purpose

This application note introduces Infineon's new OptiMOS™ 6 150 V family of MOSFETs and demonstrates the performance improvement achieved over OptiMOS™ 5 in low switching frequency applications such as motor drives. A brief introduction to the technology highlighting its technical benefits is followed by an extensive experimental evaluation comparing OptiMOS™ 6 150 V with the previous generation MOSFETs.

Intended audience

The intended audience for this document is design engineers, technicians, and developers of electronic systems.

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1 The new OptiMOS™ 6 150 V

1.1 Features and benefits

OptiMOS™ 6 150 V was developed for improved system performance, combining exceptionally low $R_{DS(on)}$, low figures of merit (FOMs), a soft diode reverse recovery behavior, a low reverse recovery peak current, and a low gate threshold voltage spread $V_{GS(th)}$. It ensures high efficiency, high power density, low EMI, and high system reliability.

These features make OptiMOS™ 6 150 V the best fit for both motor drives and SMPS applications, supporting the trend toward sustainability and decarbonization while enabling designs for higher efficiency, higher power densities, reduction in the number of paralleled MOSFETs, and cost effectiveness.

For motor drive applications where paralleling and low EMI is required, OptiMOS™ 6 150 V is best suited for applications such as e-scooters, micro EVs, forklifts, golf carts, and other battery-powered motor drives.

For more details about OptiMOS™ 6 150 V's impressive performance capabilities in high-switching frequency applications, such as switch mode power supplies (SMPS), see www.infineon.com/optimos-6-150v.

1.2 Target applications

Some applications that will benefit from the new Infineon OptiMOS™ 6 150 V are shown in Figure 1.

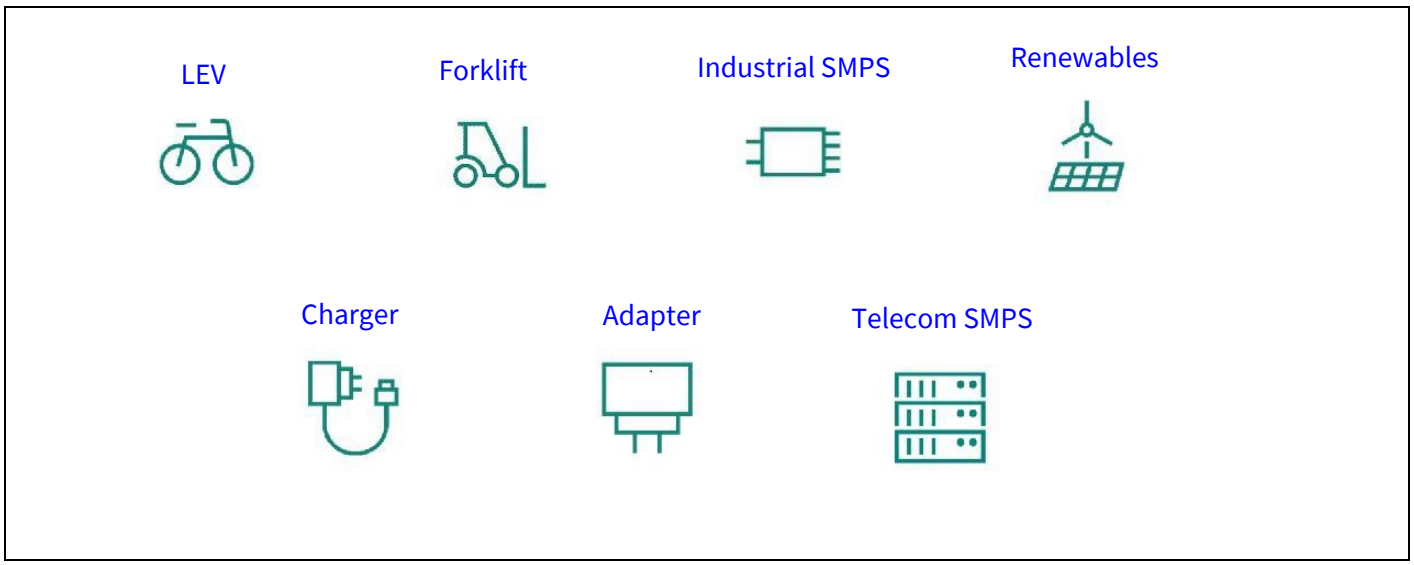

Figure 1 List of main applications targeted by the new Infineon OptiMOS™ 6 150 V

1.3 Technology parameters comparison between OptiMOS™ 5 150 V and OptiMOS™ 6 150 V

In the following sections, technology parameters important for motor drives of the latest OptiMOS™ 6 150 V technology will be compared with its predecessor, OptiMOS™ 5 150 V. The focus will be on performance comparison of the best-in-class devices of OptiMOS™ 6 150 V (IPF026N15NM6 [2]) and OptiMOS™ 5 150 V (IPB044N15N5 [3]).

1.3.1 Datasheet comparison for OptiMOS™ 5 150 V and OptiMOS™ 6 150 V

Table 1, compares datasheet values for devices from OptiMOS™ 5 150 V and OptiMOS™ 6 150 V. The table focuses on parameters that are most important for motor drives (see datasheets [4] and [5] for more details).

Table 1 Datasheet comparison between OptiMOS™ 5 150 V and OptiMOS™ 6 150 V

Parameter	Symbol	Unit	Conditions	OptiMOS™ 5 IPB044N15N5	OptiMOS™ 6 IPF026N15NM6
Drain-source on-state resistance (max. value)	$R_{DS(on),max}$	mΩ	T_j = 25°C; V_{GS} = 10 V	4.4	2.6
			T_j = 25°C; V_{GS} = 15 V	–	2.5
Transconductance, (typical value)	$g_{fs,typ}$	S	See note [1]	144	180
Thermal resistance, junction - case	R_{thJC}	K/W	Typical/maximum	0.3/0.5	–/0.38
Drain current	$I_{D,cont}$	A	T_C = 25°C	174	239
	$I_{D,pulse}$	A	T_C =25°C	696	956
Gate threshold voltage	$G_{S(th)}$	V	Min., Typ., Max See note [2]	3, 3.8, 4.6	3, 3.5, 4.0

[1] OptiMOS™ 5: $|V_{DS}| > 2|I_D|R_{DS(on)max}$, I_D = 87 A; OptiMOS™ 6: $|V_{DS}| > 2|I_D|R_{DS(on)max}$, I_D = 100 A
[2] OptiMOS™ 5: $V_{DS} = V_{GS}$, I_D = 264 µA; OptiMOS™ 6: $V_{DS} = V_{GS}$, I_D = 276 µA

1.3.2 On-state resistance $R_{DS(on)}$

The on-state resistance ($R_{DS(on)}$) is the most important parameter for the choice of MOSFETs for motor drives. Figure 2 compares the $R_{DS(on)}$ values for the new OptiMOS™ 6 150 V technology to the previous generation of OptiMOS™ 5 150 V MOSFETs. It reveals a significant reduction of 40.9% and 41.25% specified for case temperatures of T_C = 25°C and T_C = 175°C respectively, and a gate source voltage of V_{GS} = 10 V, thereby improving the price performance of the OptiMOS™ 6 MOSFET.

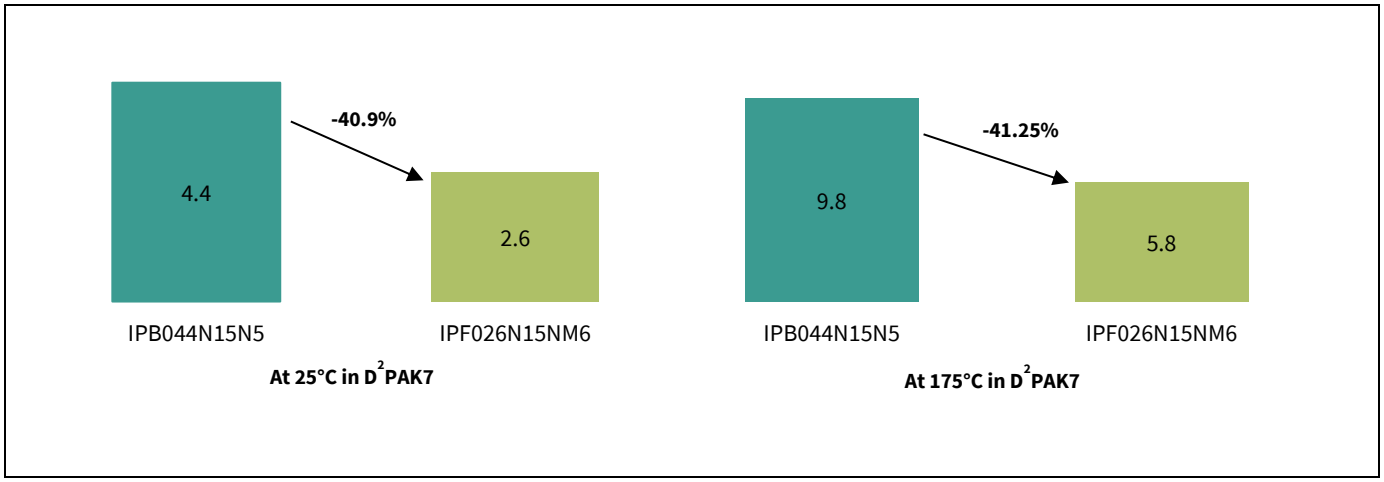

Figure 2 Comparison between the maximum $R_{DS(on)}$ (mΩ) for OptiMOS™ 6 150 V and OptiMOS™ 5 150 V MOSFETs in D²PAK7 for 25°C (left) and for 175°C (right)

The new OptiMOS™ 6 150 V

The decreased $R_{DS\,(on)}$ brings a series of advantages for the end application, such as:

- Reduction of conduction losses
- Reduction of the number of paralleled MOSFETs, saving cost and PCB space and improving power density
- Choice of a smaller package without compromising the $R_{DS(on)}$ value

The temperature shows a pronounced influence on the $R_{DS(on)}$. The relationship between $R_{DS(on)}$ and the temperature is given by:

$$R_{DS(on)} = R_{25}\left(1 + \frac{\alpha}{100}\right)^{T-25}$$

Equation 1 Relation between $R_{DS(on)}$ and temperature

Where α is the temeprature coefficient and R25 the $R_{DS(on)}$ at 25°C. The temperature coefficients are almost matching for the investigated MOSFETs, see Figure 3.

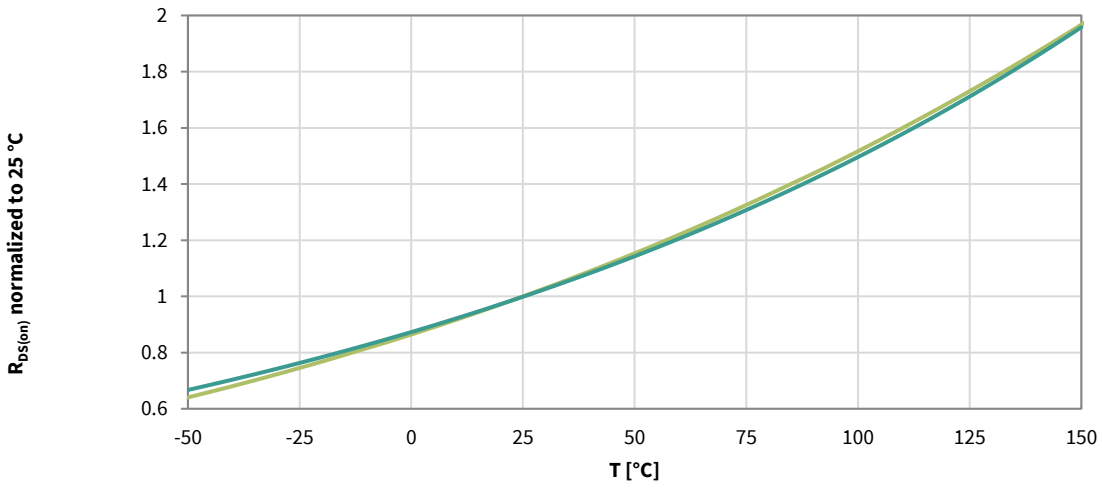

Figure 3 $R_{DS(on)}$ normalized to 25°C over the MOSFETs' junction temperature (left); absolute $R_{DS(on)}$ temperature dependency of OptiMOS™ 5 and OptiMOS™ 6 (right)

1.3.3 Internal gate resistance R_g and gate drive circuit

At turn-on, the gate of the MOSFET is effectively an uncharged capacitor. Assuming an ideal voltage source at the gate, the current is limited only by the internal gate resistor. Both MOSFETs show a similar internal gate resistance. The typical internal gate resistor for the OptiMOS™ 5 MOSFET is 0.8 Ω and for OptiMOS™ 6 is 1.04 Ω. In motor drive applications, the typical external gate resistance is >10 Ω which leaves enough room for adjustments.

The investigated MOSFETs are often used in a hard switching half-bridge topology as shown in Figure 4. Therefore, the switching behavior in such an arrangement is of particular interest. Figure 5 compares the I_D and V_{DS} waveforms for the low-side switch Q_2 at a hard turn-on event of the high-side switch Q_1 and a positive load current I_L. For both the $V_{DS,LS}$ and $I_{D,LS}$ waveforms, OptiMOS™ 6 shows improvements.

To compare OptiMOS™ 6 with OptiMOS™ 5, the dv_{DS}/dt at the high-side switch for a 100 A turn-on event is matched. To achieve the same dv_{DS}/dt for both MOSFETs, a gate resistor of 110 Ω is necessary for OptiMOS™ 5

and 85 Ω for OptiMOS™ 6 at turn-on. A comparison of the waveforms for a turn-off event for an R_g of 15.1 Ω for both MOSFETs exhibits a lower dv_{DS}/dt and a higher di/dt for OptiMOS™ 6.

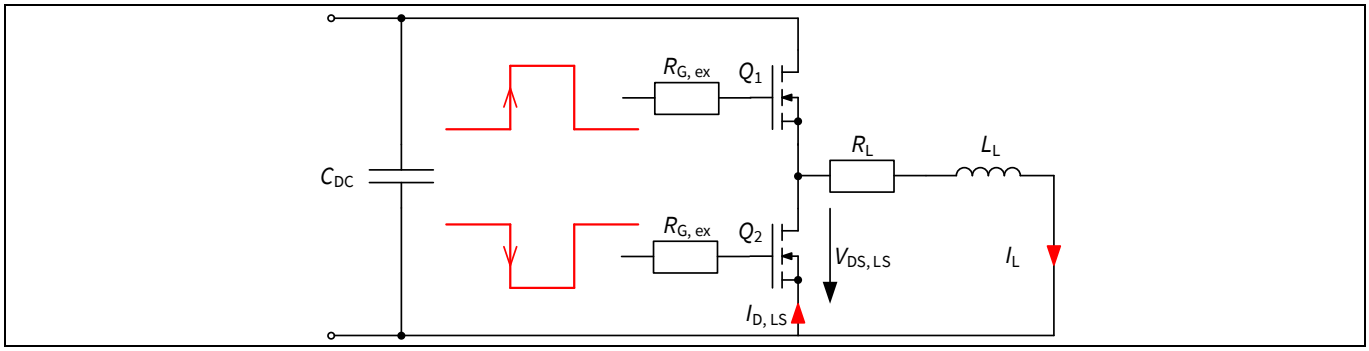

Figure 4 Half-bridge test circuit

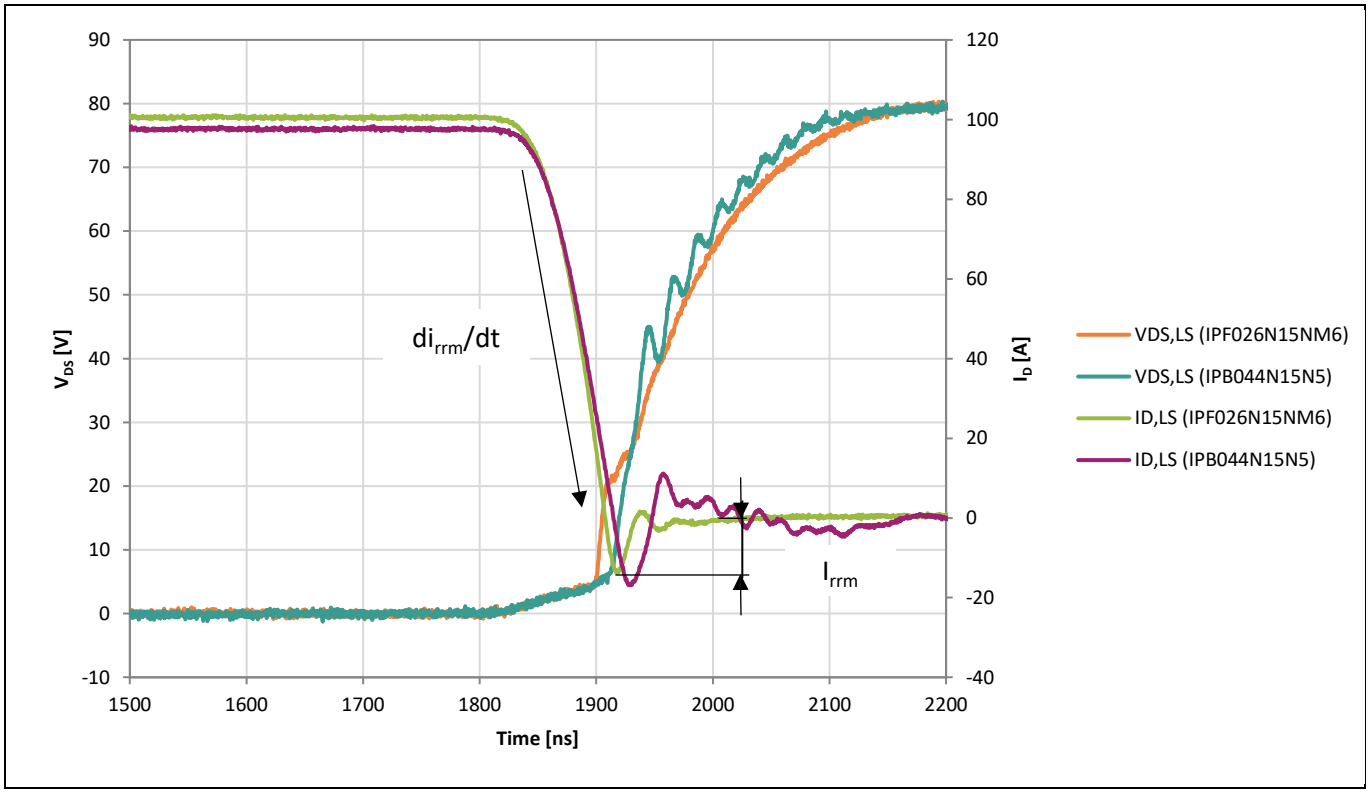

Figure 5 I_D and V_{DS} waveforms for the low-side MOSFET for a half bridge turn-on event

The reverse recovery charge (Q_{rr}) of the body diode is a source of losses and electromagnetic interference (EMI) and is influenced by the di_{rrm}/dt. However, a comparison of the MOSFETs' Q_{rr} specified in the datasheets ([4] and [5]) cannot be done because they are tested under different conditions. Figure 6 shows the results of a double-pulse test performed for OptiMOS™ 5 and OptiMOS™ 6 at a 50 A pulse with a matched di/dt of 500 A/µs. From the waveforms, we can conclude that OptiMOS™ 6 has both a lower reverse recovery charge (Q_{rr}) and a lower peak reverse recovery current ($-I_{rrm}$). These results contribute to lower EMI and lower power losses.

This app note compares the best-in-class FETs of both technologies. If the closest $R_{DS(on)}$ match of OptiMOS™ 6 would be used for the comparison, the reduction in Q_{rr} and $-I_{rrm}$ would be even higher.

The new OptiMOS™ 6 150 V

The current slope di_{rrm}/dt and $-I_{rrm}$ describes the softness factor of the diode. This factor is especially important for motor drive applications in which fast current transitions can cause significant EMI. OptiMOS™ 6 shows a 40% higher diode softness factor as shown in Figure 6.

Comparing the diode reverse recovery behavior side-by-side of the two investigated MOSFETs, the improvements can be quantified with absolute numbers as shown in Figure 6:

- Q_{rr} area of IPF026N15NM6 is reduced by 30% over IPB044N15N5
- $-I_{rrm}$ of IPF026N15NM6 is reduced by 22% over IPB044N15N5
- Decreased Q_{rr} and I_{rrm} for a 40% higher diode softness

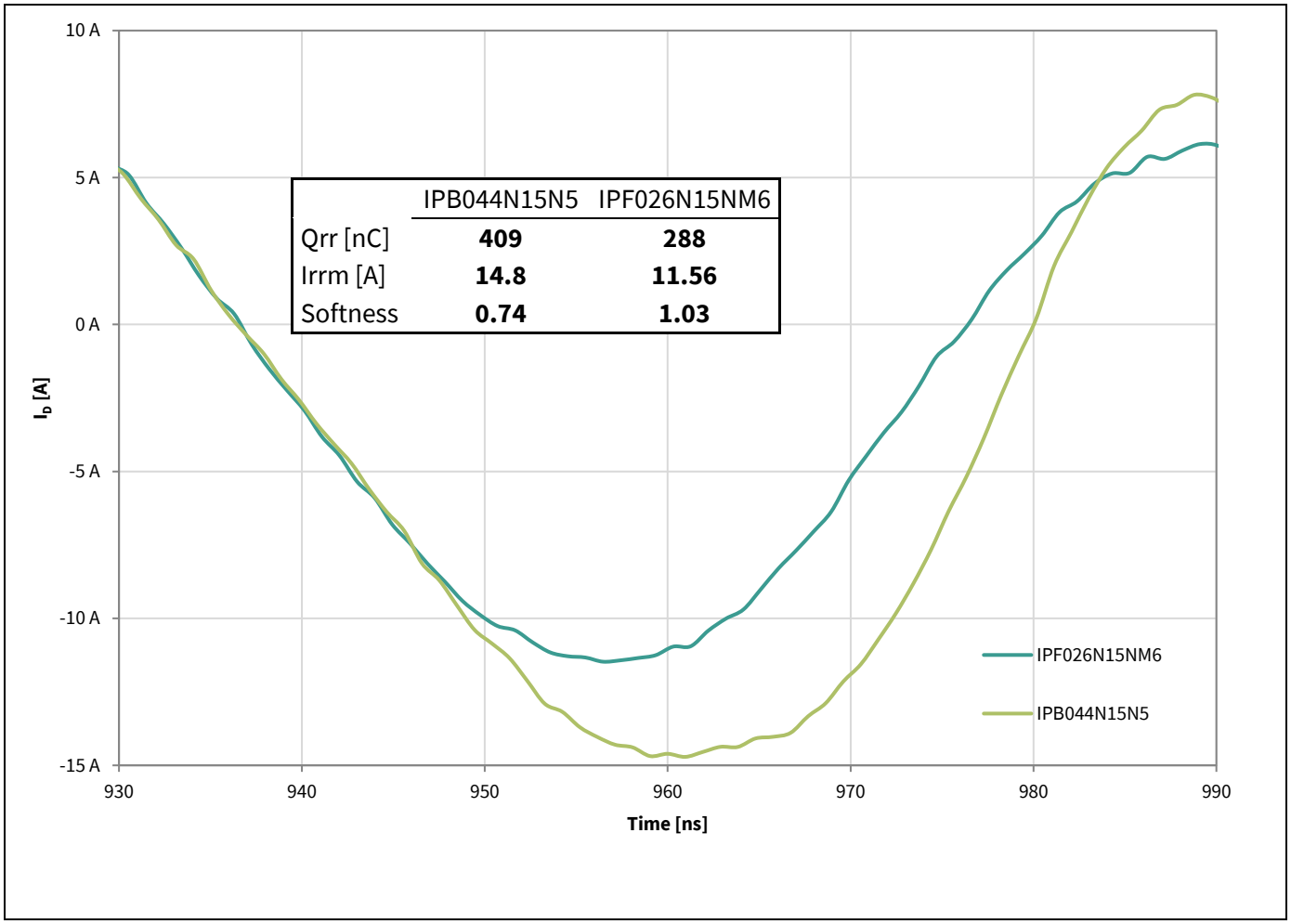

Figure 6 **Q_{RR} - Reverse recovery current of IPB044N15N5 and IPF026N15NM6 at T_j = 25°C, I_D = 50 A, di_D/dt = 500 A/µs**

The improvements of OptiMOS™ 6 are also visible on the gate signals. Figure 7 shows the gate-source voltage of the low-side MOSFET for a half bridge turn-on event. The induced V_{GS} stays well below the minimal $V_{GS(th)}$ of 3 V for both investigated MOSFETs. Hence, no induced turn-on is expected for both MOSFETs. However, OptiMOS™ 6 shows a lower amplitude and frequency of gate ringing, which could improve electromagnetic interference (EMI) results. A similar picture is given by Figure 8 showing V_{GS} of the high-side MOSFETs, with OptiMOS™ 6 again showing a slightly lower ringing amplitude.

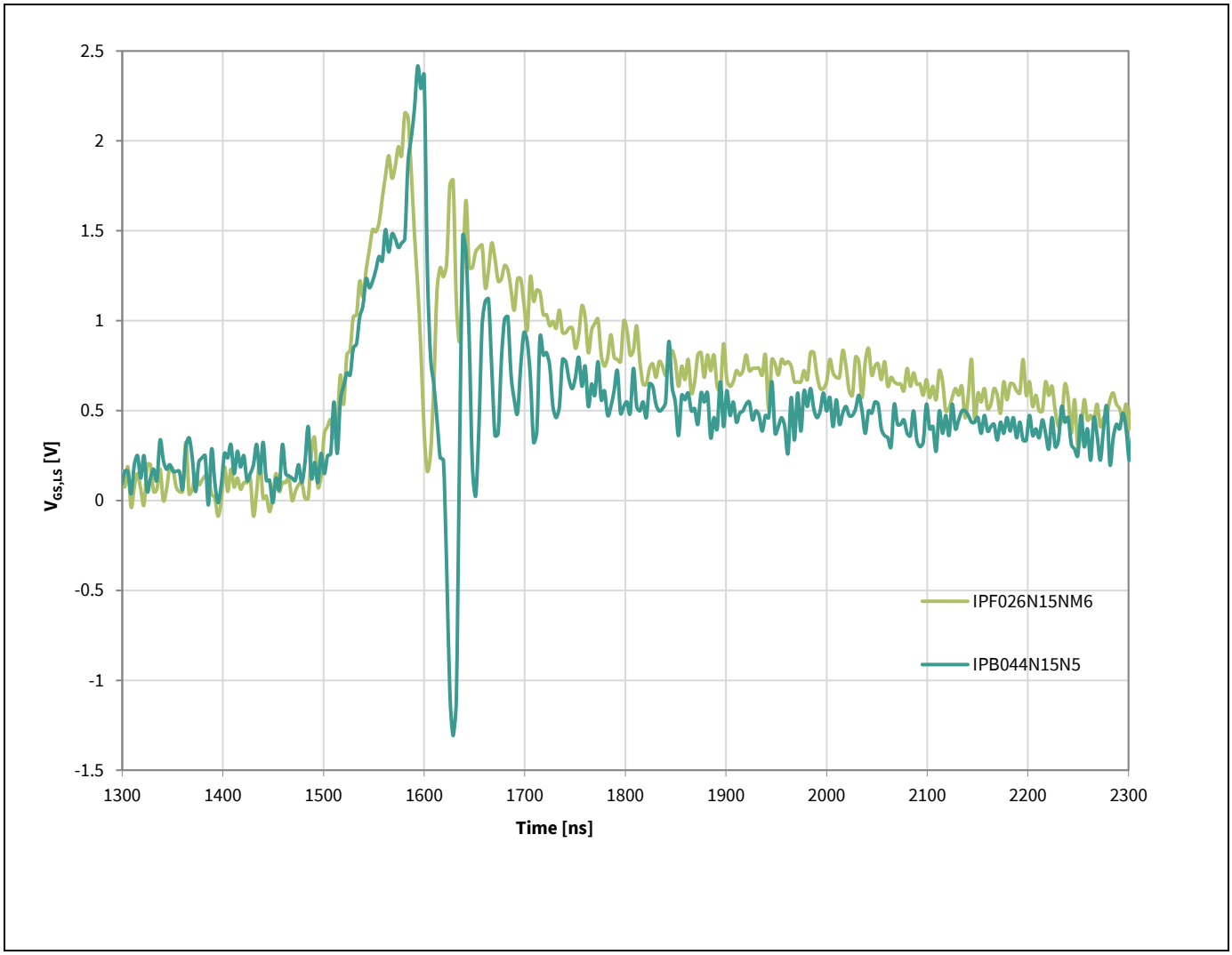

Figure 7 **Gate-source voltage for the low-side MOSFETs for a turn-on event of IPB044N15N5 and IPF026N15NM6 at T_j = 25°C, I_D = 100 A**

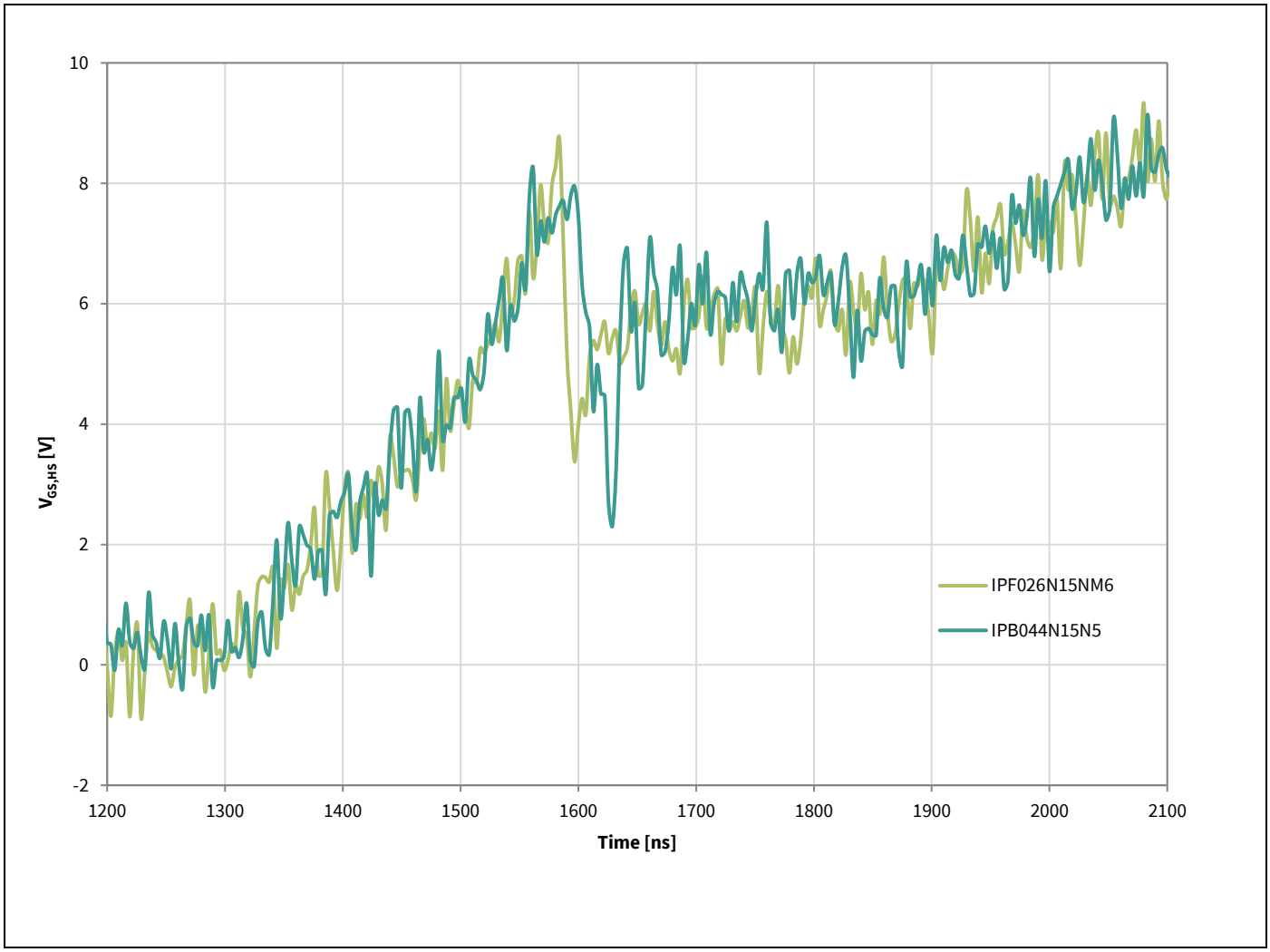

Figure 8 **Gate-source voltage for the high-side MOSFETs for a turn-on event of IPB044N15N5 and IPF026N15NM6 at T_j = 25°C, I_D = 100 A**

The gate resistors are adjusted for a matched dv/dt at a turn-on on the high-side switches as shown in Figure 9. Therefore, with the same external gate resistor we would get slower dv/dt transitions. When migrating from OptiMOS™ 5 to OptiMOS™ 6, this resistor needs to be adjusted to a slightly lower value for OptiMOS™ 6 if the same dv/dt is targeted.

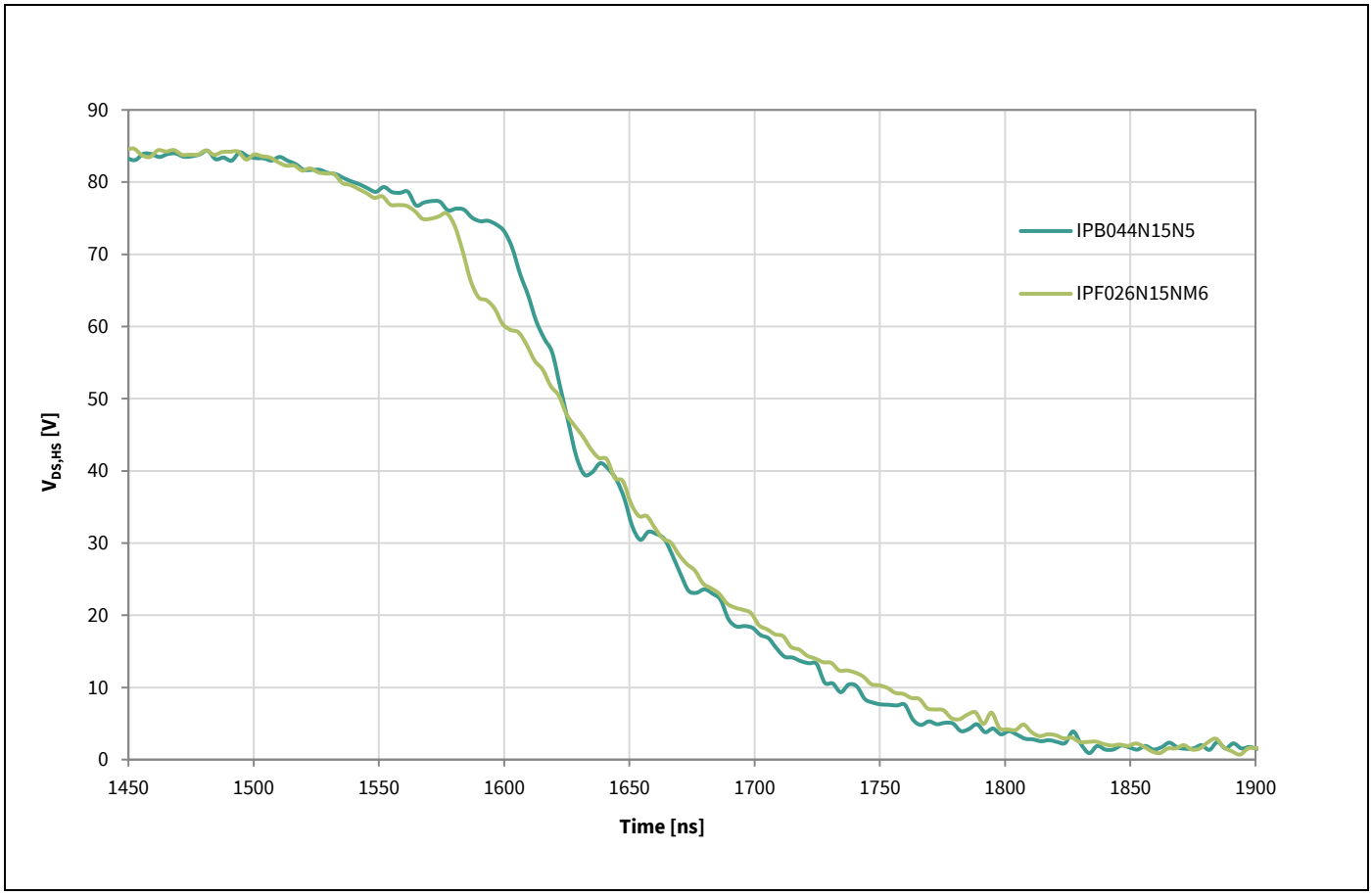

Figure 9 **Drain-source voltage for the high-side MOSFETs for a turn-on event of IPB044N15N5 and IPF026N15NM6 at T_j = 25°C, I_D = 100 A**

1.3.4 Input capacitance C_{iss}, reverse recovery capacitance C_{rss}, and output capacitance C_{oss}

At turn-on, the gate of the MOSFET behaves like an uncharged capacitance. The parameter C_{iss} describes this capacitance value and is the sum of the gate-source C_{GS} and the gate-drain capacitance C_{GD}:

$$C_{iss} = C_{GS} + C_{GD}$$

Equation 2 **Input capacitance at turn-on**

Due to the MOSFET's internal structure, C_{iss} is dominated by C_{GS}. So, for the same current at the gate, the MOSFET with the lower C_{GS} will have a faster di_D/dt, due to a faster charging of C_{GS}. To slow down the di_D/dt, a higher external gate resistor or external capacitor can be used.

C_{rss} and C_{oss} are the reverse transfer capacitance and output capacitance of the MOSFET respectively. These two capacitances are directly responsible for the drain-source voltage waveform. A more linear C_{rss} and C_{oss} will result in a smoother and more linear transition of $V_{DS.}$ Regarding linearity, OptiMOS™ 5 150 V and OptiMOS™ 6 150 V show a similar behavior as shown in Figure 10.

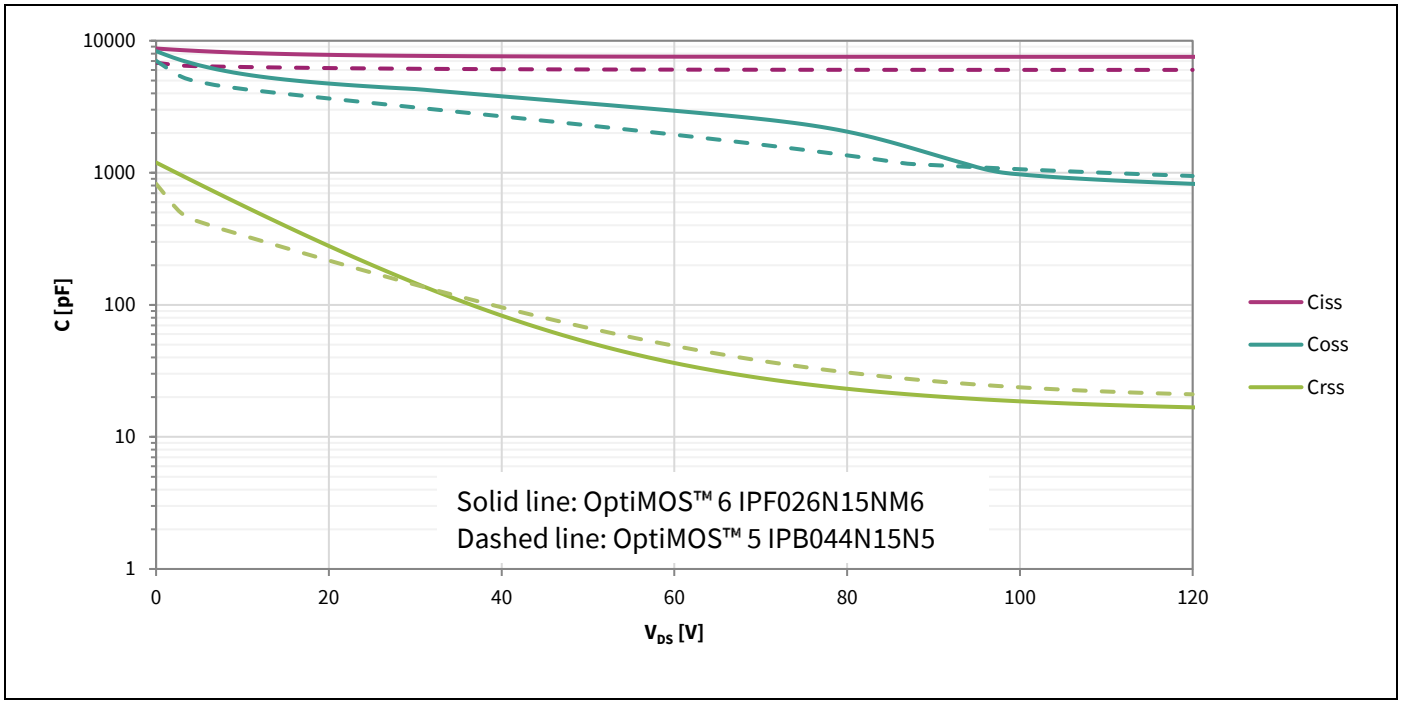

Figure 10 Capacitances of IPB044N15N5 and IPF026N15NM6

1.3.5 Gate charges

The latest OptiMOS™ 6 generation of MOSFETs boasts optimized FOMs, resulting in a low value of $R_{DS(on)} \times Q_g$. To achieve a lower $R_{DS(on)}$, the total gate charge Q_g is slightly increased from 80 nC for OptiMOS™ 5 to 105 nC for OptiMOS™ 6. The energy related to the charge and voltage of a capacitor is equal to:

$$E_C = \frac{1}{2} Q \cdot V$$

Equation 3 Energy related to a charge and a voltage of a capacitor

Thus, for OptiMOS™ 6 150 V MOSFET a slightly higher energy has to be applied to the gate to fully turn-on the MOSFET compared to OptiMOS™ 5 150 V generation.

For every switching period the energy related to Q_g has to be dissipated in the gate drive circuit. Thus, the power losses caused by the charge and discharge of the gate capacitance are:

$$P_{Qg} = \frac{1}{2} Q \cdot V \cdot f_{sw}$$

Equation 4 Energy related to a charge and a voltage of a capacitor

Switching frequencies f_{sw} for low-voltage, high-power motor drive applications are typically in the range of 8 to 20 kHz. With a typical switching frequency of 10 kHz, a gate drive voltage of 15 V, and the Q_g of the datasheets [4] [5] (OptiMOS™ 5: 80 nC; OptiMOS™ 6: 105 nC), the losses increase from 6 mW for OptiMOS™ 5 to 7.9 mW for OptiMOS™ 6. Compared to overall losses these gate driver losses are insignificant.

1.3.6 Thermal resistance junction-case R_{thJC}

Due to the state-of-the-art production process, the safety margin for $R_{thJC,max}$ can be reduced. Consequently, the new $R_{thJC,max}$ value provides a more realistic result for system design engineers. OptiMOS™ 6 shows a 24% lower typical R_{thJC} for a decreased $R_{DS(on)}$. Thus, OptiMOS™ 6 can handle a higher current than OptiMOS™ 5 without increasing the junction temperature (T_J) enabling higher power capability for the same system temperature.

For pulses whose duration is too short to reach a package thermal equilibrium, the behavior is described by the thermal impedance Z_{thJC}. In motor drive applications, short, high-current peaks are possible. For this reason as well Z_{thJC} is an important parameter for device selection. OptiMOS™ 6 shows a lower Z_{thJC} for all pulse durations as shown in Figure 11. The lower Z_{thJC} increases the pulsed current robustness and thus contributes to the system reliability.

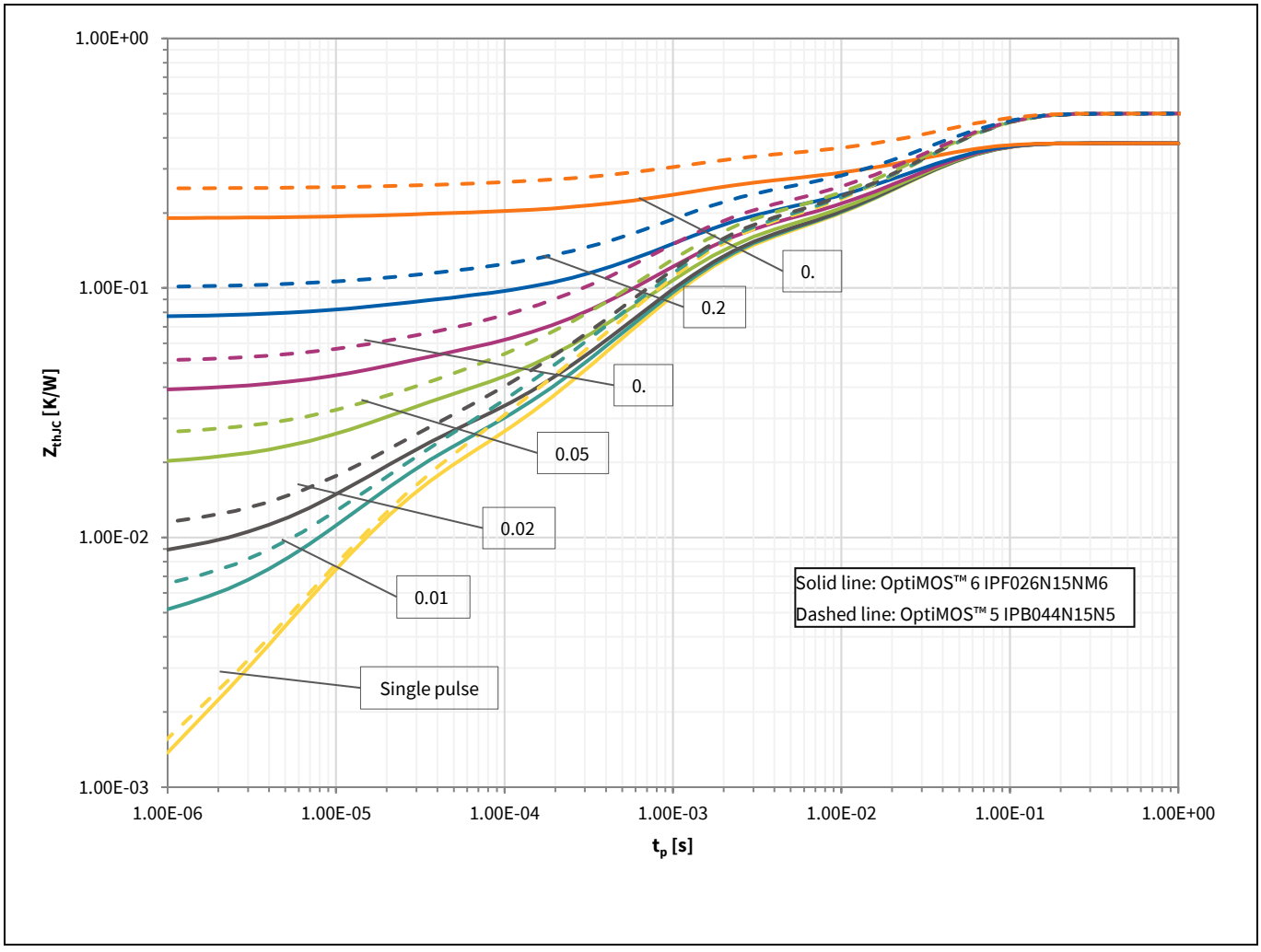

Figure 11 Thermal impedance Z_{thJC} of the device for OptiMOS™ 5 150 V and OptiMOS™ 6 150 V

1.3.7 Transconductance

OptiMOS™ 6 uses a new cell structure that shows a slightly higher transconductance. In general, lower transconductance is better for current sharing among parallel MOSFETs. At the test current of 87 A, OptiMOS™ 5 shows a transconductance value of 144 S whereas at a test current of 100 A OptiMOS™ 6 shows a value of 180 S as shown in Figure 12. In motor drives applications, the smaller difference in $V_{GS(th)}$ between paralleled

OptiMOS™ 6 devices will have more impact than a lower transconductance of OptiMOS™ 5. In summary, OptiMOS™ 6 will have better current sharing due to lower $\Delta V_{GS(th)}$ (1 V for OptiMOS™ 6 and 1.6 V for OptiMOS™ 5).

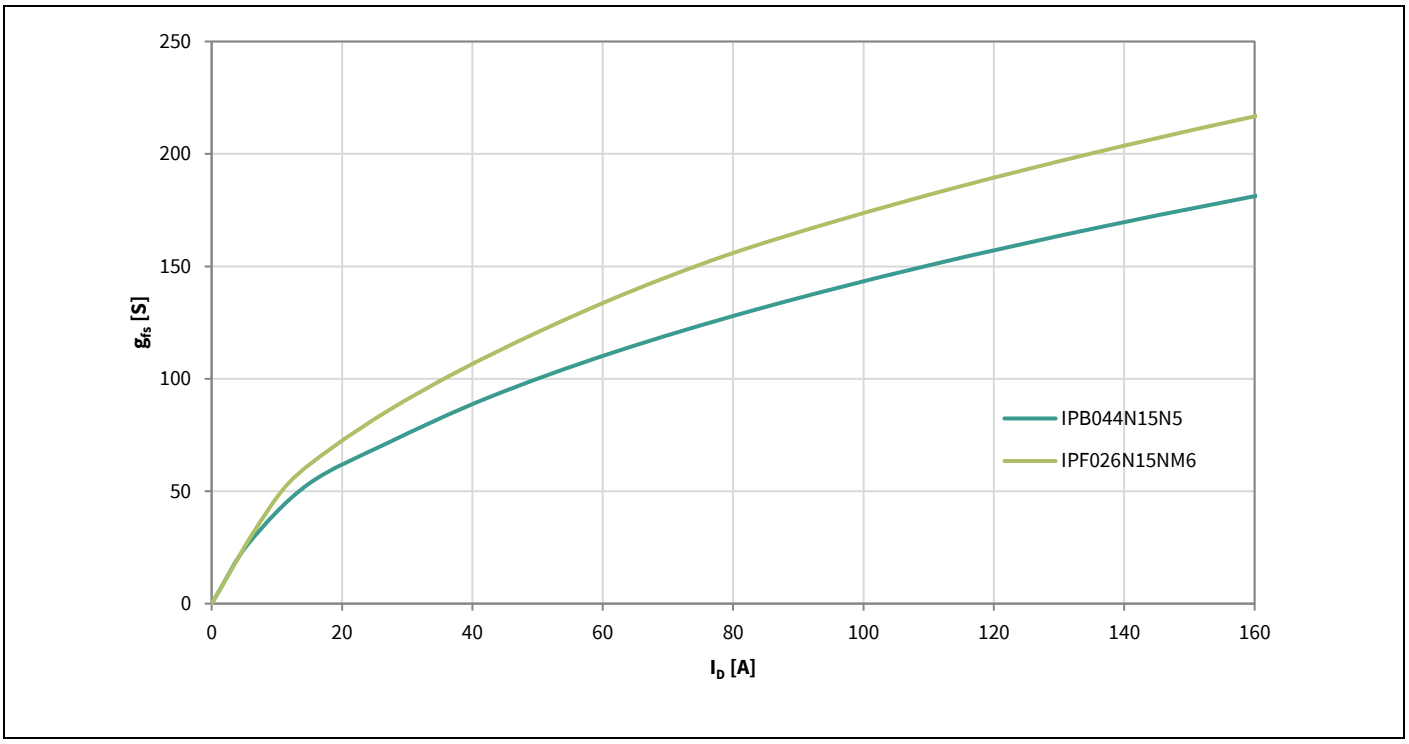

Figure 12 Typical transconductance of the device for OptiMOS™ 5 150 V and OptiMOS™ 6 150 V

1.3.8 Gate threshold $V_{GS(th)}$ and $\Delta V_{GS(th)}$ voltage

When the gate-source voltage reaches $V_{GS(th)}$ during turn-on transition, a drain current starts to flow. The gate threshold voltage in OptiMOS™ 6 is decreased to 3.5 V (typical) from 3.8 V for OptiMOS™ 5. The value for $V_{GS(th)}$ drops with increasing temperature as shown in Figure 13.

In applications with gate ringing due to a high dv_{DS}/dt, a lower $V_{GS(th)}$ can cause the MOSFET to turn-on unintentionally. Thus, a decreased $V_{GS(th)}$ can enhance the gate-source noise sensitivity. The lower threshold voltage of OptiMOS™ 6 is compensated by the lower induced voltage due to a better charge ratio C_{GD}/C_{GS} as shown in Figure 7. In addition, the typically used external C_{GS} will also improve the noise gate-source immunity.

The minimum to maximum value of $V_{GS(th)}$ of OptiMOS™ 6 has been reduced to 1 V versus OptiMOS™ 5 which has a $\Delta V_{gs(th)}$ of 1.6 V. This improvement is attributed to the technology improvements as well as the state-of-the-art manufacturing equipment and processes followed by Infineon.

In applications where MOSFETs need to be paralleled, the difference of $V_{GS(th)}$ values among paralleled MOSFETs is the most critical parameter for equal dynamic current sharing. OptiMOS™ 6 is a very good candidate for MOSFET paralleling due to the reduced $\Delta V_{gs(th)}$. For more details see [1].

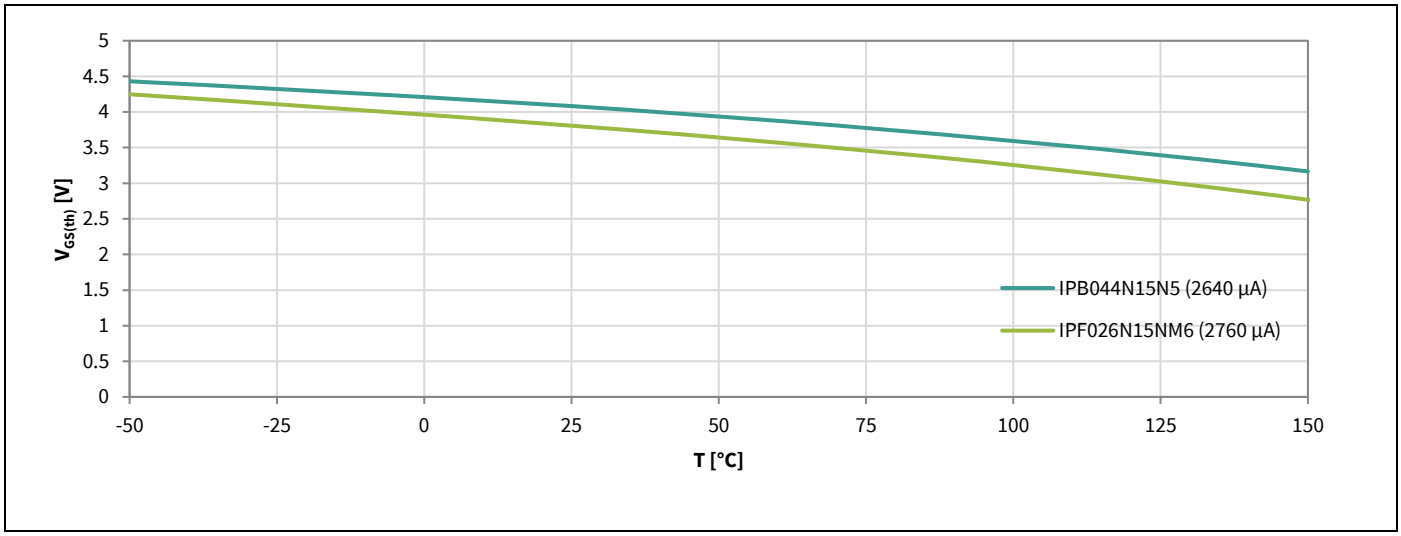

Figure 13 Gate threshold voltage $V_{GS(th)}$ of OptiMOS™ 5 150 V and OptiMOS™ 6 150 V

1.3.9 Avalanche characteristics

If VDS exceeds VDS,max, electric fields can occur inside the MOSFET that exceed the maximum permissible field strength and lead to a breakdown of the body diode through impact ionization. Electron-hole pairs created by the high field strengths undergo a multiplication effect and the MOSFETs enters the avalanche mode. In this operation mode, high currents pass though and high voltages occur across the MOSFET, simultaneously. The resulting losses and the high current can lead to degradation or even destruction of the MOSFET and so it should be ensured in the system design that the MOSFET does not enter the avalanche mode. Nevertheless, in motor applications, in the event of a fault, due to high currents and loop inductances, voltages can occur that exceed VDS,max causing the MOSFET body diode to break down. Therefore, a higher single pulse avalanche energy (EAS) contributes to improved system reliability. Some designers even use EAS as an indicator of the MOSFETs' short-circuit robustness. Compared to OptiMOS™ 5, the EAS for OptiMOS™ 6 is increased from 470 mJ at a 100 A pulse to 1012 mJ but at a 60 A pulse. In general, lower currents allow for higher avalanche energies for single pulse events. Thus, for a meaningful comparison, the MOSFETs have to be tested under identical conditions.

Figure 14 compares the maximum allowed avalanche current (I_{AV}) for the avalanche duration (t_{AV}) to not exceed the maximum junction temperature. As can be seen, OptiMOS™ 6 can withstand the same avalanche current for a longer duration, resulting in improved overall system reliability and robustness.

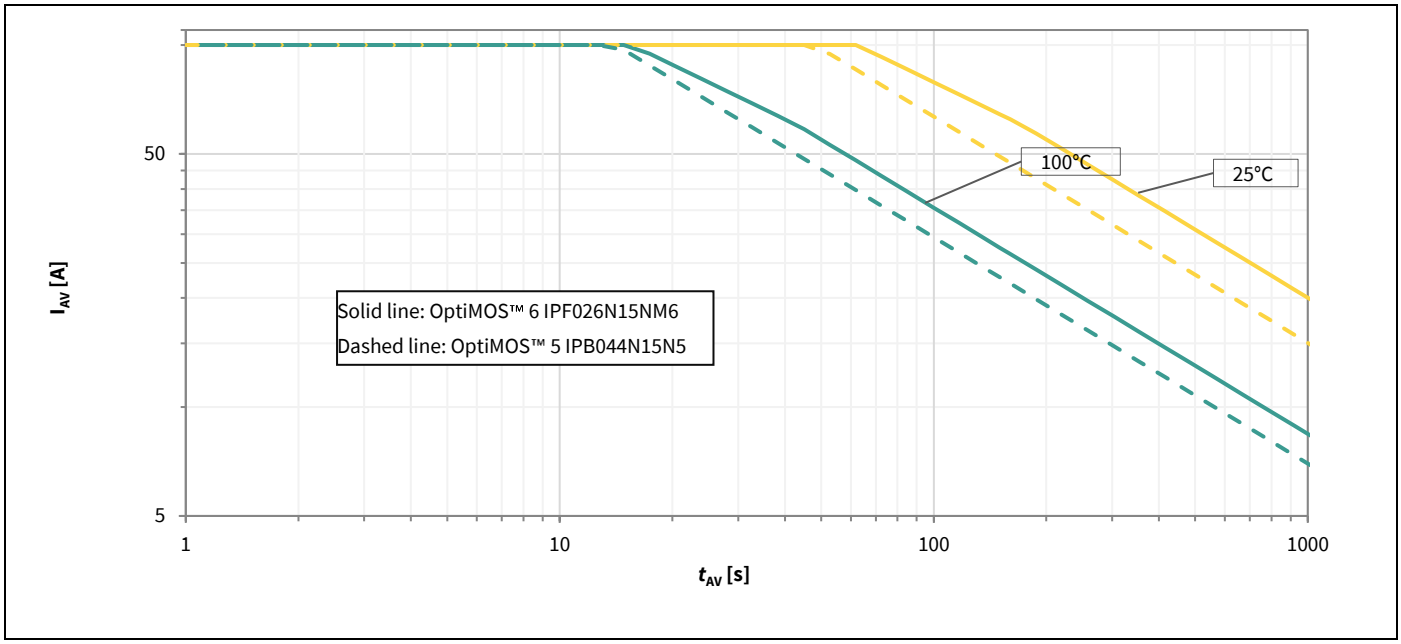

Figure 14 Avalanche characteristics of OptiMOS™ 5 150 V and OptiMOS™ 6 150 V

2 Experimental results

2.1 Bench test platform and conditions

For the bench test the inverters with the devices under test (DUTs) were loaded with an induction motor (IM) at the same inverter operating point (input voltage, duty cycle, switching frequency, and synchronous speed of the IM). The load torque of the motor was varied to match the heatsink temperatures at 100°C. The output current of the inverter represents the performance of the investigated MOSFETs. A render of the test platform used is shown in Figure 15.

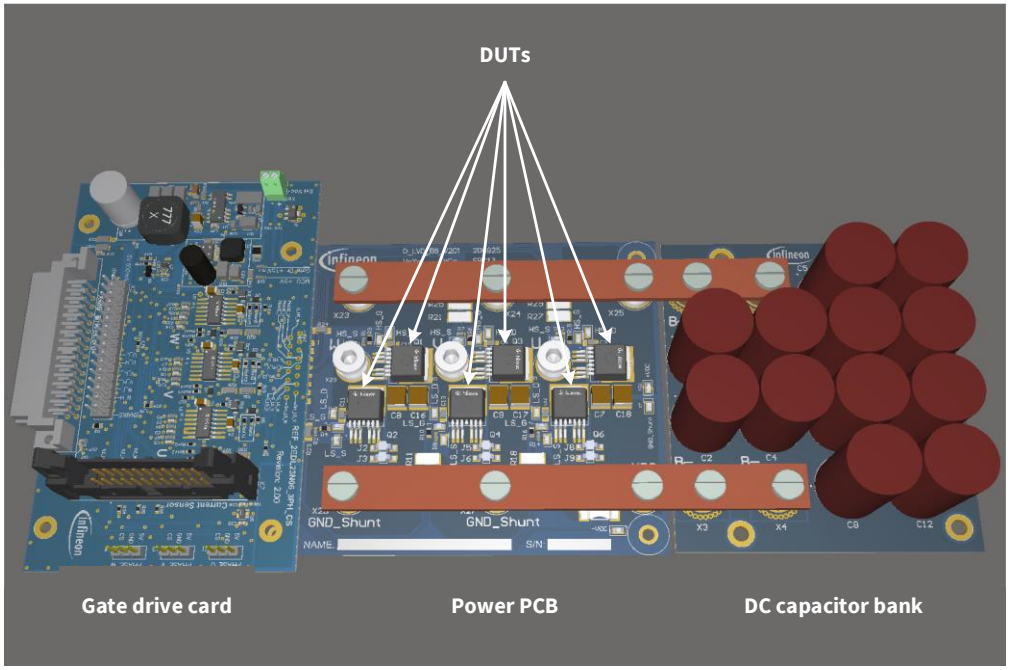

Figure 15 A render of the test platform

The following test conditions were applied.

- Topology: 3-phase inverter; 6 MOSFETs; single MOSFET per switch (no paralleling)
- PCB type: Single layer IMS with aluminum core
- DC bus voltage: 84 V
- Switching frequency: 10 kHz
- Modulation: Sinusoidal SVM
- Dead time (between high and low-side in a single half bridge): 700 ns
- Duty cycle: 38%
- Load varied to reach 100°C at the heatsink

2.2 Constant heatsink temperature test

The mechanical load of the IM is varied for the conditions above to match 100°C at the heatsink for a thermal steady state. The inverter output current is used as the performance characteristic.

2.2.1 Measurement results

The average of the measured $R_{DS(on)}$ for all six MOSFETs at 25°C is given in Table 2. With increasing temperature the $R_{DS(on)}$ value increases as well. $R_{DS(on)}$ is extrapolated to the appropriate T_J temperature according to the temperature coefficient given in the datasheet [4] [5] as shown in Figure 3. For a heatsink temperature of 100°C the $R_{DS(on)}$ increases from 3.10 mΩ to 5.16 mΩ for OptiMOS™ 5 IPB044N15N5 and from 2.14 mΩ to 3.49 mΩ for OptiMOS™ 6 IPF026N15NM6 respectively, see Table 2.

Comparing the output current for a heatsink temperature of 100°C for OptiMOS™ 5 and OptiMOS™ 6 reveals a current increase of about 11.9% for OptiMOS™ 6.

Table 2 Measurement results

	25°C	100°C				
	$R_{DS(on)}$	T_{max}	T_{av}	$R_{DS(on)}$	I	ΔI
	mΩ	°C	°C	mΩ	A	%
OptiMOS™ 5 IPB044N15N5	3.29	106.1	104.7	5.16	52.9	Reference
OptiMOS™ 6 IPF026N15NM6	2.14	108.0	106.1	3.49	59.15	11.9

2.2.2 Static (conduction) losses

For motor drive applications with a rather low switching frequency the MOSFETs' losses are usually dominated by conduction losses. These losses can be determined easily with the $R_{DS(on)}$ and the RMS value of the inverter output current.

$$P_{con} = R_{DS(on)} I_{rms}^2$$

Equation 5 Conduction losses

For 100°C, at the heatsink, the extrapolated $R_{DS(on)}$ and the measured inverter output currents of Table 2 are used. This results in 43.31 W conduction losses for all six MOSFETs of the inverter for IPB044N15N5 and 36.58 W conduction losses for IPF026N15NM6 at a heatsink temperature of 100°C, as shown in Table 3.

Table 3 Conduction losses

	100°C
	P_{con}
	W
OptiMOS™ 5 IPB044N15N5	43.31
OptiMOS™ 6 IPF026N15NM6	36.58

2.2.3 Dynamic (switching) losses

For hard switching topologies, like the inverter used in the test platform, high voltages and currents occur simultaneously at the power switches. The MOSFETs should be robust enough to handle these high-power peaks. As opposed to conduction losses, the switching losses are much more difficult to predict and should be measured.

Figure 16 shows the V_{DS}, I_D, and P_{sw} waveforms of the high-side switch for a turn-on event of the half-bridge and a positive output current of 100 A. When comparing OptiMOS™ 5 and OptiMOS™ 6, it can be concluded that the switching energy to turn on OptiMOS™ 6 is slightly higher, indicated by the area under the power curve.

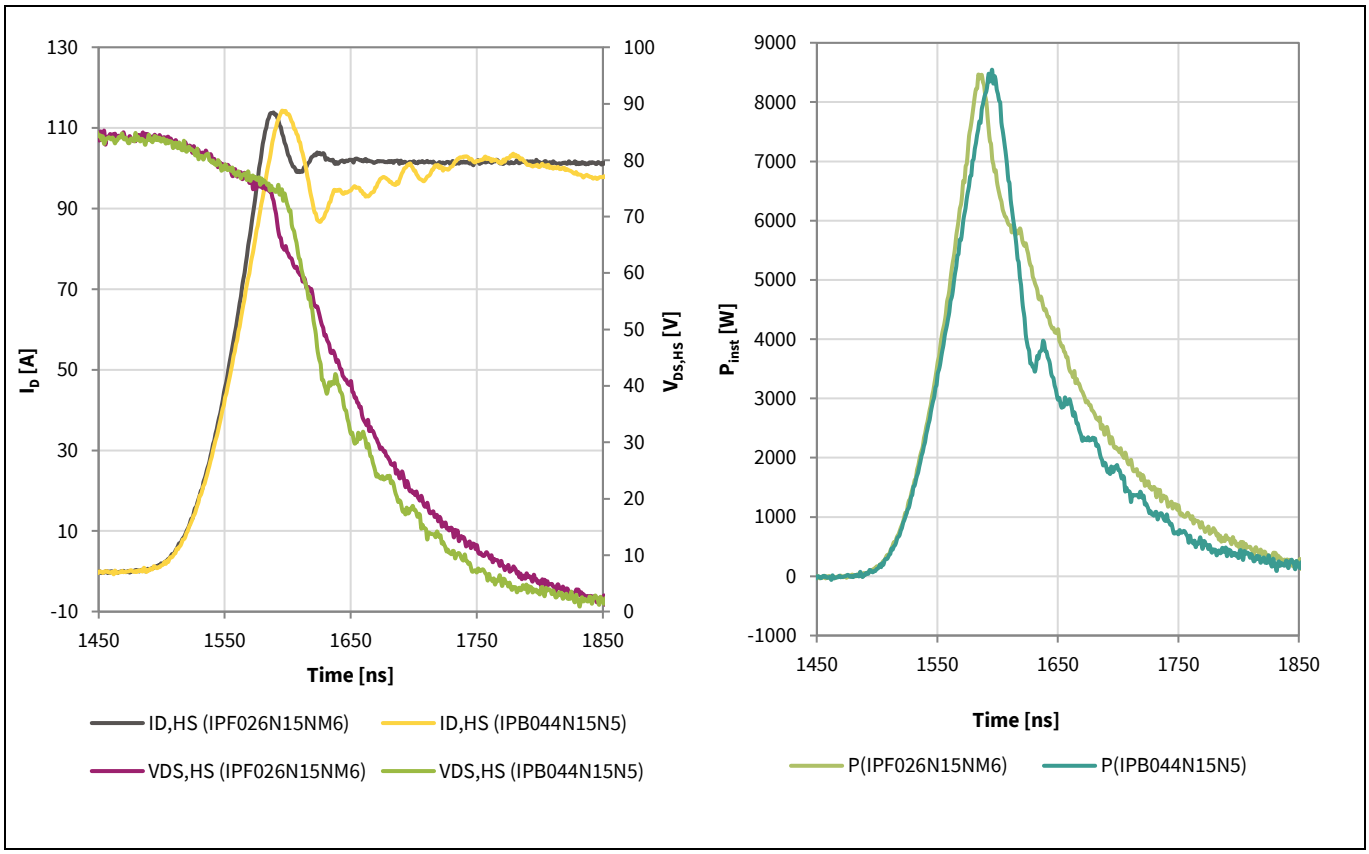

Figure 16 Turn-on waveforms of OptiMOS™ 5 and OptiMOS™ 6 at I_D = 100 A; drain-source voltage and drain current (left) and instantaneous power (right)

Figure 17 shows similar waveforms as Figure 16 for a turn-off event of the half bridge. OptiMOS™ 6 shows a faster decay of I_D current resulting in lower turn-off losses.

Experimental results

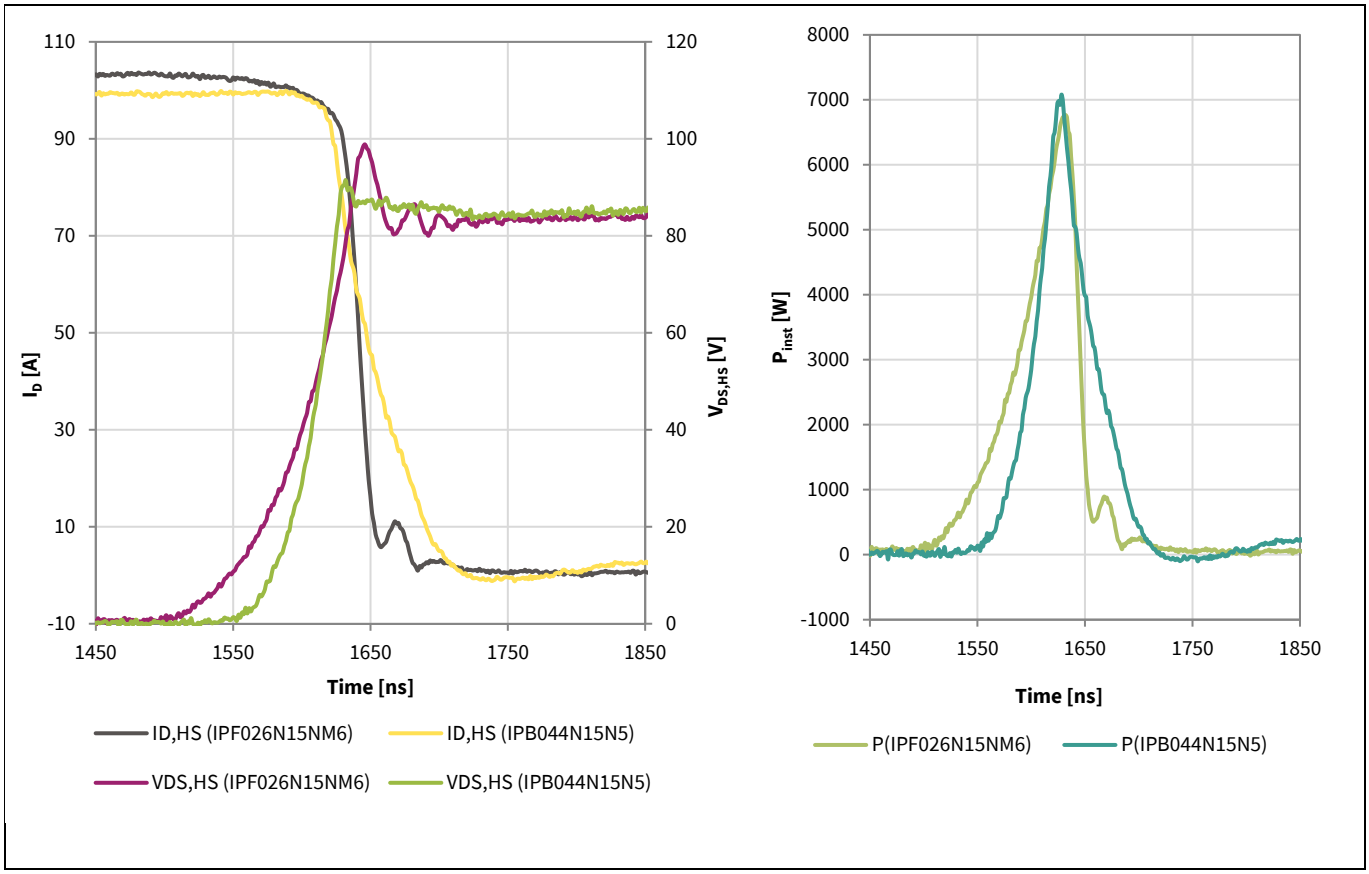

Figure 17 Turn-off waveforms of OptiMOS™ 5 and OptiMOS™ 6 at I_D = 100 A; drain-source voltage and drain current (left) and instantaneous power (right)

Table 4 summarizes the switching loss values for a matched dv/dt of 0.3 V/ns at the high-side MOSFETs and an output current of 100 A.

Table 4 Switching energies for the investigated MOSFETs at I_D = 100 A

	Turn-on energy (84 V and 100 A)	Turn-off energy (84 V and 100 A)	Total switching energy	
	µJ	µJ	µJ	%
OptiMOS™ 5 IPB044N15N5	778	407	1185	Reference
OptiMOS™ 6 IPF026N15NM6	837	361	1198	+1.2

With a difference of only 1%, both MOSFETs show very similar switching losses. With the circuitry that is typically used in motor drives, the dv/dt and di/dt values can be adjusted for OptiMOS™ 6, thereby affecting the switching losses as well.

2.2.3.1 Total switching losses

The switching losses are a function of I_D. During one electrical period (T_{el}) of the IM I_D changes constantly, and so do the switching losses. To determine the total switching losses of the MOSFETs for a given phase current double-pulse tests for 10 A, 25 A, 50 A, 75 A, and 100 A were performed and the switching losses for the individual currents calculated.

Experimental results

The switching frequency ($T_{PWM} = 1/f_{PWM}$) defines the time between two turn-on events and therefore the position of the n^{th} switching event within the phase current waveform is defined. The amplitude of the drain current for the n^{th} switching event is given by

$$\hat{I}_D(n) = \sqrt{2} I_{rms} \, sin\left(\frac{2\pi}{n_{max}} n\right)$$

Where n_{max} is defined by the ratio of the electrical frequency (T_{el}) and the switching period (T_{PWM})

$$n_{max} = \frac{T_{el}}{T_{PWM}}$$

Equation 6 Amplitude of the drain current of the n^{th} switching event

The switching losses (E_{sw}) for every single switching event are estimated by means of a quadratic interpolation of the measured switching losses. It is obtained by dividing the sum of the switching losses for a whole period of the drain current by T_{el}.

$$P_{sw} = \frac{\sum_n^{nmax} E_{sw,n}}{T_{el}}$$

Equation 7 Switching losses for the n^{th} switching event

At an output current of 52.9 A, OptiMOS™ 5 shows 15.5 W switching losses. With OptiMOS™ 6 the switching losses are 18.8 W but at an increased current of 59.15 A.

Table 5 Total switching losses for the investigated MOSFETs at 100°C

	100°C
	P_{sw}
	W
OptiMOS™ 5 IPB044N15N5	15.5 W at 52.9 A
OptiMOS™ 6 IPF026N15NM6	18.8 W at 59.15 A

2.2.4 Total losses

Figure 18 shows the comparison of OptiMOS™ 5 and OptiMOS™ 6 conduction and switching losses for a heatsink temperature of 100°C. Compared to OptiMOS™ 5, OptiMOS™ 6 allows for a 11.9% increase in inverter output current while maintaining the same heatsink temperature, and higher efficiency see Figure 18.

Experimental results

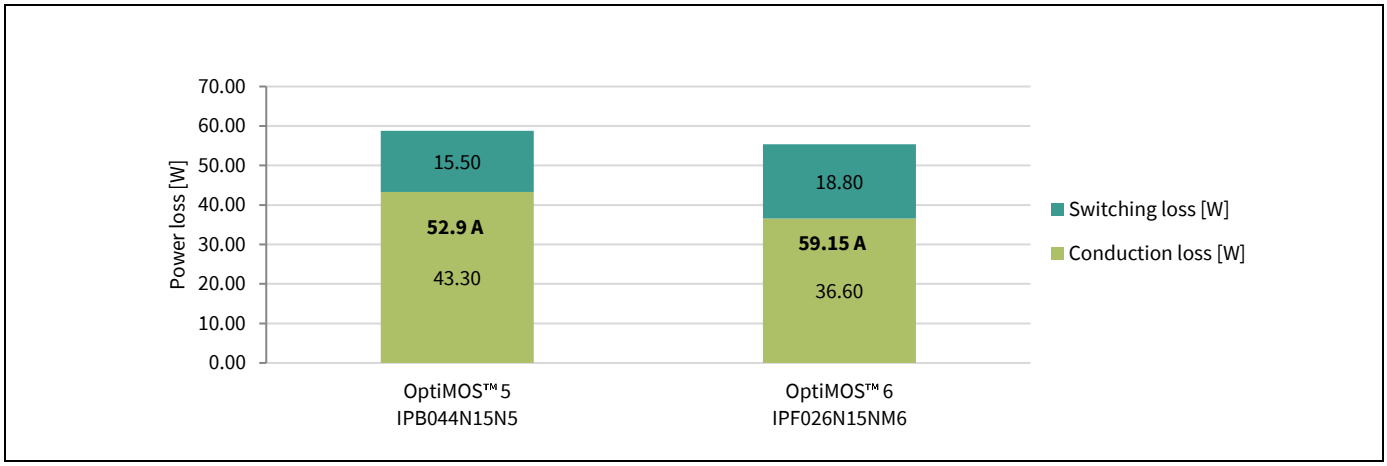

Figure 18 Comparison of the switching and conduction losses of OptiMOS™ 5 and OptiMOS™ 6 for a heatsink temperature of 100°C

As indicated in Equation 6 and Equation 7,the switching losses increase with increasing current. This increase in switching losses limits the inverter's output current increase to a value that is lower than the one expected due to $R_{DS(on)}$ decrease.

2.3 Peak power

So far, the MOSFETs only have been compared in a thermal steady-state condition. However, for LEVs and motor drives in general, the peak power of the inverter is also an important performance parameter. Accelerating or going uphill are typical examples of peak power events. During a peak power or overload event, much higher losses than in the steady state are dissipated in the MOSFET. Consequently, the MOSFET will heat up further, and the duration of this event has to be limited to avoid MOSFET overstress. The allowed peak power duration depends on the system's thermal impedance, the starting conditions, and the losses dissipated in the MOSFET.

Figure 19 compares the peak power capability of the two investigated MOSFETs, independent of the thermal system's performance. As for the thermal steady-state test, the dv/dt at the high-side FETs for a turn-on event was matched to 0.3 V/ns, and the di/dt ranges from 460 A/µs for the 10 A pulse up to 1600 A/µs for the 150 A pulse. The graph provides the losses of all six MOSFETs of the inverter for a given overload current. Thus, it could be either used to estimate the pulse duration by reading the MOSFET losses for a given current and thermal system performance or to determine the overload current for the allowed MOSFET losses.

Experimental results

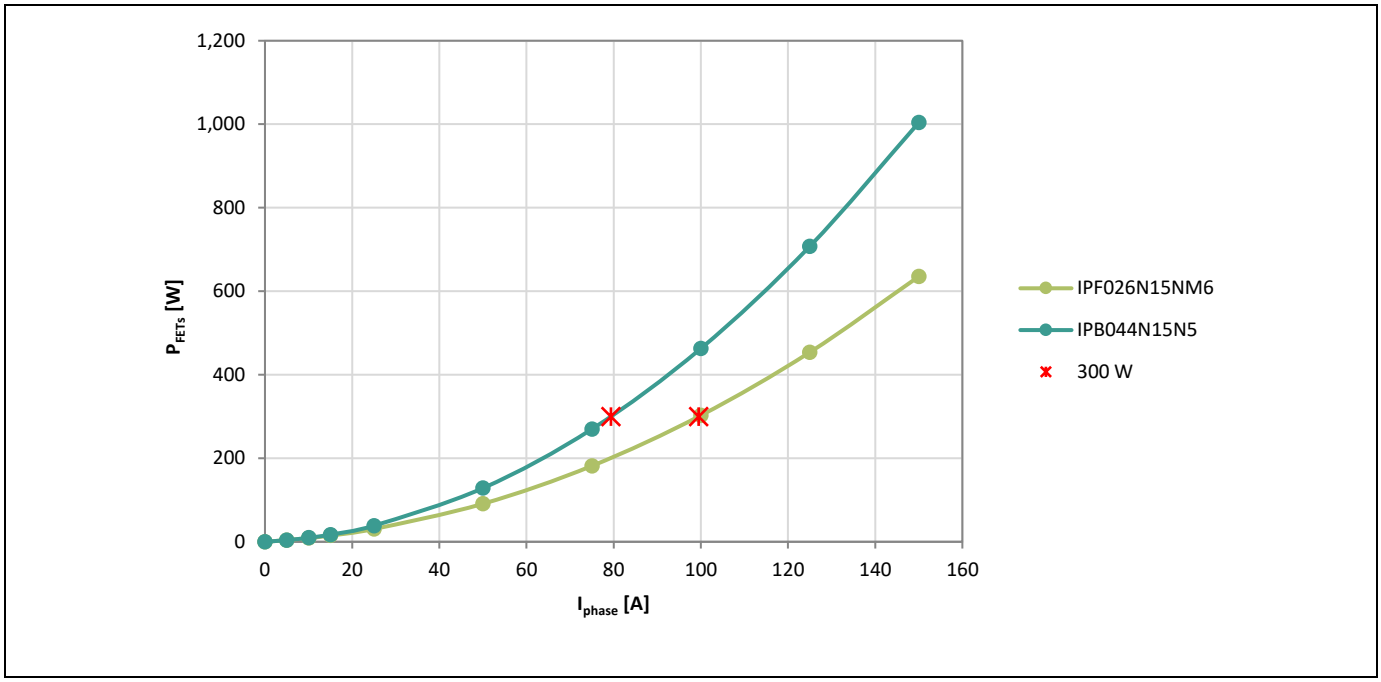

Figure 19 Losses of all six MOSFETs of the inverter as a function of the output current

Comparing the overload current for both MOSFETs at losses of 300 W reveals an increase of the phase current for OptiMOS™ 6 of almost 22 A or 27% compared to OptiMOS™ 5.

Table 6 Peak power currents at 50 W MOSFET losses

	I_{phase}	ΔI
	A	%
OptiMOS™ 5 IPB044N15N5	80.2	Reference
OptiMOS™ 6 IPF026N15NM6	101.9	27

3 Conclusion

This application note introduces the OptiMOS™ 6 150 V family of MOSFETs. The new technology is a result of more than twenty years of Infineon's experience in advanced trench MOSFET design. It comes with a redesigned MOSFET cell, showcasing the industry's best $R_{DS(on)}$. Furthermore, parameters most relevant to motor drives show improvements in the latest OptiMOS™ 6 150 V technology. Of particular importance is the reduction in the on-state resistance. A narrow gate threshold voltage spread optimizes the paralleling of OptiMOS™ 6 150 V devices [1]. Together with the soft diode behavior, the low reverse recovery charge, and the increased avalanche robustness, OptiMOS™ 6 150 V enhances the system efficiency and reliability across all operating conditions, and reduces EMI when compared with the previous OptiMOS™ 5 technology.

Moving to the OptiMOS™ 6 from its predecessor allows for a 27% higher phase current in a peak power event where MOSFET losses are around 300 W as shown in Figure 19.

Ultimately, OptiMOS™ 6 150 V allows for a system cost reduction without compromising reliability or performance and is available in a large portfolio comprising a wide range of $R_{DS(on)}$ as well as a variety of packages. This provides flexibility in new designs and enables increased performance in existing designs, where it can be employed as a drop-in replacement with higher efficiency and system level cost reduction.

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