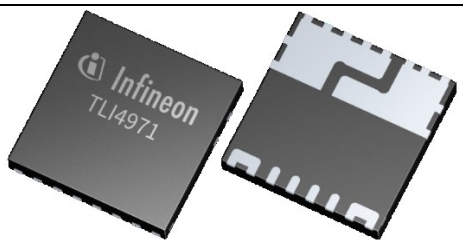
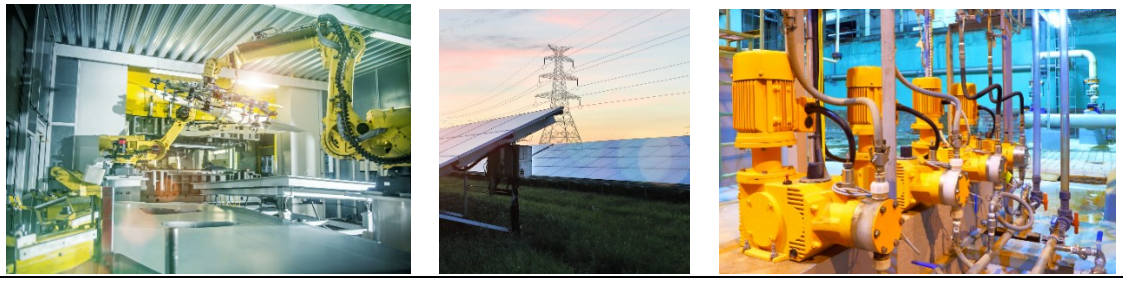
Current Sensor TLI4971

Solder and PCB recommendation and thermal management guideline



Infineon Core less Current Sensor for high voltage industry applications



About this document

Scope and purpose

The printed circuit board (PCB) layout and soldering are important recommendations for the sensor to achieve better thermal and accuracy performance. In order to have less resistance due to solder joints, this document gives a recommendation for the stencil and refers the Infineon assembly recommendation for PG-TISON-8 packages [1]. This document shows a possible and proper setup of a current sensing application board by using the Infineon leadless current sensor (TLI4971). In addition, it provides the recommendations for mounting the TLI4971 in the PCB to measure the primary current for better performance and accuracy. The following key aspects been discussed:

- Assembling instructions of the sensor on a reference PCB
- Ideal and non-ideal layout guidelines
- Stray field cancellation
- TLI4971 package
- Reference PCB dimensions and the layer stack up recommendations.
- Thermal management of the sensor for the following PCBs
  - For reference PCB
  - For electric drive system.

Intended audience

- TLI4971 current sensor users.
- Current Sensor Module Designer.

Table of contents

1 Introduction

The TLI4971 is an open loop lead less Hall based current sensor in a small Quad flat No Leads (QFN) package of size 8x8x1 mm (see Figure 3).

1.1 Footprint

The Figure 1 shows the top and bottom view of the sensor package. The bottom view and the footprint of the package shows (see Figure 2) the double L – shape which has designed for achieving the maximum sensitivity by a minimum power loss due to the low insertion resistance.

During the primary current measurement, the current flows from the current trace on the PCB into the L-shape pads of the device package. Therefore, a PCB layout recommendation has described in this document to achieve good sensitivity from the input current to output voltage.

The big exposed pads of the device gives a good thermal connection from the internal current rail to the solder and then to PCB. This fact enables a stable and good temperature behavior in the system by providing a proper Cooling methodology.

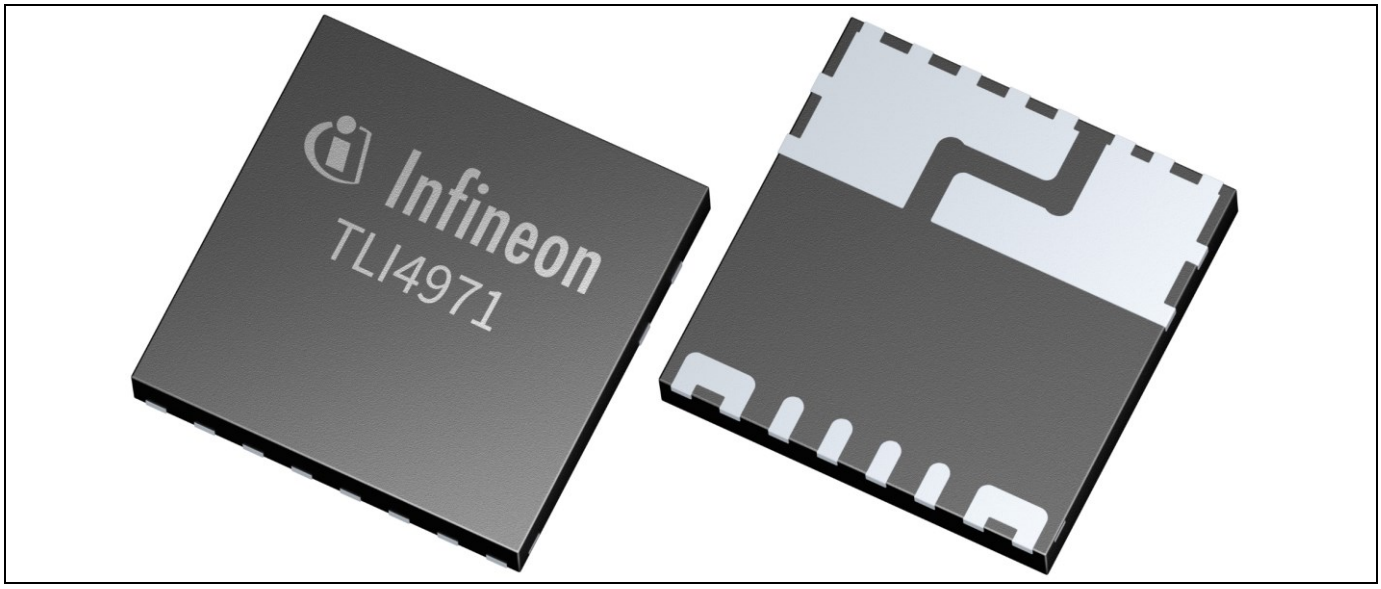


Figure 1 TLI4971 TISON-8 Package Top and Bottom View

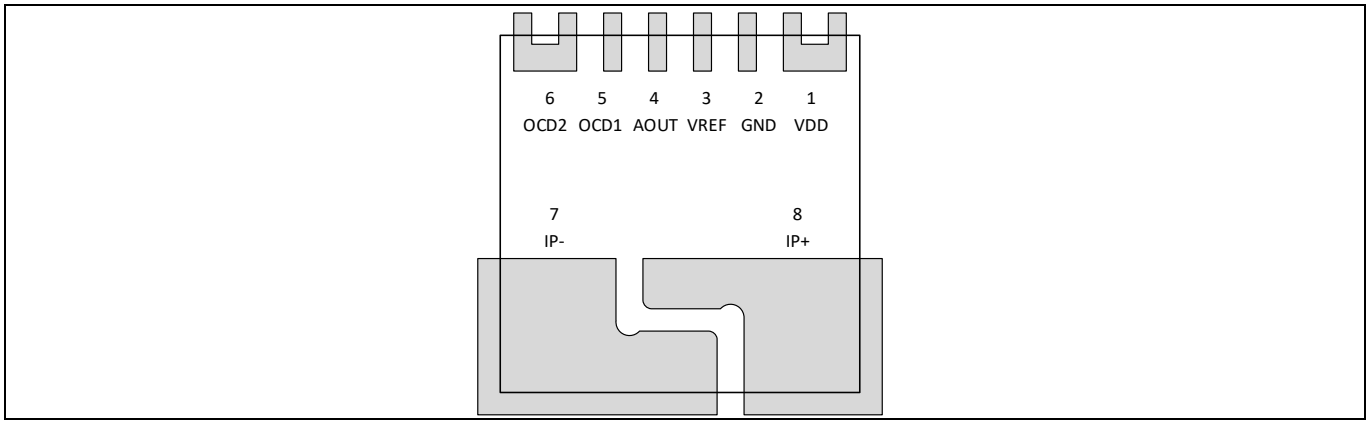


Figure 2 TLI4971 Footprint with Pin Naming

Figure 3 shows the footprint dimensions. The package outlines are 8 x 8 x 1 mm. The further details of the package dimensions has shown in Figure 4.

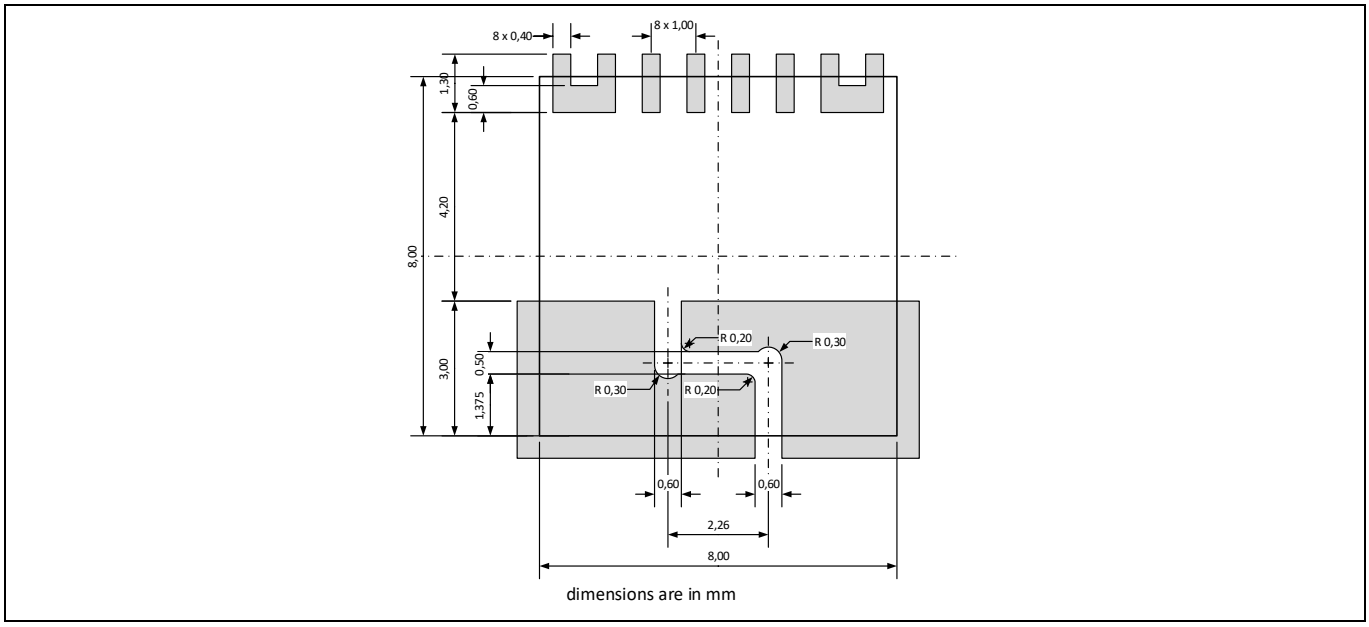


Figure 3 TLI4971 Footprint with Dimensions

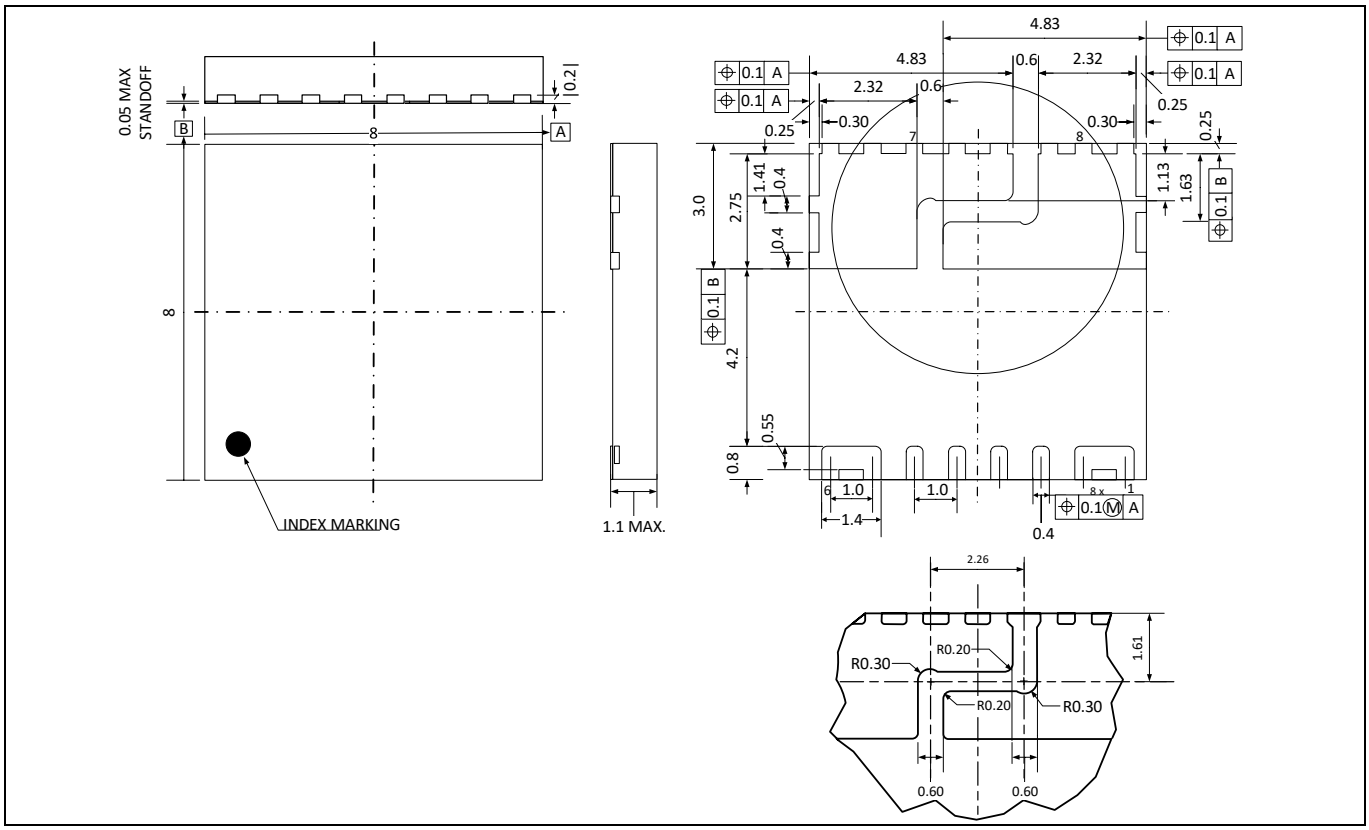


Figure 4 TLI4971 Package Outline

1.2 Solder Stencil

To have a homogenous solder connection between the current rail and the PCB, i.e. to reduce the solder voids, a defined stencil has recommended as shown in the Figure 6. The small SMD package supports state of the art PCB assembling processes. The soldering methodology illustrates an important parameter to achieve the good accuracy and thermal performance.

- The recommended stencil thickness is a 120um, laser cut, and brushed stainless steel. Figure 5 shows the recommended stencil dimensions.
- The recommended solder type is INDIUM 8.9 HF SAC305 Typ-4.
- As surface finish recommendation, use LEAD FREE HASL or chemical tin (do not use ferromagnetic materials like nickel to avoid hysteresis effects)
- For further details, please refer the PG-TISON-8-X packages document [1]

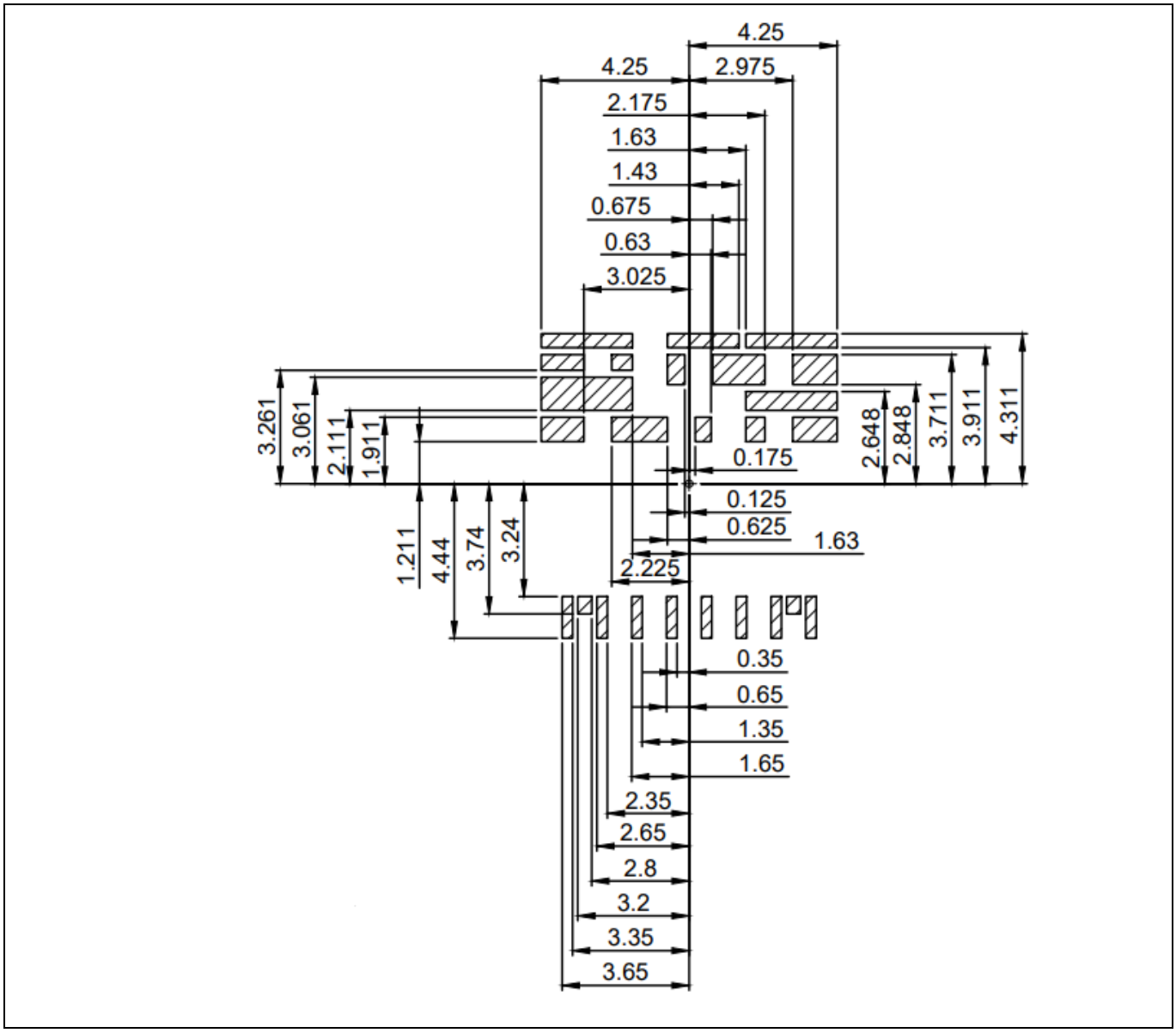


Figure 5 Stencil with Dimensions (all dimensions are in mm)

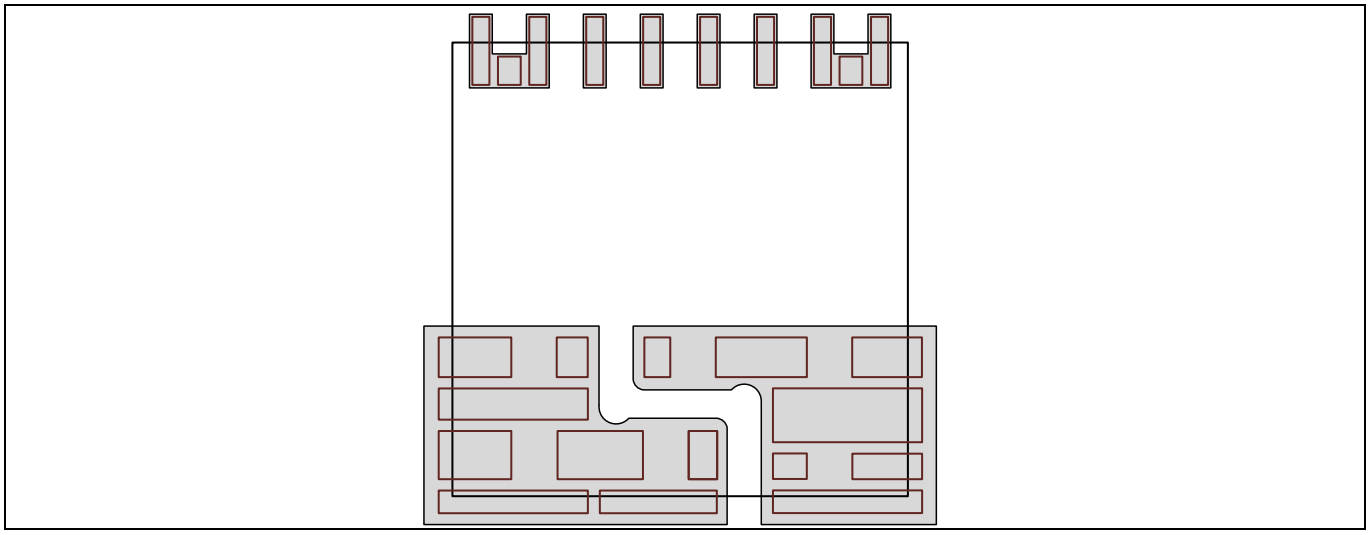


Figure 6 Stencil on TLI4971 Footprint

1.3 Layout Recommendations

The sensor measures the primary current by measuring the differential magnetic field, which makes the sensor very robust against stray fields without any need of shielding. Figure 7 shows the position of the differential Hall elements. As the TLI4971 sensor has used to measure the high current up to 120Apk in high voltage applications with different sensitivity levels, refer the datasheet [2] for further information, a proper layout is necessary to achieve better thermal performance.

In addition to the analog output, the sensor provides a second independent path for a fast over current detection (OCD) signals. A proper guarding method has discussed in the following sections to avoid the cross talk between the signals.

Due to the small 8x8 mm QFN package the sensor fits into all the designs, which has size restrictions. The device has inherent functional isolation with a clearance and creepage distance of 4mm between the HV current rail and the LV signal pins, which allows the use in high voltage applications.

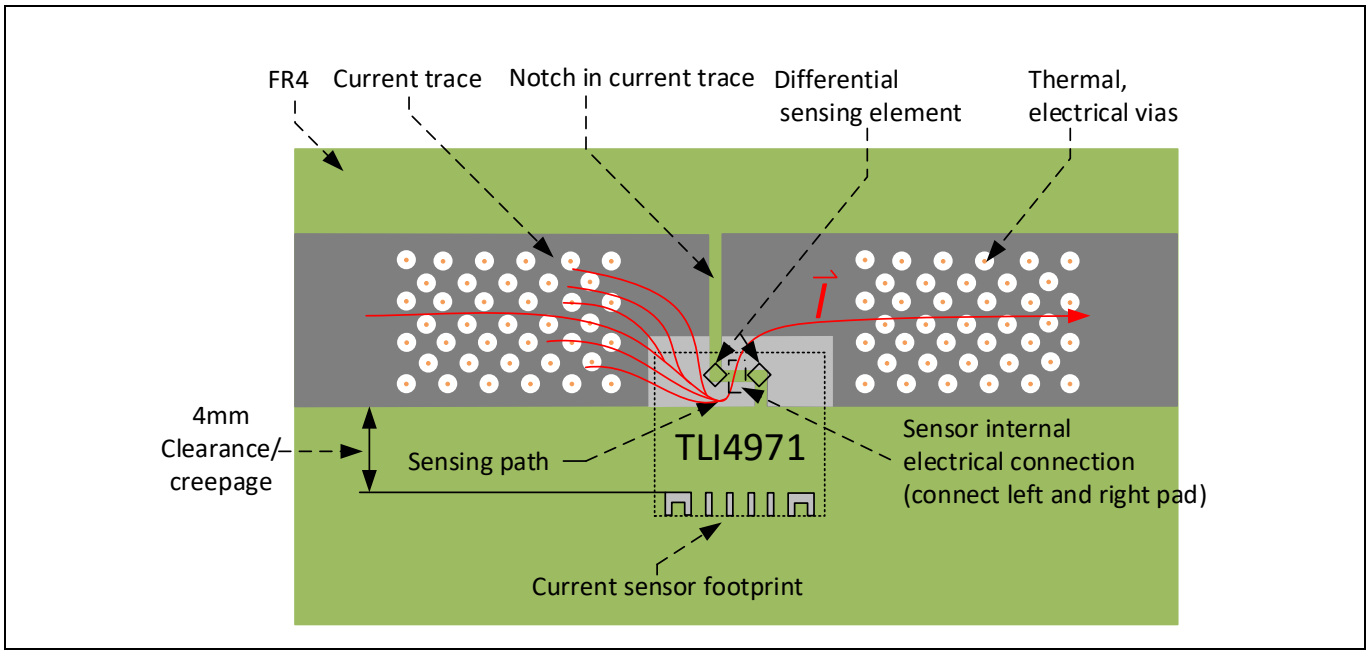


Figure 7 TLI4971 Layout Example and Sensing Principle

The Figure 7 shows a recommended placement of TLI4971 on a PCB to measure the current. Connect the two exposed pads (IP+ and IP-) to the current traces on the PCB such that the two sharp edges of the cut in the PCB current traces align to the senor's hall elements as shown in Figure 7.

There shall be a cut in the PCB current traces in order to force the current to flow through the sensor internal current rail from IP+ to the IP- terminals. Do not bypass the sensor since the current shall flow through the sensor to measure the current.

The Figure 8 shows ideal layout guidelines and the block out area where the LV signals have traced through this area and avoid placing any power traces through the block out area.

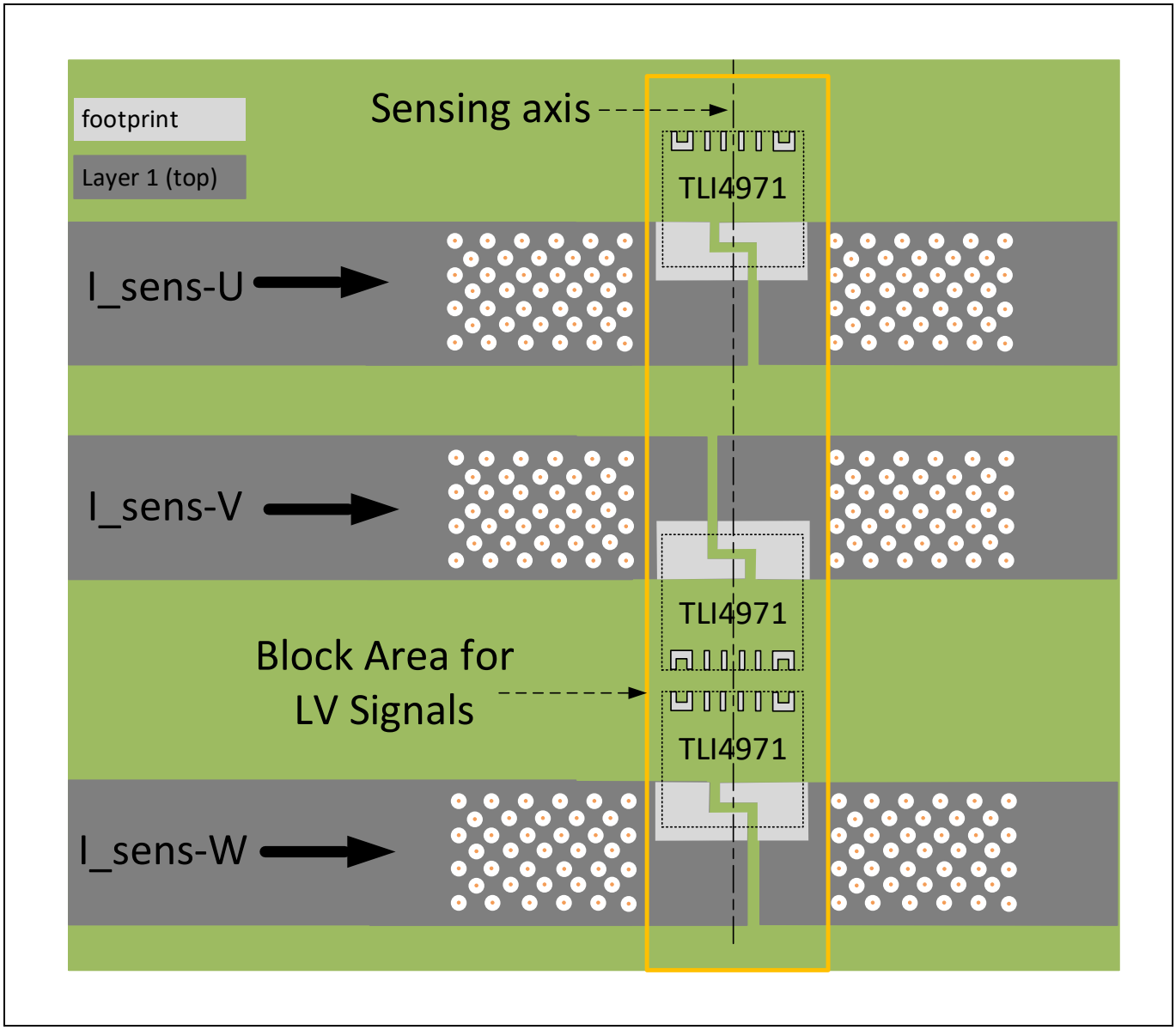


Figure 8 Ideal Layout Guidelines

The Figure 9 shows the non-ideal layout guidelines for the PCB design as the stray field from the perpendicular current (I_error) carrying conductor to the I_sens-U, I_sens-V and I_sensW carrying conductor where the TLI4971 has placed, which is parallel to the sensing axis as shown in Figure 9, causes an extra error in the sensor output. Please refer the section 1.7 for further information. In the below figure, the current traces of I_sens-U, I_sens-V and I_sens-W have traced through the layer 1 which are perpendicular to I_error current trace in layer2.

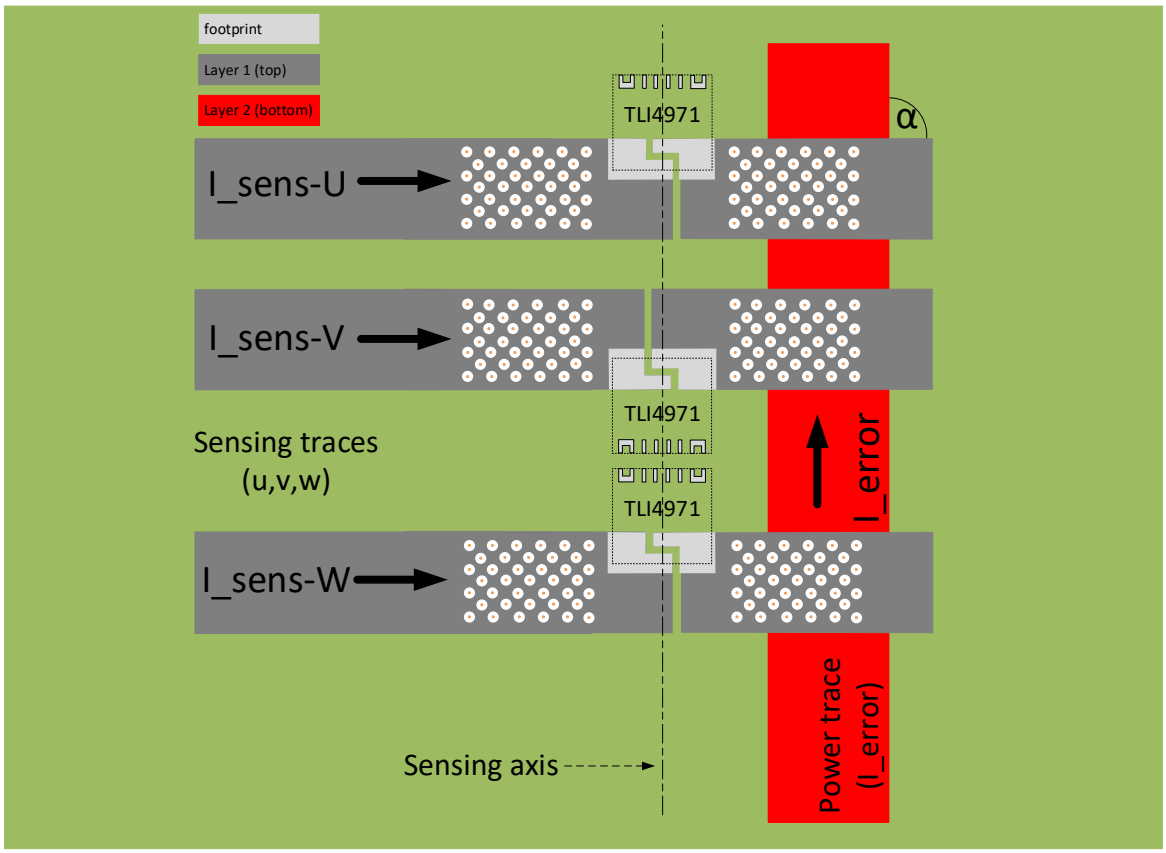


Figure 9 Non-Ideal Layout Guidelines (Refer to Angel Alpha)

The Figure 10 shows another non-ideal layout guideline for the PCB design as the stray field from the perpendicular current, which is parallel to the sensing axis as shown in below figure, causes an extra error in the sensor output. Please refer the section 1.7 for further information.

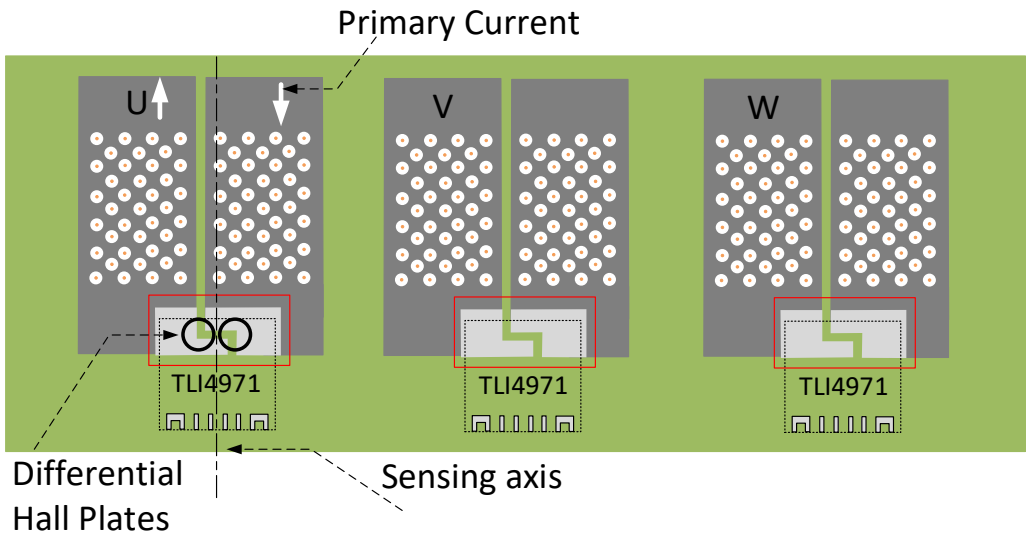


Figure 10 Non-Ideal Layout Guidelines2

1.4 Thermal Recommendations

For better thermal management, place thermal vias in the PCB current traces close to the sensor's footprint as shown in Figure 11. The maximum current capability has limited by the temperature rise of the sensor. The temperature at the sensor solder joint should not exceed the maximum allowed temperature of 105°C. In addition, it has not recommended having higher temperatures when using FR4 material. For high current applications, it has recommended to connect the device with an external heat sink. Furthermore, an increase of the current trace width helps to increase the thermal mass as well as the thermal conductivity to the heat sink as shown in Figure 11.

Incase if the current trace width is more, it has recommended to place a notch in parallel to the current trace path as shown in Figure 11. By placing this cut, the current path respectively the current density in the sensing path do not change when compared with the layout shown in Figure 7 and Figure 11. This cut is necessary as the current direction entering through the device plays an important role in sensitivity variations. It always recommended, allowing the current through the device from the left and right sides of the pads instead of the top and bottom of the pads, when you look at the Figure 11, to achieve higher sensitivity.

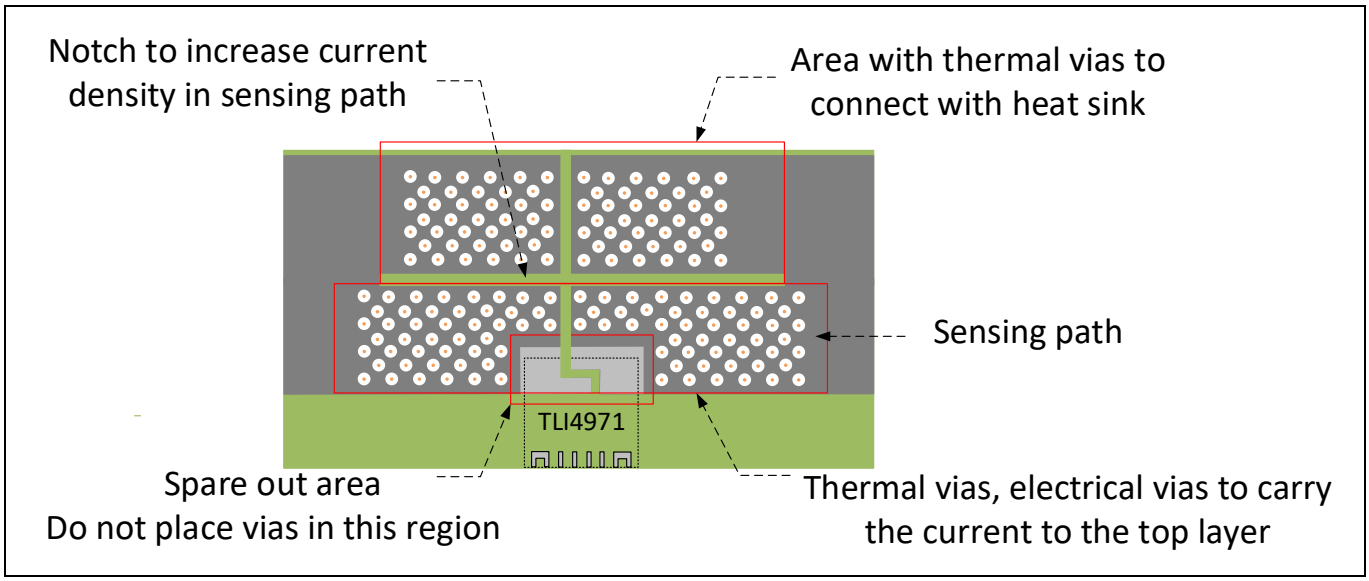


Figure 11 TLI4971 Layout Recommendation for Thermal Performance

1.5 Layout Optimization

The Figure 12 shows the two different topologies for comparison to optimize the PCB size used for the current sensor placement. The total space required for the current sensor on the PCB is less for Topology 2 (below picture of Figure 12) compared to Topology 1 (top picture of Figure 12). If we assume that the HV current trace width is X (mm) for each phase, then the minimum 4mm reduced irrespective of the space required for the other LV traces of the current sensor.

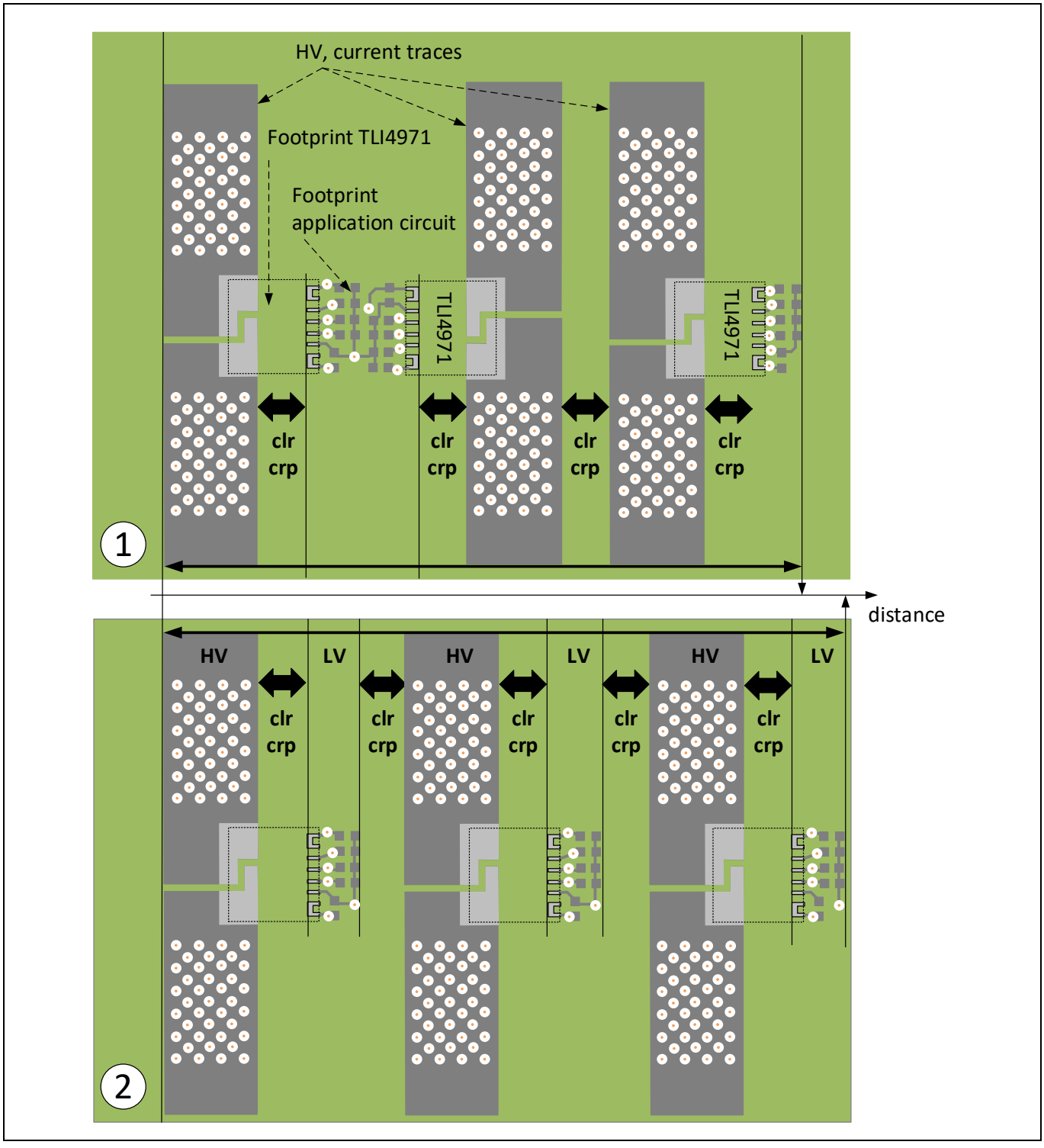
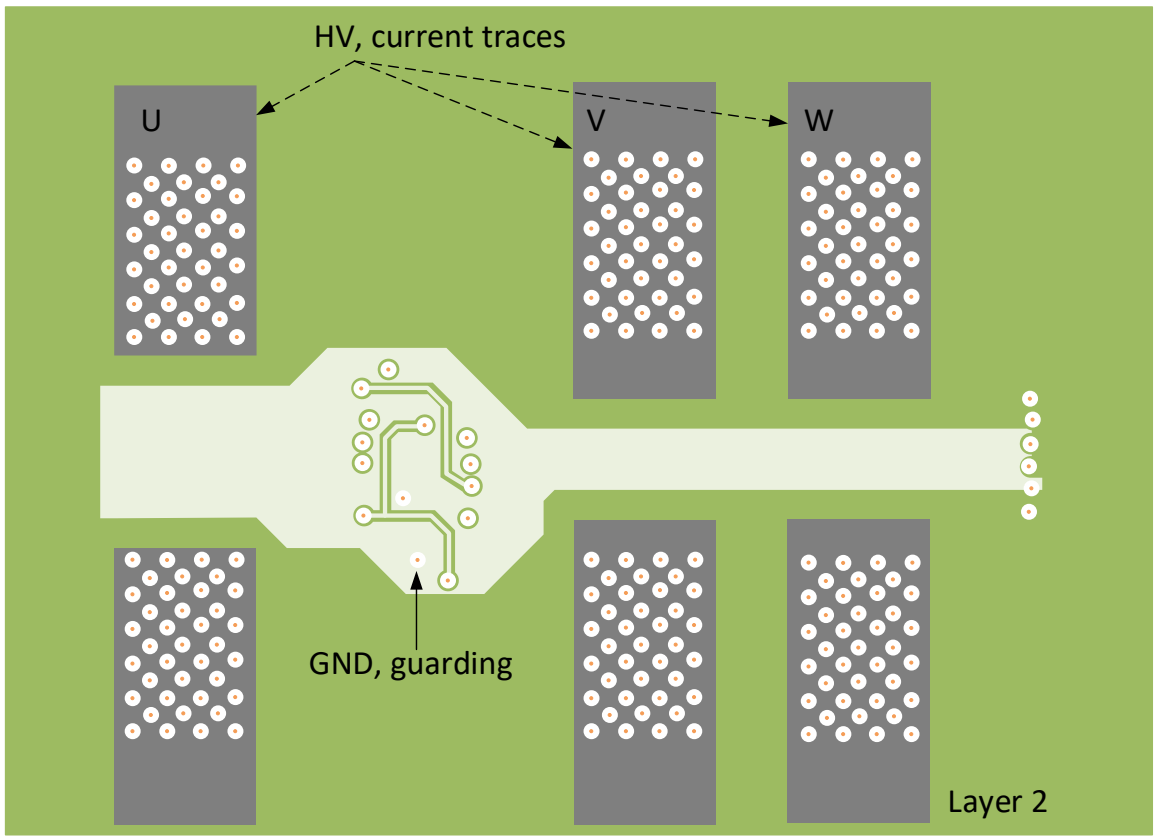


Figure 12 TLI4971 layout optimization

1.6 Signal Conditioning or Guarding Trace

The Figure 13 shows the current sensor placement in each layer and its current carrying HV traces in the PCB. In addition, it describes the signal layer guarding concept in the PCB. Here, the sensor LV output signals have traced through the layer 3 to protect from crosstalk & capacitive coupling by placing guard trace in the Layer 2, which has connected to the sensor ground.



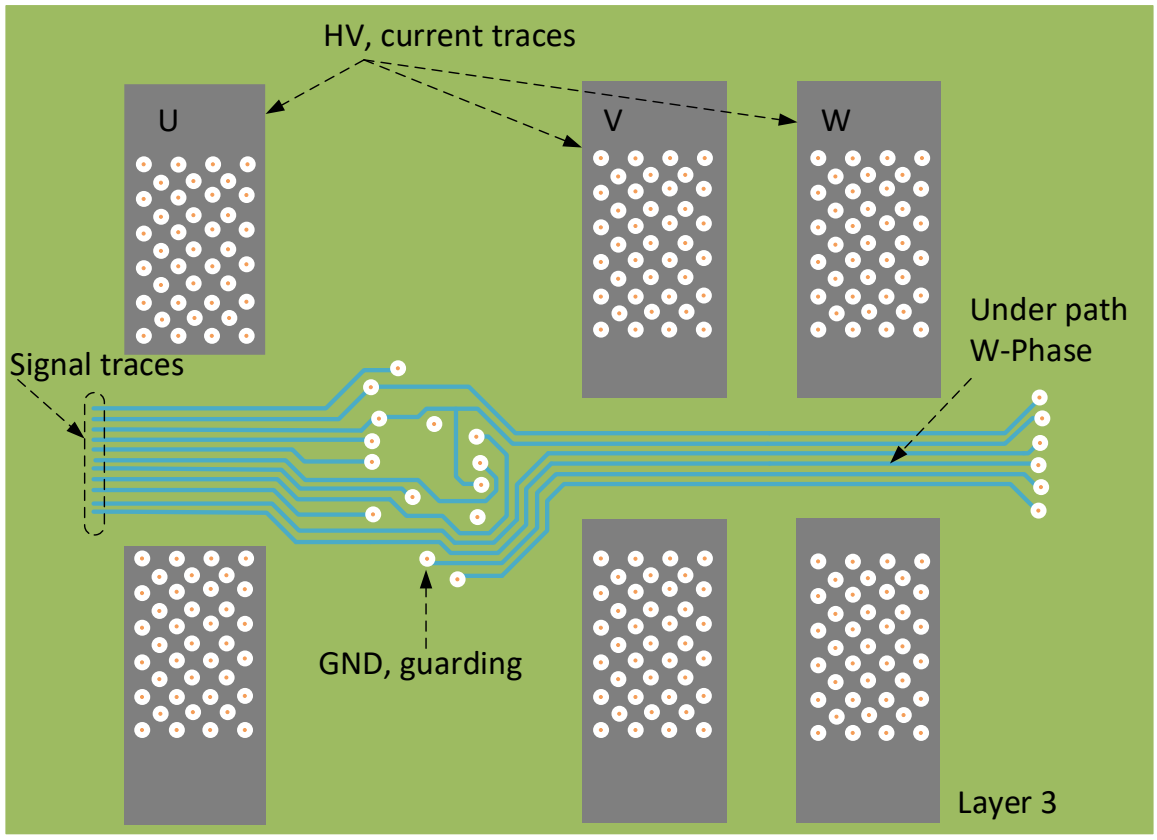


Figure 13 TLI4971 guarding principle

1.7 Intrinsic Stray-Field Robustness

Besides the differential measurement principle, the current sensor has an intrinsic stray field cancelation because of the physical alignment of the Hall sensor plates to the internal current rail. Hence, the stray field has canceled out, as the Hall plates in the current sensor perceives the same magnitude of magnetic field.

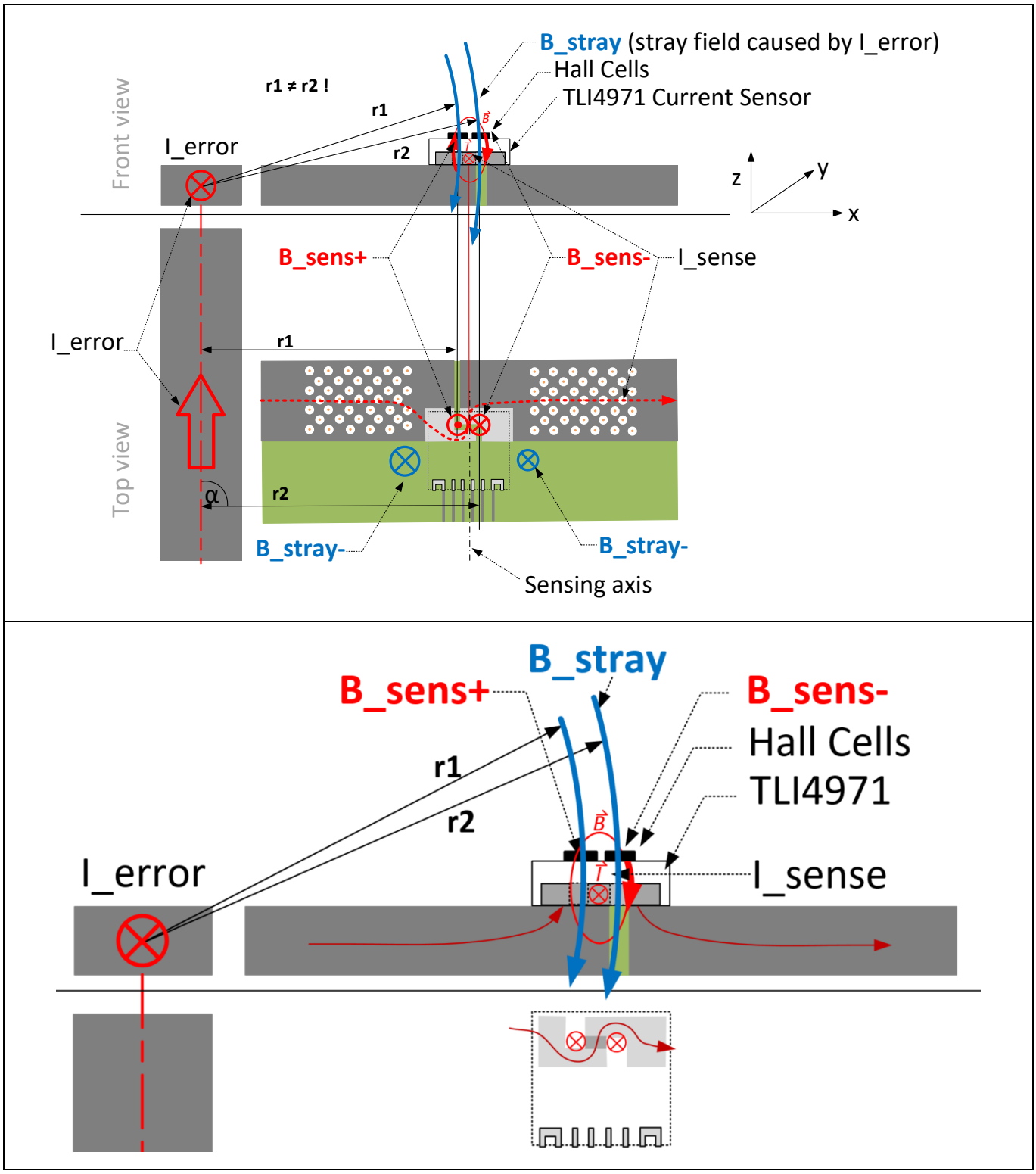


Figure 14 Stray Field Radial to Sensing Axis

The Figure 14 describes the stray field due to the neighboring conductor in blue color arrows, which interacting with the hall elements of the TLI4971. Both the Hall elements experiences the same magnitude of the stray field as they have placed in-line along the y-axis.

The below equation describes the influence of the angle α and radius 'r1' and 'r2' to the measured signal. The intrinsic stray field compensation works only for axial stray fields. Please consider the following layout recommendation as shown in the Figure 15 to achieve better accuracy performance.

$$B_{diff} = \mu_0 \frac{I_{err}}{I_{sense}} \left(\frac{1}{r_1} - \frac{1}{r_2}\right) \cos\alpha$$

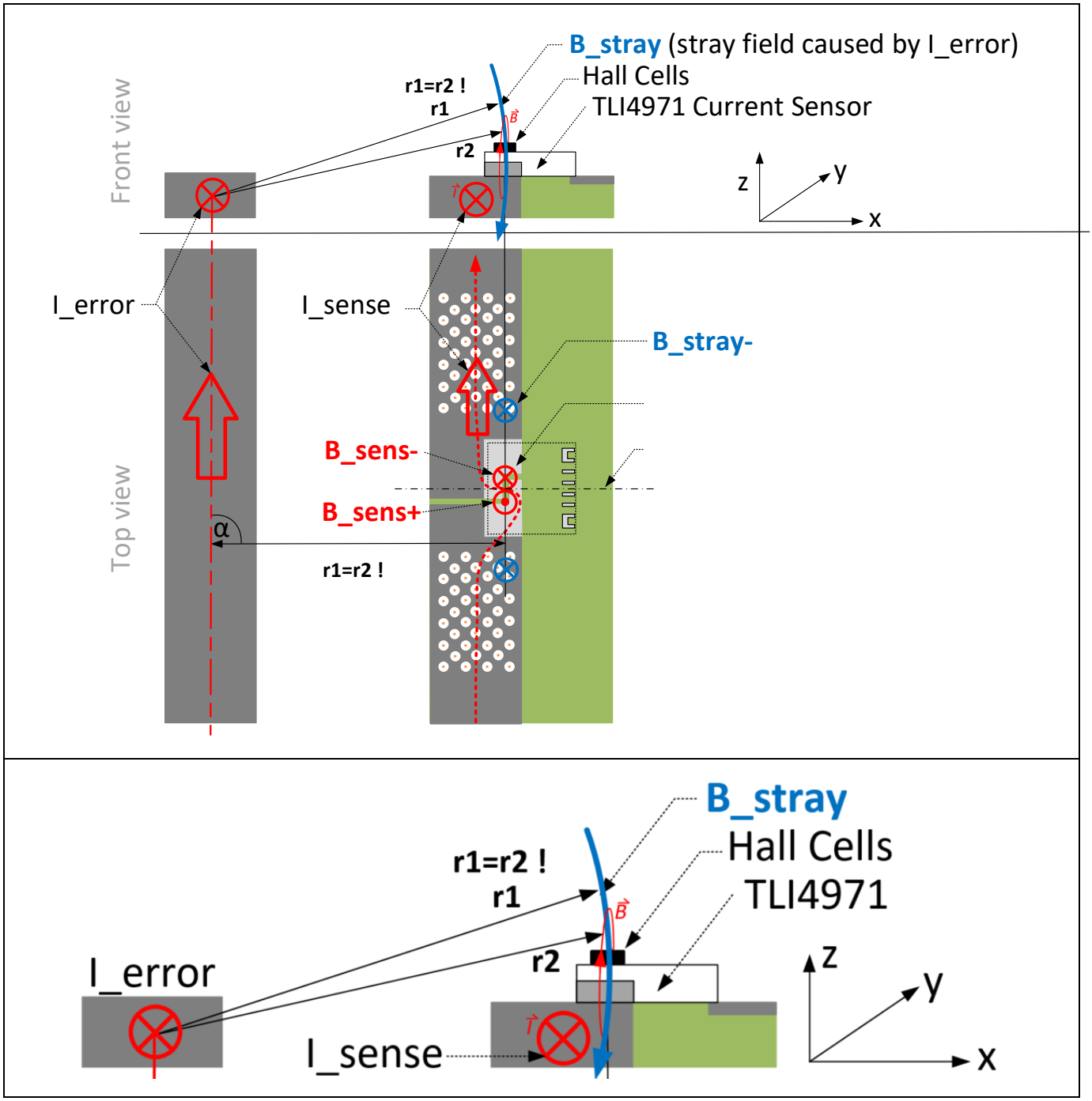


Figure 15 Stray Field Axial to the Sensing Axis

2 Infineon Single-phase Reference PCB

This chapter gives a layout recommendation for the TLI4971 for 4-layer reference PCB. The Figure 16 and Figure 17 shows the dimensions of the Infineon reference PCB for high current loads up to 70A_{RMS}. The layer stack of the PCB has shown in Figure 18. The different layers of the PCB have connected through the vias electrically and thermally. These vias have recommended for enabling a better temperature management. The vias helps to distribute the temperature between the layers in the PCB. It has not recommended for placing the vias in the footprint of the sensor.

Due to the lead less package, the hot spot of the sensor has directly connected to the PCB through the solder joint. Therefore, thermal resistance is very less when compared with the leaded packages, which gives an improved thermal performance for high loads. The insertion resistance of the sensor soldered on the PCB is 225µΩ. The R_{TH} of the sensor on the Infineon reference PCB is maximum 0.6K/W.

For high voltage application, an isolation clearance of 4mm has specified. The arc cavity in the PCB traces shown in the recommended reference boards are intending to meet the clearance distance between high voltage and low voltage side of the sensor board. The functional maximum rated working voltage has specified as 975V_{peak}.

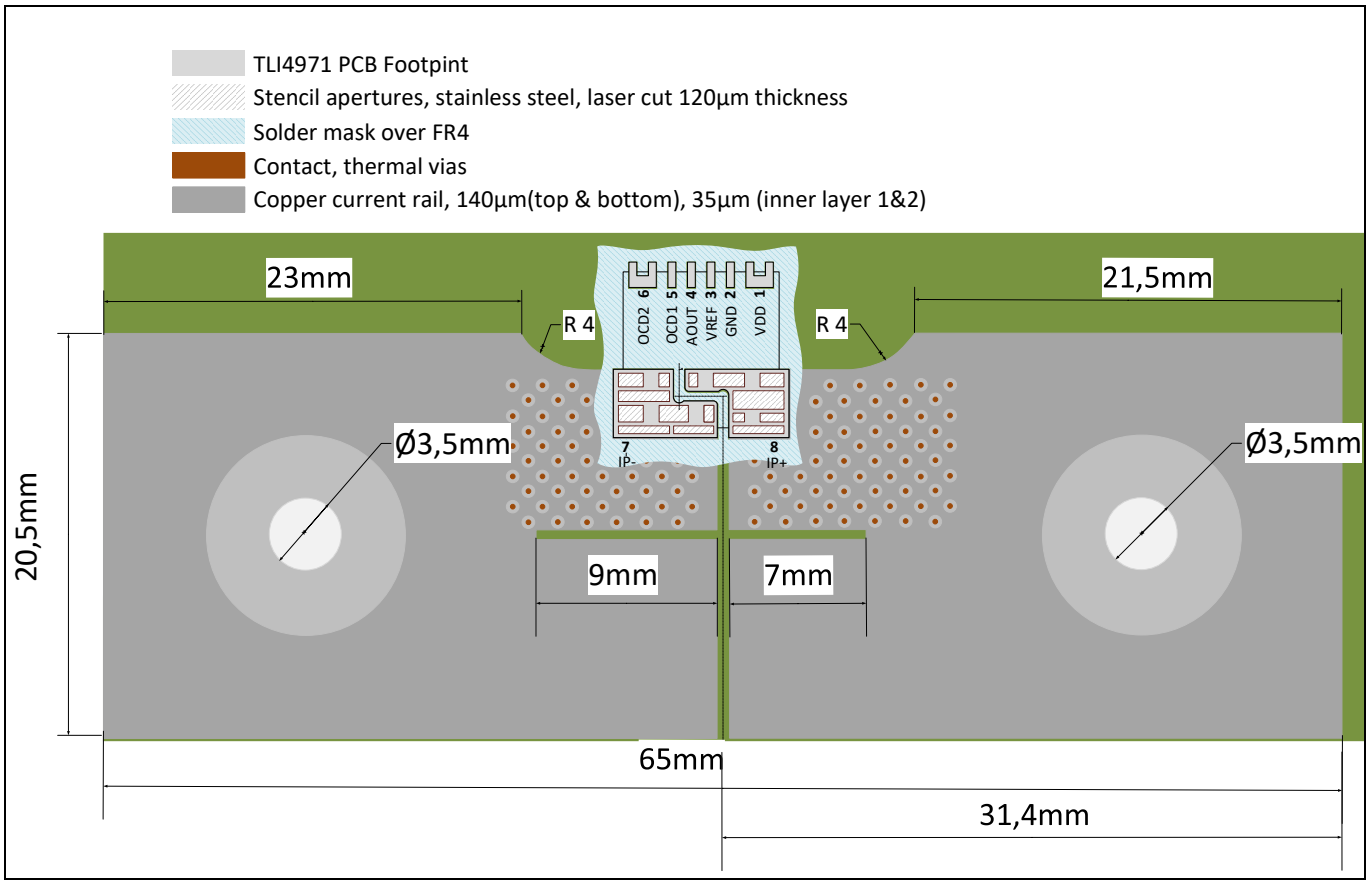


Figure 16 Infineon Reference PCB for 70A_{RMS}

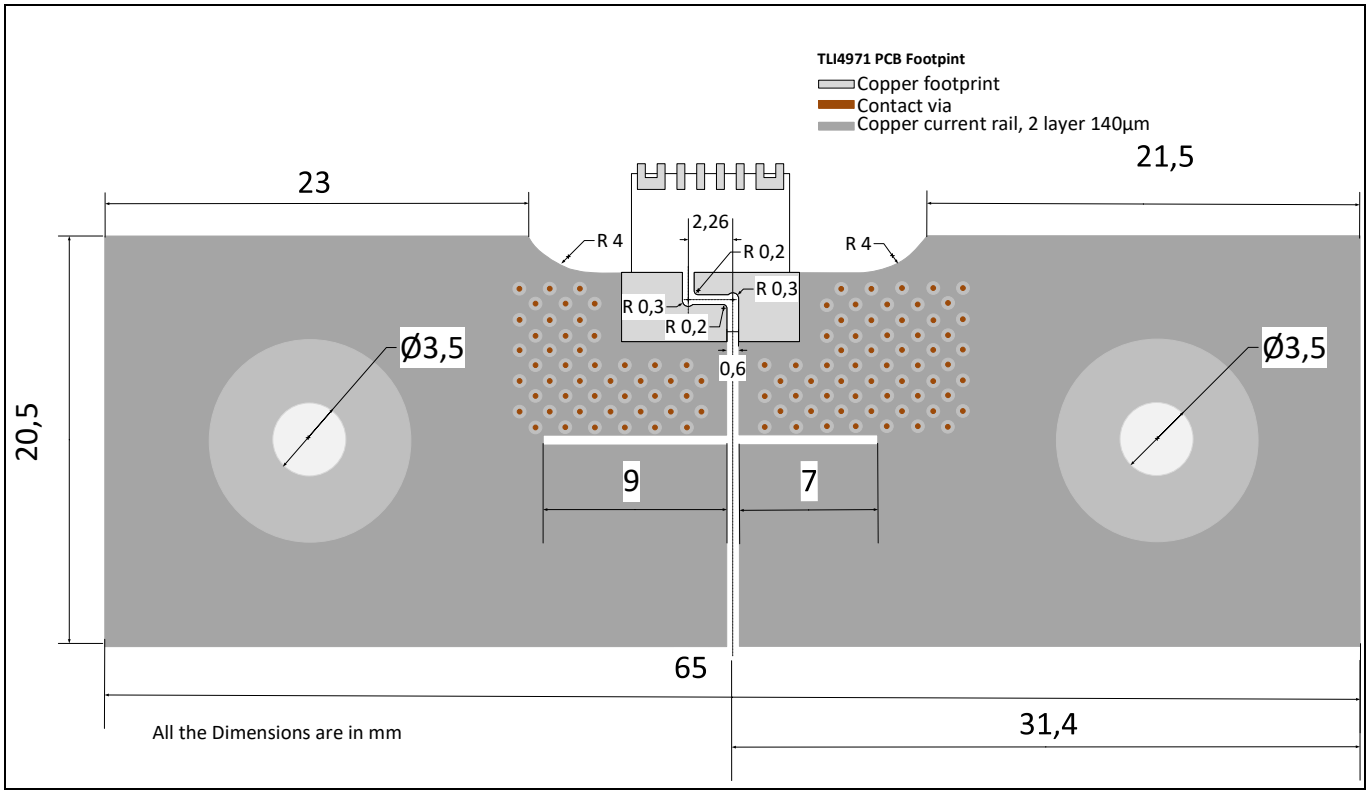


Figure 17 PCB Dimensions for Infineon Reference PCB

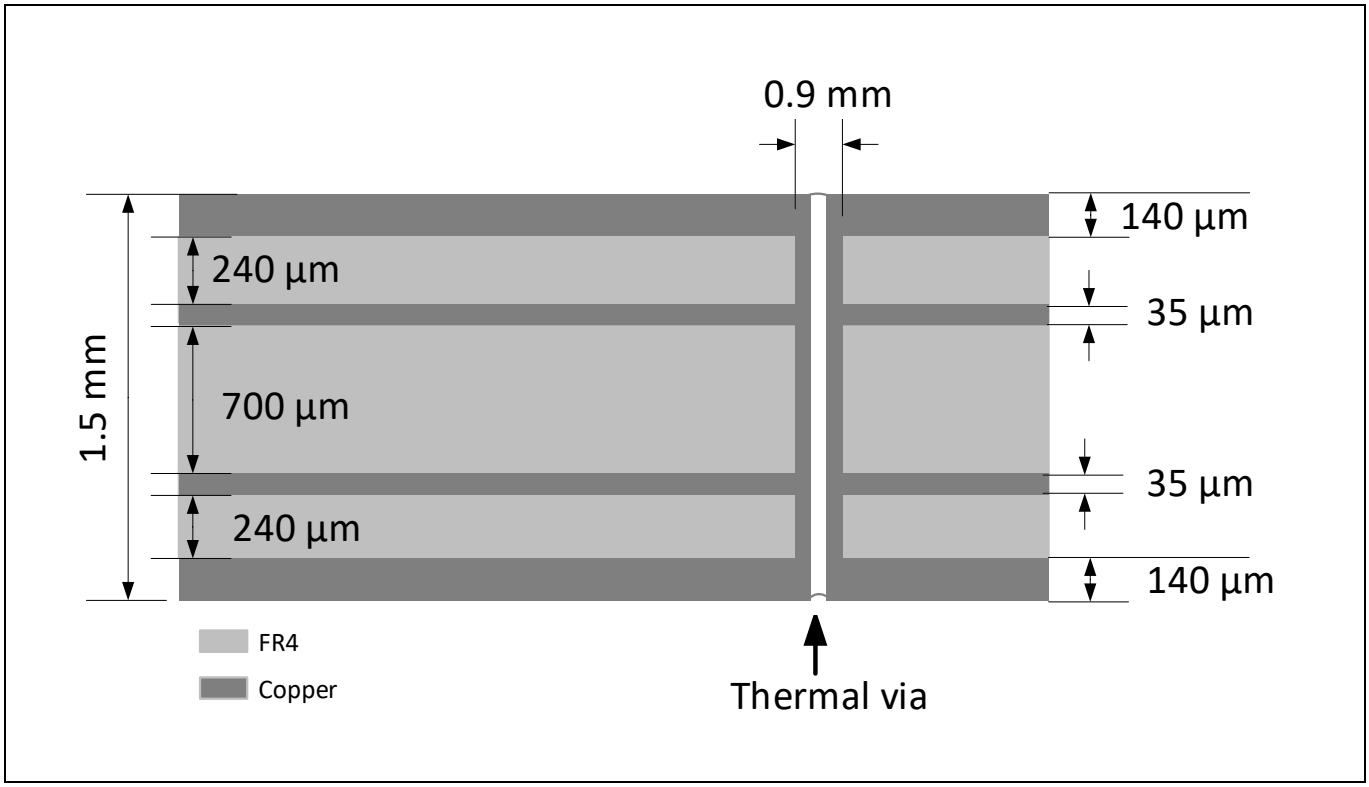


Figure 18 Reference Board Layer Stack

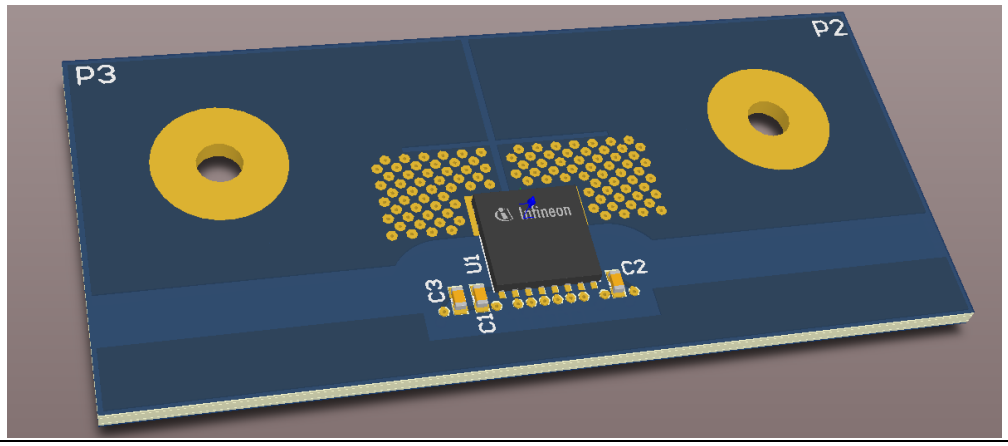


Figure 19 Reference board with TLI4971 and capacitors on V_{DD} and analog pins

Figure 19 shows the single-phase board with the current sensor and the capacitors placed on it and Figure 18 shows the layer stack of the reference PCB.

2.1 Reference board specification for 70A RMS

Table 1 Single-phase reference board specification

Position	Description	Thermal Conductivity [W/mK]
Board dimension	65mm x 30mm x 1.5mm	-
PCB Material	FR4	0.3
Copper metallization	4 layers 140/35/35/140 µm	388
Cooling Area in	584 mm^2 + 620 mm^2	-
Thermal Vias	∅ = 0.3 mm; plating 25 µm; 57 + 50 pcs.	-
Package Attach [50µm]	solder	55
Surface finish	Lead free HASL	

2.2 Sensitivity and R_{TH} overview

Table 1 Rth and change of sensitivity for different PCB setups

Current rail Layer Stack [µm]		Change of sensitivity related to reference PCB sensitivity [%]	R_{TH} junction to solder [K/W]	Note
Top layer	140	-0.088	0.254	
Inner layer 1	140			
Inner layer 2	140			
Bottom layer	140			
Top layer	140	0	0.281	Infineon single phase reference PCB for $70A_{RMS}$
Inner layer 1	35			
Inner layer 2	35			
Bottom layer	140			
Top layer	105	+2.075	0.3	
Inner layer 1	35			
Inner layer 2	35			
Bottom layer	105			
Top layer	75	+4.905	0.325	
Inner layer 1	35			
Inner layer 2	35			
Bottom layer	75			
Single layer	75	+6.734	0.35	
4 Layer	All layers are 35um	+8.509	0.25	

3 Cooling Strategy

3.1 Electric Drive Application

Infineon TLI4971 has developed to carry the high current. Depending on the current load, the device needs to connect to a thermal sink in order to limit the maximum solder temperature. In high power applications, the device has typically placed close to the power stage, which has directly connected to the system's heat sink.

To improve the thermal behavior of the sensor in high power applications, increase the number of thermal vias and enlarging the copper area are best practices. Figure 20 shows a recommended setup to measure the current in a 20kW Inverter. Here a thermal pedestal has used to connect the sensor board to the temperature sink of the power stage.

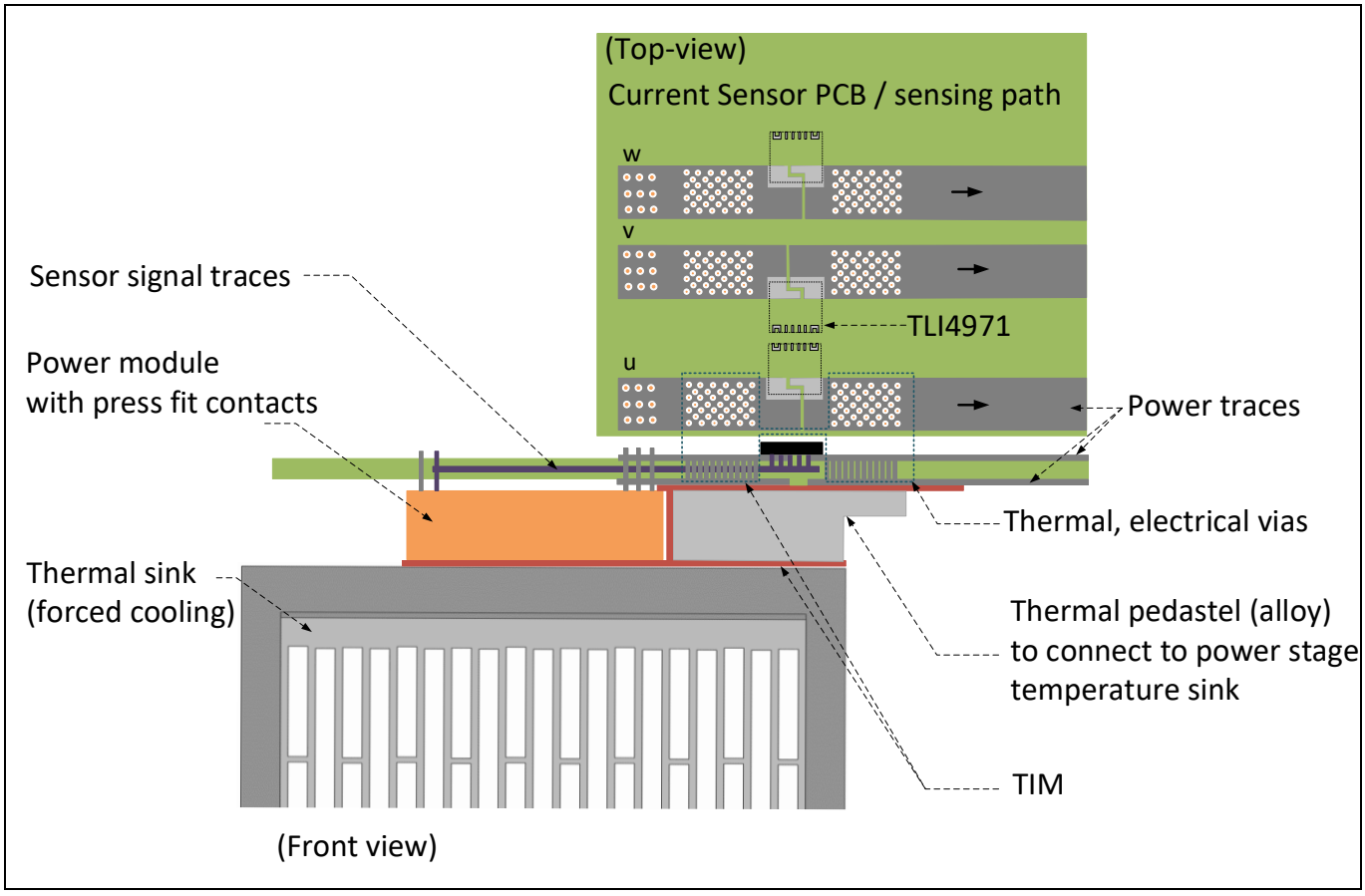


Figure 20 Cooling method for the Electric Drive PCB

Figure 20 shows a power module connected with TIM to a thermal sink. Furthermore it shows the power PCB where the current gets measured by TLI4971. The current sensor PCB has connected with an alloy pedestal in order to establish a good thermal connection between the current sensor path and the temperature sink.

4 Glossary

Notation	Description
QFN	Quad flat No Lead
TISON	Thin-profile Integrated Small Outline Non-leaded
SMD	Surface Mount Device
PG-TISON	Plastic Green Thin-profile Integrated Small Outline Non-leaded
B_Stray	Stray Field Magnetic Flux Density
PCB	Printed Circuit Board
B_Sens+/B_Sens-	Magnetic Flux Density of Hall Plates
EVAL	Evaluation
TIM	Thermal Interface Material
OCD	Over Current Detection
HV	High Voltage
LV	Low Voltage

5 References

[1] Recommendations for Board Assembly of Infineon Discrete Packages without Leads, Revision 1.0 dated 2018-08-29

[2] TLI4971 datasheet, Revision 1.0

Revision history

Document version	Date of release	Description of changes
V 01.00	20.12.2019	Initial Version