12V 1A AUTOMOTIVE FLYBACK CONVERTER for AUTOMOTIVE APPLICATIONS

Switching Mode Power Supply (SMPS) based on OPTIREG™ TLE8386-2EL low-side-sense controller and IPD50N08S4-13 OptiMOS™-T2

Scope and purpose

This document presents the solution for a 12V 1A flyback converter based on the Infineon OPTIREG™ TLE8386-2EL controller and IPD50N08S4-13 OptiMOS™-T2. The user is guided through the component selections, the circuit design and, finally, an overview of the experimental results are presented.

The TLE8386-2EL is part of the Automotive OPTIREG™ family and it implements a low-side-sense current mode controller with built in protection features. The device is AECQ-100 qualified.

The IPD50N08S4-13 is an AEC-Q101 qualified 80V N-channel enhanced mode MOSFET, it is part of the OptiMOS™-T2 family.

Intended audience

This document is intended for power supply design engineers, application engineers, students, etc., who need to design a Flyback converter for automotive power applications where a galvanic isolation between two voltage domains is required. In particular the focus is on a battery connected flyback that delivers up to 12W at 12V output voltage; the intention is to provide the user with all of the needed information to fully design and characterize the SMPS bringing it from an engineering concept to its production. Specific features and applications are:

- 48V to 12V Automotive applications
- Isolated current mode SMPS
- Flyback regulators with auxiliary sensing

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description of warranty of a certain functionality, condition or quality to the device.

The Application note is intended to provide important information about the usage of the device in the application and what to consider during hard- and software development.

This document is a compilation of important topica and hints, which have been collected during the product introduction. It does not cover all topics or features of the device.

Table of contents

1 Introduction

This is an engineering report for an automotive 12V, 1A Switching Mode Power Supply (SMPS) designed in a flyback topology. It is mainly intended for 48V to 12V applications, but the results can be reused also for other voltage domains. The document is intended to provide a technical guideline for desigining the SMPS starting from a collection of the specifications, their circuit implementation and finally the validation results.

The AECQ-100 OPTIREG™ TLE8386-2EL is used as a flyback controller in combination with the primary switch IPD50N08S4-13 OptiMOS™-T2. The extended power supply range of the controller make it suitable for harsh automotive applications, its current mode control loop make it suitable for a wide bill of material variation thanks to a dedicated compensation pin. Finally the controller embeds some protection features such as output overvoltage protection, over current protection and over temperature shutdown that improve the reliability of the system.

The IPD50N08S4-13 OptiMOS™-T2 is an AECQ-101 qualified N-channel enhanced mode MOSFET. It is 80V capable and it is 100% avalanche tested.

The reference design board operates at 400 kHz switching frequency in the [0-1]A load range at 12V nominal output, the functional input voltage range is [6-35]V. The secondary side output voltage control is implemented via an auxialiary winding that avoids the using of galvanic isolated devices (e.g. optocouplers) to feed the sensed voltage.

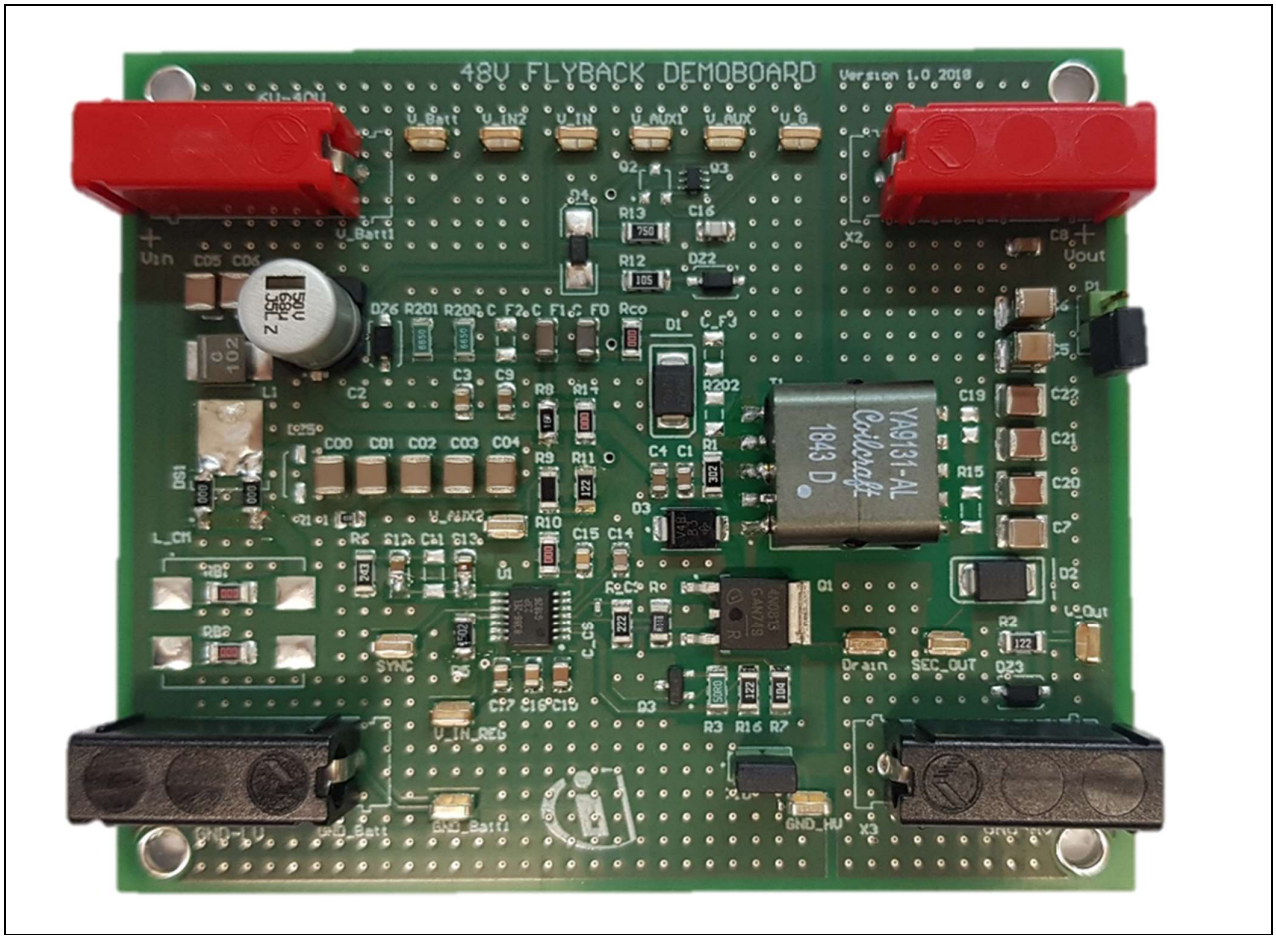


Figure 1 Top side of the reference design board

2 Technical specification

Table 1 Power supply technical specification

Input voltage – VIN	6-35V
Output voltage – VOUT	12 V ±13%
Rated output current – IOUT	1000 mA
Rated output power – POUT	12 W
Auxiliary Voltage - VAUX	12V ±10%
Auxiliary Current - IAUX	300mA (1)
Switching frequency - fsw	400kHz
Efficiency –Eta	81 % @ 13.5Vin, 800mA
System dimensions	90 mm x 75 mm x 18 mm (L x W x H)
Isolation	750Vrms for 1min

Notes

(1) – The auxiliary voltage is not part of this design and it is used only for regulation purposes. It is recommended to not further load it.

3 List of product features

Table 2 Table 2 lists the features of the TLE8386-2EL controller – please refer to [1] for more details about the product.

Table 3 TLE8386-2EL List of features

• Wide input voltage range from 4.75V to 45V
• Constant Current or Constant Voltage Regulation
• Very Low Shut Down Current Iq<2uA
• Programmable switching frequency in the 100kHz-700kHz range
• Output Overvoltage Protection
• External Soft Start adjustable by capacitor
• Over Temperature Shutdown

4 Circuit description

4.1 Circuit schematic

The following picure shows the schematic of the designed flyback converter. The following paragraphs describe the details of the main blocks.

Circuit description

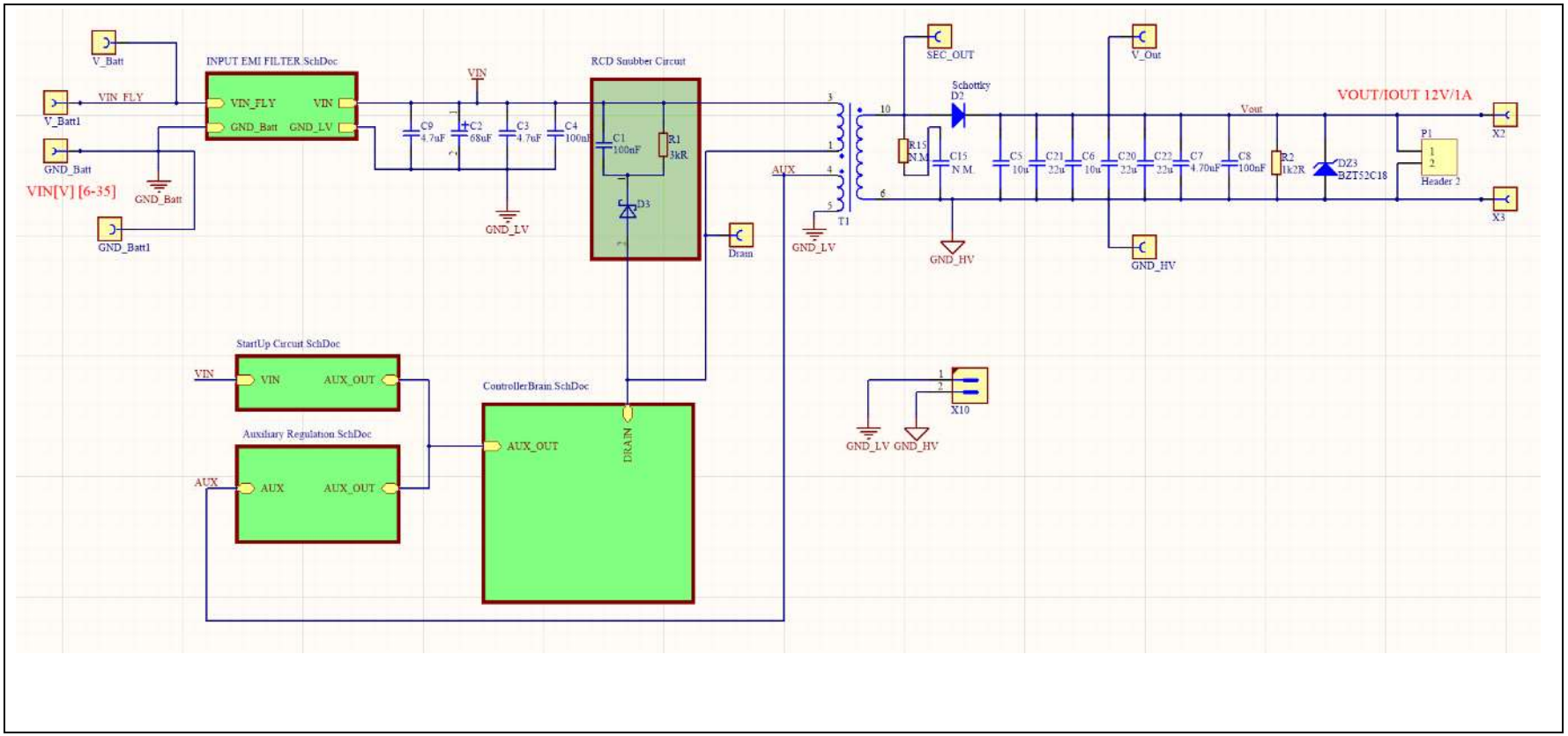


Figure 2 Schematich of the flyback converter

4.2 EMI filter and REVERSE battery diode

The EMI filter block is necessary to reduce the conducted electromagnetic emission of the SMPS that are typically due to its switching activities. The circuit, visible in Fig. 3, implements both a common mode filter (i.e. L_CM) and a differential low pass second order filter (i.e. L1, C00). This latter one has to be designed with a cut off frequency lower than the switching frequency, usually one decade lower, of the SMPS in order to reduce the noise due to the switching activity itself. The selection of the cut off frequency is done at a first round as a trade off between the desired attenuation and the physical size and cost of the filter. It is important to remember that the conducted emission profile of the final solution is a combination of multiple factors – the EMI filter contributes to improve them, but proper board layout represents the base requirement.

The reference design implements a filter with a cut off frequency of about 50kHz.

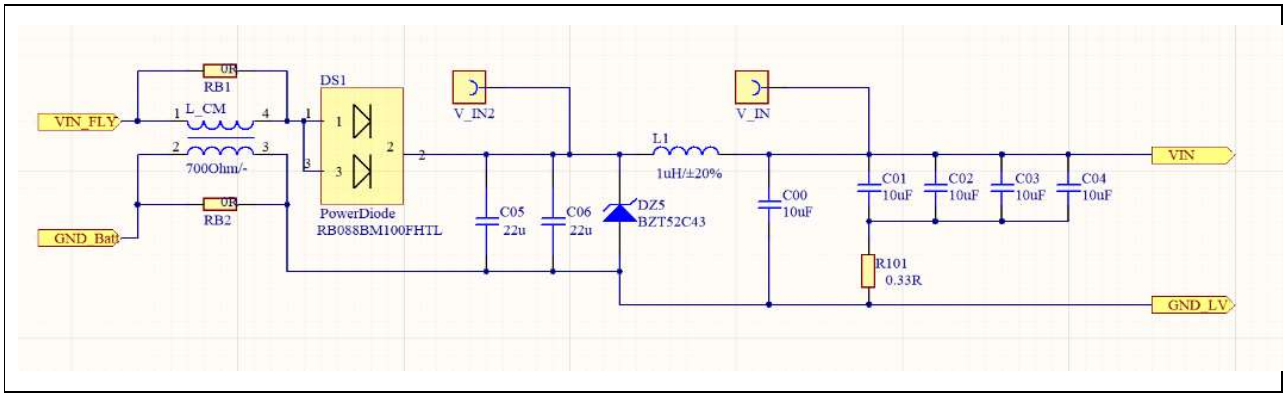


Figure 3 Circuit schematic of the input EMI filter and reverse battery diode

Fig. 3 shows also the reverse battery diode DS1 that prevents system damages due to possible reverse polarity connection errors of the input voltage. The components of both the reverse polarity diode and the EMI filter have to be selected according to the maximum input current of the flyback.

4.3 Primary side snubber

During the on phase of the OPTIMOS™ the energy is stored in the magnetizing inductance of the transformer, this is then delivered to the secondary side during the off phase when the diode D1 and D2 will turn on. This would automatically clamp the drain of Q1 at VIN+nVout where *n* is the primary to secondary side turn ratio of the transformer. The transformer leakage inductance also stores energy during the on phase of Q1, this is then delivered on the stray capacitance of Q1-drain during the off phase. This brings to a resonance condition between the stray inductance and the capacitance itself. The side effect is an overvoltage on the MOSFET that, if not clampled, will reach a peak of about:

$$V_{DS-Q1} = VIN + n * VOUT + I1\sqrt{Llk/C_{stray}}$$

Where I1 is the current of the primary side at the beginning of the off phase of Q1, Llk is the transformer leakage inductance and Cstray is the parasitic capacitance on drain of Q1. The extra voltage due to this resonance is not controlled because of its nature and it has to be mitigated with a proper clamping of Q1-drain. This is usually obtained with a RCD snubber (see Fig. 2) that dissipates the energy stored in the leakage inductance, this happens when Vds-Q1 reaches VIN+nVOUT and the diode D3 is turned on. The energy is then dissipated in R1.

4.4 OPTIREG™ and OPTIMOS™

The core of the SMPS is the combination of the controller with the power MOSFET. They are defining the regulation parameters, system stability, protection features and efficiency.

The controller is the TLE8386-2EL part of OPTIREG™ family – it is an AECQ-100 qualified current mode basic smart boost controller.

Fig. 4 shows the block diagram of the controller. The PWM controller measures the output voltage via a resistor divider connected between Pin FB and ground, and determines the appropriate pulse width duty cycle (on time). An over voltage protection switches off the converter if the voltage at Pin FB exceeds the over voltage limit. If the connection to the output voltage resistor divider should be lost, an internal current source connected to Pin FB will draw the voltage above this limit and shut the external MOSFET off. The current mode controller has a built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty). An additional built in feature is an integrated soft start that limits the current through the primary inductor and the external power switch during Initialization. The soft start time TSS is adjustable using an external capacitor CSST:

$$T_{SS} = C_{SST} x\, 2.00V/10uA$$

The switching frequency may be adjusted by using an external resistor connected between FREQ and GND pins. It is also possible to exploit the SYNC pin to synchronize the switching frequency with an external source.

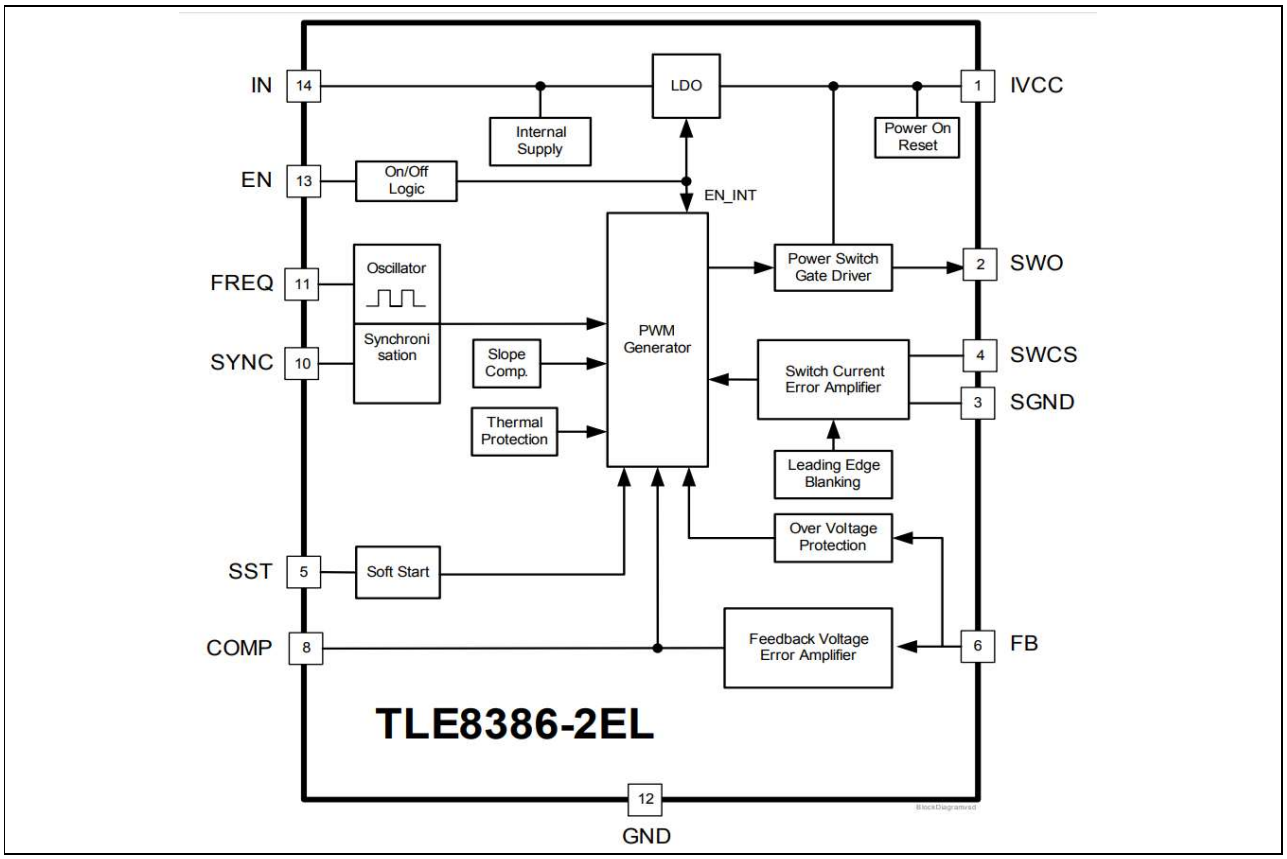


Figure 4 Power management of the IC

Fig. 5 shows the circuit schematic where the TLE8386-2EL is used in the application. Particular details about compensation network, frequency selection and gate driving are shown.

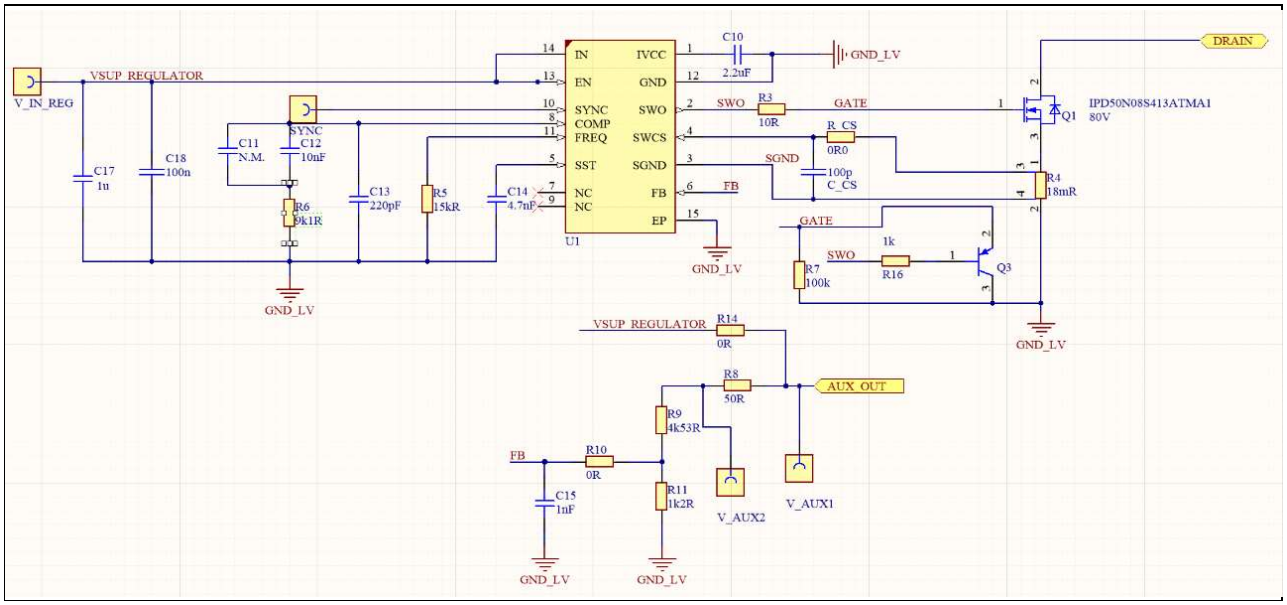


Figure 5 Circuit schematic of TLE8386-2EL and IPD50N08S4-13

The Q1 is the OPTIMOS™ n-channel MOSFET used for this application. It is an 80V capable AECQ-101 qualified device with capability of working up to 175°C and it is 100% tested for avalanche.

In order to improve the EMI performances an active gate driving network has been implemented. This is the combination of R3, R16 and Q3. It specifically avoids spurious turn on of Q1 during sharp dV/dt on its drain by enhancing the sink current of the driving circuitry during the off phase of the MOSFET.

4.5 Secondary side rectification

The secondary side rectification circuit is a simple diode rectifier with filter capacitors. Diode D1 is a Schottky type, selected to meet the current and reverse voltage requirements. Its low forward voltage reduces the power loss in D1, and therefore lowers its temperature and improves the overall efficiency.

Selection of output capacitor Cout (i.e. C5, C6, C7, C8, C20, C21, C22) directly affects the output voltage ripple. The output voltage ripple is reduced by selecting an ultra low-ESR and high ripple current capacitor. Typically, ceramic capacitors are used for this purpose.

The voltage class of the capacitor has to match the output voltage specification (i.e. 12Vout), then 25V class capacitor represent an optimum choice.

4.6 Feedback loop with auxiliary sensing

The galvanic isolation has to be maintained between the two voltage domains that are separated by the transformer. This creates the power path from the 12V domain, where the controller is sit, to the secondary side domain where the 12Vout is delivered. The feedback network has to typically keep the same isolation requirements of the transformer and it can be typically implemented with optocouplers. These would be then part of the control loop concurring to its gain with their current transfer ratio (CTR) parameter. The CTR has typically a wide lot to lot and temperature variations that affect the accuracy of Vout. The lot to lot variation can be mitigated by trimming the feedback network in the final production line of the SMPS; this creates an extra

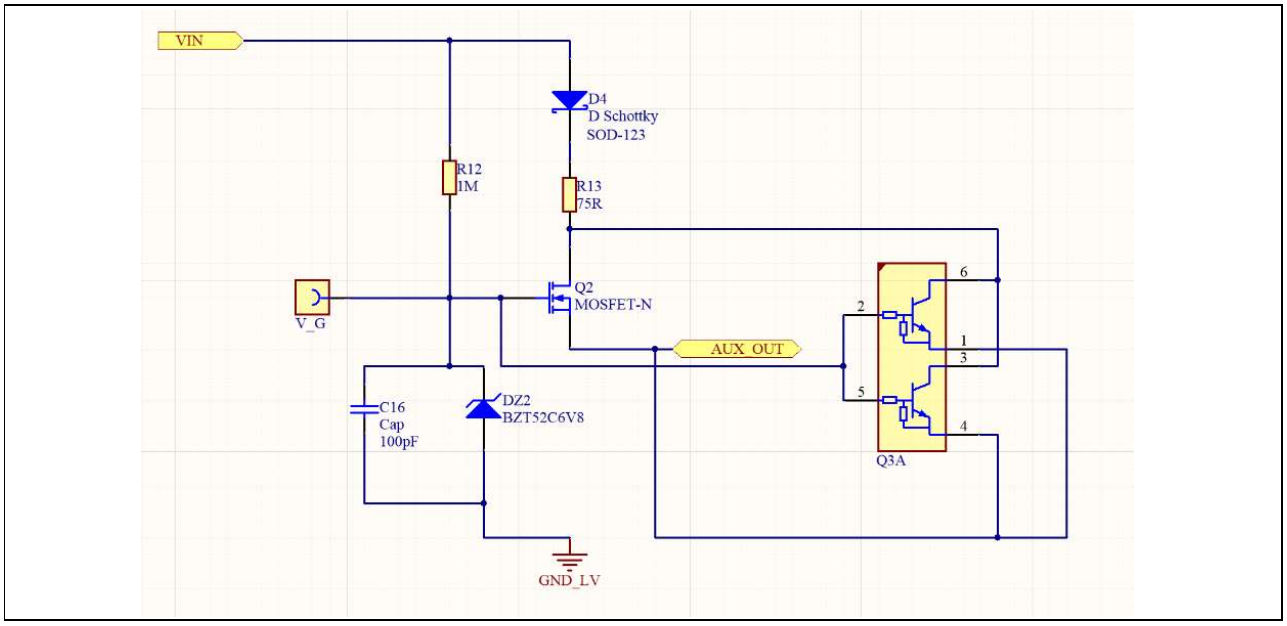
cost for the product. It is possible to use a different control loop technique that allows to solve this issue: this is called Auxiliary Sensing and it is part of this reference design.

The auxiliary sensing requires to use a transformer with a third winding called auxiliary. It emulates the secondary side of the transformer where VOUT is delivered and its output can be kept on the primary side domain. The auxiliary circuit implements the same functionalities as the secondary side where a diode and a filter capacitor are used to rectify the voltage. It is recommended that the diode of the auxiliary has the same characteristics of what is used in the secondary side.

The feedback network is finally completed with the voltage divider that is visible in Fig. 5 as R9 and R11; a capacitance C15 is also used to remove undesired noise in the feedback path.

4.7 Start-Up Circuit

The 12V voltage domain in the automotive environment suffers of high instability of the voltage source that can drop down to 6V or lower. In order to cope with this situation the output voltage of the auxiliary circuit is exploited to supply the controller, this always guarantees a stable supply voltage but during the first start-up phase when the system has not reached the steady state yet. This initial phase can be supported with a supplementary circuit whose schematic implementation is shown in Fig. 6 and that is named: start-up circuit.



Circuit description

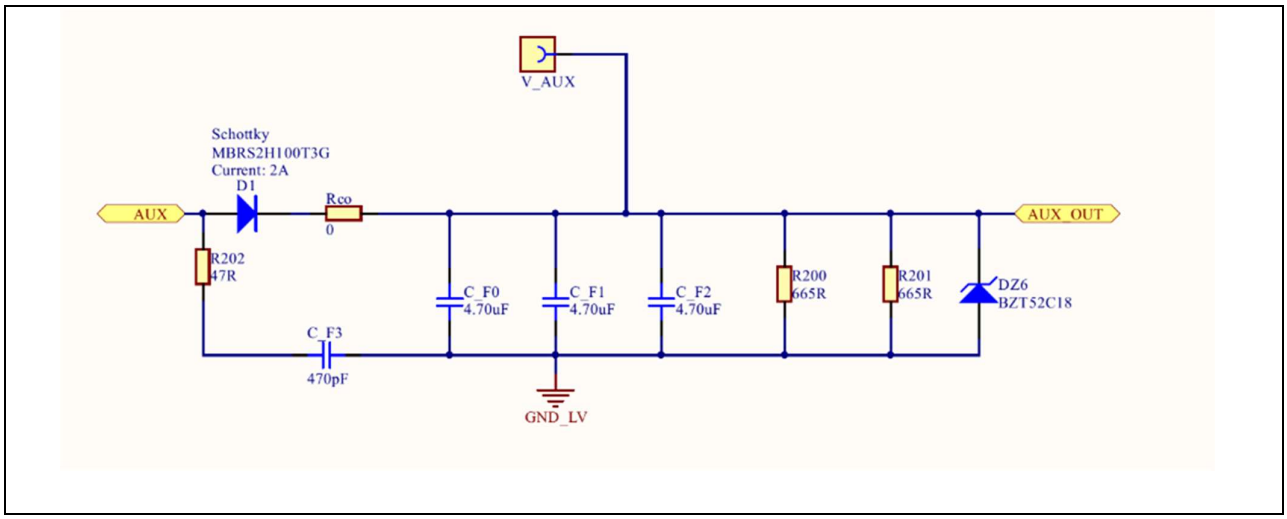


Figure 6 Start-up circuit

The input voltage will charge the auxiliary capacitance Caux (i.e. C_F0, C_F1 and C_F2) during the start-up phase until the TLE8386-2EL will start to work and regulate. From that point on the auxiliary circuit will take over supplying the controller itself by turning the MOSFET Q2 off. The gate voltage on Q2 is clamped to both protect it and to avoid spurious turn on.

5 OPTIREG™ TLE8386-2EL controller

The TLE8386-2EL controller belongs to the OPTIREG™ family: a dedicated power IC portfolio for automotive applications. The TLE8386-2EL includes built-in features as enable, soft start, frequency selection, frequency syncronization, internal gate driver, over-voltage, over-current and over-temperature protections.

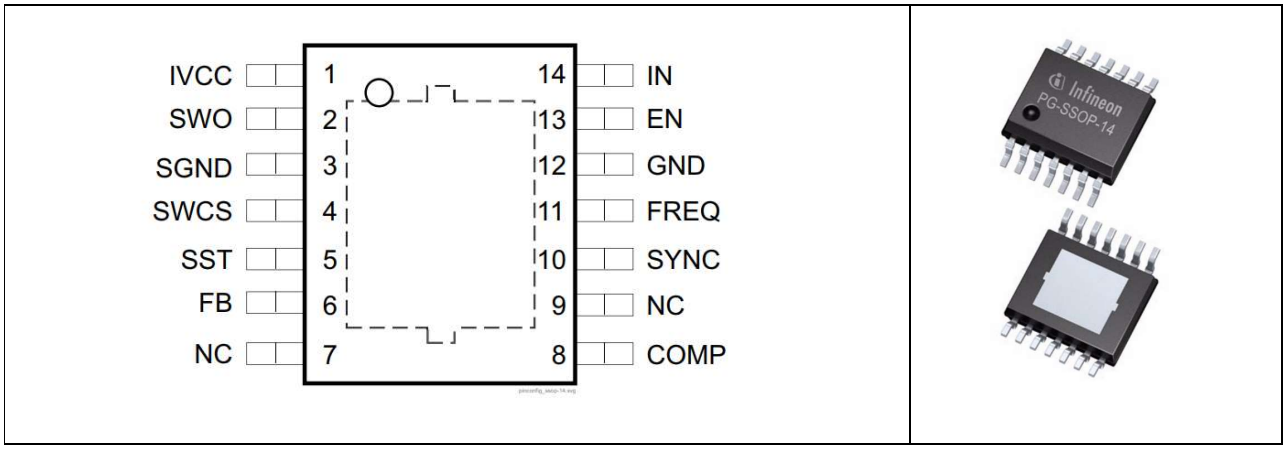


Figure 7 Pin configuration of TLE8386-2EL and package highlight

For full details about the TLE8386-2EL controller, see [1].

5.1 Peak primary current control

The primary current is sensed by the external shunt resistor R4 and it is then transduced to a voltage signal as shown in Fig. 8 – this signal is used to both control and protect the system. This signal is amplified and then compared with the feedback signal for cycle by cycle peak current limit operation. If the amplified current sense signal exceeds the feedback signal, the on-time T_{on} of the switching cycle is terminated and Q1 turned off.

The current capability of the power MOSFET has to be selected according to the designed overcurrent threshold. Because of its crucial feature the sensed signal has to be as clean as possible, therefore it is recommended to:

- Locate the current sense resistor as close as possible to the TLE8386-2EL.
- Use short traces between the power MOSFET and ground.
- Select the current sense resistor value in order to have the Vsensepeak lower than the adjusted current limit threshold – 20% margin is recommended. Resistor value tolerance and its possible temperature deratings have to be considered.
- Select the current sense resistor in order to not overcome the maximum drain current Idmax of the power MOSFET.
- Implement a 4-wire connection of the resistor in order to improve the sensing.

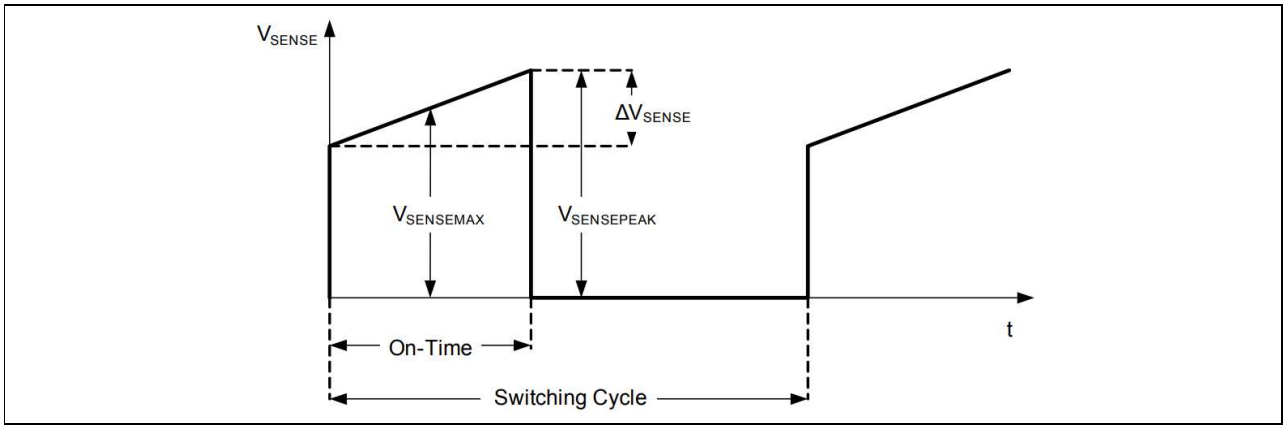


Figure 8 Current sensed signal

The peak of the sensed current is compared with the embedded overcurrent threshold and the power MOSFET is turned off in case it is crossed.

5.2 Over Voltage, Open Feedback and Over Temperature Protections

The TLE8386-2EL embeds several protections like over voltage, open feedback and over current. During an overvoltage the gate driver outputs SWO will turn off. In the event of an overtemperature condition the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. If the connection from pin FB to the output voltage resistor divider should be lost, an internal current source connected to Pin FB will draw the voltage above this limit and shut the external MOSFET off.

The power MOSFET is turned off by the controller even in case of junction over temperature condition of the controller itself. Automatic restart happens as soon as the junction temperature of TLE8386-2EL is cooled down.

6 PCB Layout

The printed circuit board (PCB) is two layer, double sided, and manufactured with the standard 1.6 mm thickness and 1oz copper. Following pictures show the board layout for each plane.

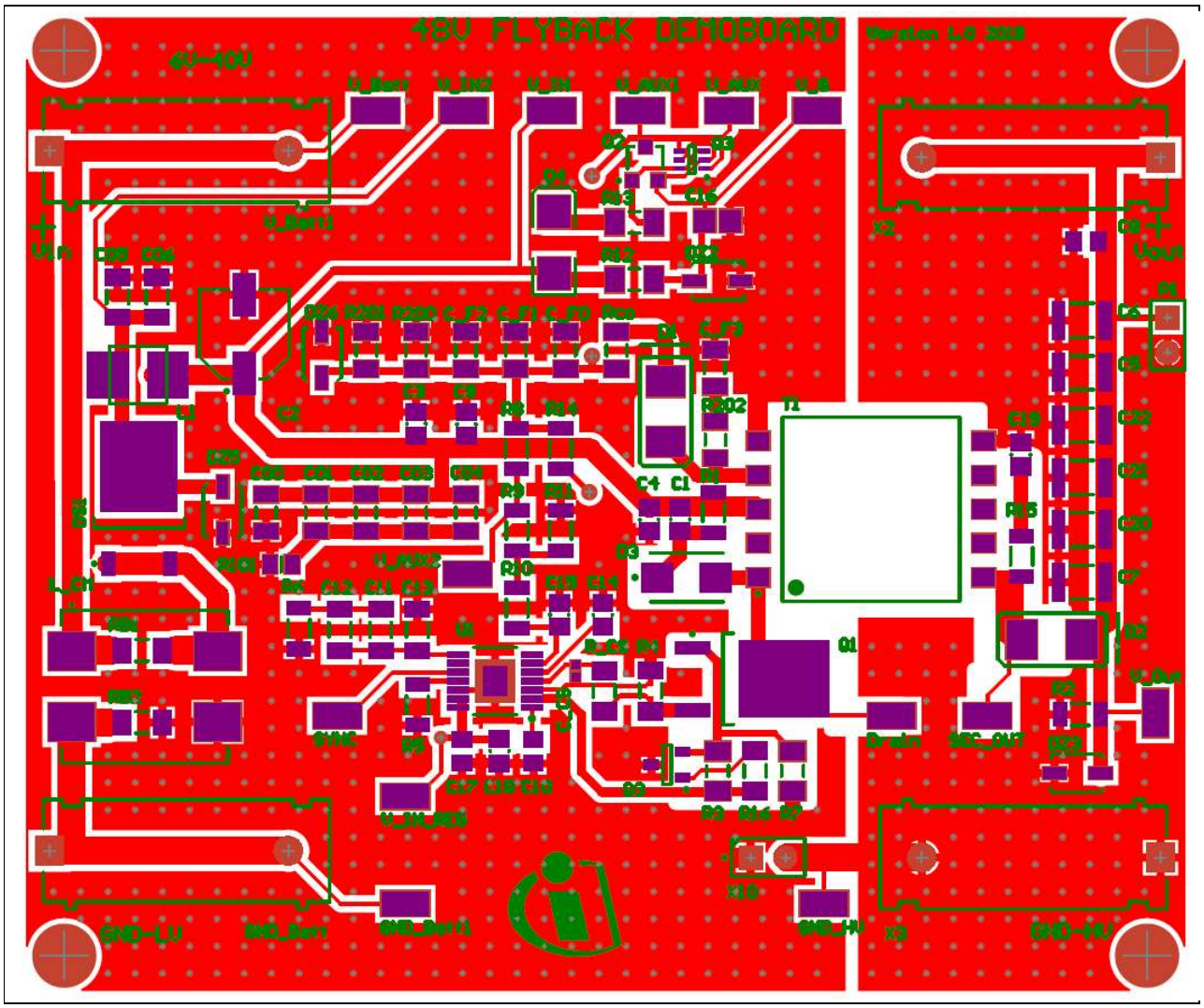


Figure 9 Layout top

PCB Layout

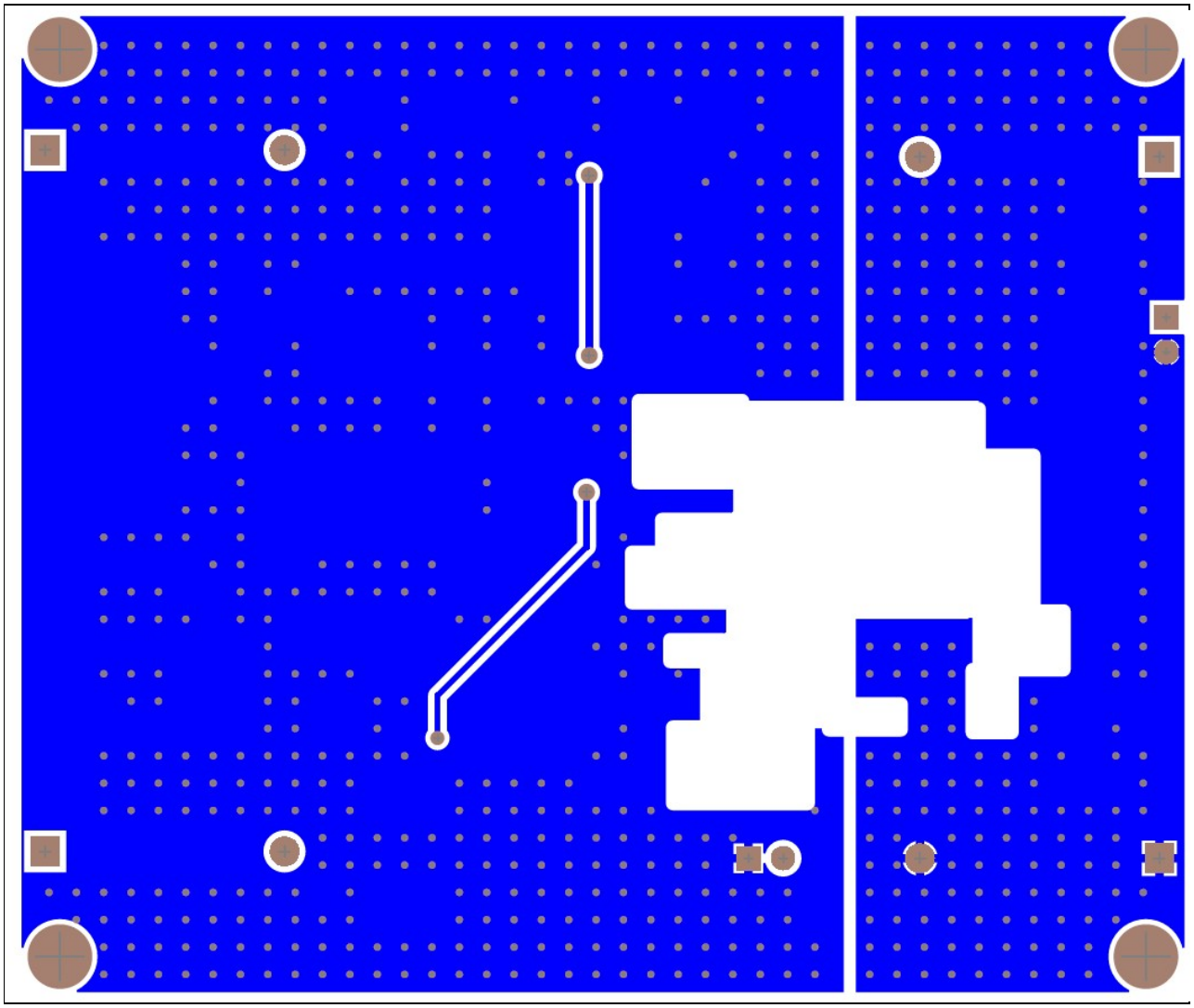


Figure 10 Layout bottom

7 Bill of materials

Table 4 Bill of materials

Designator	ManufacturerPartNumber	Value	Quantity
C00, C01, C02, C03, C04	UMK325AB7106KMHT	10u	5
C1, C4	GCD21BR72A104KA01L	0,1u	2
C2	HHXC500ARA680MHA0G	68u	1
C3, C9	GCJ31CC71H475KA01L	4,7u	2
C05, C06	CGA6P3X7R1E226M250AB	22u	2
C5, C6	UMK325AB7106KMHT	10u	2
C7	CGA6M2X7R1E475M200AD	4,7u	1
C8	C0805S104K5RACAUTO	0,1u	1
C10	C2012X7R1E225K125AE	2.2u	1
C11 (*)			1
C12	C0805C103K1HACAUTO	10n	1
C13	GCM21A5C2E221JX01D	220p	1
C14	80-C0805C472J2GECAUT	4,7n	1
C15	80-C0805C102M4RECAUT	1n	1
C16	80-C0805C101KBRAUTO	100p	1
C17	GJ821BR71H105KA12L	1u	1
C18	C0805C104K5RAC	0,1u	1
C19 (*)			1
C20, C21, C22	CGA6P3X7R1E226M250AB	22u	3
C_CS	C0402C101F5GAC	100p	1
C_F0, C_F1, C_F2(*)	GCJ31CC71H475KA01L	4,7u	3
C_F3			1
D1	MBRS2H100T3G		1
D2	MBRS2H100T3G		1
D3	VSSB410S-E3		1
D4	STPS1L60ZFY		1
DS1	RB088BM100FHTL		1
DZ2	BZT52C6V8-HE3-18		1
DZ3, DZ6	BZT52C18-HE3-08		2
DZ5	BZT52C43-HE3-18		1
Drain, GND_Batt1, GND_HV, SEC_OUT, SYNC, V_AUX, V_AUX1, V_AUX2, V_Batt, V_G, V_IN, V_IN1, V_IN_REG, X8	534-5019		14
GND_Batt, X3	973582100		2
L1	XEL4020-102MEC		1
L_CM (*)			1
P1	826646-2		1
Q1	IPD50N08S413ATMA1		1
Q2	UM6K33N		1
Q3 (*)			1
R1	ERA-8AEB302V	3K	1

Bill of materials

R2, R11	ERA-8AEB122V	1K2	2
R3	ERJ-U08J100V	10R	1
R4	WSL1206R0180FEA18	18mR	1
R5	ERA-8AEB153V	15K	1
R6	ERA-8AEB912V	9K	1
R7	ERA-8AEB104V	100K	1
R8	TNPW120650R0BEEN07	50R	1
R9	ERA-8AEB4531V	4K530R	1
R10, R14	ERJ-U080R00V	0R	2
R12	ERA-8AEB105V	1M	1
R13	ERA-8AEB750V	75R	1
R15 (*)			1
R16	ERA-8AEB122V	1K2	1
R101	ERJ-8RQJR33V	0.33R	1
R200, R201	ERJ-U08F6650V	665R	2
R202 (*)			1
R_CS	ERJ-U080R00V	0R	1
Rco,RB1,RB2	ERJ-U080R00V	0R	1
T1	YA9131-AL		1
U1	TLE8386-2		1
V_Batt1, X2	973582101		2
X10	826646-2		1

(*) Not mounted

8 Transformer specification designed by Coilcraft

8.1 Electrical diagram

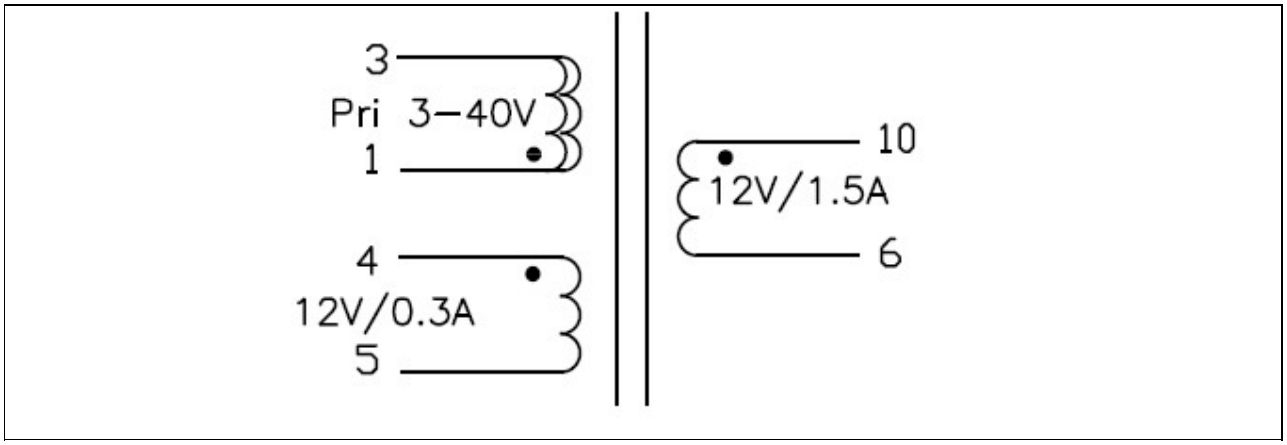


Figure 11 Transformer electrical diagram

8.2 Electrical specification

Table 5 Transformer electrical specification

Inductance [uH] at 300kHz, 0.1Vrms		
Pin	MIN	MAX
1-3 at 0A	7.6	8.4
1-3 at 11A	7.0	
DC Resistance [Ohm]		
Pin	MIN	MAX
1-3		0.044
10-6		0.265
4-5		0.55
Leakage Inductance [uH] at 300kHz, 0.1Vrms, 0A		
Pin	Short pin	MAX
1-3	10-6	0.11
4-5	10-6	0.43
Turn ratio – 0.05Vrms, 30kHz to pin 1-3		
Measure Pin	MIN	MAX
10-6	1.94	2.06
4-5	1.94	2.06

8.3 Transformer Mechanical Specifications

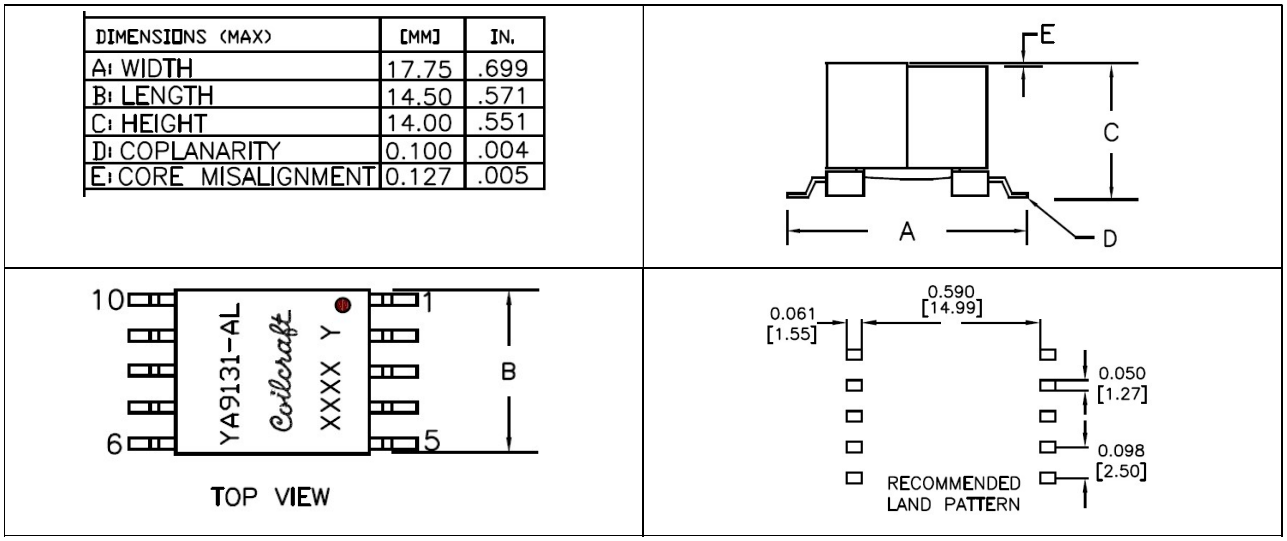


Figure 12 Transformer build diagram

9 Test results

9.1 Efficiency

Efficiency measurements are performed at room temperature and at 13.5V input voltage. Here below the summary of the result. The system reaches a maximum efficiency value of 81.1% at 800mA load condition. The reverse battery diode has been by-passed for this analysis.

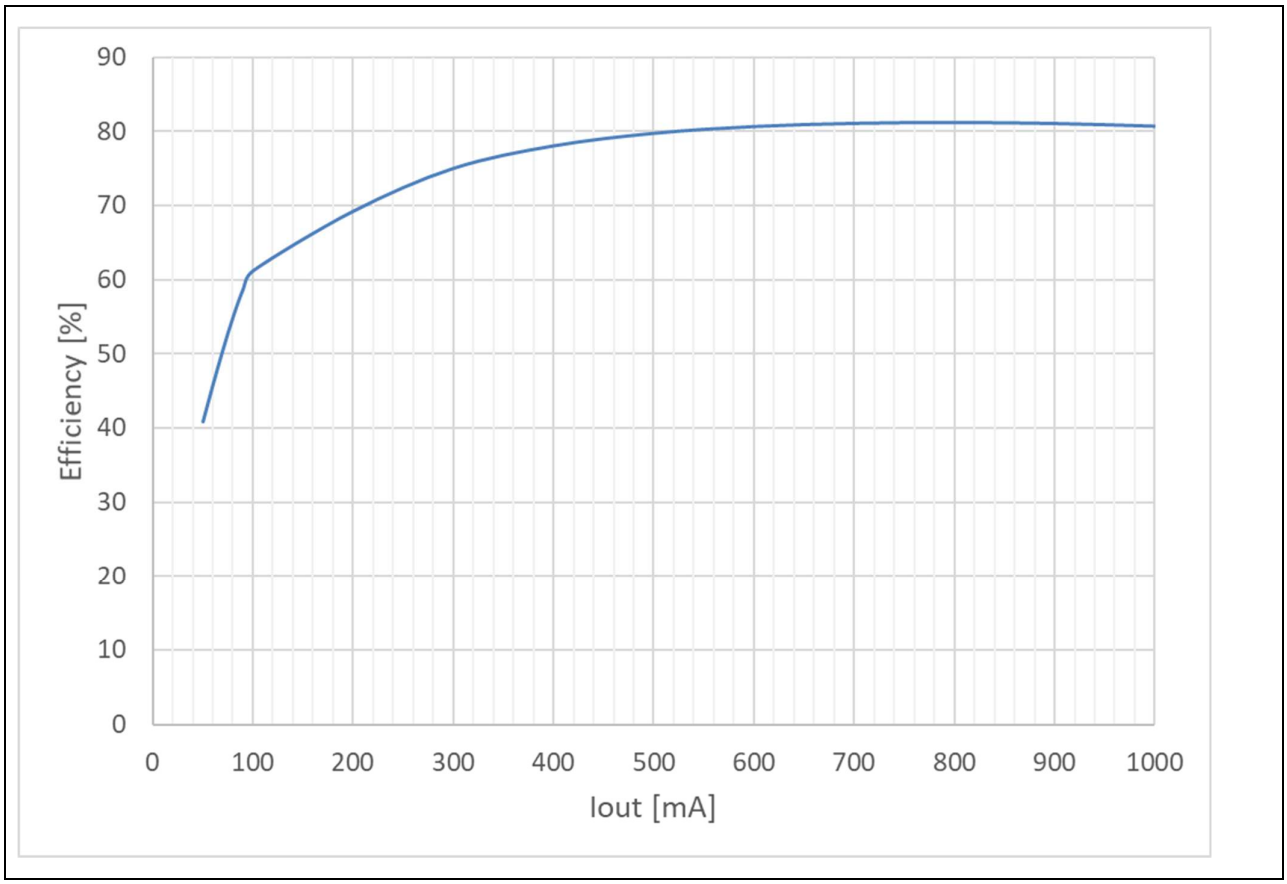


Figure 13 Efficiency versus output current voltage

9.2 Line and load regulation

Line and load regulation are both validated in the [6-35]Vin and [0-1]A ranges. Here below the summary curves. The reverse battery diode has been by-passed for this analysis. The line regulation remains within 2% and 6% of the average regulated voltage at 0.5A and 1.0A respectively. The load regulation remains within 8.5% over the full load and at 13V input voltage conditions.

Test results

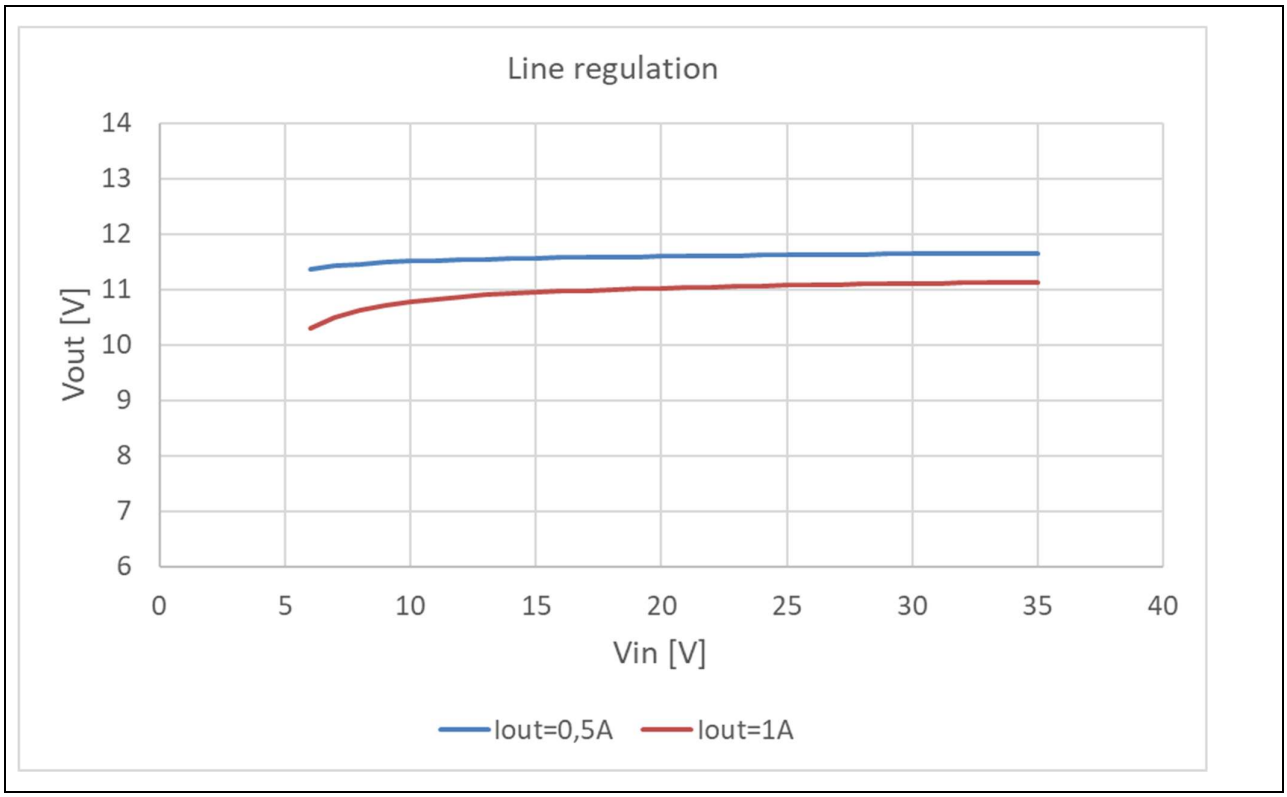


Figure 14 Line regulation at both half full load conditions

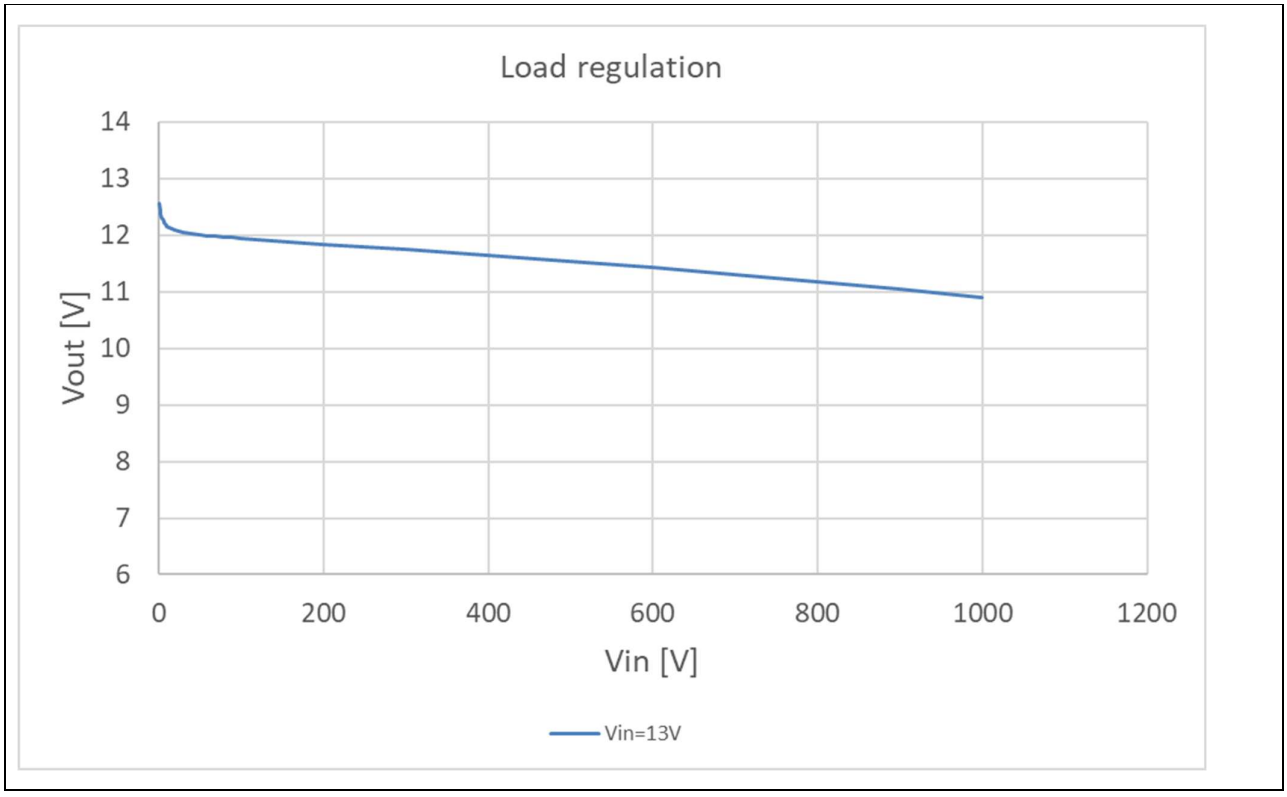
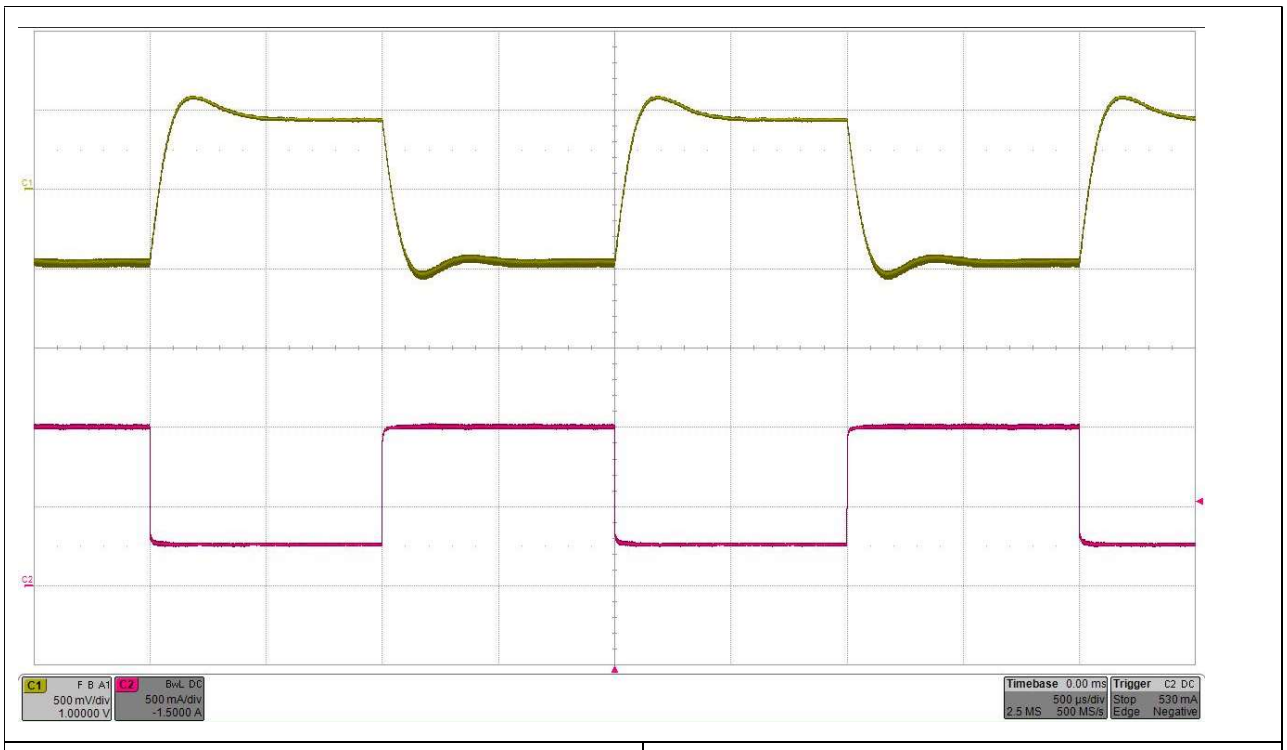


Figure 15 Load regulation at 13Vin input voltage condition.

9.3 Load Step Response

Load step response of the system is shown in the following picture. Multiple load steps from 0.25A to 1A has been applied with ripple voltage of about 1V.



CH1: Vout (AC coupled)) (green curve)	**CH2:** Iout (magenta curve)

Figure 16 Output voltage ripple

9.4 Thermal performance

Thermal performance of the board is shown in the following picture. It has been measured with an Infrared camera at 1A output load. The input voltage Vin was set at 12.5V.

Test results

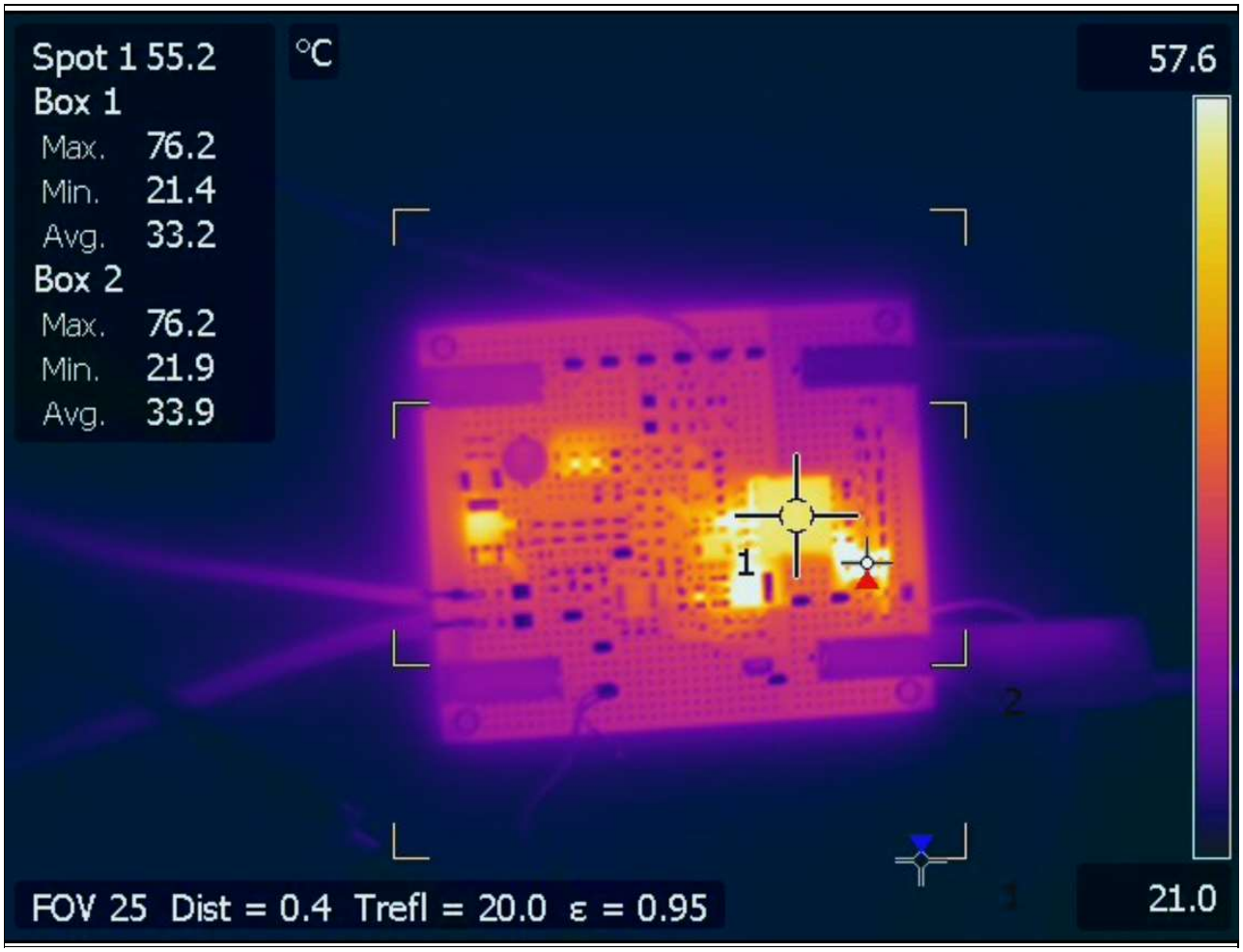


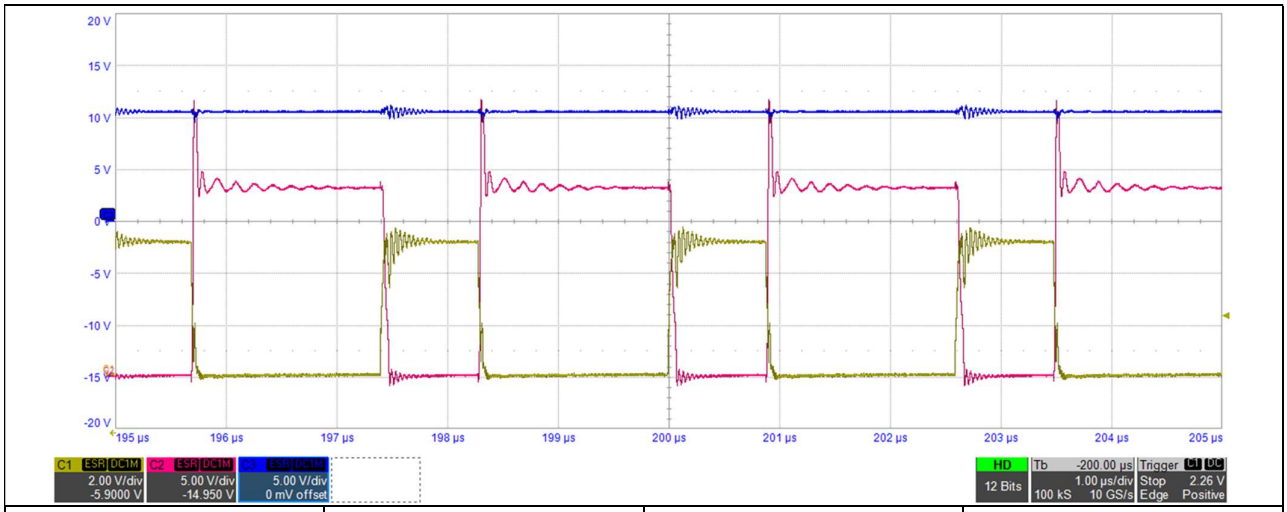
Figure 17 Thermal picture – top and bottom side

The hottest component is the diode D2, with a temperature of 76.2°C. The transformer temperature is 55.1°C at an ambient temperature of 22.5°C.

10 Waveforms

10.1 Switching waveforms at steady state

The following picture shows the switching waveforms at 1A load and 13Vin condition.

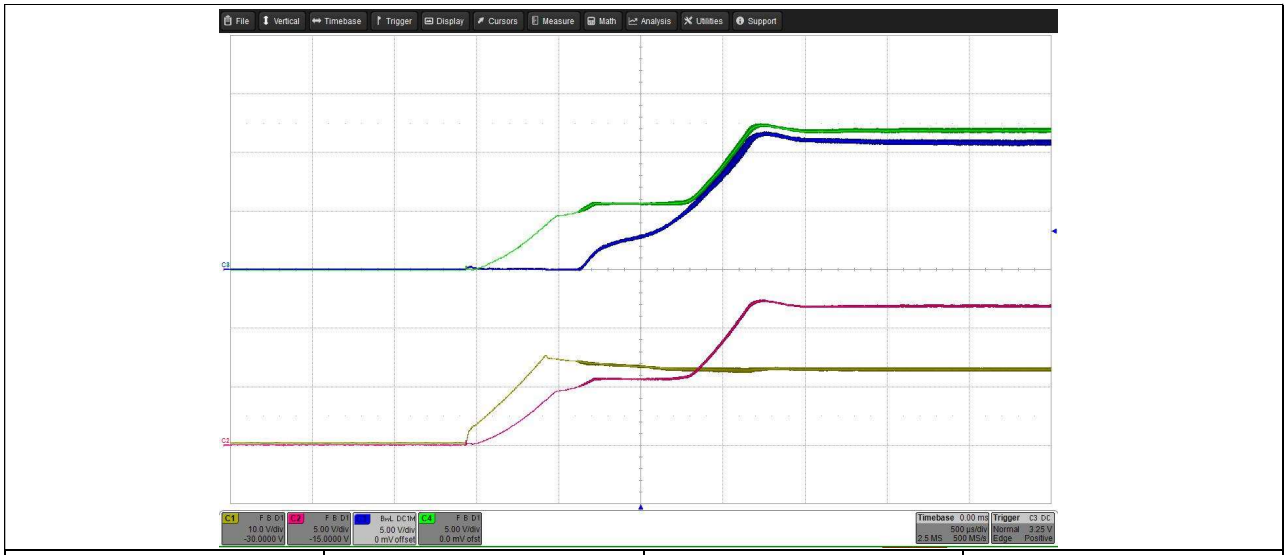


CH1: Vgate (Q1) (yellow)	**CH2**: Vdrain (Q1) (magenta)	**CH3**: Vout (blue)	

Figure 18 OPTIMOS™ drain and source voltage waveforms at 13Vin and full load

10.2 Startup

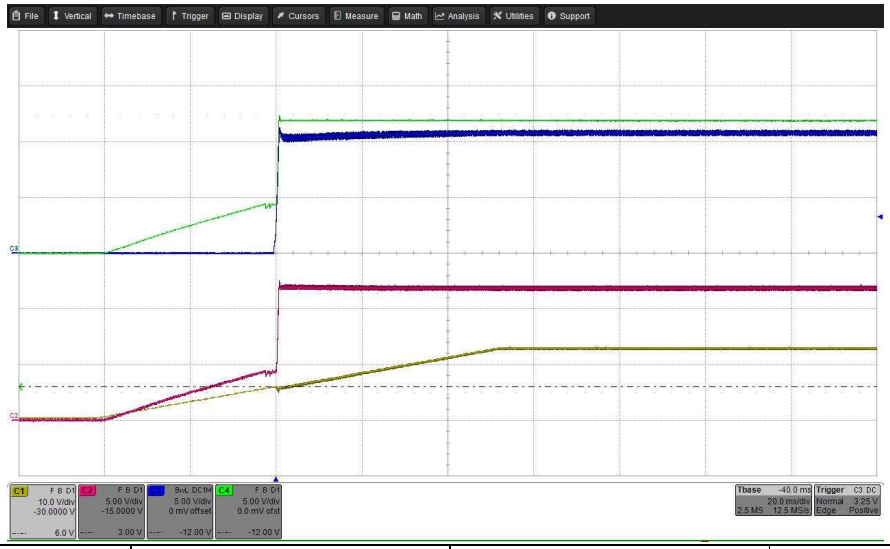
Following waveforms show the system startup behavior at 1A load and 13.5Vin conditions. The start up is shown with both a slow (i.e. 100ms) and a fast (i.e. 500us) input voltage ramp.



CH1: VIN (yellow)	**CH2&CH4**: V_aux (magenta)	**CH3**: Vout (blue)	500us Vin ramp

Figure 19 Startup profile with fast Vin ramp.

Waveforms



CH1: VIN (yellow)	**CH2&CH4**: V_aux (magenta)	**CH3**: Vout (blue)	500us Vin ramp

Figure 20 Startup profile with slow Vin ramp.

11 Evaluation board quick start guide

Following picture shows the evaluation board (EVM) that has been designed according to what described in this document.

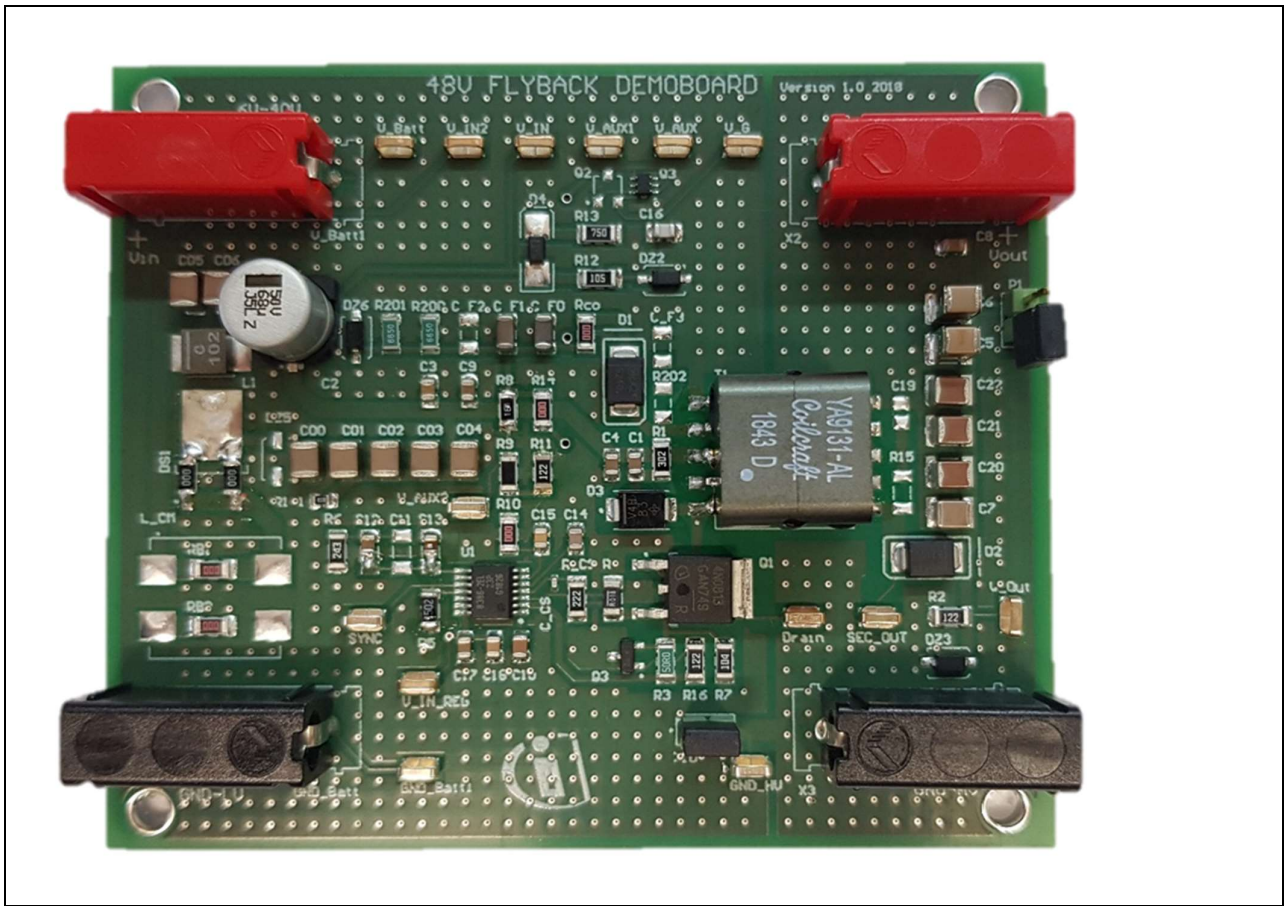


Figure 21 Figure. 34 Evaluation board picture

Please follow the procedure described here below for a quick start-up.

- Connect your input power supply to the VIN and GND_LV banana sockets. These are the positive and negative terminals respectively. The power supply has to set with a current compliance equal or higher than 3A for board operation in the whole input voltage range.
- Connect the load on the secondary side of the flyback through the connectors Vout and GND_HV – positive and negative terminals respectively.
- Use P1 connector for precise sensing of the regulated output voltage.
- Keep X10 mounted for shorting GND_LV and GND_HV reference voltages.
- Turn the input power supply on.

12 References

[1] Infineon Technologies, Datasheet TLE8386-2EL

[2] Infineon Technologies, Datasheet IPD50N08S4-13 OptiMOS™-T2

Revision history

Major changes since the last revision

Page or Reference	Description of change
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