The new OptiMOS™ 6 100 V family of MOSFETs

Latest Infineon trench MOSFET technology setting the new industry standard

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About this document

Scope and purpose

This document introduces Infineon's new OptiMOS™ 6 100 V family of MOSFETs. Based on Infineon's latest trench MOSFET technology, which takes advantage of a revolutionary cell design, the brand new OptiMOS™ 6 100 V brings together the benefits of exceptionally low on-state resistance and superior switching performance. These features make the OptiMOS™ 6 the best fit for high-switching frequency applications, supporting the trend toward significantly higher efficiency while enabling design for higher power densities and cost-effectiveness.

Typical applications for these MOSFETs include telecom, server and datacom as well as solar, drones, e-bikes power tools and other battery-powered applications (BPAs).

This application note showcases the performances achieved by using the new OptiMOS™ 6 100 V, focusing on fast-switching DC-DC telecom switch-mode power supplies (SMPS). First, a brief introduction to the technology, highlighting its technical benefits, is given. Next, an extensive experimental evaluation is carried out, comparing OptiMOS™ 6 100 V to the previous generation of OptiMOS™ 5 100 V MOSFETs.

Intended audience

This application note is targeted at application engineers and designers of telecom DC-DC SMPS.

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1 Introduction: The new OptiMOS™ 6 100 V

1.1 Features and benefits

In the development of a new silicon technology, special care must be taken in the definition of its specifications, in order to bring significant system-level advantages and added value to the customer. Infineon's 20+ years of experience in trench MOSFET technology development together with the system-level expertise gained by supporting customers in developing end applications are behind the development of the new OptiMOS™ 6 100 V.

The latest Infineon best-in-class (BiC) technology is specifically optimized for high-frequency SMPS. Showing the industry's best figure-of-merit (FOM), it helps with achieving high efficiency, high power density and high system reliability.

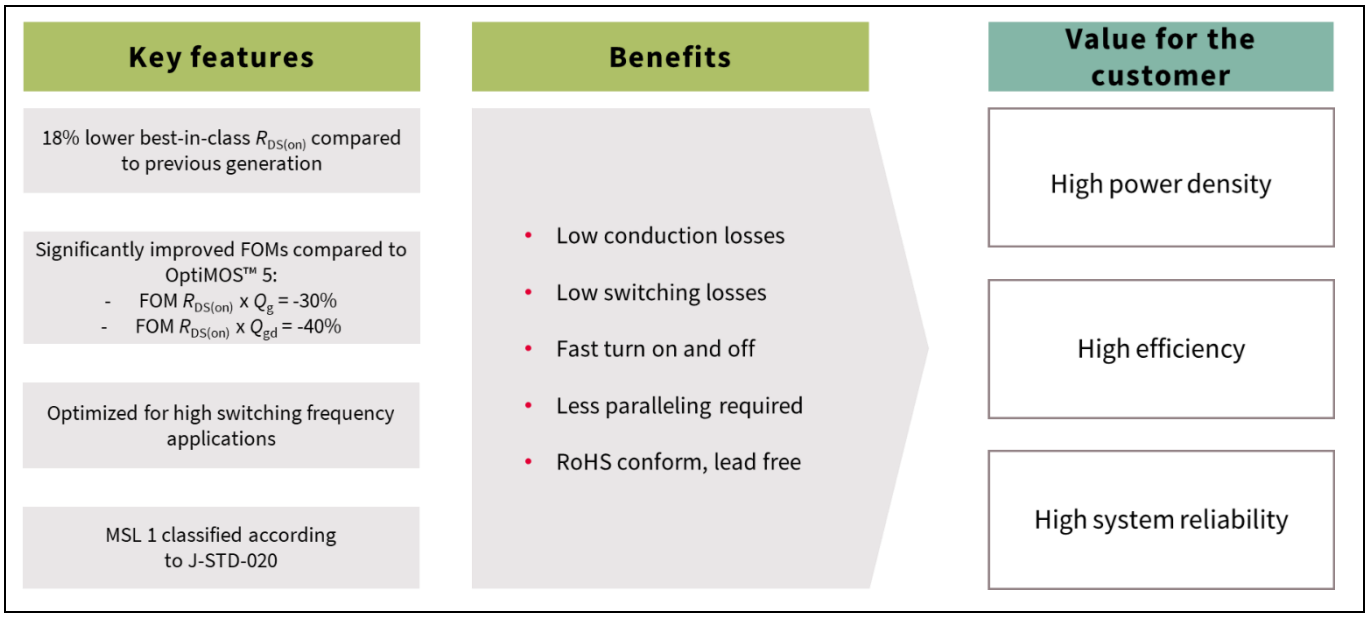


Figure 1 Key features and benefits of the new OptiMOS™ 6 100 V MOSFET technology

The new OptiMOS™ 6 100 V comes with a novel cell design, exploiting a full tri-dimensional charge compensation principle and enabling remarkable improvements in the specific on-state resistance. The new cell structure also comes with a completely redesigned gate-trench, leading to an outstanding reduction of the gate-to-drain charge Q_{gd} and total gate charge Q_g. The introduction of the metal gate technology enables ultimate switching uniformity throughout the die area, by precisely controlling the local R_g to its nominal value. The metal gate technology also proves an effective intrinsic barrier against dv/dt-induced parasitic re-turn-on of the MOSFET. Due to its lower resistivity compared to poly-silicon, it allows the most uniform gate potential distribution between the cells.

The new OptiMOS™ 6 100 V comes with a broad product portfolio (section **3**), and is packaged in SuperSO8 and PQFN 3.3x3.3, thus covering a wide range of applications.

1.2 Target applications

The new OptiMOS™ 6 100 V shows very well-balanced improvements across all the FOMs, a serious advantage for high-frequency SMPS operation, as well as solar, where losses are associated with both charges (switching) and on-state resistance (conduction).

Indeed, the new technology is specifically optimized for high-frequency SMPS, suitable for both hard- and soft-switching applications.

The BiC $R_{DS(on)}$ also enables OptiMOS™ 6 100 V to be used in low-voltage motor drives in BPAs such as drones, e-bikes and power tools, as well as for the disconnect switch in battery management systems (BMSs). A list of main applications targeted by the new Infineon OptiMOS™ 6 100 V is shown in **Table 1**.

Table 1 List of main applications targeted by the new Infineon OptiMOS™ 6 100 V

Application	Topology	Fitting
Telecom brick converters/SMPS	Hard-switched full-bridge/half-bridge	Primary-side MOSFETs
Telecom 5G RFPA PSUs	Cascaded: buck + DCX	Control/SR MOSFETs
Solar optimizers	Buck, buck-boost	Control/SR MOSFETs
Drones	B6 (3Φ, 2L inverter)	All positions
e-bikes	B6 (3Φ, 2L inverter)	All positions
Power tools	B6 (3Φ, 2L inverter)	All positions
BMSs	Battery protection switch	Series pass transistor

Figure 2 gives a more detailed overview of the possible applications targeted by the new Infineon OptiMOS™ 6 100 V.

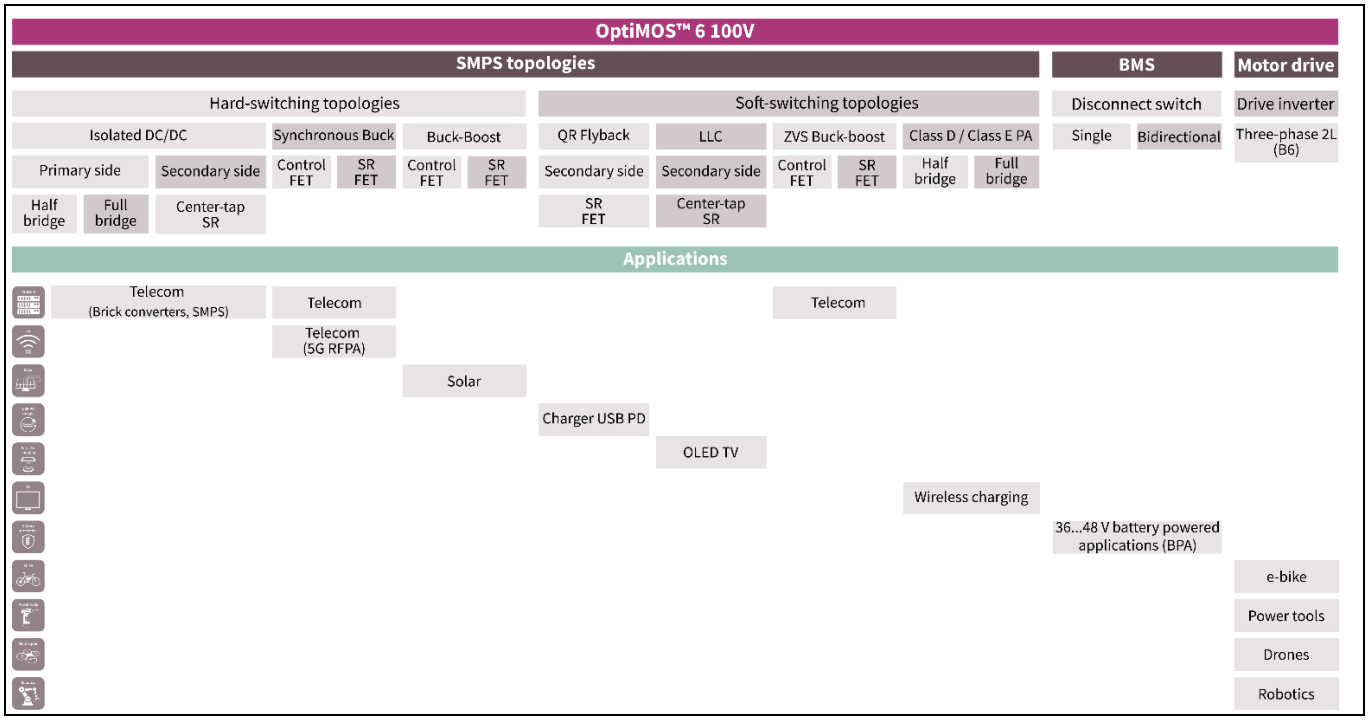


Figure 2 Overview of applications targeted by the new Infineon OptiMOS™ 6 100 V

1.3 Technology parameters comparison between OptiMOS™ 6 100 V and OptiMOS™ 5 100 V

In the following sections the latest OptiMOS™ 6 100 V technology will be compared with its predecessor, OptiMOS™ 5. First, the focus will be on single devices (BiC devices, i.e., with the minimum $R_{DS(on)}$) in the different families' portfolios. Later, the discussion will be generalized to the respective families by comparing the FOMs of the technologies.

1.3.1 Datasheet comparison for BiC devices

In **Table 2**, a datasheet comparison is given for BiC devices with OptiMOS™ 6 100 V and OptiMOS™ 5 100 V. The table focuses on parameters that are most important for high-switching frequency SMPS.

Table 2 Datasheet comparison between OptiMOS™ 6 100 V and OptiMOS™ 5 100 V BiC devices

Specification	Symbol	Unit	Conditions	Infineon OptiMOS™ 6 ISC022N10NM6		Infineon OptiMOS™ 6 ISC027N10NM6		Infineon OptiMOS™ 5 BSC027N10NS5	
Max. on-state resistance	$R_{DS(on)}$	mΩ	T_J = 25°C	2.24		2.7		2.7	
Thermal resistance, junction to case	R_{thJC}	°C/W	Case bottom (typ./max.)	0.29/0.59		0.34/0.69		0.4/0.7	
Max. junction temperature	$T_{J,max}$	°C		175		175		175	
Drain current	I_D	A	T_C = 25°C	230		192		194	
	$I_{D,pulse}$	A	T_C = 25°C	920		768		776	
Typ. charges	Q_{gs} Q_{gd} Q_g	nC	See notes [1) 2)]	27[1)] 12.6[1)] 73[1)]	24[2)] 11.9[2)] 73[2)]	21.6[1)] 10.1[1)] 58[1)]	19[2)] 9.6[2)] 58[2)]	28[1)] 18[1)] 89[1)]	28[2)] 18[2)] 89[2)]
Typ. input capacitance	C_{iss}	pF	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	5400		4300		6300	
Typ. output capacitance	C_{oss}	pF	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	1200		960		970	
Typ. reverse transfer capacitance	C_{rss}	pF	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	19		16		43	
Typ. output charge	Q_{oss}	nC	V_{GS} = 0 V, V_{DS} = 50 V	135		107		114	

[1)] Value given for the conditions: V_{DD} = 50 V, I_D = 67 A.
[2)] Datasheet published value. Value depends on the datasheet-defined operating conditions.

1.3.2 On-state resistance $R_{DS(on)}$

The new OptiMOS™ 6 100 V technology shows significant improvement in terms of specific on-state resistance, compared to the previous generation of OptiMOS™ 5 100 V MOSFETs. The specific on-state resistance is an important parameter of the technology.

Figure 3 shows the comparison between the maximum on-state resistance, specified for a gate-to-source voltage V_{GS} = 10 V, declared in the datasheet of BiC products of the OptiMOS™ families. The BiC OptiMOS™ 6 100 V, packaged in SuperSO8, records a decrease of 18 percent in $R_{DS(on)}$ compared to the previous BiC OptiMOS™ 5 100 V.

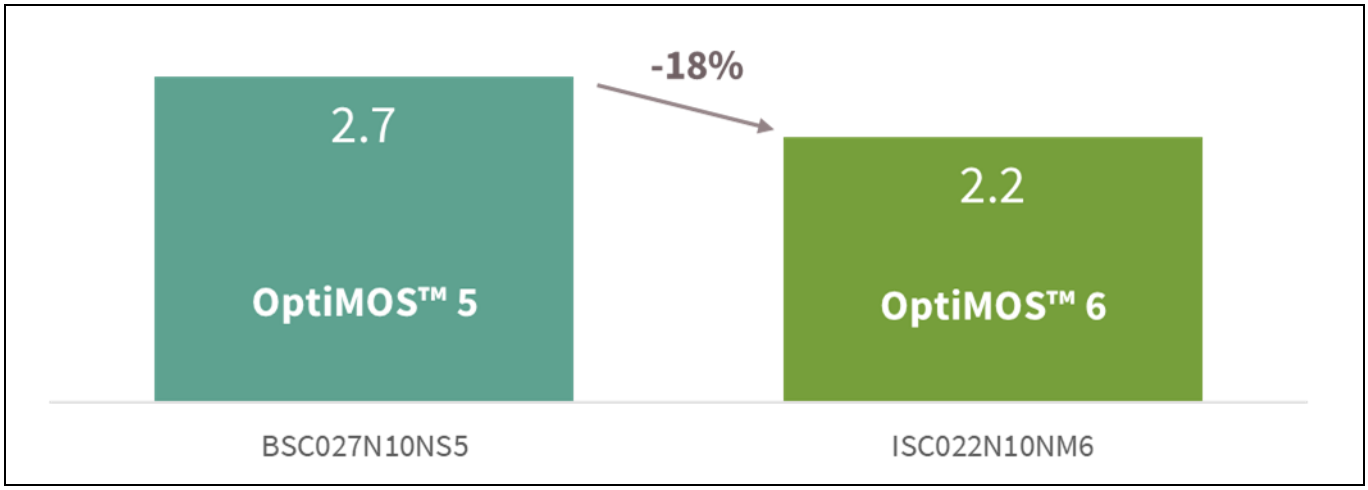


Figure 3 Comparison between the maximum on-state resistance (mΩ) for the BiC 100 V MOSFETs in PQFN 5x6

The new OptiMOS™ 6 100 V comes with the industry's best specific on-resistance FOM. This brings a series of advantages for the end applications, such as:

1. Reduction of conduction losses by a factor of up to 18 percent.
2. The improvement in $R_{DS(on)}$ would enable reduction of the number of paralleled MOSFETs, saving both cost and PCB real estate and improving the power density.
3. Depending on the application, it would be possible to choose a smaller package (e.g., PQFN 3.3 x 3.3) without compromising the $R_{DS(on)}$.
4. For the same $R_{DS(on)}$ – compared to OptiMOS™ 5 – the new OptiMOS™ 6 100 V will bring price/performance benefits with improved efficiency, as will be shown in section **2.1**.

1.3.3 Technology FOM_g, and gate-to-drain charge figure-of-merit FOM_{gd}

The innovative gate-trench engineering of the new OptiMOS™ 6 100 V leads to an outstanding reduction of both gate-to-source and gate-to-drain specific capacitances. This is reflected in the gate figures of merit FOM_g and FOM_{gd}, with an improvement of 30 percent and 43 percent respectively, when compared to the previous generation of OptiMOS™ 5 100 V MOSFETs (**Figure 4**).

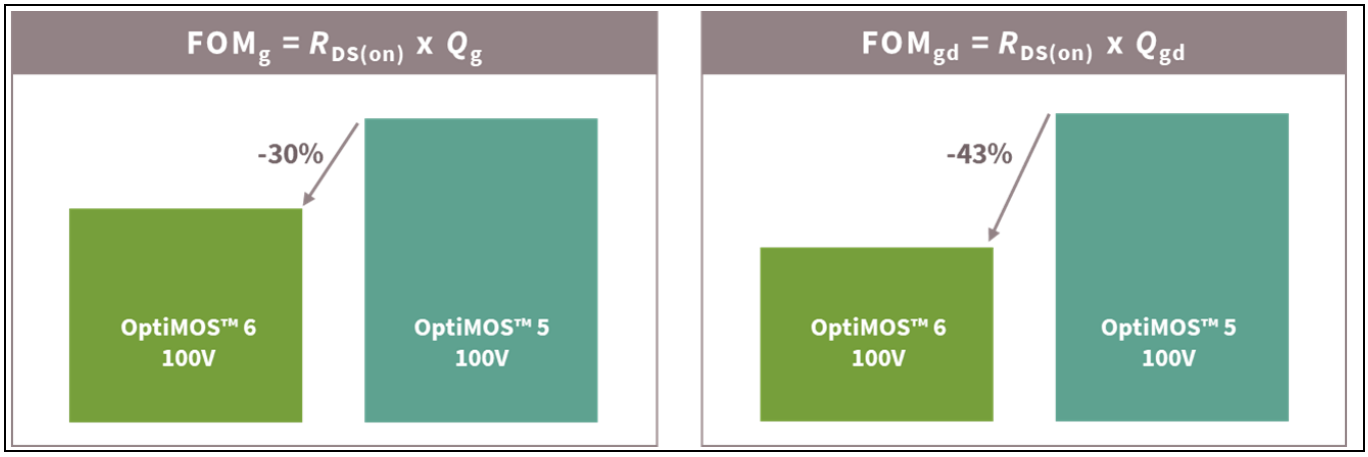


Figure 4 Comparison of gate charge and gate-to-drain charge FOM_g and FOM_{gd} for OptiMOS™ 5 100 V and OptiMOS™ 6 100 V families

The FOM_g – usually referred to simply as FOM – represents a synthetic performance indicator of a technology, and it is usually expressed as mΩ x nC. $R_{DS(on)}$ is a measure of the conduction losses, while Q_g impacts on both the driving losses and part of the switching losses, as it embeds Q_{gd}. In order to minimize the total losses, both $R_{DS(on)}$ and Q_g need to be minimized: the lower the FOM the better, as this minimizes the product of both of these quantities.

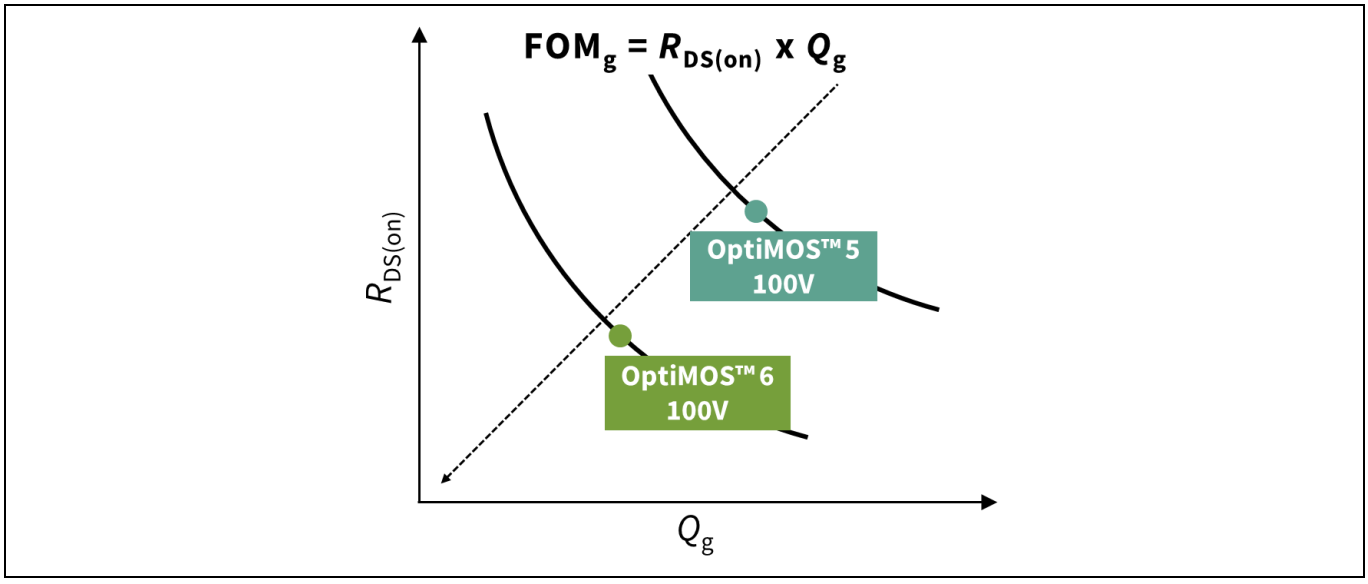


Figure 5 FOM imposes a trade-off between $R_{DS(on)}$ and Q_g for a given technology

For a given technology, it is not possible to reduce the $R_{DS(on)}$ without impacting the charges, because this requires a bigger chip or parts paralleling. The only way to bring an improvement in both $R_{DS(on)}$ and Q_g is by moving to a new technology, with a better FOM (**Figure 5**).

In **Figure 6** the gate charge characteristics for devices with the same $R_{DS(on),max}$ of 2.7 mΩ are plotted, available in both OptiMOS™ 6 100 V (ISC027N10NM6) and OptiMOS™ 5 100 V (BSC027N10NS5) product portfolios, in a SuperSO8 package. The new OptiMOS™ 6 100 V ISC027N10NM6 shows an outstanding reduction of 35 percent of total gate charge compared to its equivalent in the OptiMOS™ 5 100 V family. The improvement recorded in gate-to-drain charge, under the particular conditions of the test, is an exceptional -45 percent, again with respect to the previous generation of OptiMOS™ 5.

The Q_g reduction translates to better efficiency – especially in light-load conditions – due to reduced driving losses $P_{aux} = Q_g \times U_{GG} \times f_{sw}$. This is of particular importance in high switching-frequency SMPS and in applications where a number of MOSFETs are paralleled, such as in motor drives. In the latter case, low Q_g also enables relaxation of the requirements in the driver current capability.

On the other hand, low Q_{gd} leads to fast-switching transients, lowering switching crossover losses, which are sometimes a non-negligible contributor to overall turn-off losses.

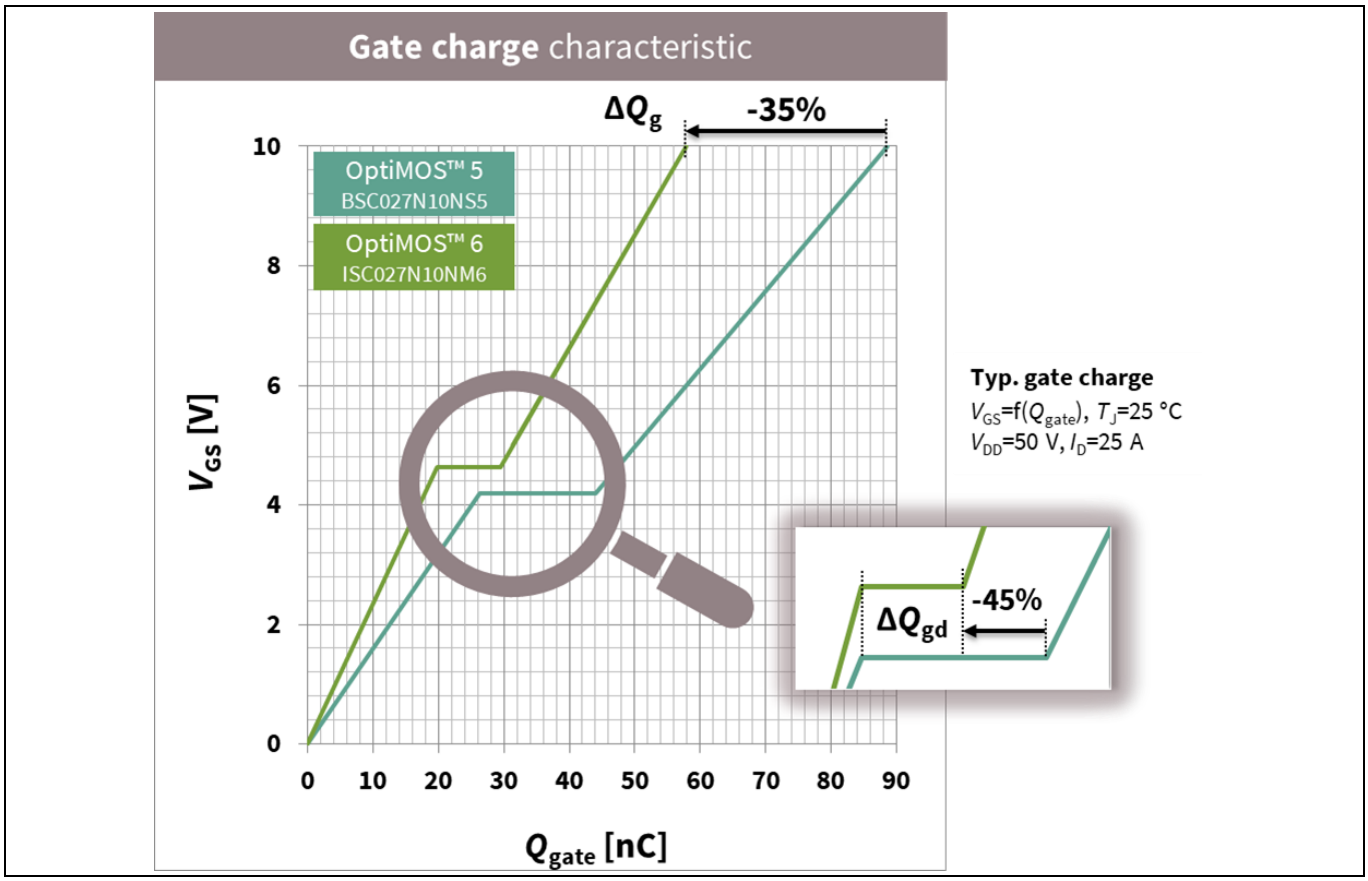


Figure 6 **Gate charge curves comparison between same-$R_{DS(on)}$ (2.7 mΩ) devices with OptiMOS™ 6 100 V (green) and OptiMOS™ 5 100 V (blue)**

1.3.4 Output charge figure-of-merit FOM_{oss}

The MOSFET output capacitance is charged in every switching cycle. In general, in hard-switched topologies, the stored energy cannot be recovered and generates a significant portion of the turn-on losses, because it is in fact dissipated across the channel during turn-on of the MOSFET.

Similarly to the technology FOM_g, the output charge figure-of-merit $FOM_{oss} = R_{DS(on)} \times Q_{oss}$ represents a synthetic indicator of how well the technology behaves in conduction and switching. Losses associated with Q_{oss} are increasingly important at high drain voltages, and scale linearly with the switching frequency. In general, in hard-switched high switching-frequency SMPS, it is desirable to have a low value for the output charge, in order to improve the efficiency.

The previous generation of OptiMOS™ 5 100 V MOSFETs already showed an outstanding output charge FOM, and therefore optimizations in OptiMOS™ 6 100 V focused on improving instead the gate-to-drain charge Q_{gd} and the total gate charge Q_g, and hence the corresponding FOMs, without impacting FOM_{oss} (**Figure 7**).

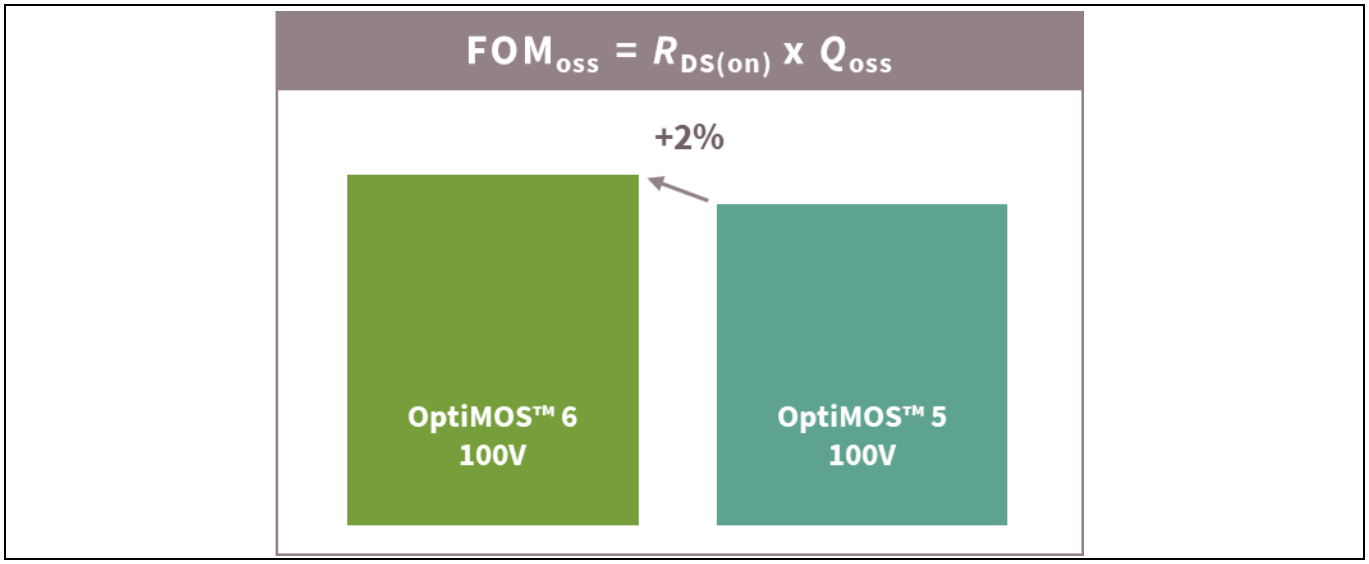


Figure 7 Comparison of output charge FOM_{oss} for the different technologies of 100 V MOSFETs

1.3.5 Transfer characteristic and safe operating area

The novel cell structure of the new OptiMOS™ 6 100 V also reflects the transfer characteristics of the MOSFET $I_D = f(V_{GS})$. The transfer characteristic is of particular importance when the MOSFET is driven to work in the linear region, that is when the MOSFET operates as a voltage-controlled current source. Because during the switching transient the MOSFET passes through the linear region of operation, the transfer characteristics also control the switching characteristics, such as the value of the Miller plateau voltage.

The transfer characteristics for BiC devices from the new OptiMOS™ 6 100 V family of MOSFETs and from the previous-generation OptiMOS™ 5 are compared (**Figure 8**). In OptiMOS™ 6, the particular design of the cell reflects a more gradual turn-on behavior of the MOSFET, hence it shows a slightly lower transconductance.

This is especially beneficial in applications other than SMPS, where the MOSFET is slowly switched or when the MOSFET is deliberately operated in the linear region, such as in hot-swap protection circuits. The advantage of a lower transconductance in these cases is that it enhances the robustness of the MOSFET against thermal runaway. Indeed, MOSFETs suffer from thermal instability at low current densities due to a positive feedback effect with temperature: for currents below the zero-temperature coefficient (ZTC) point, the transfer characteristics show a positive temperature coefficient, leading the hottest part of the chip to sustain more and more current, in turn increasing the temperature further. This self-sustaining phenomenon (current filamentation) leads to the formation of hotspots in the die, potentially leading to failures.

MOSFETs with a ZTC point placed at high drain currents are more susceptible to suffer from thermal runaway. The transfer characteristic of the new OptiMOS™ 6 100 V sees this point shifted to lower currents, while also showing a limited gain in transconductance over the junction temperature between 25°C and 175°C (**Figure 8b**), increasing robustness against thermal runaway. Together with an excellent junction-to-case thermal resistance, the new OptiMOS™ 6 shows significant safe operating area (SOA) improvement, as is clear from the comparison in **Figure 9**.

For a better insight into the thermal runaway phenomenon in MOSFETs and its origin, please refer to Infineon application notes **[1]**, **[2]**.

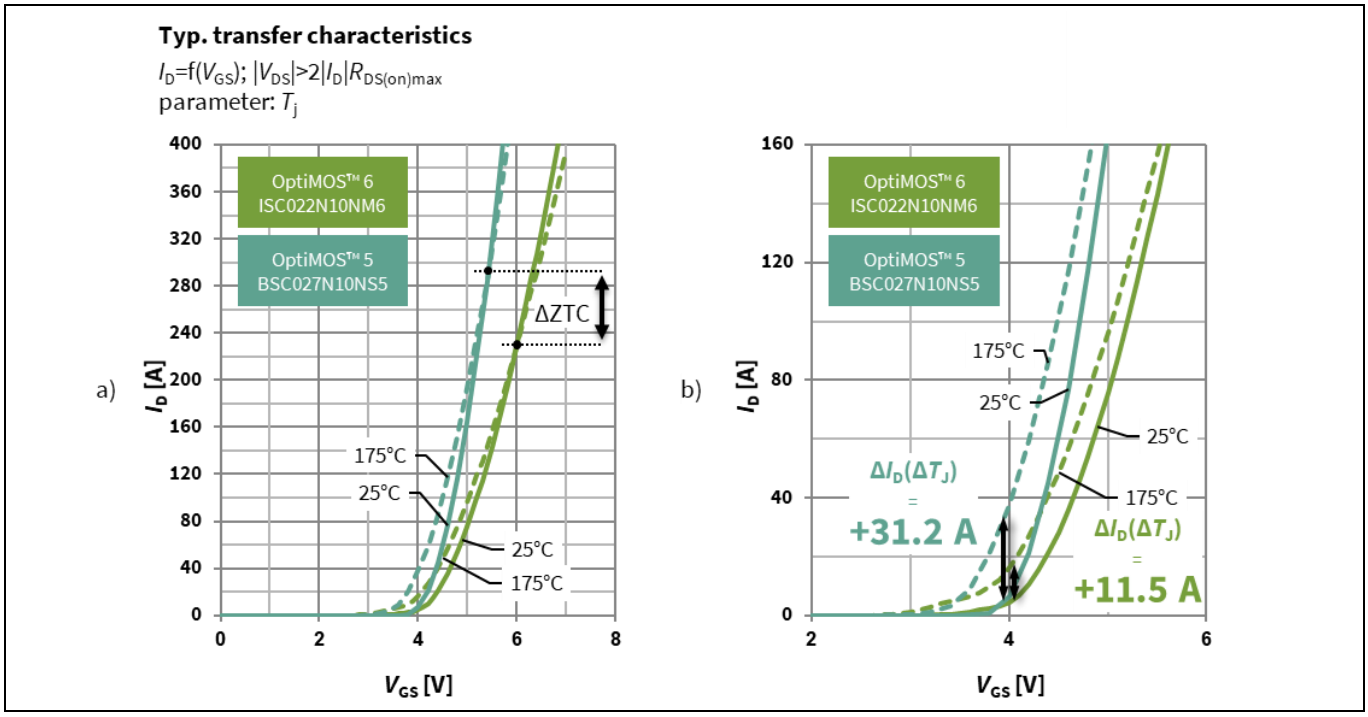


Figure 8 **Comparison of typical transfer characteristics of BiC devices from OptiMOS™ 5 100 V and OptiMOS™ 6 100 V families of MOSFETs**

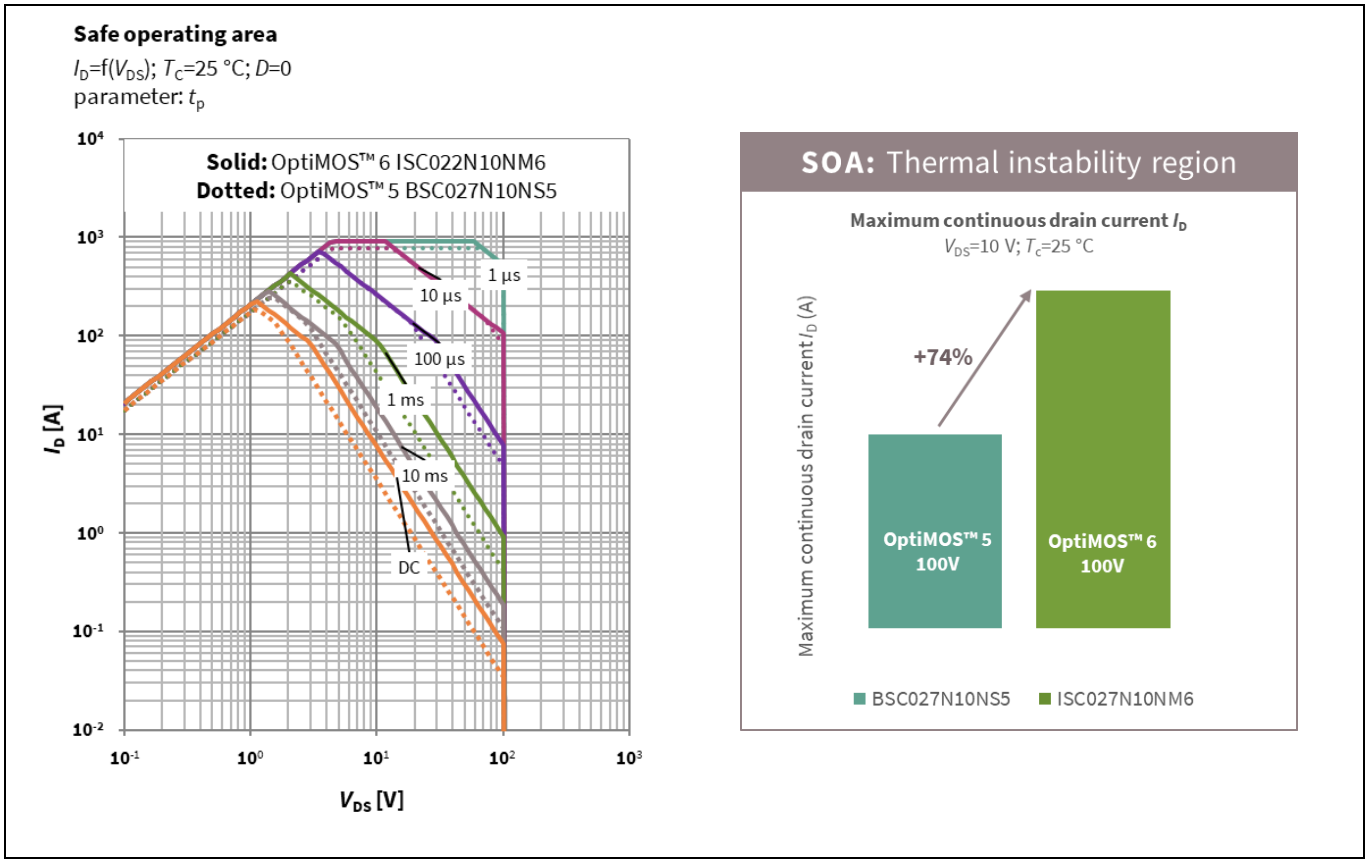


Figure 9 **Left: SOA comparison between BiC devices selected from OptiMOS™ 6 100 V and OptiMOS™ 5 100 V families of MOSFETs. Right: improvement in DC current capability in linear operation due to SOA improvement**

Note: The SOA diagram is provided within the ideal case of package temperature held at T_C = 25°C. When power pulse is applied, junction temperature rises according to the transient thermal impedance Z_{thjC}. In Infineon's OptiMOS™ power transistor datasheets, the $R_{DS(on)}$-limited region is traced, considering the worst-case value for the on-state resistance, i.e., the maximum value expected at T_J = 175°C.

In improving modern trench MOSFET technologies, a narrowing trend in SOA was observed as a trade-off for the lowering of specific on-state resistance. The new OptiMOS™ 6 100 V technology comes with a wider SOA, especially for power pulses in the millisecond range, without compromising the $R_{DS(on)}$. This would make the new OptiMOS™ 6 100 V a feasible candidate for BMSs as a protection switch, or in telecom as a hot-swap switch.

2 Experimental results

In the following sections experimental results are reported, focusing on actual state-of-the-art implementations for high-frequency SMPS.

Experimental evaluations are carried out for two different SMPS applications:

1. The first application presented is a telecom DC-DC intermediate bus converter (IBC), in a distributed-power open standards alliance (DOSA) quarter-brick form factor. The converter is based on a full-bridge topology with full-bridge rectification, where both conduction and switching losses impact the overall system efficiency, due to its hard-switching nature. The right fit for this application is a device combining the lowest possible $R_{DS(on)}$ with the need for low charges, and the best fit – for a typical 600 W converter – is found in devices in the ~6 mΩ range. The new OptiMOS™ 6 100 V ISC060N10NM6, 6 mΩ $R_{DS(on),max}$ packaged in SuperSO8 is compared in this application with the BSC050N10NS5 from the previous generation of OptiMOS™ 5 MOSFETs.
2. The second application presented is a telecom DC-DC converter based on a zero-voltage switching (ZVS) inverting buck-boost topology. In this soft-switching application the dominant source of losses arises from conduction, hence the right-fit device is the BiC, showing the lowest possible $R_{DS(on)}$. The new OptiMOS™ 6 100 V ISC022N10NM6, 2.2 mΩ $R_{DS(on),max}$ packaged in SuperSO8 is compared in this application with the BSC027N10NS5 from the previous generation of OptiMOS™ 5 MOSFETs.

For both applications, efficiency measurements, thermal data and waveforms are provided for comparison.

2.1 Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter

2.1.1 Introduction

Within a telecom or datacom power system, an isolated DC-DC IBC is typically employed in the conversion chain, to take a nominal -48 V input and generate a 12 V bus for the downstream point-of-load (PoL) converters (**Figure 10**). It is common for this architecture to be implemented with a modular approach. Modularity specifically addresses:

- Standardization
- Scalability
- Fault tolerance
- Simple maintenance

This is necessary to satisfy the demanding requirements of a telecom power system. IBCs usually come as power modules, in a family of standardized form factors and footprints set by the DOSA and commonly known as brick power modules. Brick converters are available from several established manufacturers, and the standard design potentially allows them to be interchanged, without changing the backbone PCB design. The standard defines only the set of mechanical outlines and the footprint for the power modules, while no electrical specifications are given. This means that modules can be designed according to different applications (telecoms, datacoms), type of system (-48 V, -60 V) or requirements imposed by the downstream PoLs. Specifically, different power-conversion topologies may be implemented, either unregulated or regulated. Unregulated topologies work like DC transformers (DCX), and generally show the best efficiency, while they rely on a tightly regulated input voltage to provide an output within specification. Regulated topologies, despite being somewhat less efficient, are usually needed to deal with the full telecom range, extending from -75 V to -36 V **[3]**.

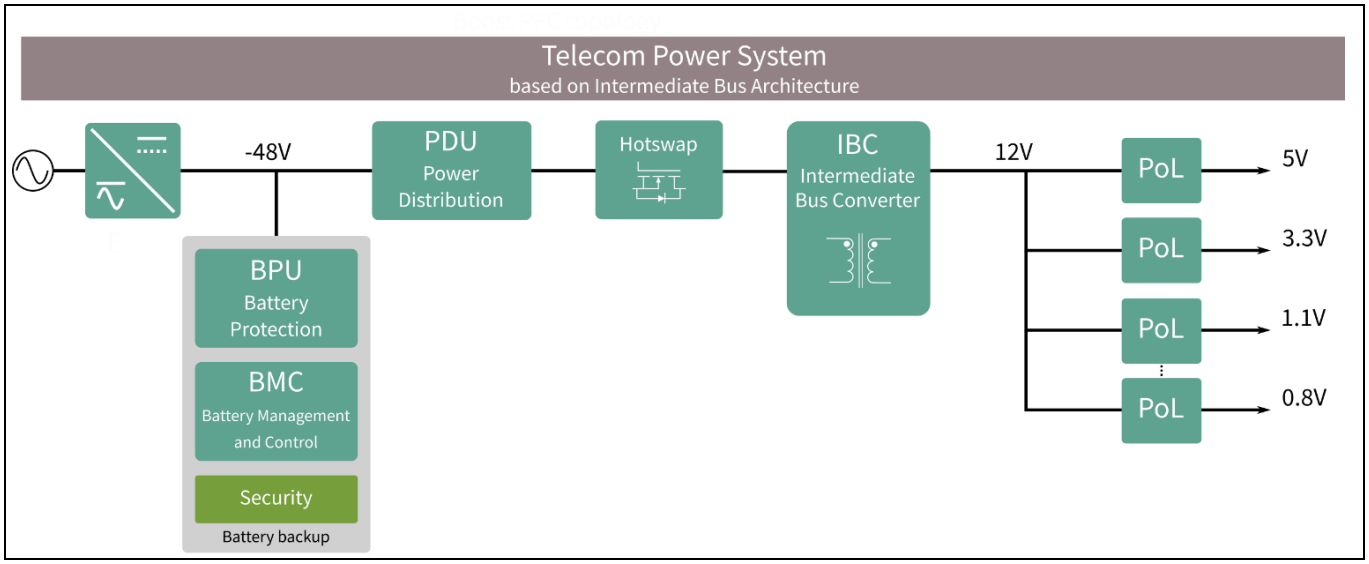
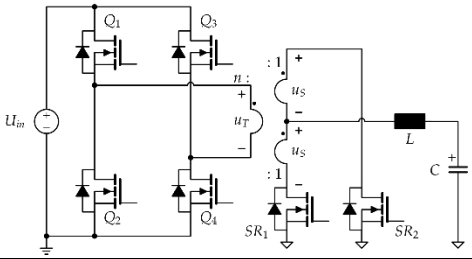
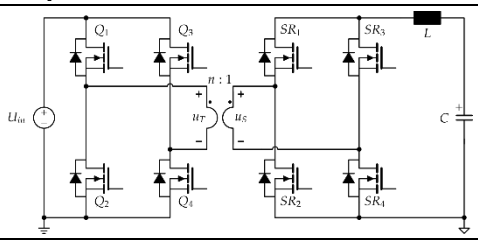


Figure 10 **Simplified schematic representation of a typical telecom power system based on the Intermediate Bus Architecture (IBA)**

In recent years, the quarter-brick format affirmed itself as the industry standard. Most typical power-conversion architectures for IBCs embracing this form factor are hard-switched and buck-derived; namely the half-bridge and the full-bridge forward-type converters. The synchronous rectification (SR) stage can either take advantage of a center-tapped transformer design or may be configured as a bridge. **Table 3** shows the simplified schematic diagrams for these topologies.

The continuous improvement in MOSFET technology in recent years has enabled the power density to increase steadily. Presently, according to datasheets published by the main manufacturers, an IBC in a standard quarter-brick typically delivers power in the range of 600 W. Infineon has developed a fully functional quarter-brick IBC evaluation unit, operating from an input voltage range of 36 to 75 V DC that provides up to 600 W output power. The unit will be introduced in the next paragraph, and is used as a first testbench to showcase performances achieved by using the new OptiMOS™ 6 100 V in a real application.

Table 3 **Full-bridge hard-switching topologies typically adopted for standard quarter-brick designs**

Topology	Circuit schematic	Cost/complexity	Efficiency	Output power
Full-bridge with center-tapped rectification (FB-CT)		Lowest cost, due to minimal part count and simpler driving on the secondary side, avoiding the use of HB drivers.	High	300 to 600 W
Full-bridge with full-bridge rectification (FB-FB)		High cost. Four SRs are required for rectification, together with two HB drivers.	Highest	600 to 800 W

2.1.2 System description

Infineon has developed a fully functional IBC evaluation unit, operating from an input voltage range of 36 to 75 V DC. The design follows the DOSA mechanical outline for high-current quarter-bricks, and regulates 12 V DC output voltage, providing up to 600 W output power.

IBCs are required to provide functional isolation. Infineon designed the main power stage to be a full-bridge topology with full-bridge SR (FB-FB), considered the best approach for these power and voltage ranges.

The outstanding performance ensured by Infineon semiconductors, the innovative cooling concept solution and the planar magnetic construction enable power density in the range of 22 W/cm^3 (360 W/in^3). The board was designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components. The module is equipped with an onboard auxiliary housekeeping supply to provide the required bias.

This Infineon 600 W isolated FB-FB quarter-brick operates in a variety of thermal environments, and sufficient cooling should be provided to ensure reliable operation.

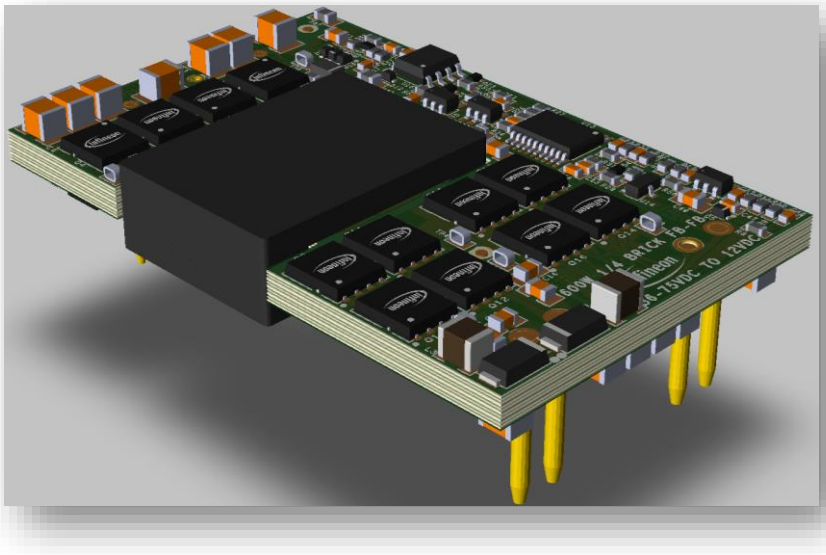


Figure 11 3D view of the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick converter

2.1.2.1 PCB description

Figure 12 shows the placement of the different components and measurement test points on the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick converter. The outer dimensions of the board, designed without enclosure, are 2.3 in. x 1.45 in. x 0.5 in. (58.42 mm x 36.83 mm x 12.7 mm), which results in a power density in the range of 22 W/cm^3 (360 W/in^3).

The PCB is fabricated from a 10-layer board. The internal layers are all 5 oz. copper (6.88 mil, 0.174 mm) thickness with the top and bottom layers at 4 oz. copper (5.5 mil, 0.140 mm) thickness. The total board thickness is 118 mils (3 mm).

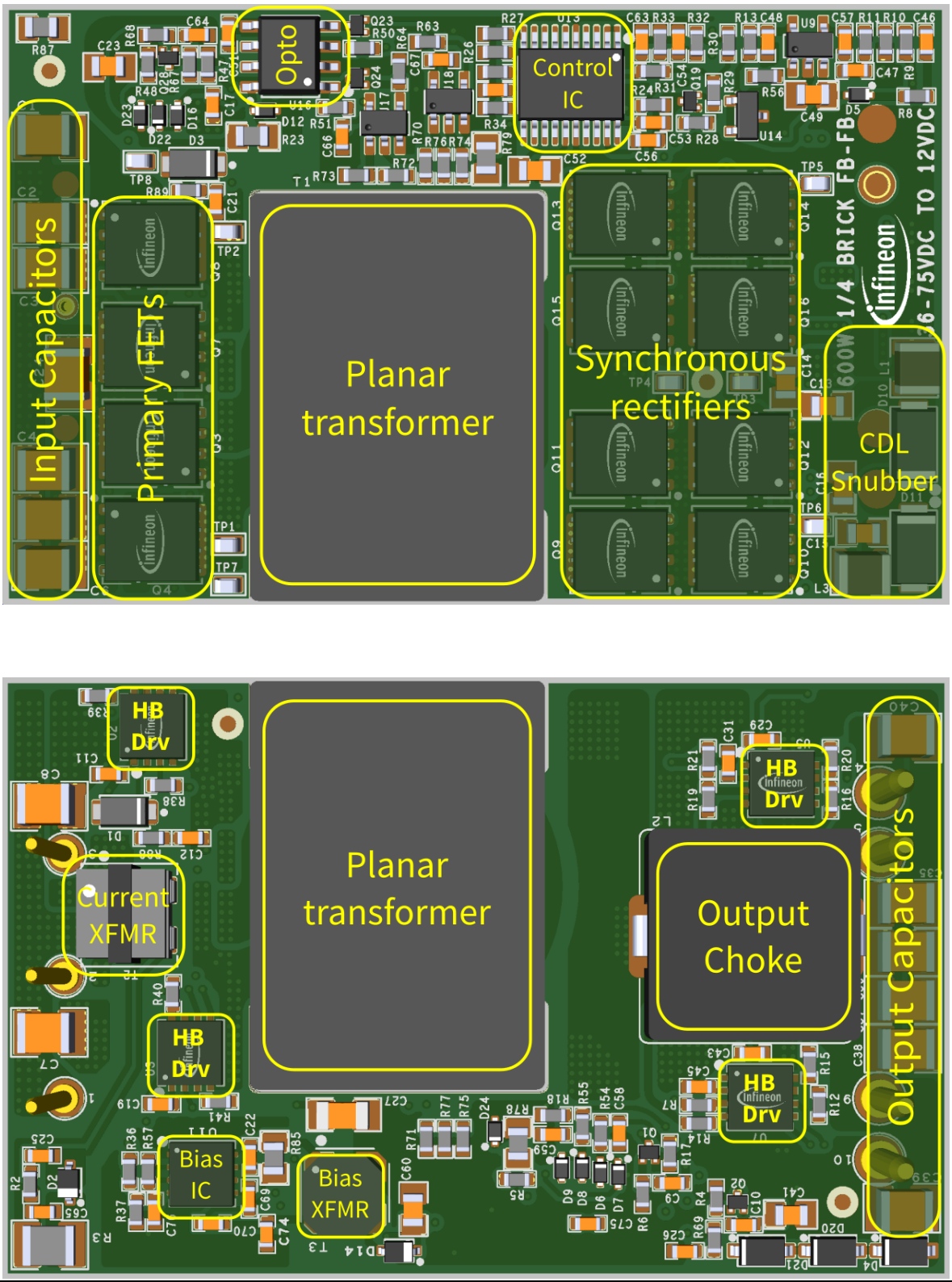


Figure 12 **Placement of the most significant components in the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick converter**

2.1.2.2 Board specifications

The specifications for the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter are given in **Table 4**.

Table 4 Specifications for the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Operating input voltage	V_{in}	36	48	75	V	
Input current RMS value	$I_{in,RMS}$		16 13 9		A	V_{in} = 36 V, P_{out} = 600 W V_{in} = 48 V, P_{out} = 600 W V_{in} = 75 V, P_{out} = 600 W
Efficiency	η	95.5%				V_{in} = 48 V, P_{out} = 420 W
Start-up voltage threshold	$UVLO_{(on)}$	32		36		
Minimum operating voltage after start-up	$UVLO_{(off)}$	29		34		
Output power	P_{out}	0		600	W	
Output voltage set-point	$V_{out,nom}$		12		V	Output regulation is achieved for V_{in} = 42 V to 75 V
Output voltage set-point tolerance	$\sigma V_{out,nom}$	-3		3	%	
Power dissipation	P_{diss}		25			
Relative output voltage regulation (load)	$\Delta V_{out}/V_{out}$			0.5	%	
Relative output voltage regulation (line)	$\Delta V_{out}/V_{out}$			0.5	%	
Output ripple and noise			120		mVpp	Measured with 0.1 µF ceramic capacitor in parallel with 10 µF tantalum capacitor, at 25°C
Output DC current	I_{out}			50	A	
Maximum output capacitance	$C_{out,max}$			1500000	µF	
Switching frequency	f_{sw}		250		kHz	
Airflow velocity	v_{air}		600 3		LFM m/s	
Functional isolation voltage	V_{iso}		1500		V	

2.1.2.3 Board schematics

The schematic diagram for the main power stage of the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter is shown in **Figure 13**.

Main power stage

The Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter has been designed with Infineon power semiconductors as well as Infineon gate drivers. In the design of the board:

- OptiMOS™ 5 100 V BSC050N10NS5, 5 mΩ in SuperSO8 package is intended to be used in the primary side of the full-bridge converter. The board is designed to fit one device per position, with a total of four power MOSFETs.
- OptiMOS™ 6 40 V BSC010N04LS6, 1 mΩ in SuperSO8 package is used as SR in the secondary side of the full-bridge converter. Two devices per position are paralleled to handle the output current, with a total of eight power MOSFETs.
- 2EDL8124G EiceDRIVER™ dual-channel junction-isolated gate drivers are used in the primary-side bridge, offering differential inputs with built-in hysteresis for inherent shoot-through protection.
- 2EDL8024G EiceDRIVER™ dual-channel junction-isolated gate drivers are used in the secondary-side bridge, offering independent inputs with built-in hysteresis for enhanced noise immunity.

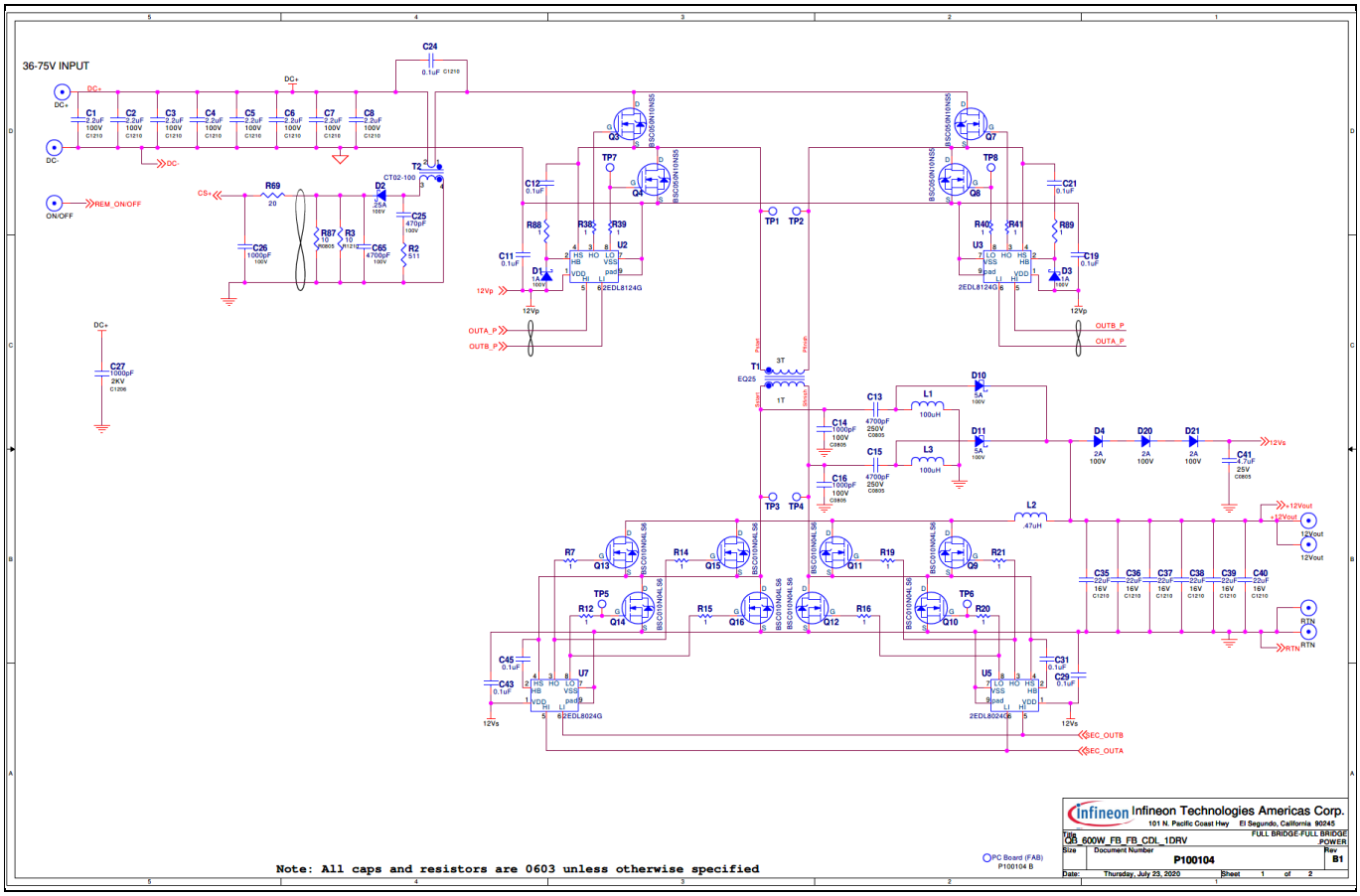


Figure 13 Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter. Schematic page 1: main power stage

2.1.3 Test setup description

2.1.3.1 Fixture board

The Infineon 600 W FB-FB 36 to 75 V to 12 V IBC, as a brick power module, is a board-mounted power supply. The backbone board must provide the necessary filter capacitor for the input and output ports, power connection terminals and a cooling fan. The power connections with the host board are made with press-fit connectors.

2.1.3.2 Description of the test setup

The actual test setup is shown in **Figure 14**. The test setup (**Figure 15**) is described here in detail.

Voltage source

- DC PSU capable of delivering at least 700 W, up to ~80 V DC
- Low-voltage, low-power DC PSU capable of providing 7 to 12 V DC to provide fan bias

Active load

- Low-voltage, high-current (more than 50 A) electronic load (operated in constant current mode)

Measurement instruments

- Input current precision current shunt resistor (20 A, 0.1 percent)
- Output current precision current shunt resistor (100 A, 0.1 percent)
- 4 x 6½ digits digital multimeters (DMMs) for input, output and shunt voltage measurement
- High-bandwidth (more than 500 MHz) digital oscilloscope (DSO) and passive voltage probes
- Thermal camera to acquire temperatures across the entire board

Test fixture board

In order to provide reliable and repeatable measurement data, it is helpful to test the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter in a proper test setup. Using Infineon's brick test fixture board is an easy way to accomplish this, with no soldering required. The test equipment is directly connected to the test fixture, while the brick module is easily plugged in and out, easing the reworking activities between different tests.

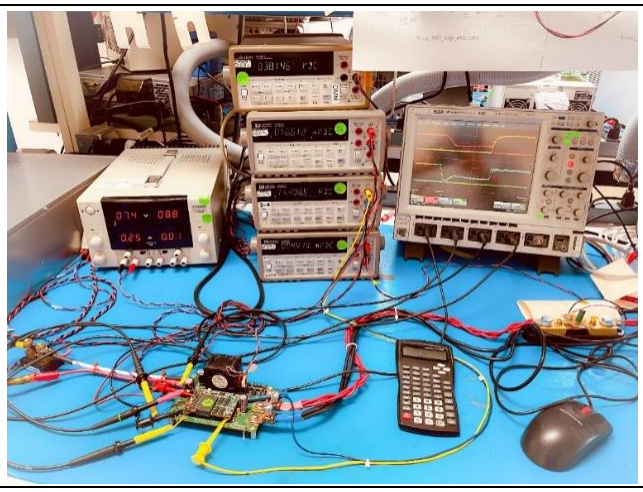


Figure 14 Actual test setup

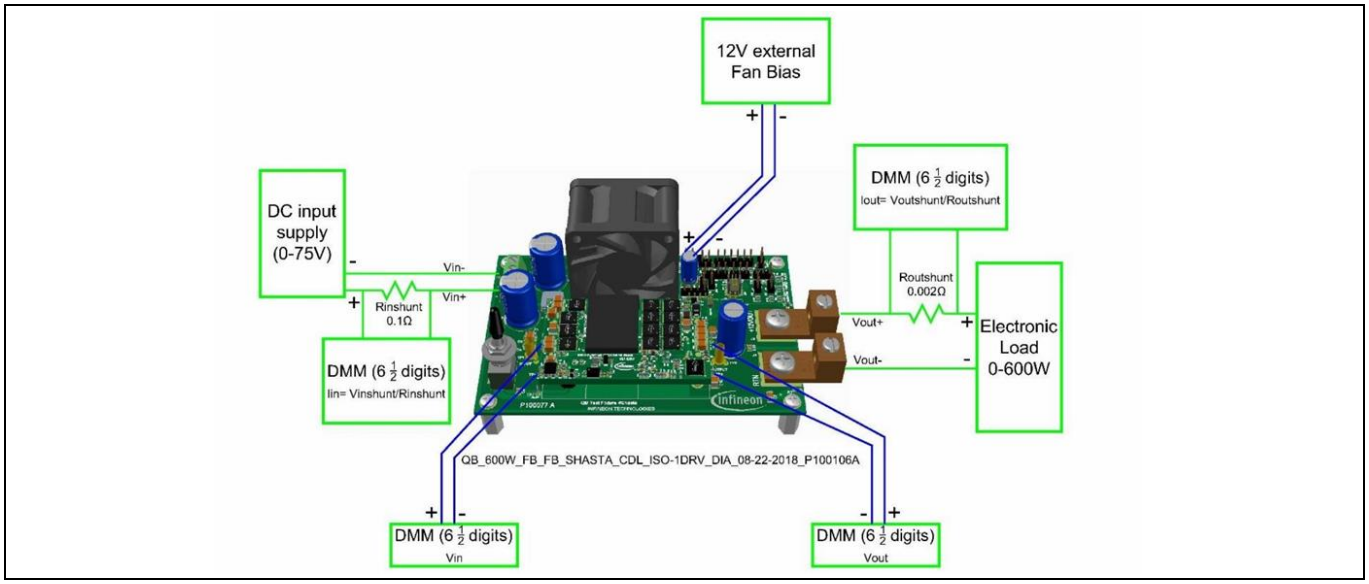


Figure 15 Test setup schematic description

2.1.4 Efficiency test

2.1.4.1 Introduction

Efficiency tests have been performed for the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter, using the test setup introduced in section **2.1.3 Test setup description**.

As shown in section **2.1.2.3 Board schematics**, the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter was originally designed using Infineon OptiMOS™ 5 100 V BSC050N10NS5 in the primary bridge. Efficiencies have been captured for the original design, as well as with the new Infineon OptiMOS™ 6 ISC060N10NM6 to replace the primary MOSFETs. Everything else is kept unchanged in the brick board and in the whole test setup. A summary of the devices under test (DUTs) and their position is given in **Table 5**.

Table 5 Devices under test – refer to schematic file reported in Figure 13

DUTs position	DUT #1	DUT #2
Primary-bridge MOSFETs: Q3, Q4, Q7, Q8	**Infineon OptiMOS™ 5** **100 V, 5 mΩ** BSC050N10NS5	**Infineon OptiMOS™ 6** **100 V, 6 mΩ** ISC060N10NM6

Note: The same unit as for the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter was used to acquire efficiencies. Efficiency is first acquired with a brand-new unit, using Infineon OptiMOS™ 5 100 V BSC050N10NS5 as primary MOSFETs, and then reworked to acquire efficiencies with the other DUT. This ensures a fair comparison between the DUTs.

2.1.4.2 Efficiency comparison at V_{in} = 48 V

Table 6 summarizes the efficiencies acquired at nominal input voltage (V_{in} = 48 V) for the different DUTs. The efficiency is measured at 600 LFM (3 m/s) airflow and captured after thermal steady-state is reached.

The efficiency curves, absolute and relative to the original setup employing OptiMOS™ 5 as DUTs, are reported respectively in Figure 16 and Figure 17.

Table 6 Measured efficiency (%) at nominal input voltage V_{in} = 48 V

Output current	Infineon OptiMOS™ 6 100 V, 6 mΩ ISC060N10NM6	Infineon OptiMOS™ 5 100 V, 5 mΩ BSC050N10NS5
5 A	88.49	87.80
10 A	92.55	92.14
25 A	95.57	95.37
35 A	95.80	95.64
50 A	95.51	95.37

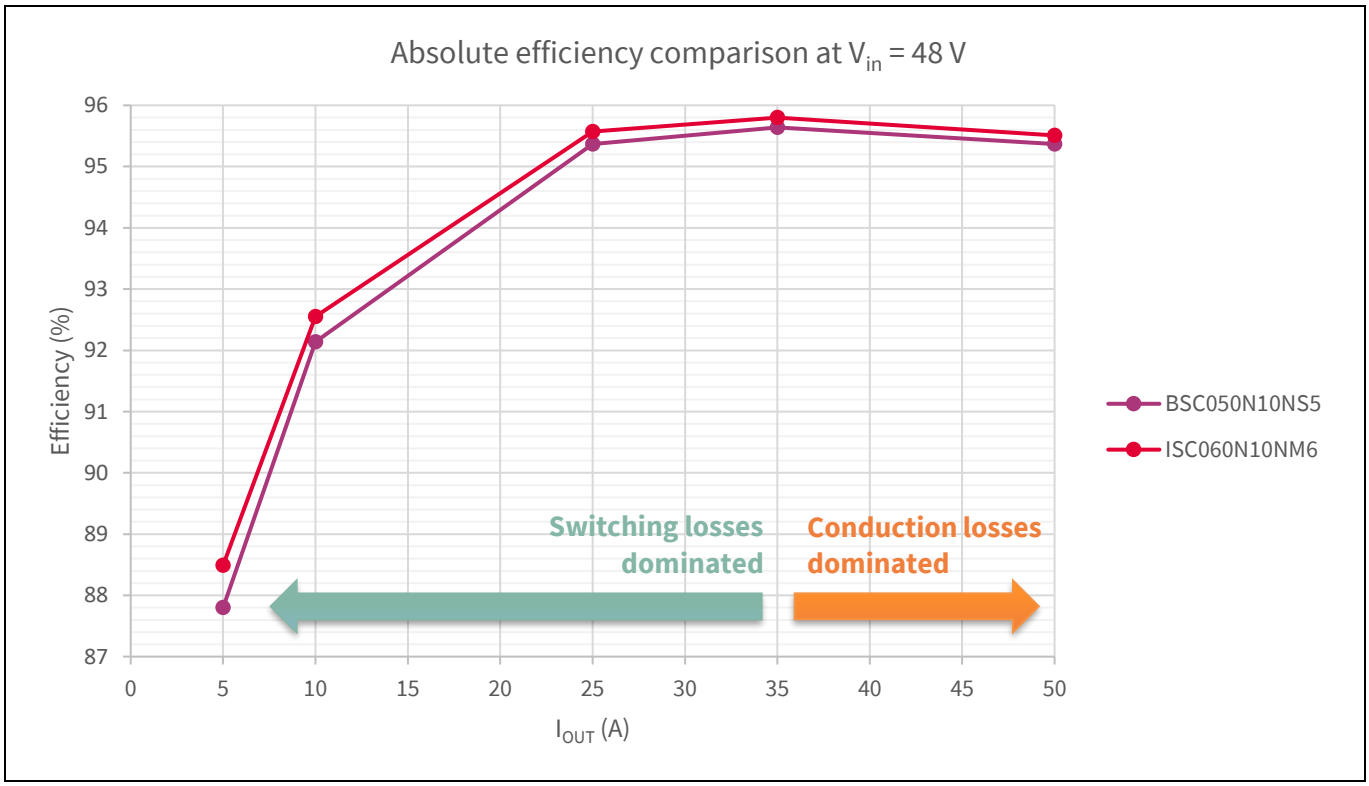


Figure 16 Absolute efficiency comparison at V_{in} = 48 V

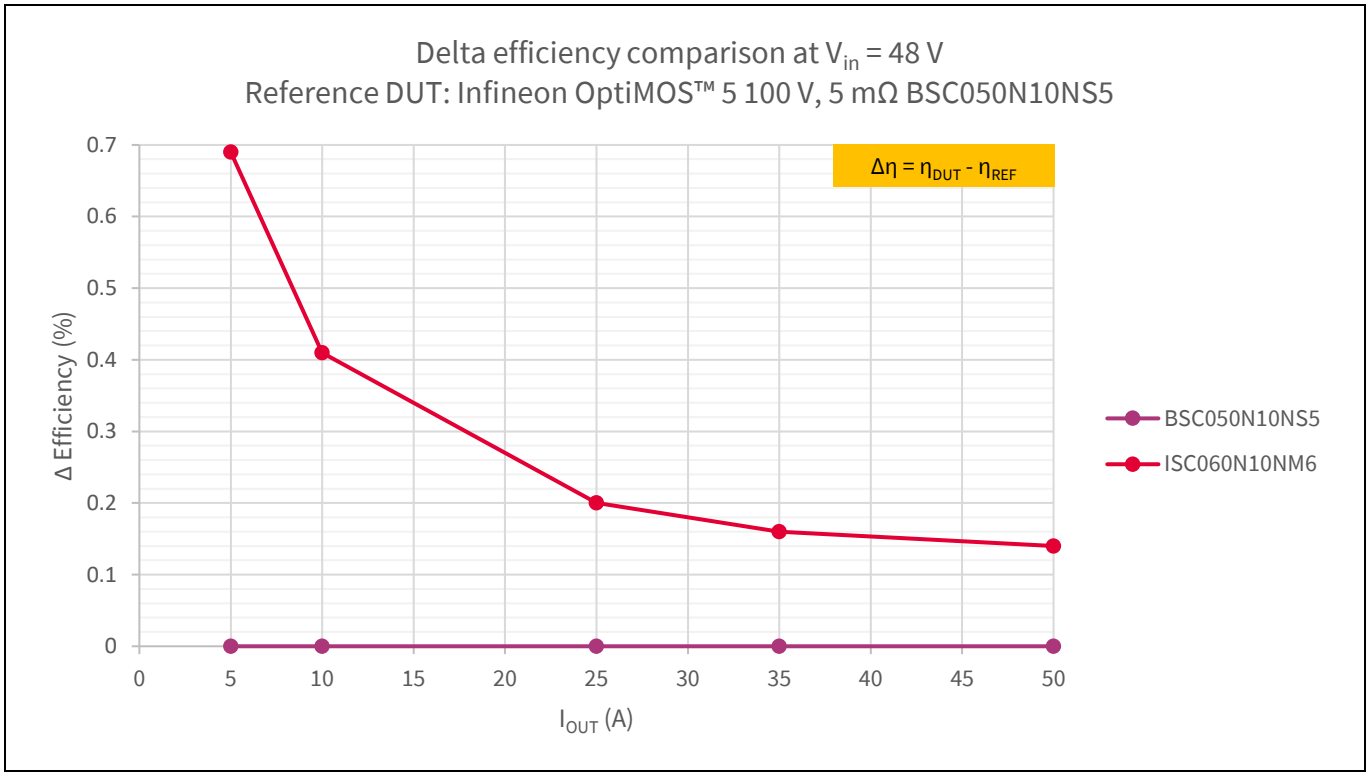


Figure 17 **Delta efficiency comparison at V_{in} = 48 V. Reference DUT: Infineon OptiMOS™ 5 100 V, 5 mΩ $R_{DS(on),max}$ BSC050N10NS5**

2.1.4.3 Efficiency comparison at V_{in} = 75 V

Table 7 summarizes the efficiencies acquired at high-line voltage (V_{in} = 75 V) for the different DUTs. The efficiency is measured at 600 LFM (3 m/s) airflow and captured after thermal steady-state is reached.

The efficiency curves, absolute and relative to the original setup employing OptiMOS™ 5 as DUTs, are reported respectively in Figure 18 and Figure 19.

Table 7 **Measured efficiency (%) at nominal input voltage V_{in} = 75 V**

Output current	Infineon OptiMOS™ 6 100 V, 6 mΩ ISC060N10NM6	Infineon OptiMOS™ 5 100 V, 5 mΩ BSC050N10NS5
5 A	82.45	81.75
10 A	89.53	88.92
25 A	93.13	92.91
35 A	93.92	93.75
50 A	94.22	93.81

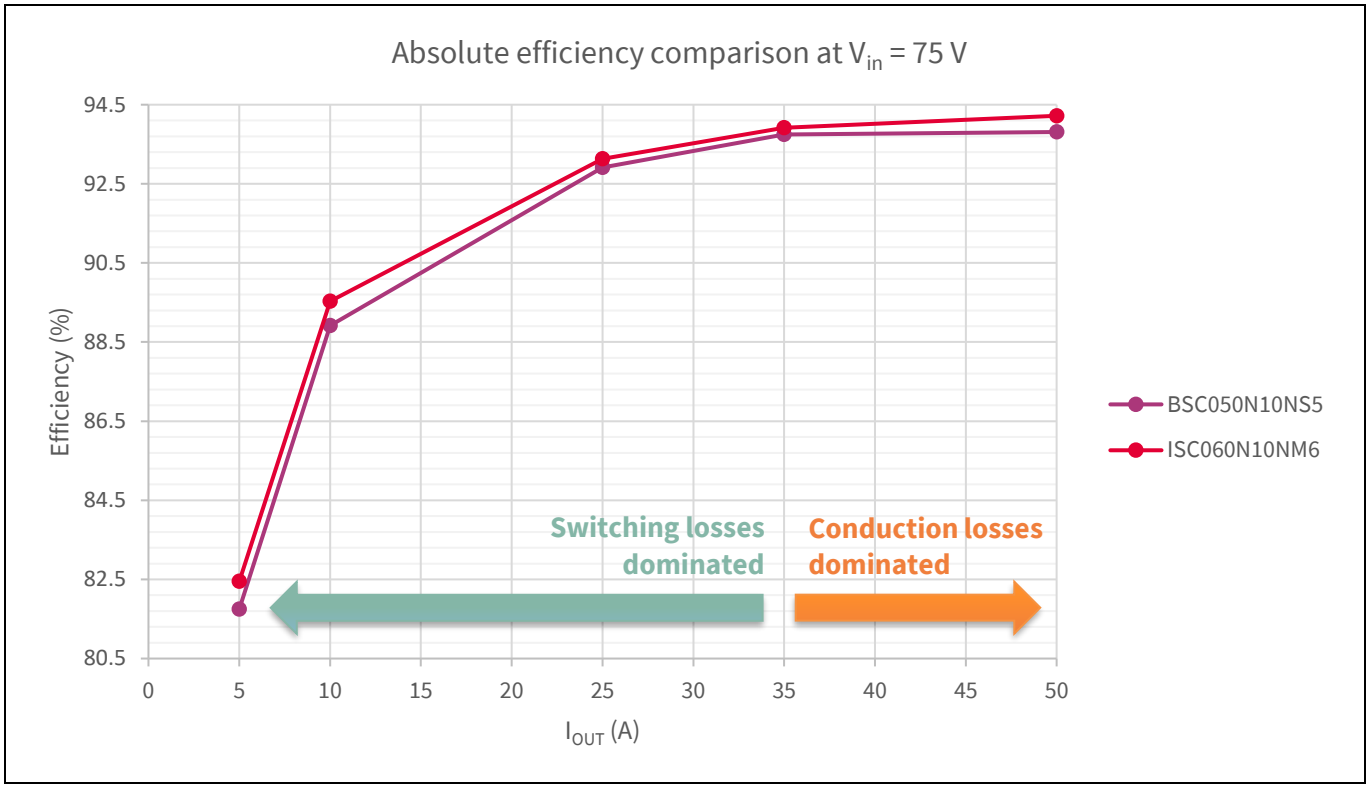


Figure 18 Absolute efficiency comparison at V_{in} = 75 V

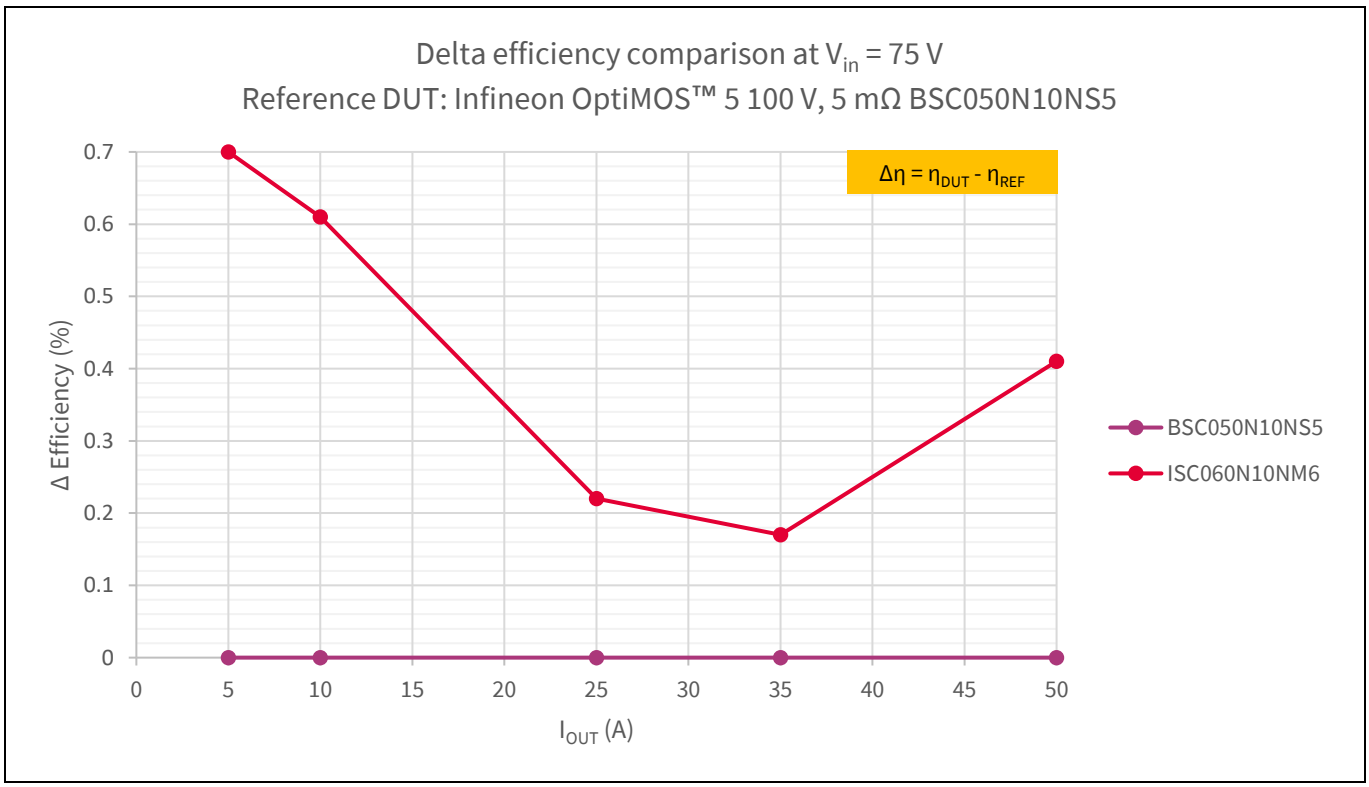


Figure 19 Delta efficiency comparison at V_{in} = 75 V. Reference DUT: Infineon OptiMOS™ 5 100 V, 5 mΩ $R_{DS(on),max}$ BSC050N10NS5

2.1.4.4 Conclusions

The efficiency plots in **Figure 16** and **Figure 18** show that a valuable gain is obtained when using the new Infineon OptiMOS™ 6 100 V in a high-performance, high-switching frequency SMPS. Compared to the OptiMOS™ 5 solution, a valuable gain in efficiency of 0.7 percent is recorded at light-load conditions, as a direct consequence of the improved switching performance. The 47 percent lower (typ.) Q_g would positively impact the power consumption from the auxiliary bias supply, while the 56 percent lower (typ.) Q_{gd} enables ultra-fast switching transients, resulting in a lower turn-off loss. Turn-on associated losses are lowered as well, through a 19 percent lower (typ.) Q_{oss}, which translates to a substantially lower energy stored in the MOSFET output capacitance, E_{oss}. The high efficiency gain recorded at light load would progressively reduce to a remarkable 0.2 percent at mid-load conditions. The load-independent losses, such as the biasing, have less and less impact as the load increases. In fact, if we assume for a moment a loss breakdown where the only source of loss is load-independent (like Q_{oss} and Q_g associated losses), and corresponding to P_Q:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{1}{1 + \frac{P_Q}{P_{out}}} \approx 1 - \frac{P_Q}{P_{out}}$$

Then, the relative efficiency qualitatively translates to an inverse proportionality with the load, $\Delta\eta = \Delta P_Q / P_{out}$, as recorded experimentally (**Figure 17**). As the load increases, the contribution of conduction – I_{RMS}^2 x $R_{DS(on)}$ – starts proportionally to show on the overall efficiency: the efficiency curve starts to bend, following a linear asymptote with the load current. At nominal line voltage, the full-load efficiency gain is still a remarkable 0.14 percent, in spite of the higher $R_{DS(on)}$ of the DUT compared with the reference design using OptiMOS™ 5.

Experimental results highlight how the new Infineon OptiMOS™ 6 100 V family – enhancing all the main FOMs in a well-balanced way – shines in applications such as high-frequency SMPS, where a trade-off with a low $R_{DS(on)}$ and excellent switching performance are needed to achieve best efficiency across the whole load range.

2.1.5 Thermal comparison

2.1.5.1 Introduction to the measurements and thermal data

Along with efficiency tests, thermal data were also acquired, using the test setup introduced in section **2.1.3 Test setup description**. Temperatures were measured across the entire brick board by using a thermal camera, after thermal steady-state was reached. In **Figure 20** and **Figure 21** the hotspot temperature recorded between the primary MOSFETs is compared for the different DUTs across all the line and load conditions. Measurements are provided for 600 LFM (3 m/s) airflow.

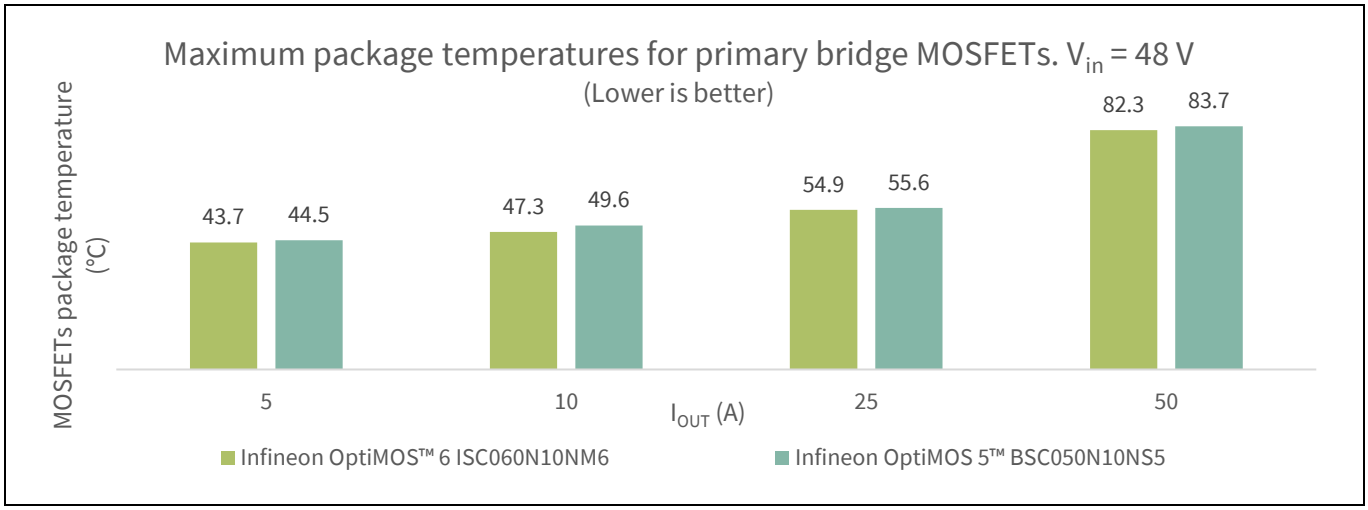


Figure 20 Maximum package temperatures for primary-bridge MOSFETs (lower is better). V_{in} = 48 V

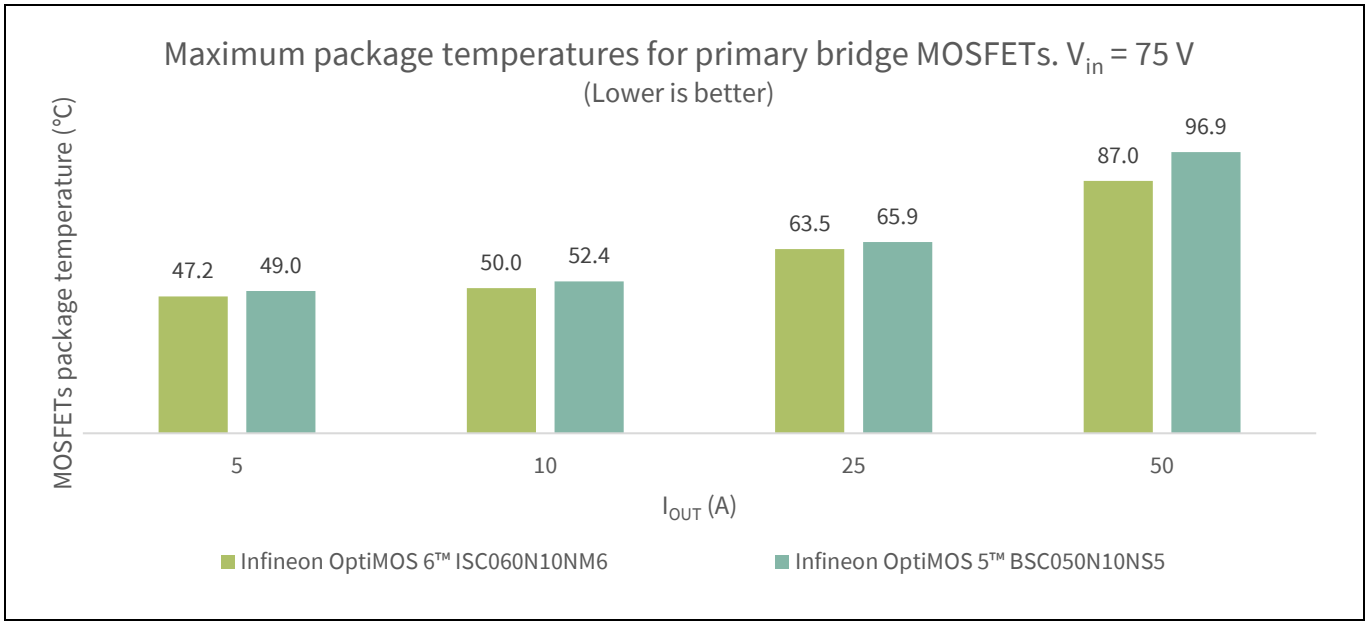


Figure 21 Maximum package temperatures for primary-bridge MOSFETs (lower is better). V_{in} = 75 V

2.1.5.2 Thermal image after prolonged operation

The Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter using OptiMOS™ 6 100 V ISC060N10NM6 in the primary bridge has been put in a prolonged worst-case operating condition, which means high-line operation (V_{in} = 75 V) with full load (I_{out} = 50 A) applied. The unit was operating under 600 LFM (3 m/s) airflow.

After burning overnight, a thermal image of the unit was captured. The thermal image is shown in **Figure 22**. It is worth noting that the primary MOSFETs' case temperature does not exceed 86°C, while the hotspot is localized at the SR stage, handling the high load current.

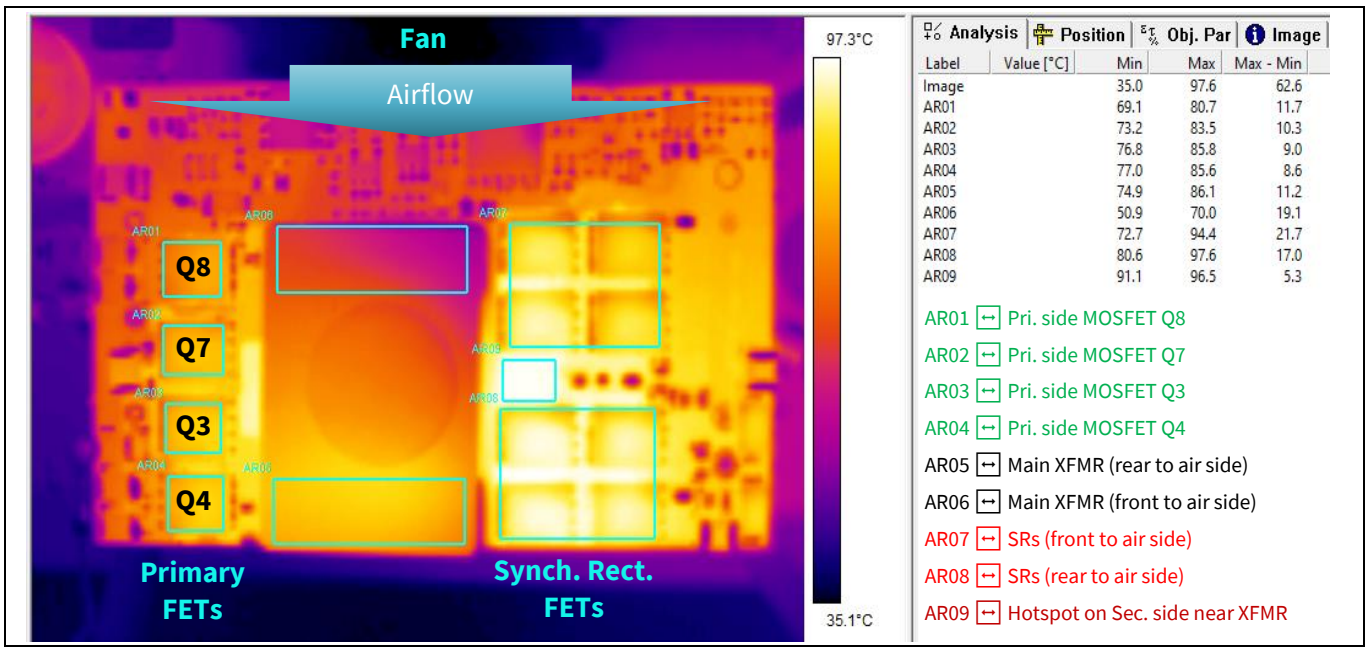


Figure 22 Thermal image of the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter using OptiMOS™ 6 100 V ISC060N10NM6 in the primary bridge, after burning overnight

2.1.5.3 Conclusions

Thermal measurements reflect the overall efficiency improvement enabled by the OptiMOS™ 6 ISC060N10NM6. While the primary MOSFETs show lower temperatures in all the line and load conditions, the advantage is also reflected at system level, with reduced thermal stress across gate drivers and onboard bias regulator (lower bias losses). Power supplies rated for telecom applications need to meet demanding requirements for the mean time between failures (MTBF), an indicator that measures system reliability. MTBF is generally measured in hours (h) and is inversely proportional to the temperature. The enhanced thermal margin is a desirable feature, because – in general terms – the temperature's influence on reliability can be described by an exponential function. While the overall system failure rate is a complex superposition of individual component failure rates, the important message to convey is that every degree gained can potentially extend the system lifetime by tens of hours.

Improving system efficiency – the result of optimizations brought at product level such as lower $R_{DS(on)}$, low Q_g, low Q_{gd} and Q_{oss} – is a fundamental measure to keep the power density increasing, while at the same time meeting the demanding reliability requirements imposed on telecom power supply modules. The new OptiMOS™ 6 100 V family enables the trend toward ultimate efficiency power conversion, helping power supply designers meet the design requirements, making life easier.

2.1.6 Operation waveforms

To conclude the comparison, waveforms were acquired for the different DUTs in the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter. Primary-side steady-state waveforms (gate-source and drain-source voltages) were acquired for the different DUTs at nominal line voltage (V_{in} = 48 V) and full load (I_{out} = 50 A).

A sketch of the control signals adopted to control the primary and secondary bridges is shown in **Figure 23**. The idealized waveforms for drain-source voltage and gate-source voltage for a generic MOSFET in the primary bridge are shown in **Figure 24**.

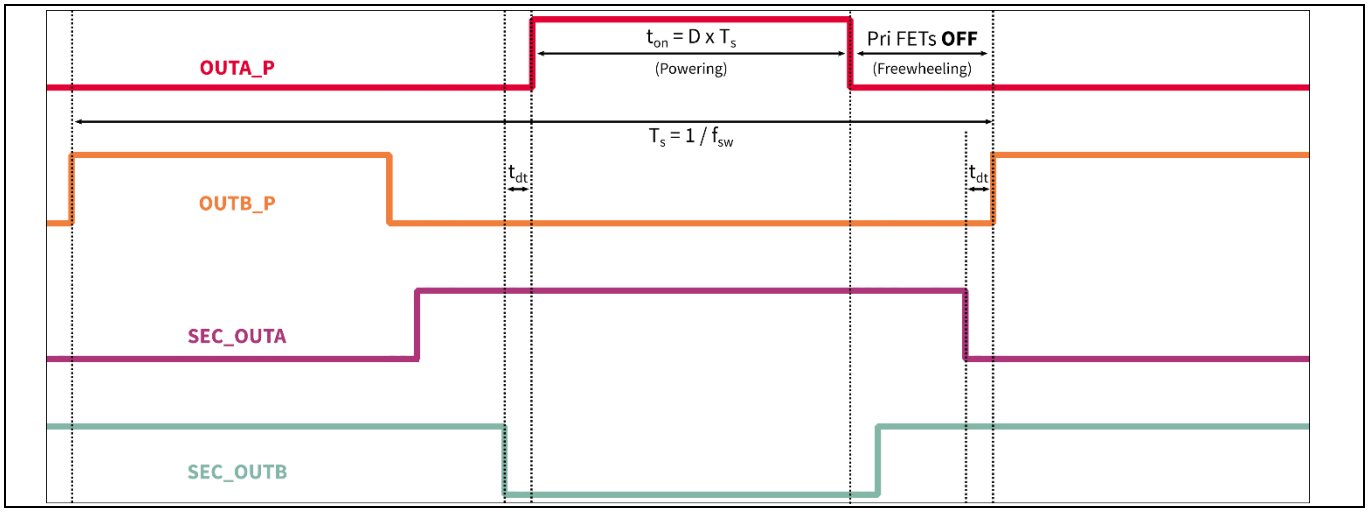
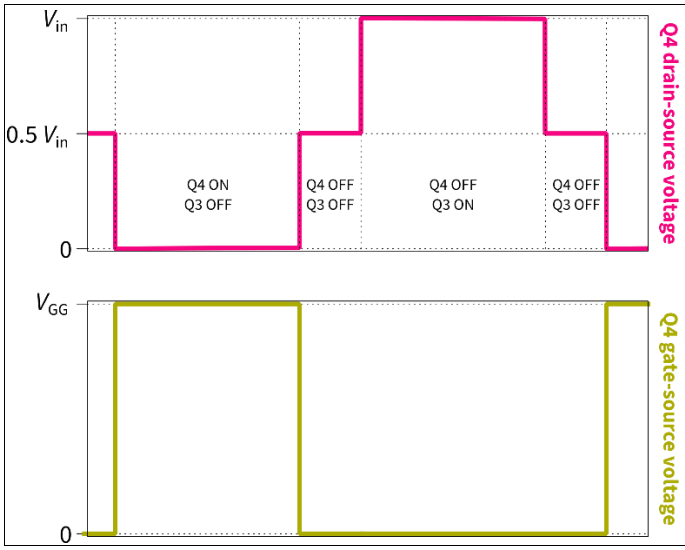


Figure 23 Schematic representation of the gating signals applied to control the FB-FB power stage



◀ *During the freewheeling phase, where all of the primary MOSFETs are controlled to be off, the midpoint voltage of each half-bridge is determined by a capacitive divider of the input voltage with the FETs' output capacitances, ideally to one-half of the line voltage. Actually, any deviation from the ideal switching in a full-bridge diagonal (driver propagation delays mismatch, different strength of the high-side driver, spread in $V_{GS(th)}$, …) will affect the charge-sharing process, moving the midpoint above or below. The behavior also changes with the line voltage, due to the voltage dependence of C_{oss}. This behavior does not affect the operation of the converter.*

Figure 24 **Sketch of the ideal primary-side MOSFETs voltage waveforms for the proposed control strategy**

Acquired waveforms for Infineon OptiMOS™ 5 BSC050N10NS5 and the new OptiMOS™ 6 ISC060N10NM6 are shown in **Figure 25** and **Figure 26**.

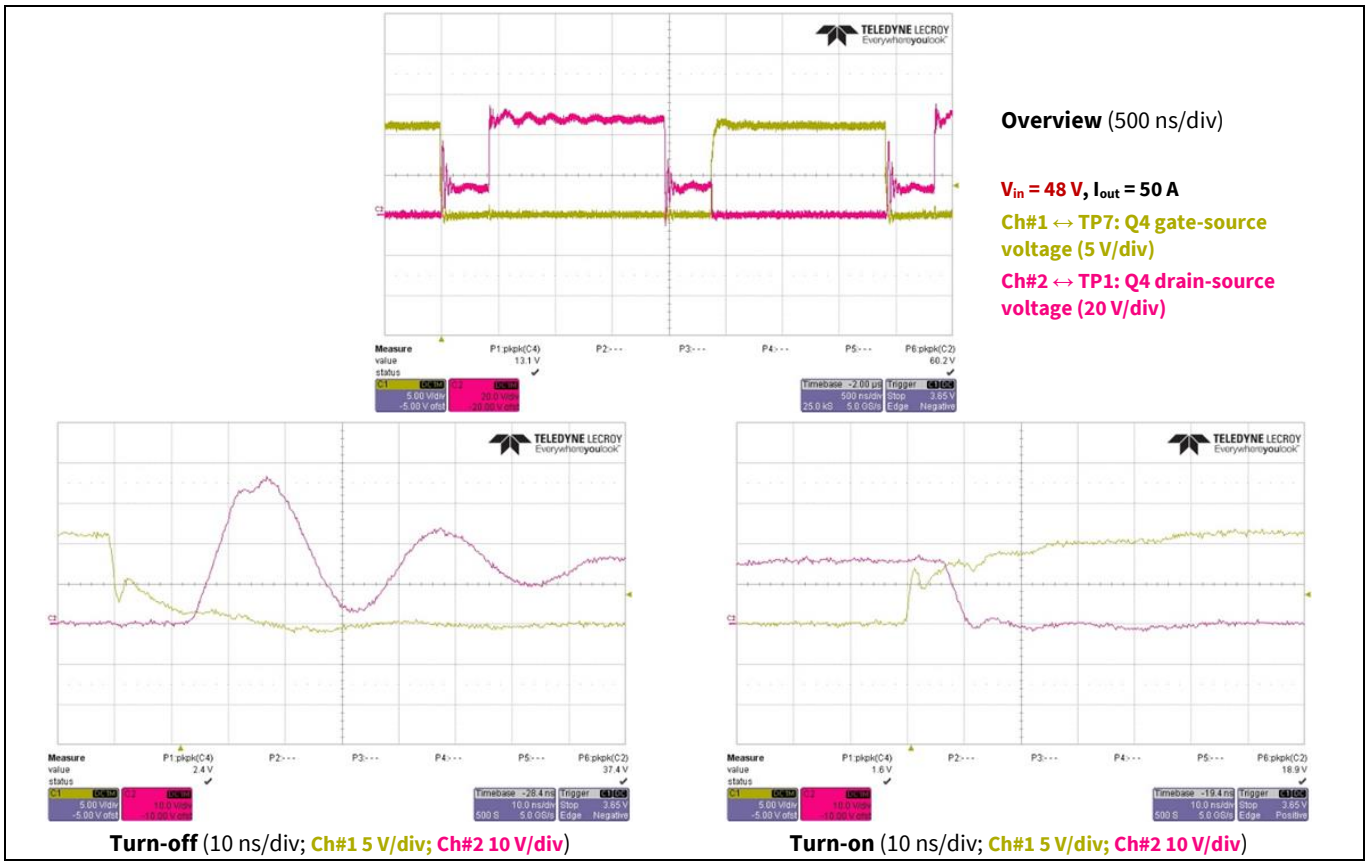


Figure 25 **Primary-side steady-state waveforms for Infineon OptiMOS™ 5 BSC050N10NS5**

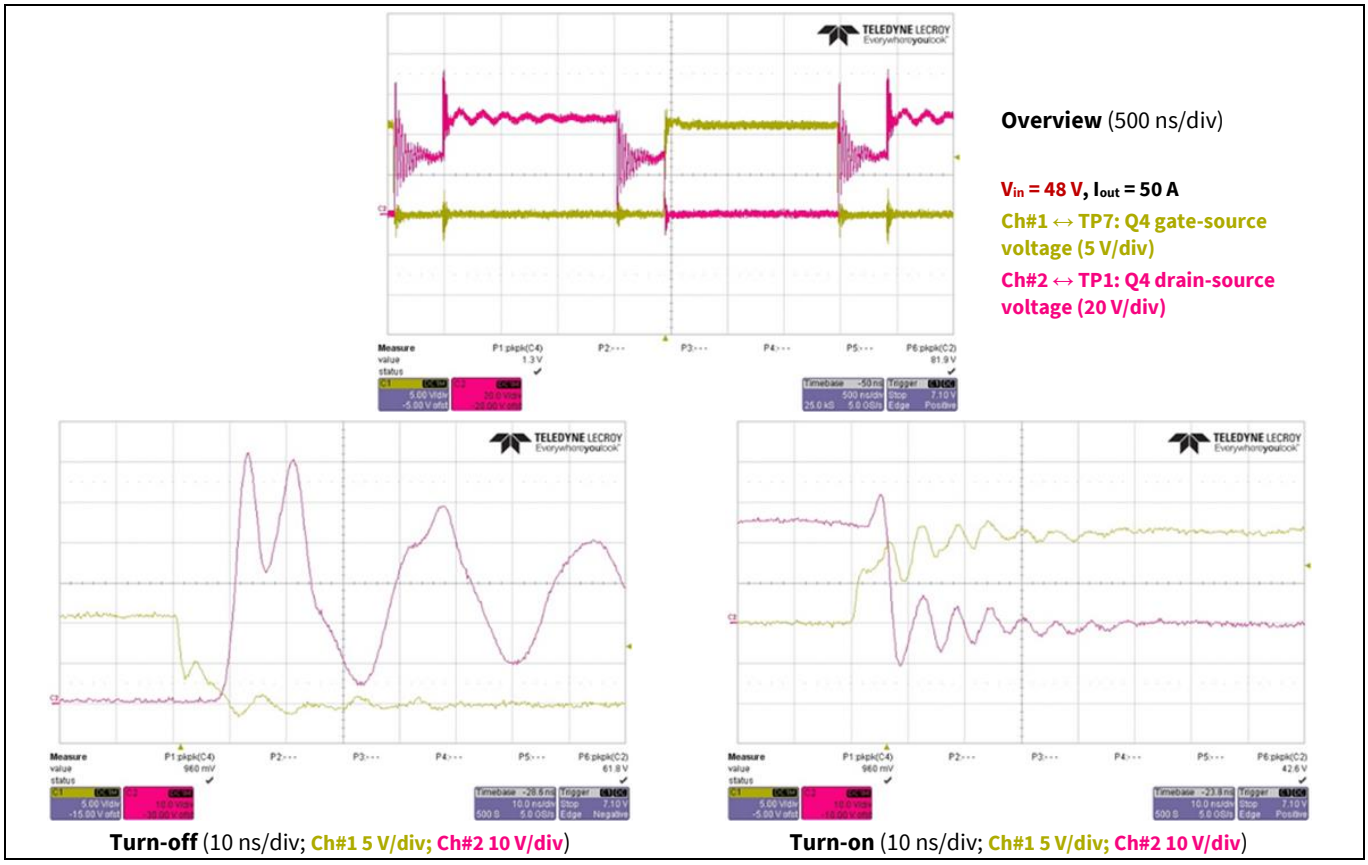


Figure 26 Primary-side steady-state waveforms for Infineon OptiMOS™ 6 ISC060N10NM6

2.1.7 Quantifying the multiple benefits of energy efficiency enabled by Infineon OptiMOS™ 6 100 V

2.1.7.1 Estimate of savings in operational expenditure (OPEX)

The remarkable increase in system efficiency brought by the new OptiMOS™ 6 100 V as a drop-in replacement for the previous Infineon OptiMOS™ 5 100 V family of MOSFETs, while enabling the power supply industry to bring ultimate reliability and power-dense solutions to the market, is beneficial for end users as well.
For mobile network operators (MNOs) energy consumption has historically been a major issue. The energy bill represents one of the highest operating expenses (OPEX), with a share of over 90 percent of the total cost. Total costs are quantified up to 10 percent of the MNO revenue, meaning that approximatively 9 percent of the revenue is spent on energy (electricity and fuel). Most of the energy serves to power the radio access network (RAN), while a smaller share is required for the backhaul (fiber infrastructure and data centers).
With the rollout of the 5G mobile network, MNOs will be forced to incur huge capital expenditures (CAPEX) and will face a significant growth in OPEX. The latter is due to the need to power a number of new sites – since 5G new radio (5G NR) relies on a denser layer of small cells – and to face the increased power consumption (initially estimated at +70 percent to +100 percent) of the existing macro base stations [4], [5], [6]. As the power consumption of 5G sites is expected to double, the cooling requirements of the sites are also expected to grow. Since most sites rely on air-conditioning (A/C) to keep temperatures within a controlled range inside the cabinet, more installed power means more heat to be extracted, hence more power drawn by the A/C.
All of these facts – together with the rising cost of energy – mean that being able to achieve the highest efficiency in power conversion is not a nice-to-have feature, but rather is essential for MNOs to lower the total cost of ownership of their services in this transition to 5G.
The new Infineon OptiMOS™ 6 100 V, when adopted in a typical DC-DC 600 W IBC, can provide a +0.2 percent increase in efficiency at half-load at nominal line voltage, and up to a +0.4 percent efficiency boost at high-line

and full-load conditions, compared to the previous OptiMOS™ 5 technology. This efficiency boost can be quantified as energy spared by mobile network operators. This can be done quantitatively by analysis of the system efficiency curves among the load, together with the knowledge of averaged DC-load profiles for a typical telecom wireless base station.

Below is an estimate of OPEX savings, carried out under several simplifying assumptions:

- Calculations are carried out for a European country with over 80 million people.
- ~84,000 multi-band (2G, 3G, 4G) base transceiver stations (BTSs) are installed in the country (estimate).
- The maximum power consumption for each of these sites (excluding A/C) is assumed to be, on average, ~7 kW. Around 90 percent of the power is needed to supply the RF power amplifiers in the remote radio units (RRUs).
- Each of these sites is supposed to be served by a single BBU. The maximum power absorbed from the BBU is 600 W. This power is delivered by the isolated IBC (-48 V to 12 V quarter-brick converter), and represents just a small share of the overall DC power needed by the site. Most of the power is needed to power the RRUs, and it is delivered by a separate DC-DC converter (**Figure 27**). The portion of DC power delivered to the RRU is typically covered by 150 V-rated devices. Stay tuned to see the advantages that the new OptiMOS™ 6 150 V will bring in this application.
- The nominal line voltage considered for the IBC is V_{in} = -48 V.
- The efficiency curves adopted for calculations are representative of the Infineon 600 W FB-FB 36 to 75 V to 12 V isolated quarter-brick DC-DC converter, and they are reported in **Figure 16**. A DC load profile (12 V bus), averaged over a long period, was considered for the particular application. Together, efficiency and load profiles are used to obtain a weighted efficiency for the system.
- Base electricity prices considered in the calculations are relative to the second half of 2020, given in EUR per kWh (€/kWh) for non-household consumers (with an annual consumption in kWh consistent with this application), and they will include all non-recoverable taxes. An average increase in prices of 2 percent yearly is considered, following the trend of the past 10 years. **[9]**
- The calculation does not assume the existence of a dual-tariff scheme for the electricity. The dual-tariff scheme is instead typical for European countries, where the cost of the energy is lower between 22:00 and 06:00. Also, peak shaving is not considered.
- The efficiency of the AC-DC stage is kept constant, $\eta_{AC/DC}$ = 98 percent.

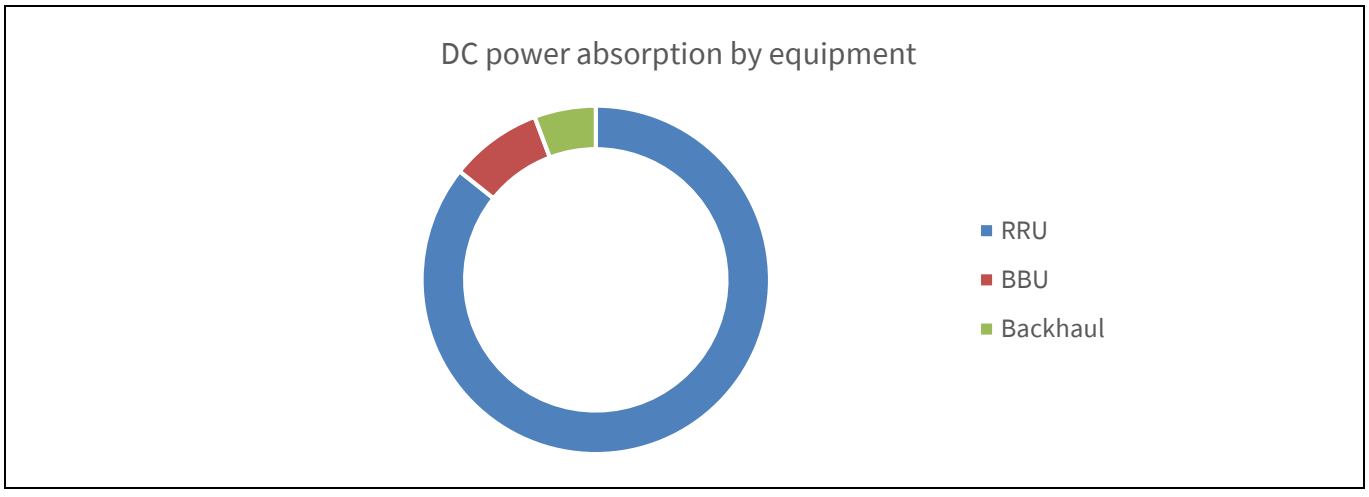


Figure 27 Typical share of the total installed DC power in a BTS site

In accordance with the assumptions above, the overall saving in OPEX is estimated in a time span of 10 years, that typically corresponds to the expected lifetime of the plant.

Note: The estimate presented here is the result of upgrading the existing platform for IBC – solely designated to power the BBU – from Infineon OptiMOS™ 5 100 V to the latest Infineon OptiMOS™ 6 100 V technology, in the primary side.

Table 8 OPEX savings estimate in 10 years (DC power for BBUs only), enabled by the adoption of the latest Infineon OptiMOS™ 6 100 V technology

Time span	Gain in weighted efficiency	Yearly cut in energy costs	Overall saving (€) in the timespan
10 years	+0.26 percent	-0.24 percent	1.01 million

The overall estimated saving, in excess of EUR 1 million, represents a valuable result in the context of the total cost of ownership of the plant. Note that this could underestimate the actual savings, as it ignores the rollout of 5G technology, which would require installation/upgrading of BBUs, using more DC power. Providing an estimate that would include 5G, limited in any case to macro stations, would be pure speculation because – to the authors' best knowledge – too few data are available and the industry trends are so unpredictable at the time of writing. In fact, the rollout of 5G would eventually be followed by the sunsetting of (part) of the legacy networks, partially offsetting the overall power consumption.

2.1.7.2 The environmental issue: making life greener

Costs are not the only drivers for change. The telecom industry, since the 2015 Paris agreement on climate change mitigation, [7] has proven to be one of the private sectors leading the trend toward carbon neutrality, by gradually committing to science-based targets (SBTs) in line with limiting global heating to 1.5°C above pre-industrial levels [8]. The new Infineon OptiMOS™ 6 100 V supports the trend toward increased efficiencies, helping customers in the telecom industry reduce emissions to net zero, making life greener.

2.2 Inverting ZVS buck-boost -(36…60) V to 12 V DC-DC converter

2.2.1 Introduction

The ordinary inverting buck-boost topology found interest in telecom power systems as a DC-DC converter to supply the RF power amplifiers (RFPAs). RFPAs need to be supplied with voltages ranging from +28 V (LDMOS RFPAs) to +50 V (GaN RFPAs), with the highest possible efficiency. Infineon developed an evaluation unit delivering up to 780 W with a DC output voltage of +28 V, from the restricted -(36…60) V input range, based on an interleaved (two-phase) inverting buck-boost **[11]**. Output voltage can be regulated up to +56 V, derating the output current to maintain the power constant. Infineon also introduced a novel active clamp auxiliary circuitry that enables transfer of the recovered charge Q_{rr} from the SR MOSFET toward the output in a non-dissipative way, contextually achieving ZVS turn-on for the control switch. The active clamp circuit effectively drives down the overall switching losses in the unit, enabling the use of BiC (lowest $R_{DS(on)}$) devices, and dramatically increasing the power density.

Alongside the +28 V output, Infineon also developed a +12 V output version for the evaluation unit, suitable for telecom equipment other than RPFA, that does not require functional isolation. In the context of the reduction of the output voltage, the rated power delivered from this unit is lowered to 600 W.

The reduced output voltage allows 100 V-rated MOSFETs to be used. Configured in this way, the Infineon ZVS buck-boost evaluation board is an excellent platform to showcase the performance achieved by the new BiC OptiMOS™ 6 100 V packaged in SuperSO8 (PQFN 5x6).

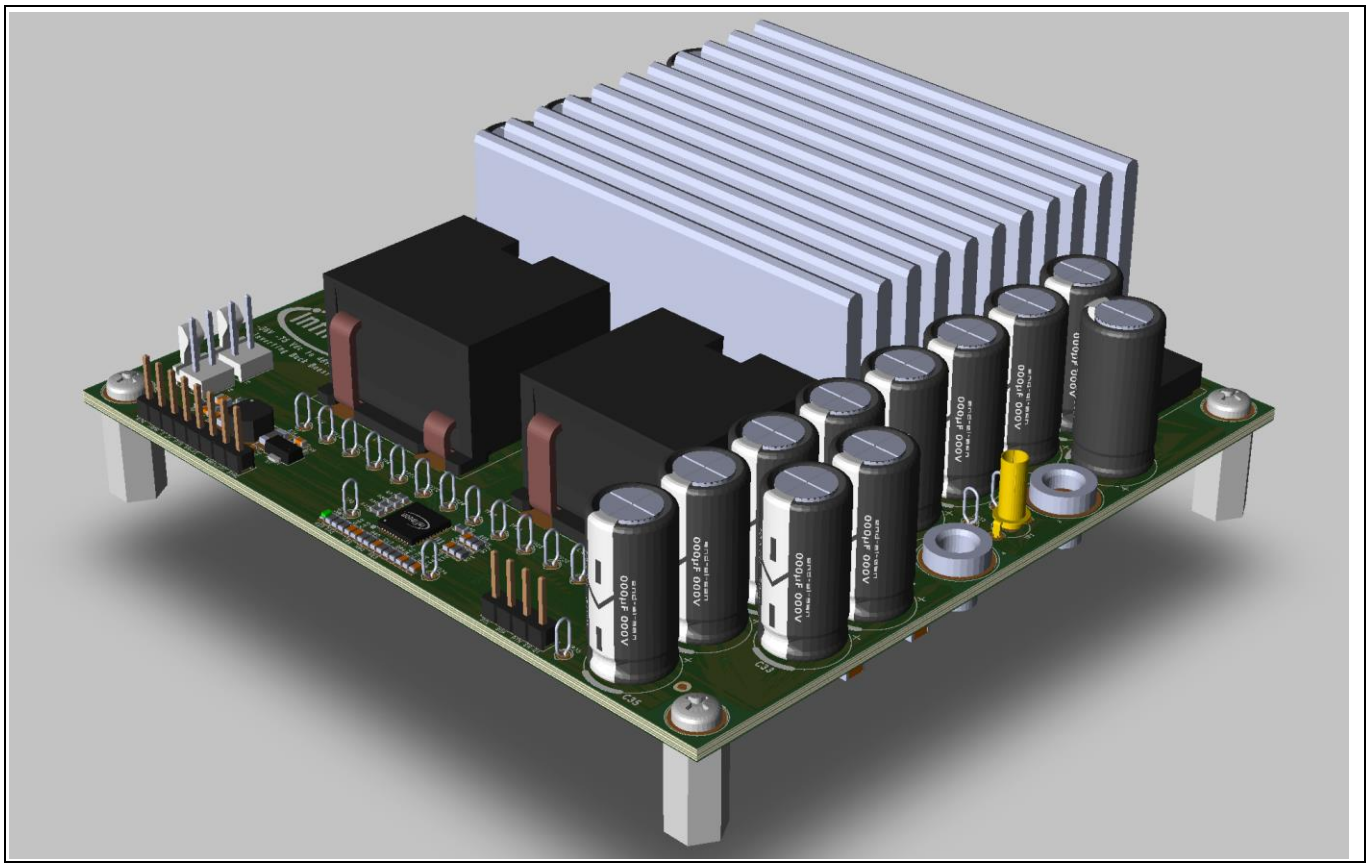


Figure 28 A 3D view of the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter

2.2.2 System description

The ordinary inverting buck-boost topology can be obtained as the cascaded connection of the elementary topologies. This connection leads directly to the four-switch buck-boost (non-inverting), usually employed to perform maximum power point tracking (MPPT) in solar optimizers. Allowing the output voltage to reverse its polarity, it would be possible to rearrange the topology, dropping two out of four switches and greatly simplifying the power stage and driving effort. This configuration takes the name of inverting buck-boost and shares with its building blocks (buck and boost) the ability to both step down and step up the input voltage. In this particular application the converter operates by stepping down the voltage from -(36…60) V to 12 V.

Output voltage is closed-loop regulated by means of a digital compensator, supported by the Infineon XDP™ integrated digital power supply controller. The XDPP1100 is a highly integrated (high-performance analog front end (AFE) state-machine-based digital control loop, and microcontroller) and programmable digital power supply controller. The device offers advanced power-control solutions for a wide variety of DC-DC power applications and supports various isolated and non-isolated topologies **[10]**.

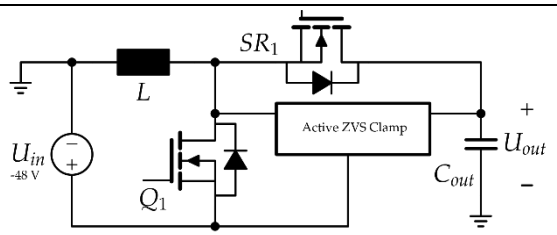
The power stage consists of two phases, operated with an interleaving angle of 180 degrees. Interleaving the power stages is beneficial in several ways. First, it enables reduction of the overall size of the converter: the interleaving angle allows harmonic cancelation to take place, relaxing the filtering requirements. Second, the power processed is divided between multiple phases, with the benefit that the power losses are also distributed across the power stages. This solution could be the only one feasible to deal with high power levels, or at least may show some advantages with respect to paralleling several semiconductors and employing bulkier passives. The inverting buck-boost shares with the buck the discontinuous input current, and with the boost the discontinuous output capacitor current. The RMS value of these quantities can be reduced by properly interleaving the power stages. Depending on the duty-cycle, the input and output capacitor currents may take advantage of the interleaving strategy.

The current measurement for the two phases is performed through DCR sensing over the relative inductors. Difference amplifiers are placed close to each inductor, and their outputs are processed by the XDPP1100 AFE. Current sensing is necessary to provide overcurrent protection (OCP) and for the current-balancing control over the two interleaved phases. Current balancing is a unique hardware-implemented feature in the Infineon XDP™ integrated digital power supply controller.

Input voltage is sensed to implement undervoltage lockout (UVLO) protection, and for telemetry purposes. At input voltages below the input UVLO limit, module operation is disabled.

The board was designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components. The module is equipped with an onboard auxiliary housekeeping supply to provide the required bias. The Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter has been designed to operate without the need for forced cooling. The unit comes with a heatsink screwed to the main PCB board, providing additional cooling for the power MOSFETs **[11]**.

Table 9 Inverting buck-boost topology basic diagram

Topology	Circuit schematic	Cost/complexity
Inverting ZVS buck-boost		Low cost, due to minimal part count. One half-bridge driver is required. The non-isolated design simplifies the control.

2.2.2.1 PCB description

Figure 29 shows the placement of the different components and measurement test points on the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter. The outer dimensions of the board, excluding the heatsink, are 4.25 in. x 4 in. x 0.87 in. (108 mm x 102 mm x 22 mm). The PCB is fabricated from a six-layer board. The internal layers are all 5 oz. copper (6.88 mil, 0.174 mm) thickness, with the top and bottom layers at 4 oz. copper (5.5 mil, 0.140 mm) thickness. The total board thickness is 67 mils (1.7 mm).

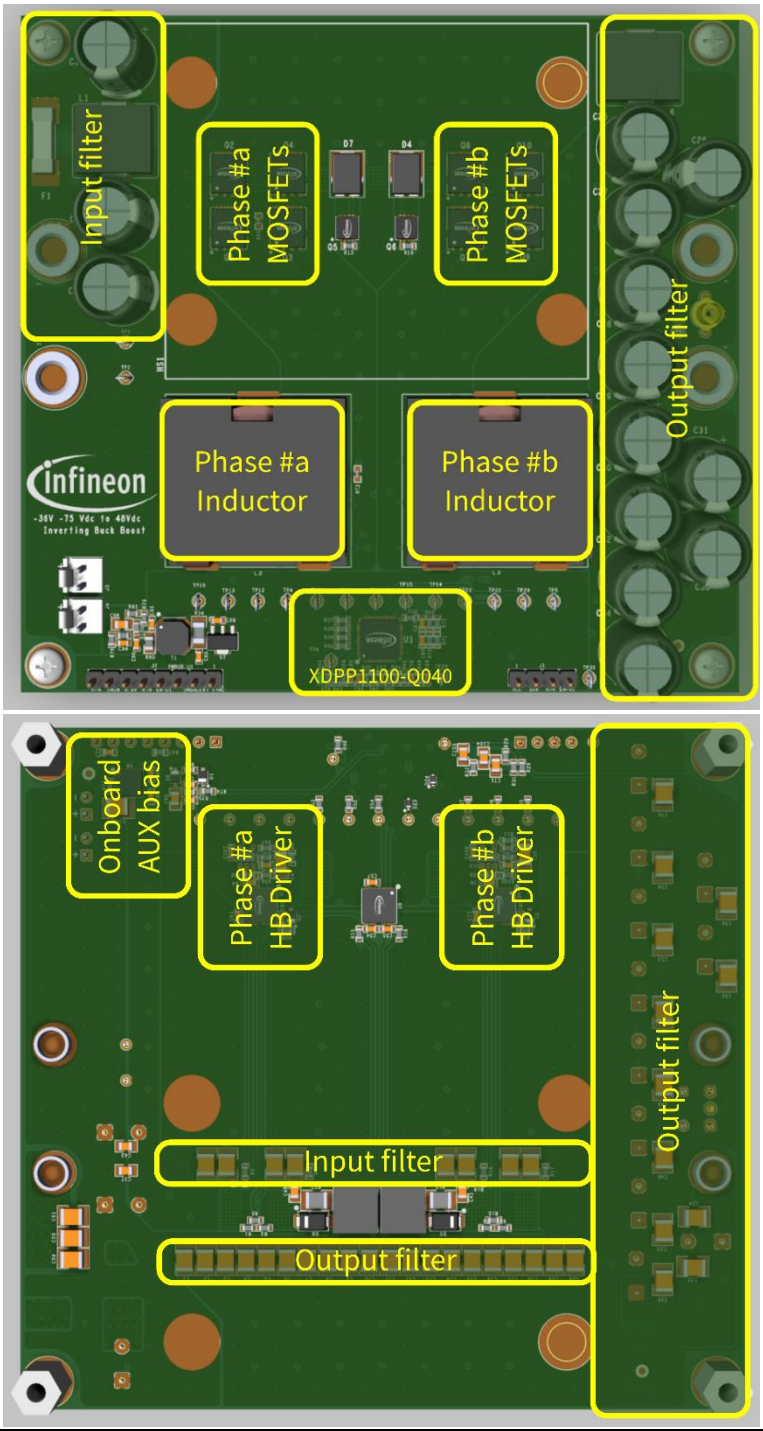


Figure 29 **Top and bottom views of the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter, where the placement of most significant components is highlighted**

2.2.2.2 Board specifications

The specifications for the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter are shown in **Table 10**.

Table 10 Specifications for the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Operating input voltage	V_{in}	-60	-48	-36	V	
Start-up voltage threshold	$UVLO_{(on)}$		33			
Minimum operating voltage after start-up	$UVLO_{(off)}$		30			
Output power	P_{out}	0		600	W	
Efficiency	η	95.5%				V_{in} = -48 V, P_{out} = 360 W
Output voltage set-point	$V_{out,nom}$		12		V	
Relative output voltage regulation (load)	$\Delta V_{out}/V_{out}$			2	%	
Output DC current	I_{out}			50	A	
Switching frequency	f_{sw}		200		kHz	
Airflow velocity	v_{air}	300 1.5			LFM m/s	

2.2.2.3 Board schematics

The simplified schematic diagram for the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter is shown in **Figure 30**.

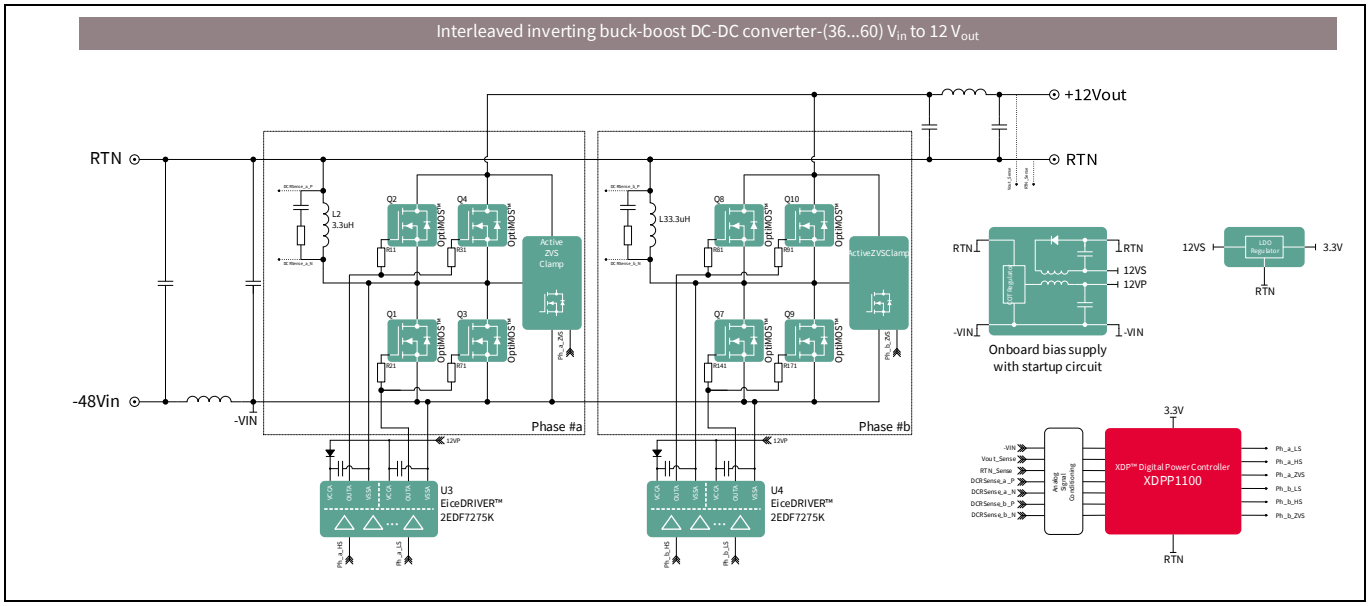


Figure 30 Simplified schematic diagram for the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter

2.2.3 Test setup description

The test setup, shown in **Figure 31**, is described here in detail. The actual test setup is shown in **Figure 32**.

Voltage source

- DC PSU capable of delivering at least 700 W, up to ~80 V DC

Active load

- Low-voltage, high-current (more than 50 A) electronic load (operated in constant current mode)

Measurement instruments

- Input current precision current shunt resistor (20 A, 0.1 percent)
- Output current precision current shunt resistor (100 A, 0.1 percent)
- Four 6½ digits DMMs for input, output and shunt voltage measurement
- High-bandwidth (more than 500 MHz) DSO and passive voltage probes
- Thermal camera and thermocouples to acquire temperatures across the board and below heatsink

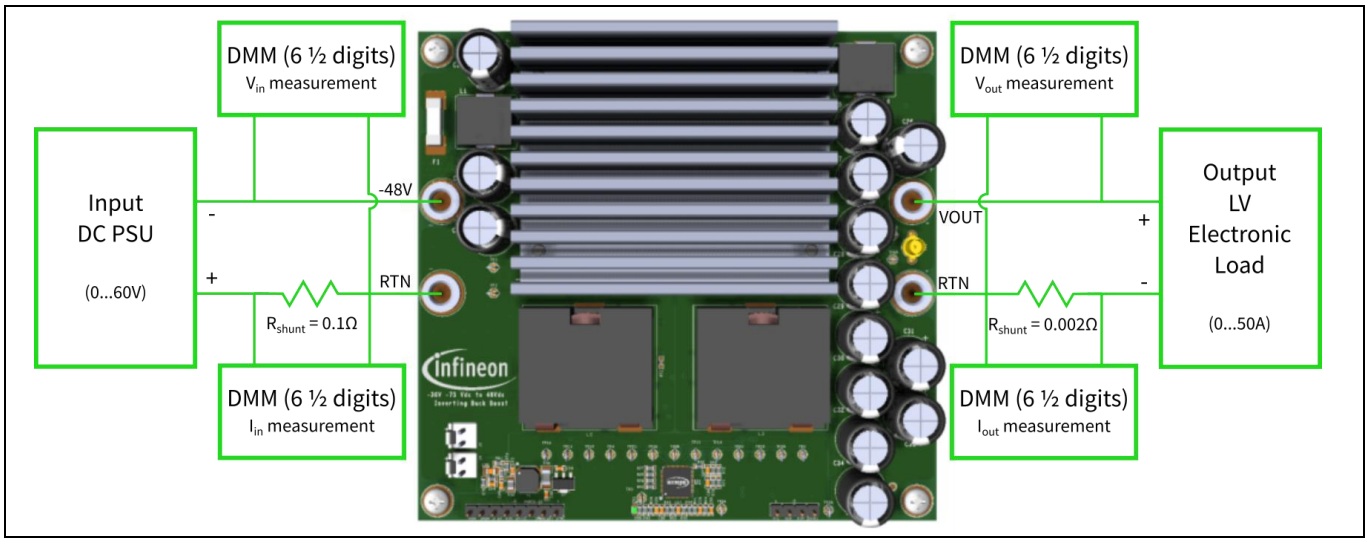


Figure 31 Top view of the board, showing schematically test setup connections

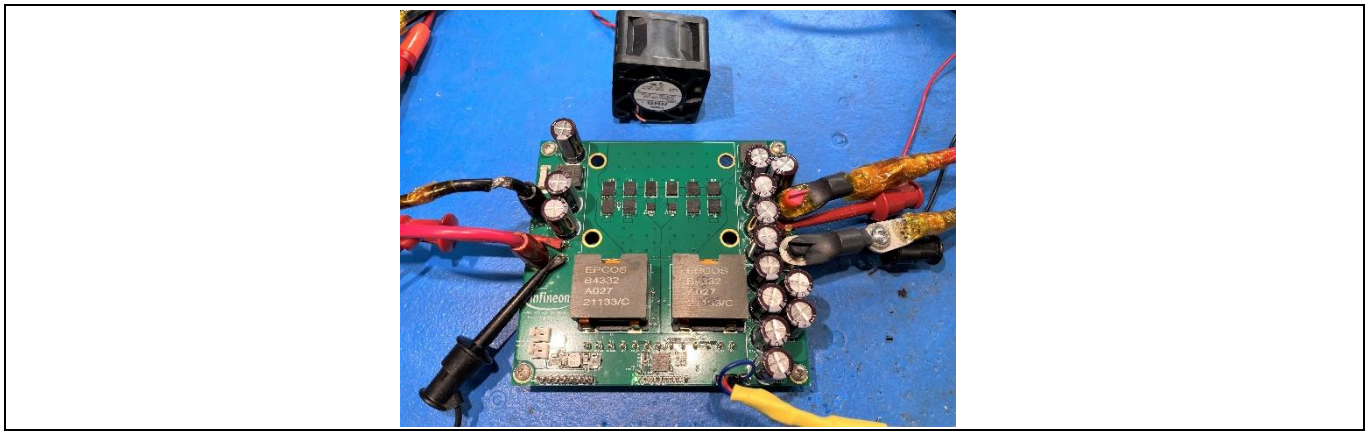


Figure 32 Actual test setup

2.2.4 Efficiency test

2.2.4.1 Introduction

Efficiency tests have been performed for the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter, relying on the test setup introduced in section **2.2.3**.

As explained in section **2.2.1 Introduction**, the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter comes with a novel active clamp auxiliary circuitry that enables transfer of the recovered charge Q_{rr} from the SR MOSFET toward the output in a non-dissipative way, and achievement of ZVS turn-on for the control switch. The active clamp circuit effectively drives down the overall switching losses in the unit, enabling use of BiC (lowest $R_{DS(on)}$) devices, and dramatically increasing the power density.

The input and output ranges allow 100 V-rated MOSFETs to be used. Configured in this way, the Infineon ZVS buck-boost evaluation board is an excellent platform to showcase the performance achieved by the new BiC OptiMOS™ 6 100 V packaged in SuperSO8 (PQFN 5x6).

Efficiencies have been captured for BiC devices in the PQFN 5x6 package: the new Infineon OptiMOS™ 6 ISC022N10NM6 together with OptiMOS™ 5 BSC027N10NS5. A summary of the DUTs and their position is given in **Table 11**.

Table 11 DUTs – refer to schematic file shown in Figure 30

DUTs position	DUT #1	DUT #2
Main power-stage MOSFETs: Q1, Q2, Q3, Q4 Q7, Q8, Q9, Q10	**Infineon OptiMOS™ 6** **100 V, 2.2 mΩ** ISC022N10NM6	**Infineon OptiMOS™ 5** **100 V, 2.7 mΩ** BSC027N10NS5

Note: The same unit as for the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter was used to acquire efficiencies. Efficiency is first acquired with a brand-new unit, using Infineon OptiMOS™ 6 100 V ISC022N10NM6 as primary MOSFETs, and then reworked to acquire efficiencies with the other DUTs. This ensures a fair comparison between the DUTs.

2.2.4.2 Efficiency comparison at V_{in} = -36 V

Table 12 summarizes the efficiencies acquired at low-line voltage (V_{in} = -36 V) for the different DUTs.

The efficiency curves are reported in **Figure 33**.

Table 12 Measured efficiency (%) at low-line V_{in} = -36 V

Output current	Infineon OptiMOS™ 6 100 V, 2.2 mΩ ISC022N10NM6	Infineon OptiMOS™ 5 100 V, 2.7 mΩ BSC027N10NS5
10 A	94.88	93.77
20 A	96.34	95.56
30 A	96.38	95.59
40 A	95.96	95.13
50 A	95.34	94.44

2.2.4.3 Efficiency comparison at V_{in} = -48 V

Table 13 summarizes the efficiencies acquired at nominal line voltage (V_{in} = -48 V) for the different DUTs. The efficiency curves are reported in Figure 34.

Table 13 Measured efficiency (%) at nominal line V_{in} = -48 V

Output current	Infineon OptiMOS™ 6 100 V, 2.2 mΩ ISC022N10NM6	Infineon OptiMOS™ 5 100 V, 2.7 mΩ BSC027N10NS5
10 A	93.96	92.65
20 A	95.77	94.96
30 A	95.96	95.20
40 A	95.72	94.88
50 A	95.27	94.26

2.2.4.4 Efficiency comparison at V_{in} = -56 V

Table 14 summarizes the efficiencies acquired at high-line voltage (V_{in} = -56 V) for the different DUTs. The efficiency curves are reported in Figure 35.

Table 14 Measured efficiency (%) at nominal line V_{in} = -56 V

Output current	Infineon OptiMOS™ 6 100 V, 2.2 mΩ ISC022N10NM6	Infineon OptiMOS™ 5 100 V, 2.7 mΩ BSC027N10NS5
10 A	93.28	91.85
20 A	95.36	94.49
30 A	95.71	94.88
40 A	95.54	94.66
50 A	95.14	94.09

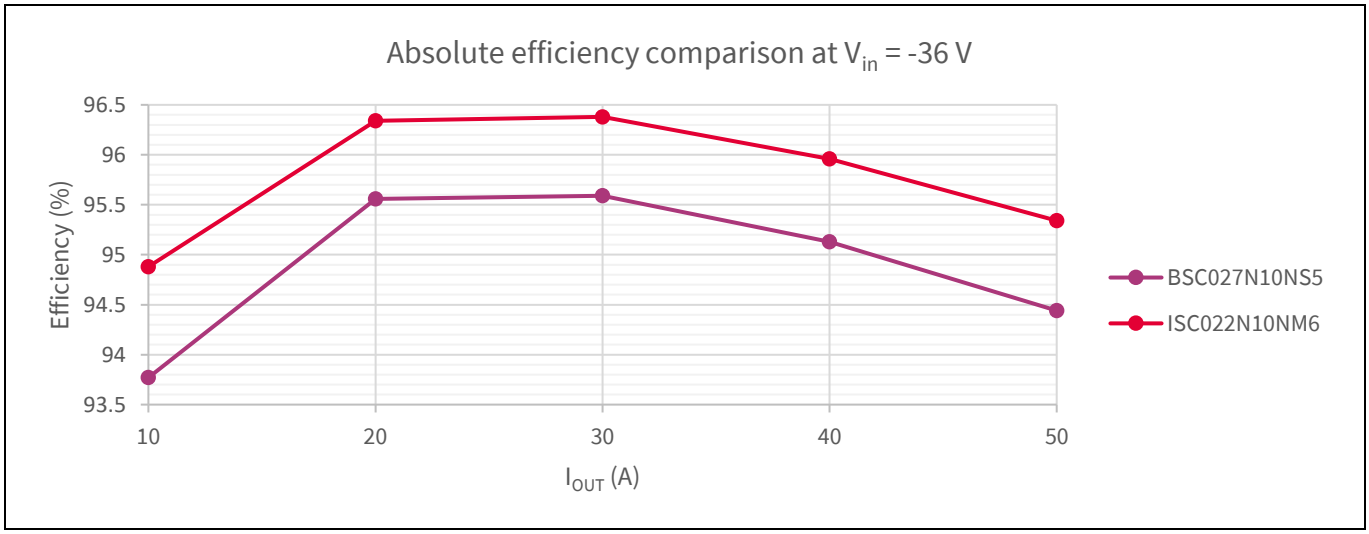


Figure 33 Absolute efficiency comparison at V_{in} = -36 V

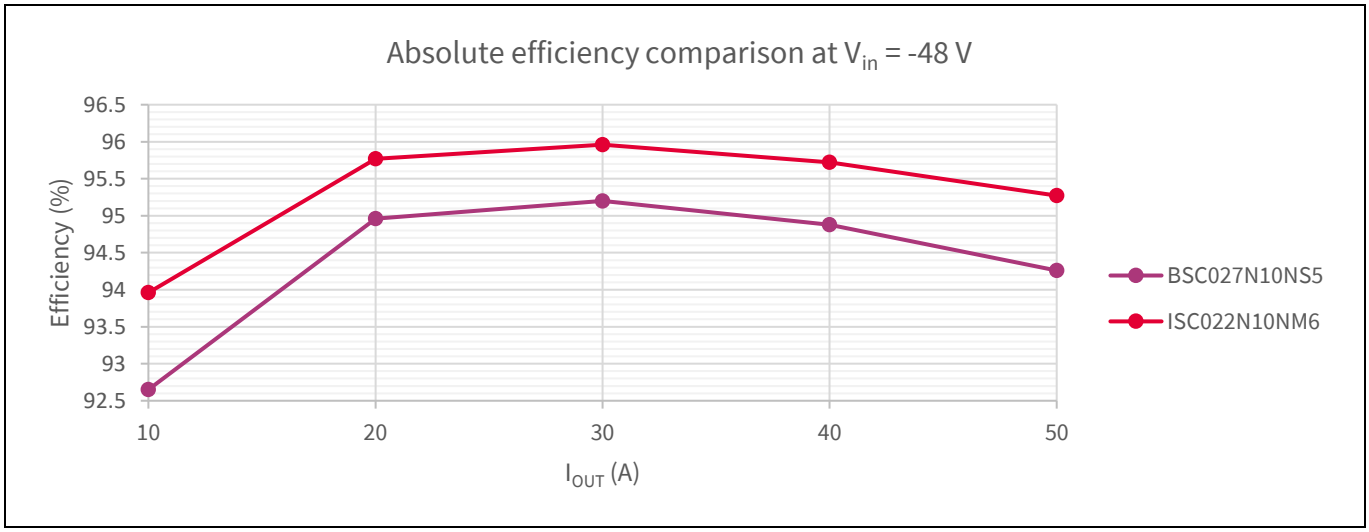


Figure 34 Absolute efficiency comparison at V_{in} = -48 V

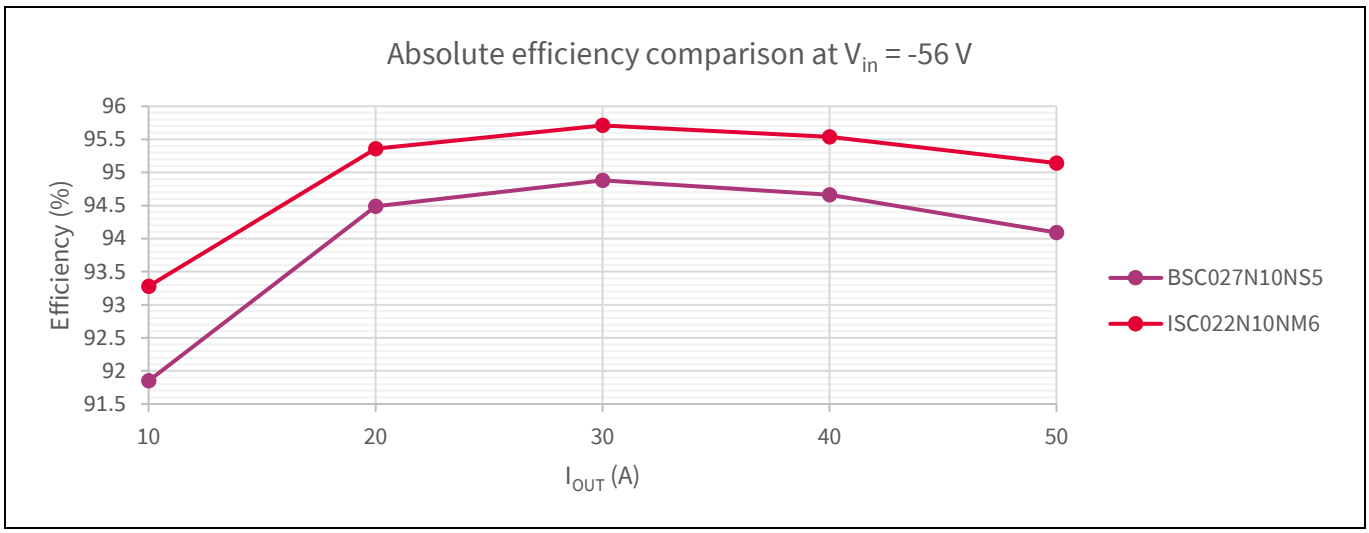


Figure 35 Absolute efficiency comparison at V_{in} = -56 V

2.2.4.5 Conclusions

The efficiency plots in **Figure 33**, **Figure 34** and **Figure 35** show a relevant improvement when comparing the new Infineon OptiMOS™ 6 100 V to the previous OptiMOS™ 5 BiC devices. The efficiency gain is quantified at approximately 1 percent at nominal line voltage and across all the load conditions.

The active clamp circuit mitigates the switching losses associated with the reverse recovery of the SR switch and enables the control switch to turn on with ZVS. The improvement in efficiency is explainable by the joint contribution of the lower driving losses, thanks to approximately 20 percent lower (typ.) Q_g, lower turn-off losses due to the lower Q_{gd} – an improvement just shy of 40 percent – and lower conduction losses with an 18 percent lower $R_{DS(on)}$. The ZVS condition achieved for the control MOSFET knocks out Q_{oss}-associated losses: Q_{oss} would only slightly impact the amplitude of the clamp resonant current.

Experimental results highlight how the new Infineon OptiMOS™ 6 100 V BiC device ISC022N10NM6 – with improved FOMs and 18 percent lower $R_{DS(on)}$ – shines in applications such as high-frequency, soft-switched SMPS where conduction losses play a crucial role in getting the best efficiency across most of the load conditions.

2.2.5 Thermal comparison

Along with efficiency tests, thermal data were also acquired for the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter. To ease the temperature acquisition over the unit, the heatsink was removed and an airflow of 400 LFM (2 m/s) provided by a fan. Temperatures were measured across the entire board with a FLIR E6390 thermal camera, after thermal steady-state condition was reached.

Thermal images were taken at nominal line voltage (V_{in} = -48 V) and full load (I_{out} = 50 A). In **Figure 36** the temperature recorded within the board is compared for the different DUTs. The hotspot temperature corresponds to the active ZVS clamp FETs and diodes (which are kept the same for the two tests). The lowest hotspot temperature (5.6°C less when compared to OptiMOS™ 5 100 V) was recorded in the setup using the new OptiMOS™ 6 100 V with the results of the reduction in total recovered charge coming from high-side switching devices.

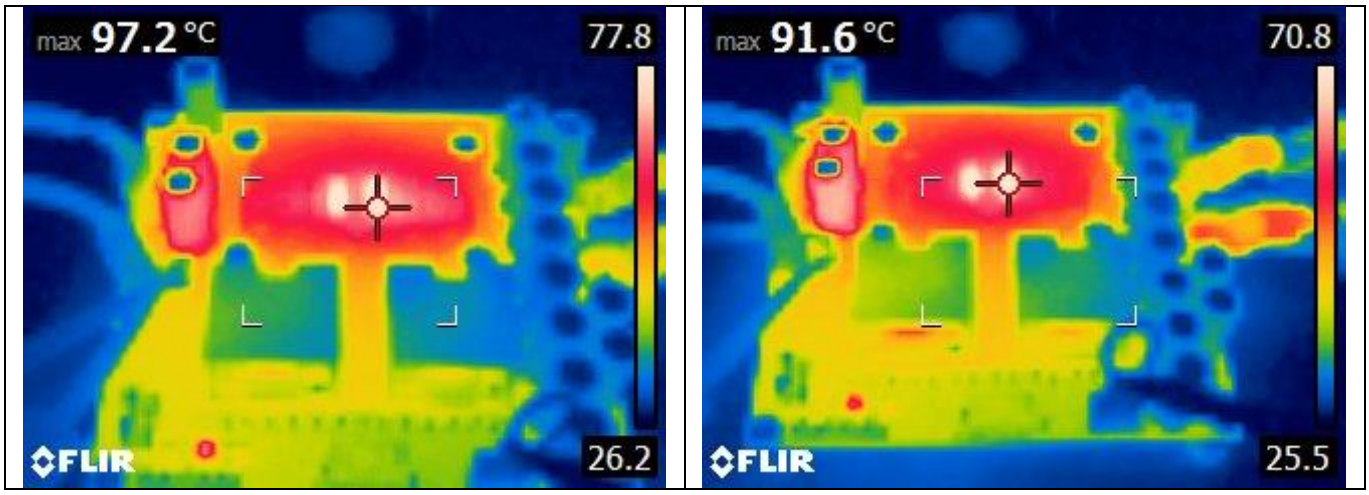


Figure 36 Thermal images of the board. Left: OptiMOS™ 5 100 V BSC027N10NS5. Right: OptiMOS™ 6 100 V ISC022N10NM6

2.2.6 Operational waveforms

To conclude the comparison, waveforms were acquired for the different DUTs in the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter. Steady-state waveforms (drain-source voltages) were acquired for the different DUTs for phase #a of the converter. Waveforms were taken at nominal input line (V_{in} = -48 V) and full load (I_{out} = 50 A) for comparison.

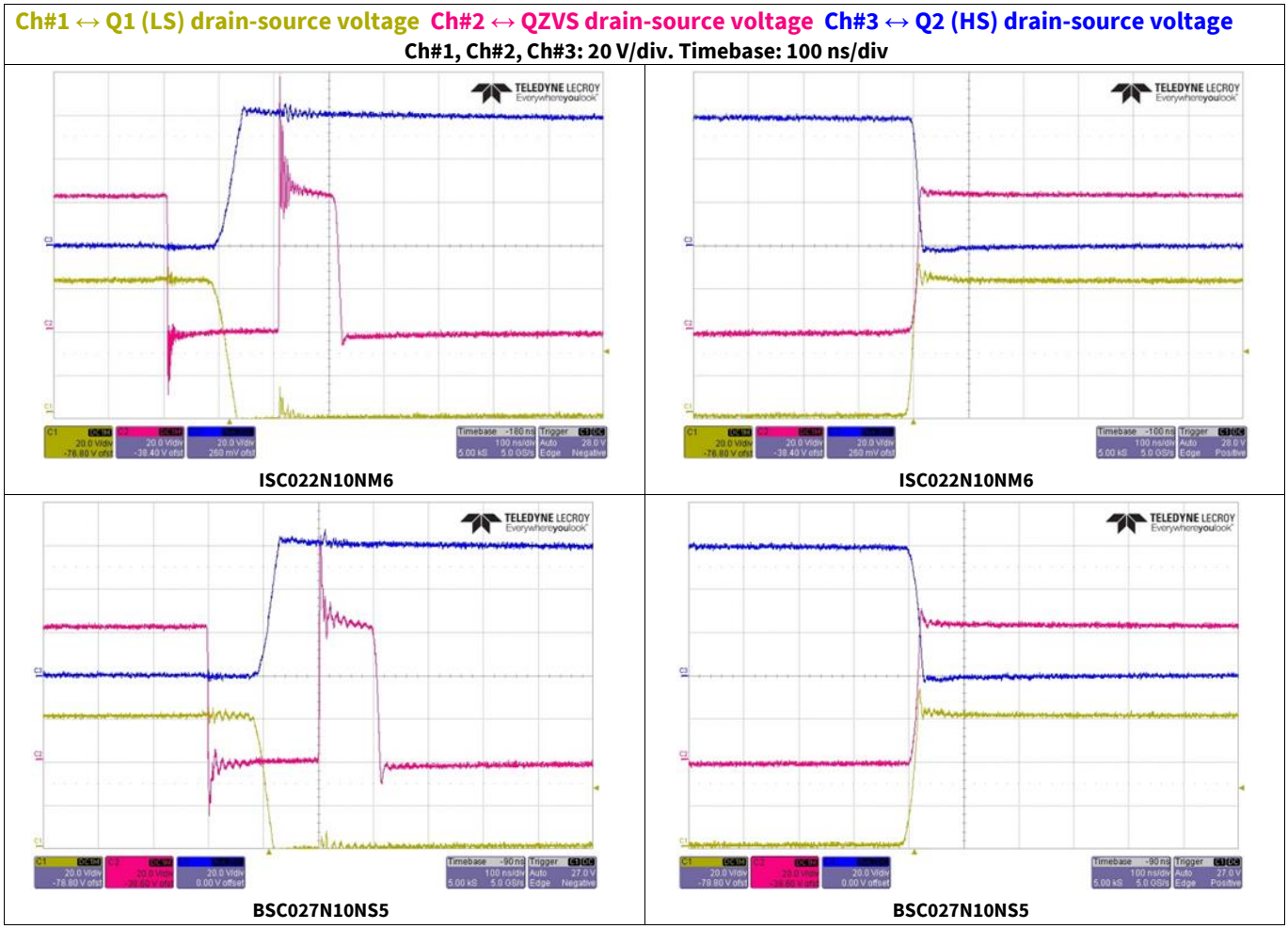


Figure 37 Steady-state waveforms for phase #a of the Infineon 600 W inverting buck-boost -(36...60) V to 12 V DC-DC converter

3 Portfolio

The new OptiMOS™ 6 100 V comes in a wide $R_{DS(on)}$ range, packaged in SuperSO8 and PQFN 3.3x3.3 (i.e., the reduced-size SuperSO8, abbreviated as S3O8). This broad portfolio makes the life of the system designer easier: the high granularity $R_{DS(on)}$ enables optimization of the design to cover the widest possible range of applications.

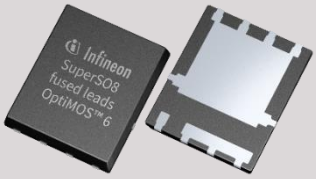
Package	Sales name	$R_{DS(on),max}$ [mΩ] @V_{GS}=10 V
SuperSO8 5x6 	ISC022N10NM6	2.2
	ISC027N10NM6	2.7
	ISC030N10NM6	3.0
	ISC060N10NM6	6.0
	ISC080N10NM6	8.0
	ISC230N10NM6	22.0
PQFN 3.3x3.3 	ISZ080N10NM6	8.0
	ISZ230N10NM6	22.0

Figure 38 OptiMOS™ 100 V product portfolio

4 Summary

The new OptiMOS™ 6 100 V family of MOSFETs is introduced by this document. The new technology, the result of Infineon's 20+ years of experience in advanced trench MOSFET design, comes with a totally redesigned cell, showing the industry's best FOMs. All the most relevant FOMs of the latest OptiMOS™ technology show improvements, resulting in a device specifically optimized for high-switching frequency SMPS applications.

With outstanding improvements brought at the device level, the new OptiMOS™ 6 100 V supports the trend toward significantly higher system efficiency and reliability. Of particular importance is the outstanding reduction in the specific on-state resistance and specific gate charge. Together with the lowest output charge, the OptiMOS™ 6 100 V provides the lowest switching losses, enhancing the system efficiency across all line and load conditions, providing significant margin to meet the demanding requirements of the telecom power arena. The new OptiMOS™ 6 100 V shows an optimized transfer characteristic, with a low temperature coefficient. This feature brings the advantage of a wider SOA, ultimately making the latest trench MOSFET technology a valid candidate for applications such as the battery disconnect switch in BPAs.

OptiMOS™ 6 100 V comes with a large portfolio comprising a wide range of $R_{DS(on)}$ and two package solutions, SuperSO8 and PQFN 3.3x3.3. This enables flexibility in new designs, and enables upgraded performance in existing designs, where it can be employed as a drop-in replacement for existing MOSFET solutions, with increased efficiency and easier thermal management.

5 Credits

The authors would like to thank the Infineon telecom application engineering group based in El Segundo, CA, who were responsible for development of the test platforms introduced in this document, as well as for carrying out the comparative tests in the applications, and providing the relative measurement data.

[1] Infineon Technologies AG. (2017, 5.) Application note: "**Linear mode operation and safe operating diagram of power MOSFETs**".

[2] Infineon Technologies AG. (2017, 7.) Application note: "**Linear FET combines advantages of planar and trench MOSFETs**".

[3] ETSI. (2016, 10.) EN 300 132-2 Power supply interface at the input to telecommunications and datacom (ICT) equipment; Part 2: Operated by -48 V direct current (DC).

[4] GSMA Intelligence. (2020, 11.) 5G energy efficiencies: green is the new black.

[5] MTN Consulting, LLC. (2020, 03.) Operators facing power cost crunch.

[6] Huawei Technologies Co., Ltd. (2019, 02.) 5G power whitepaper.

[7] The Paris Agreement: **https://unfccc.int/process-and-meetings/the-paris-agreement/the-paris-agreement**.

[8] GSMA. (2021, 04.) Mobile Net Zero: State of the Industry on Climate Action 2021.

[9] Source: Eurostat

[10] Infineon Technologies AG. (2020, 6.) Application note: "**The XDPP1100 digital power supply controller**".

[11] Infineon Technologies AG. (2021, 8.) Application note: "**XDPP1100 two-phase interleaved buck-boost**".

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