Optimizing CoolMOS™-based power supplies to meet EMI requirements

About this document

Scope and purpose

Improving efficiency is a key consideration for AC-DC Switch Mode Power Supply (SMPS) designers. As the performance of silicon Superjunction (SJ) MOSFETs improves, the intrinsic capacitances of the MOSFET are reduced, which results in faster switching speeds when used as plug-and-play replacements. This has the benefit of improving switching losses, but with the consequence of increased Electromagnetic Interference (EMI). Because of this, in some designs fast-switching SJ MOSFETs need special attention during design to pass EMI compliance testing.

In this application note we will discuss the impact of components and parasitics involved with the switching MOSFET and how to control MOSFET switching to improve the EMI signature. Low-power designs tend to be the most challenging for EMI, due to often lacking a metal enclosure or shielding, as well as a very high cost pressure that does not allow for any additional EMI mitigating components. In low-power designs the Flyback converter is still the dominant topology so this will be the primary focus, but the principles can be applied to other topologies.

Intended audience

SMPS designers interested in moving to the latest SJ-based CoolMOS™ MOSFETs.

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1 EMI overview

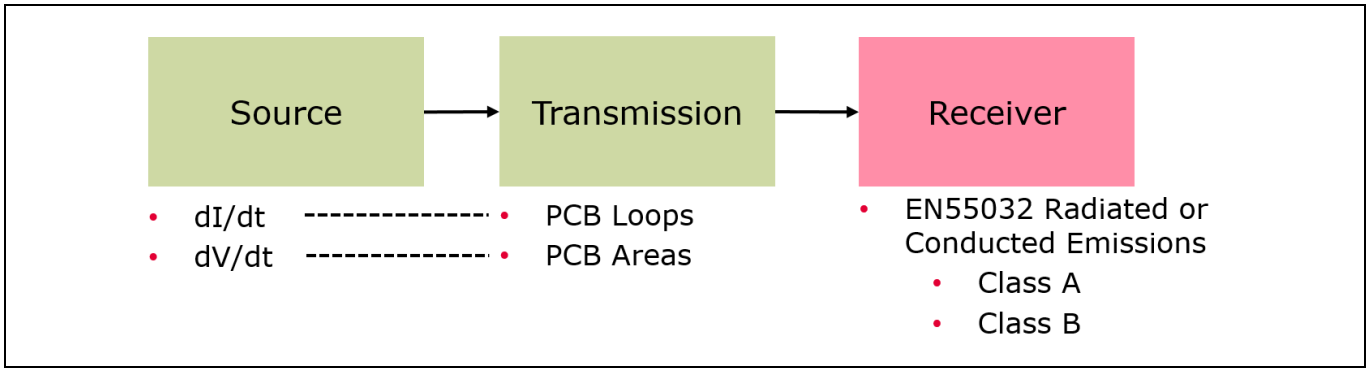

Figure 1 The basic blocks in the EMI pathway: source, transmission and receiver

EMI compliance is important to ensure that noisy power supplies are not interfering with radio signals or the behavior of other nearby electronic devices. Any spurious signal above 10 kHz needs to comply with regulations. There are two main categories of EMI testing. The first is conducted emissions, where the signals are conducted directly through the cable, which is typically measured from 150 kHz to 30 MHz, and the second is radiated emissions, which is measured with an antenna and is typically measured from 30 MHz to 1 GHz. Different applications will have different legal requirements, but these are the key categories when referring to EMI.

EMI compliance is simple in theory, but always difficult to manage in practice due to being very reliant on system parasitics, which are not always well known. These parasitics make it nearly impossible to simulate or predict based purely on schematic values. EMI, whether radiated or conducted, can be thought of as having three key pieces in the system: there is a noise source, a transmission pathway and a receiver. The receiver settings are set by the legal regulations of the application, so this means to become compliant the only options are to either reduce the noise source, or the transmission pathway to the receiver.

In radiated emissions the noise source is always a current or voltage changing with time, and this coupling pathway to the receiver is always a loop for changes in current with time or an area for changes in voltage with time. This can cause either inductive or capacitive coupling to the end receiver. In conducted emissions the signal will couple directly as currents flow through the cable to the receiver, and at higher frequencies there will also be coupling due to dI/dt and dV/dt due to loops and PCB areas back onto the main power cable.

To understand why we care about the dV/dt and dI/dt it is important to look at the harmonic content of a trapezoidal waveform, as shown below.

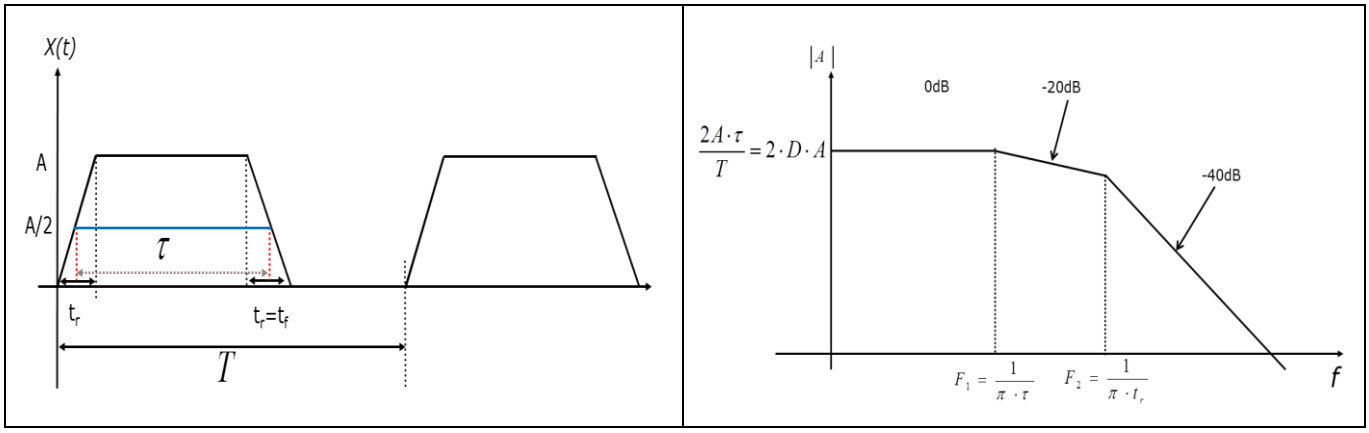

Figure 2 Left: trapezoidal waveform in the time domain; Right: harmonic content of a trapezoidal waveform

EMI overview

It can be seen in Figure 2 in the image on the right that there are two important roll-off points of the harmonic content of the trapezoidal waveform. The first is related to the period of the on-time of the waveform. The rise time and fall time then correspond to the -40 dB/decade roll-off point, which has a very large impact on the overall noise in the system. Because of this, slowing down rise and fall times of the different waveforms in a design can help to reduce the noise source.

The problem with reducing dV/dt and dI/dt is that this usually adds losses to the system, because during these switching periods energy is dissipated in the MOSFETs. To maximize efficiency it is always best to first focus on reducing the transmission of noise to the outside world, and only slow down the MOSFETs as a last resort.

This application note will look at how to slow down the dV/dt and dI/dt of the MOSFET as well as some techniques to reduce the transmission of noise.

2 Sources of noise in a Flyback

The critical current loops and voltage nodes for EMI are shown below in Figure 3 for a Flyback converter.

The critical node for voltage dV/dt is the drain of the MOSFET, and this area should be kept as small as possible in the layout of the design to prevent noise from coupling to other nodes in the system and from getting onto the input and output power cables.

The critical current loops for high dI/dt in the Flyback converter are the output rectifier loop, the MOSFET turn-on current loop and the RCD snubber clamping loop. All of these loops should be kept to a minimal area to reduce the amount of inductive coupling to other nodes and to the cable and the outside world.

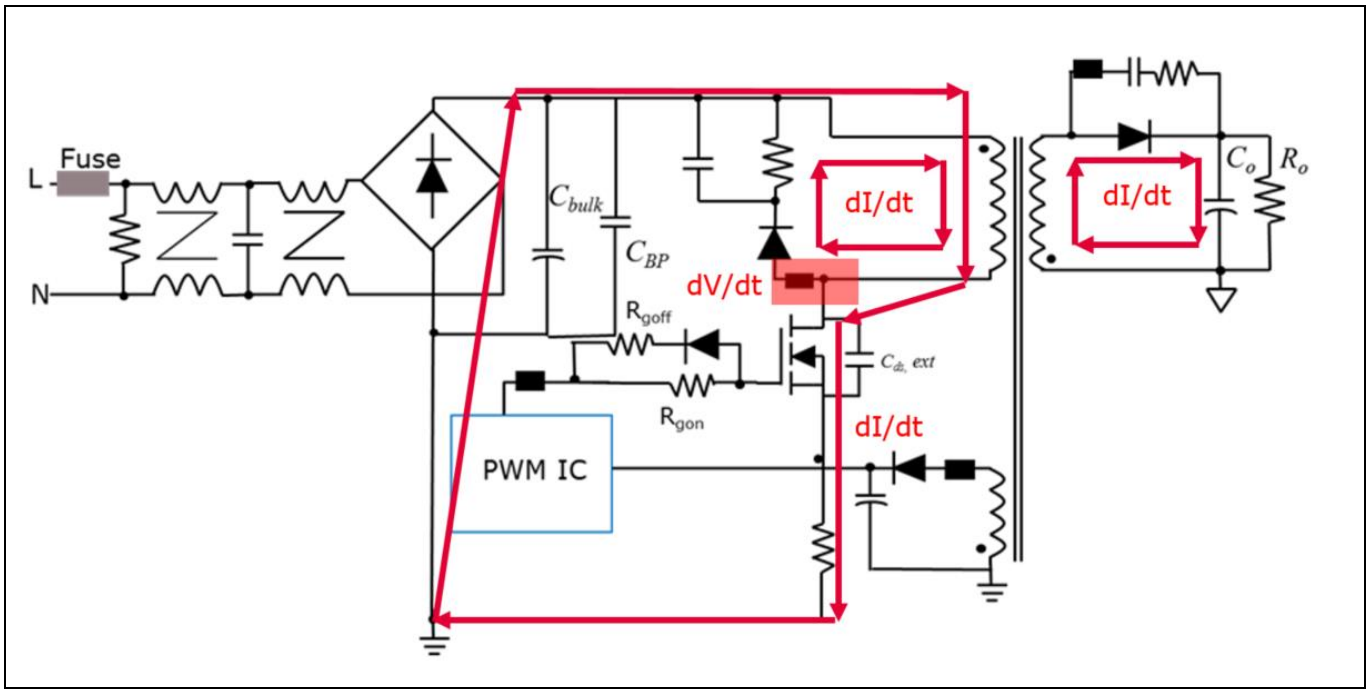

Figure 3 Typical Flyback power supply and key dV/dt net, dI/dt loops

Now that we have seen the critical loops and nodes in the system we will take a look at the MOSFET parameters and surrounding components that affect the dI/dt and dV/dt on the primary-side current loops and voltage nodes in a Flyback converter during turn-on and turn-off.

2.1 MOSFET turn-on noise

To see how the switching behavior of a MOSFET is affected by the external components, we will be using the Infineon 40 W adapter board EVAL_40W_19V_FLYB_P7 as a reference, operating at 230 V AC with an external constant voltage gate driver placed on the board.

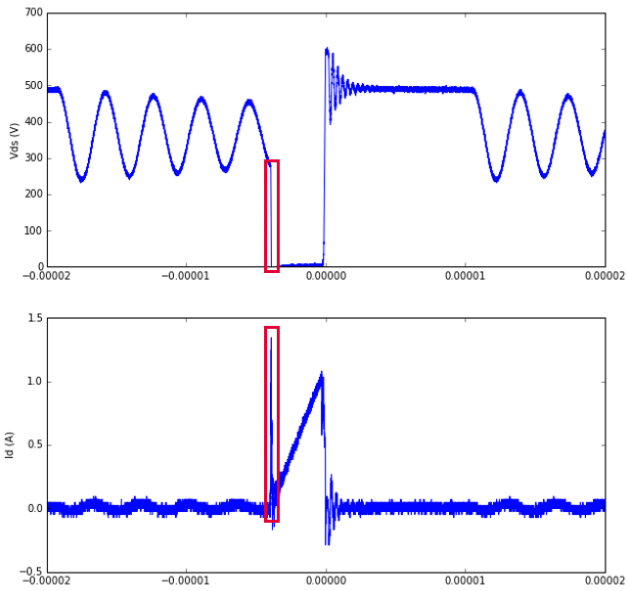

Figure 4 Typical Flyback turn-on drain source waveform (top) and current waveform (bottom) with the MOSFET turn-on portion highlighted in red

The waveforms shown in Figure 4 are of the 40 W board. As shown in the red boxes, there is a dV/dt caused as the MOSFET discharges energy stored in the output capacitance of the device as well as the energy stored in the lumped capacitance of the system parasitics. This dV/dt also ends up generating a corresponding discharge current, and so the faster the capacitance is discharged, the higher the current spike that will be generated.

Now the equations that determine the turn-on slopes in a DCM Flyback are as follows:

$$\frac{dV_{ds}}{dt} = \frac{V_{gs}}{R_{g\_on\_tot} \cdot C_{gd\_tot}}$$

$$I_{drain} = C_{ds_{tot}} \cdot \frac{dV_{ds}}{dt}$$

From this it can be seen that either an external C_{gd} capacitance can be added or the turn-on gate resistance can be increased to slow down the turn-on dV/dt. The turn-on spike current is controlled by gate resistance and C_{gd} as well, and it is also beneficial to reduce the total C_{ds} capacitance. Notice that C_{gs} does not play a role in the dV/dt or dI/dt of the MOSFET, so placing an external C_{gs} capacitor for EMI does not make sense.

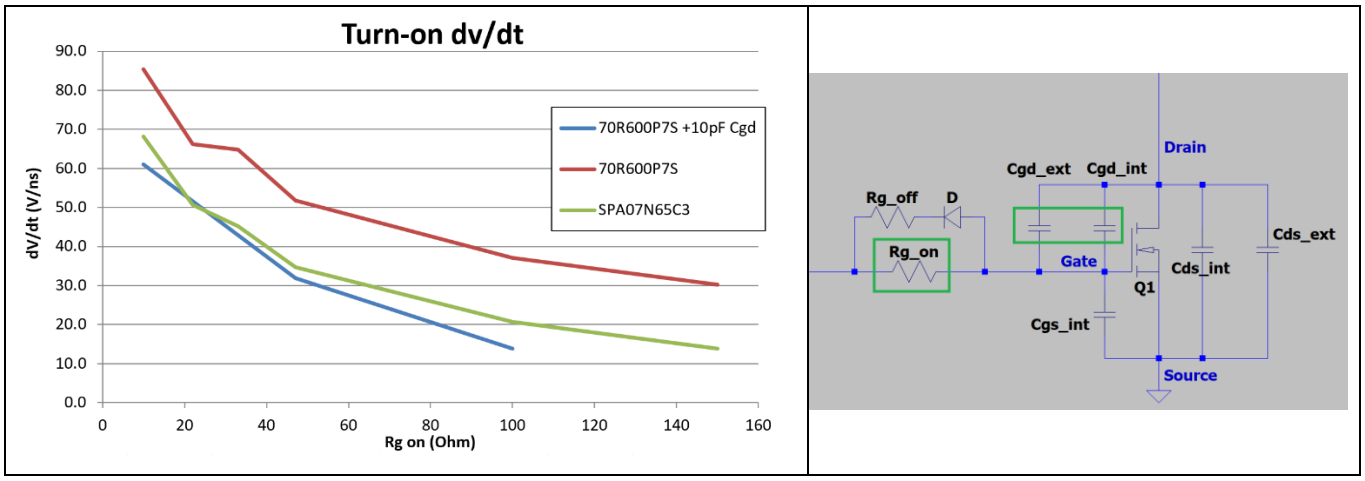

Figure 5 Effect of R_{g_on} and C_{gd} external (C_{gd_ext}) on turn-on dV/dt

Now the 40 W adapter was first tested with an SPA07N65C3 MOSFET to use as a slow switching reference since it is an older technology generation. The total gate resistance was adjusted from 10 Ω up to 150 Ω. It can be seen that as the R_g is increased the dV/dt of the system slows down. When replacing the C3 device with an IPA70R600P7S it can be seen that the dV/dt with the same R_g external is increased. The SPA07N65C3 with an R_g external of 40 Ω has a dV/dt of 40 V/ns while the P7 would need approximately 90 Ω to achieve 40 V/ns.

Adding a 10 pF 1 kV ceramic capacitor as a C_{gd} external then makes it so the P7 device has a similar turn-on dV/dt as the C3 device, but note that this will have a negative impact on the efficiency.

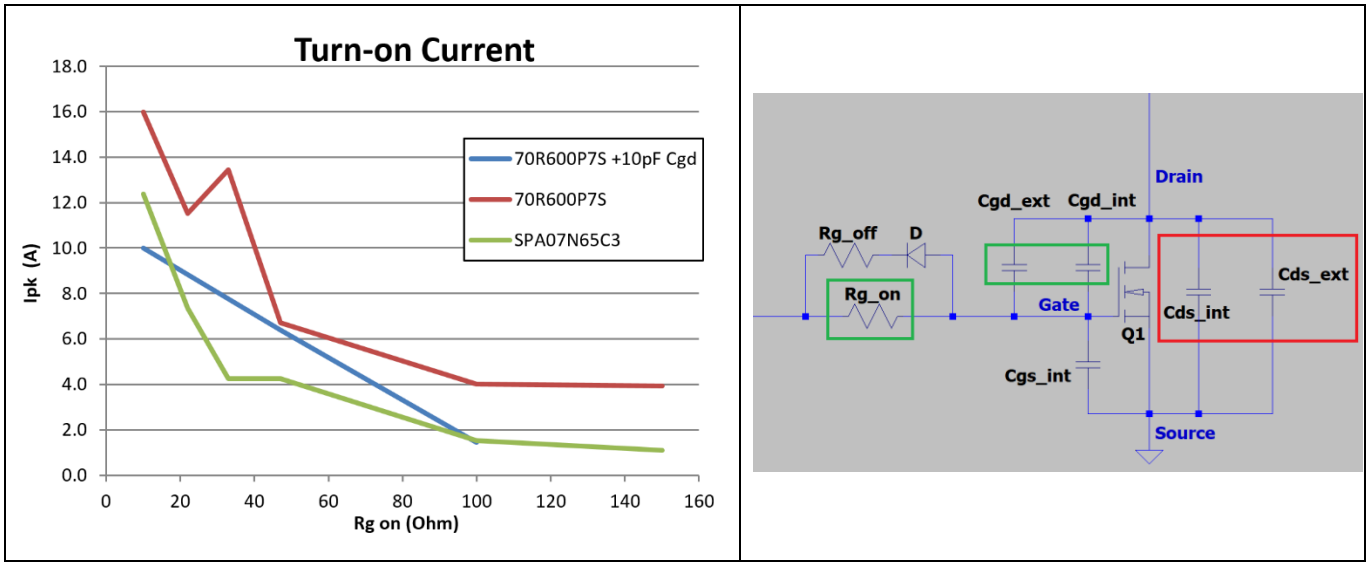

Figure 6 Effect of R_{g_on} and C_{gd} external (C_{gd_ext}) on turn-on dI/dt

Now the turn-on current spike follows the same trend as the dV/dt. By increasing the R_{g_on}, the turn-on current spike can be reduced and this causes the turn-on current dI/dt to be reduced. Adding the 10 pF of C_{gd} external then helps to make it so the current spike of the P7 is similar to the C3 device.

2.2 MOSFET turn-off noise

The same exercise with the 40 W adapter was also performed to check the turn-off noise of the MOSFET.

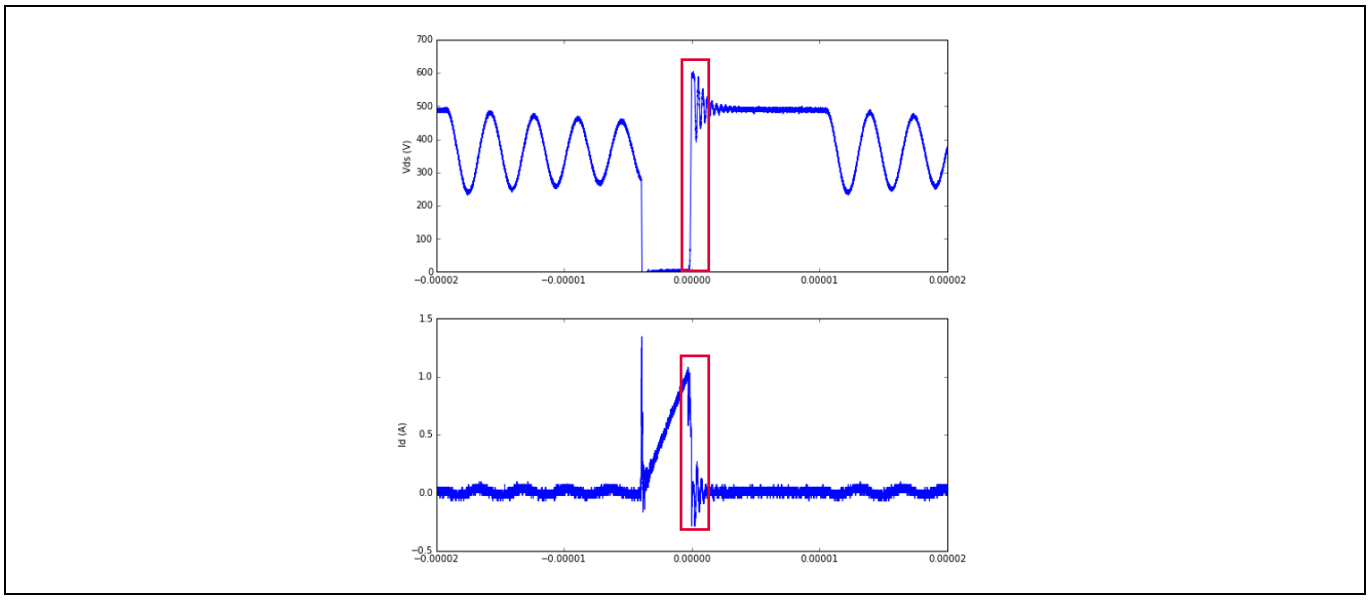

Figure 7 MOSFET turn-off dVDS/dt with turn-off slope highlighted in red and turn-off dI/dt slope highlighted in red

Figure 7 shows the turn-off dV/dt and dI/dt of the MOSFET. Here the energy stored in the magnetizing and leakage inductance transfers to the output capacitance of the C_{ds} of both the MOSFET and the overall system lumped parasitic capacitance. When the device is resistance limited the dV/dt of the device can be controlled using the same parameters that were used for the turn-on of the device.

$$\frac{dV_{ds}}{dt} = \frac{V_{gs}}{R_{\text{goff\_tot}} \cdot C_{gd\_tot}}$$

Once again it can be seen that the turn-off resistance and C_{gd_total} play a role in the switching times.

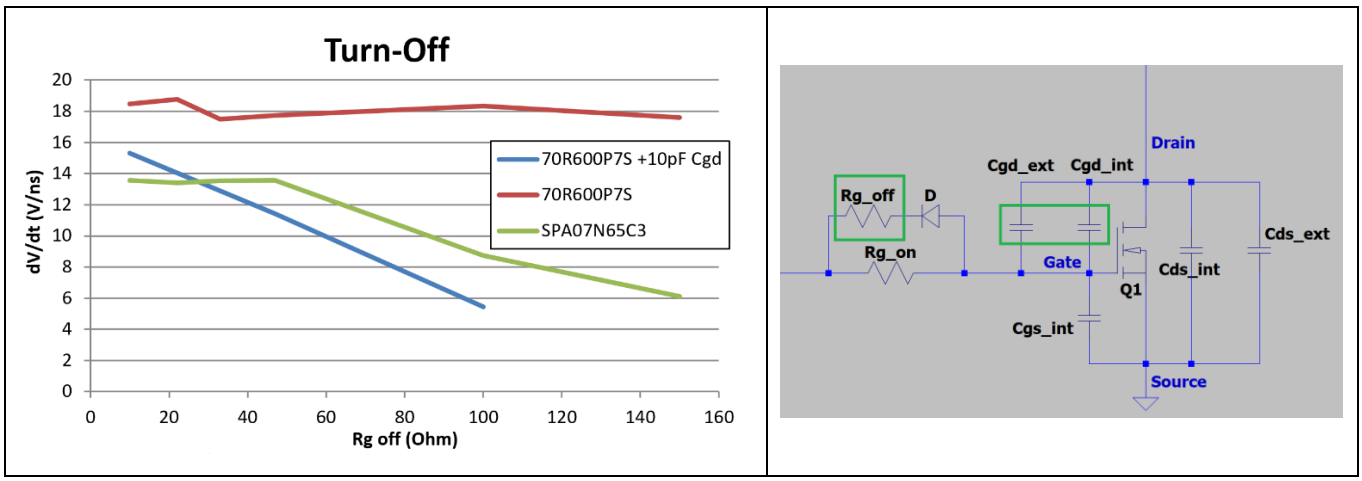

Figure 8 Turn-off dV/dt of the MOSFET vs. $R_{g\_off\_total}$

Figure 8 again shows the test results of the 40 W adapter dV/dt while varying the total external gate resistance. Even with 10 Ω of $R_{g\_off\_total}$ it can be seen that the fastest dV/dt is 18 V/ns, which we do not see in the turn-on until we get to at least 100 Ω of external gate resistance. Because the dV/dt is higher during the MOSFET turn-on, this makes it so the turn-off dV/dt usually does not have as large an impact on the EMI as the MOSFET turn-on.

In the testing done in the 40 W adapter it can be seen that the SPA07N65C3 and the IPA70R600P7S with 10 pF C_{gd} external both follow the trend of a lower dV/dt with an increasing gate resistance. The IPA70R600P7S without 10 pF does not follow this trend, however, so something else is going on. To better understand why the IPA70R600P7S does not seem to be controlled with the R_{g_off} we need to understand Early Channel Shut-Down (ECSD).

2.3 MOSFET Early Channel Shutdown

Normally a MOSFET will be controlled during turn-off by the external R_g and the C_{gd} total, similar to the turn-on of the device. Under certain conditions the MOSFET will turn off before the voltage on the output has begun to rise. This condition is ECSD. During this condition, the MOSFET behaves like a capacitor being charged by a current source. When the ECSD mode of operation is occurring, the slope of the turn-off is controlled by the following:

$$\frac{dV_{ds}}{dt} = \frac{I_{drain}}{C_{ds\_tot}}$$

Since the I_{drain} of the system is constrained by the design, the only way to slow down the MOSFET is to add some external C_{ds} capacitance.

The point where the ECSD occurs can be calculated by using the following equation:

$$R_{g\_ECSD} < \frac{V_{plateu} \cdot C_{ds\_tot}}{I_{drain} \cdot C_{gd\_tot}}$$

From this it can be seen that the ratio of C_{ds_tot}/C_{gd_tot} plays an important role, and it also makes it clear why in the 40 W measurements the P7 with no external C_{gd} looked uncontrollable. The P7 has a low C_{gd} when compared to the C3 devices, and this makes it so it was in ECSD even to beyond 150 Ω R_g external. This is done in the P7 technology intentionally to help improve the turn-off efficiency, but can make the P7 seem uncontrollable by just adjusting the R_{g_off}. By adding 10 pF C_{gd} the ECSD point was shifted to a lower R_{g_off} and the P7 became controllable by R_g external in a manner similar to a C3 device. The best way to control dV/dt of the MOSFET during turn-off while in ECSD is to increase the external C_{ds} capacitor value. However, this has a negative consequence on turn-on dI/dt, so a balance needs to be struck between these two noise sources.

2.4 Parasitic ringing and ferrite beads

We discussed the basic concepts of MOSFET dV/dt and dI/dt in the previous section and have seen the typical nets and loops associated with these transients, and which MOSFET parameters affect these noise sources. Figure 9 shows the Flyback power supply with different parasitics throughout the circuit.

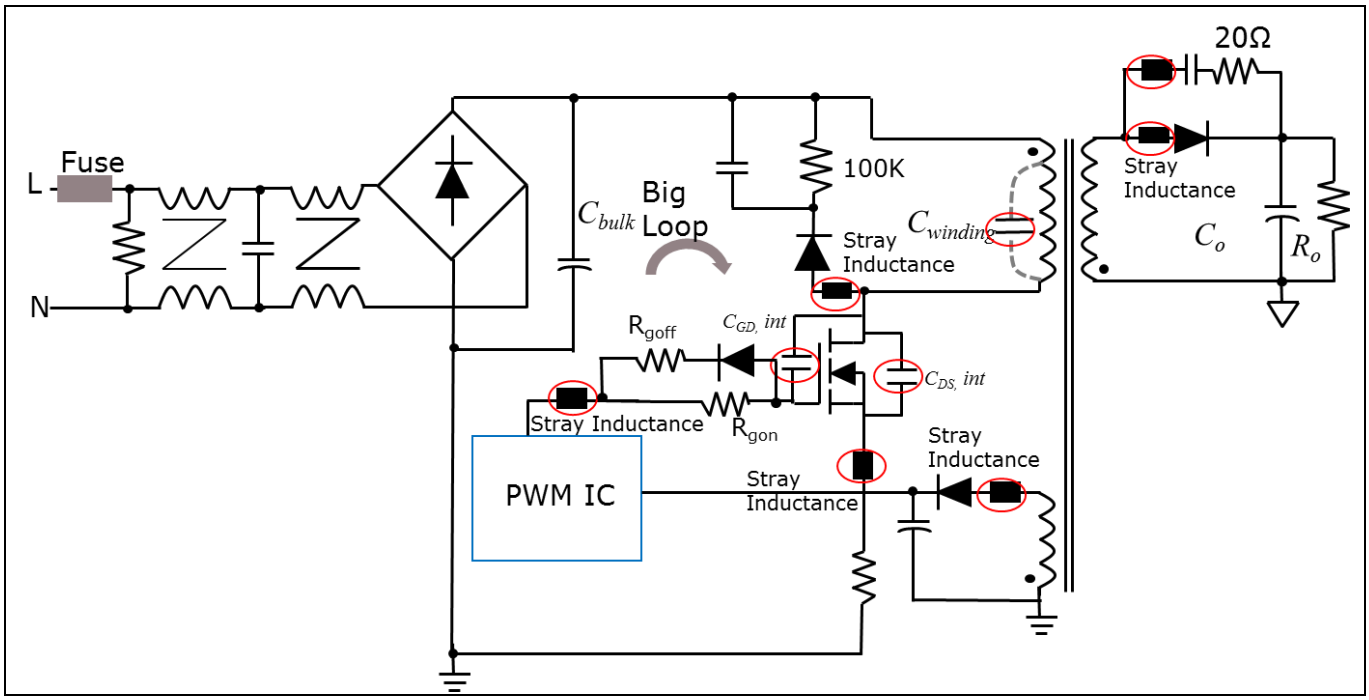

Figure 9 Flyback power supply and some associated parasitics

The various parasitics include stray inductances at the drain and source of the MOSFET as well as stray inductance in the gate driving stage, and stray inductances at the transformer output, output diode and the snubber stage. Stray inductance that is generally a few nH in value often leads to large voltage overshoots based on the dI/dt in the loop. Similarly, the stray capacitances include the MOSFET internal parasitics (including output capacitance and transfer capacitances) and the transformer winding capacitances that cause currents due to the dV/dt present at that net. The interaction of these noise currents and voltages leads to EMI.

From the previous figure, the various dI/dt sections present in the MOSFET loops have the following consequences:

- Noise voltage due to stray inductance at the gate
- Noise voltage due to stray inductance at the source
- Noise voltage due to stray inductance at the drain
- Noise voltage due to a big loop in the primary stage

To slow the dI/dt an extra, known inductance is added into the circuit. As this known inductance is in series with the stray inductance, the total value is always in the range of the added inductance, which is known to the designer. A ferrite bead is a passive device that filters high-frequency noise energy over a broad frequency range. It becomes resistive over its intended frequency range and dissipates the high-frequency energy in the form of heat.

Ferrite beads should be used carefully in the system, however. Adding ferrite beads does not always help because it is a complex impedance with frequency, and it can reduce noise at some frequencies while making noise even worse at other frequencies. A simple example of this would be unwanted resonance due to combining the ferrite bead with a decoupling capacitor for low-pass filtering. In this case you would filter higher frequencies, but introduce an LC resonance into the system. With a proper understanding and consideration of the ferrite bead's behavior, though, these issues can be avoided.

L_{bead}, the bead inductance, is calculated by the following equation:

$$L_{bead} = \frac{X_L}{2\pi f}$$

From a typical ferrite bead datasheet, the region where the bead is most inductive gives the frequency f, for example f = 30 MHz, then the X_L reactance at 30 MHz is found to be 233 Ω.

The above equation gives an inductance value (L_{bead}) of 1.2 µH for the typical ferrite bead. Most ferrite beads used in SMPS are in the range of 1.2 µH to 2.2 µH.

The parasitic capacitance and the DC resistance of the bead should be verified from the device datasheet so that impedance is effective at the desired frequency and DCR losses are minimized. Applying ferrite beads correctly can be an effective and inexpensive way to reduce high-frequency noise and switching transients.

Thus, a properly selected ferrite bead can be placed at the dI/dt transient sections of the MOSFET. The dI/dt of reverse recovery of the rectifier in the output and aux power circuit is controlled by switching on the primary side of the MOSFET. Hence, placing a bead at these points also helps reduce the EMI caused by dI/dt effects.

A ferrite bead on the source of the MOSFET should be used with caution, however. With EMI it is desirable to provide the lowest impedance return path to ground as possible. By adding a ferrite bead the whole MOSFET and noisy drain pad will have an even higher impedance to return to ground, and in some cases this can cause even more radiated EMI to be introduced into the system.

2.5 RCD snubber network

Aside from the MOSFET dV/dt and dI/dt a common source of EMI noise is the Flyback snubber network.

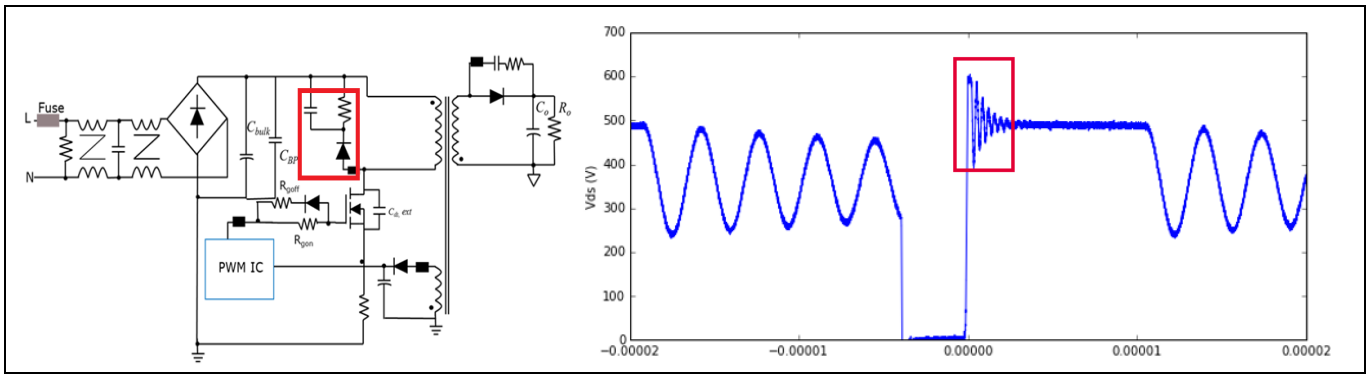

Figure 10 Left: typical RCD snubber network shown in red; Right: snubber and parasitic LC ringing

When the snubber begins conducting it causes the LC ringing of the C_{ds} total capacitance and transformer leakage inductance to go from a dampened sine wave with a main fundamental to something closer to a square wave, and the diode conduction has a reverse recovery spike and non-linear waveform. This waveform then introduces additional radiated noise. In order to improve the EMI of the snubber network an additional 5 Ω to 10 Ω in series with the RCD snubber network as well as a slower diode can help to reduce the noise created by the snubber network. Instead of using an ultra-fast diode such as the US1K, a standard diode such as a S1K should be used. This diode is slower to conduct, reducing the amount of radiated noise due to a longer reverse recovery time. The additional reverse recovery time has a nice additional effect of reducing the energy stored in the RCD capacitor and thus also helps improve the system efficiency.

2.6 Summary of lowering noise sources

As mentioned previously, slowing down the MOSFET operation is usually the last choice for improving a system's EMI because it has the consequence of reducing system efficiency. We will use the following circuit configuration to review what components need to be adjusted for each of the noise sources.

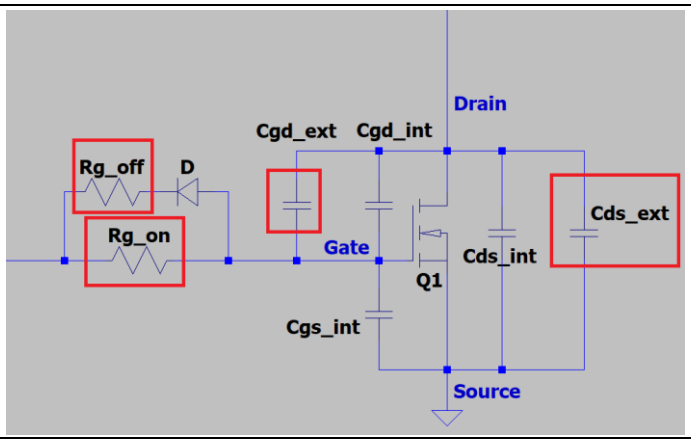

Figure 11 Basic MOSFET configuration with key EMI adjustment components highlighted in red

Table 1 Slowing down the MOSFET switching noise sources

Turn-on dV/dt	Turn-on dI/dt	Turn-off dV/dt Controlled	Turn-off dV/dt ECSD
Add C_{gd} external	Add C_{gd} external	Add C_{gd} external	
Increase R_{g_on}	Increase R_{g_on}		
		Increase R_{g_off}	
	Decrease C_{ds} external		Increase C_{ds} external

It can be seen in the table above that the C_{ds} external has the effect of making the turn-on dI/dt worse while making the turn-off dV/dt better. This means that there is usually a balance required, and that if the C_{ds} external is increased to slow down the turn-off dV/dt, the R_{g_on} or C_{gd} external also needs to be increased to maintain a similar turn-on dI/dt.

Sources of noise in a Flyback

The common options for dampening out ringing in the system are to place a ferrite bead in the following locations:

1. MOSFET drain (be careful about the ferrite bead DC resistance!)
2. MOSFET gate
3. Snubber network
4. Output diode
5. Output diode snubber

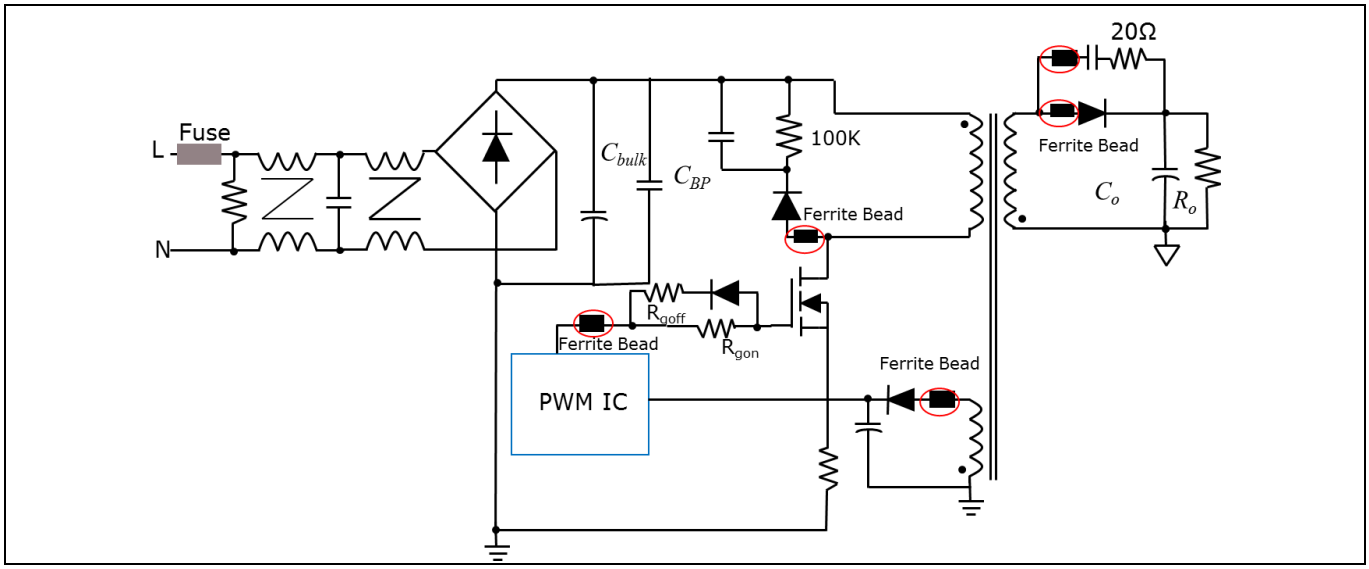

Figure 12 Common ferrite bead placement points for MOSFET dI/dt reduction

2.7 Flyback/PFC estimating substitution values

A common situation is when an old design is being updated from older-generation devices to newer CoolMOS™ generations. In this situation it is useful to have first estimated values to get similar turn-on and turn-off dV/dt and dI/dt since the EMI requirements need to be met without many degrees of design freedom. Usually for low-power Flybacks it is safe to assume the CoolMOS™ P7 will be in ECSD so then the following technique can be used by taking data from the device datasheets:

1. Take the C_{oss} of the reference part and the new part and take the difference in the linear region of the C_{oss} curve.
2. Since the newer-generation device output capacitance is lower the difference should be added to the external C_{oss}.
3. Take the ratio of the C_{rss} curves from the datasheet of the old C_{rss} divided by the new C_{rss}. This gives an idea of the difference in the MOSFETs' C_{gd}.
4. Multiply this ratio of old MOSFET C_{gd}/new MOSFET C_{gd} by the R_{g_on} to get the new R_{g_on}.

Now we will take a look at a practical example, below:

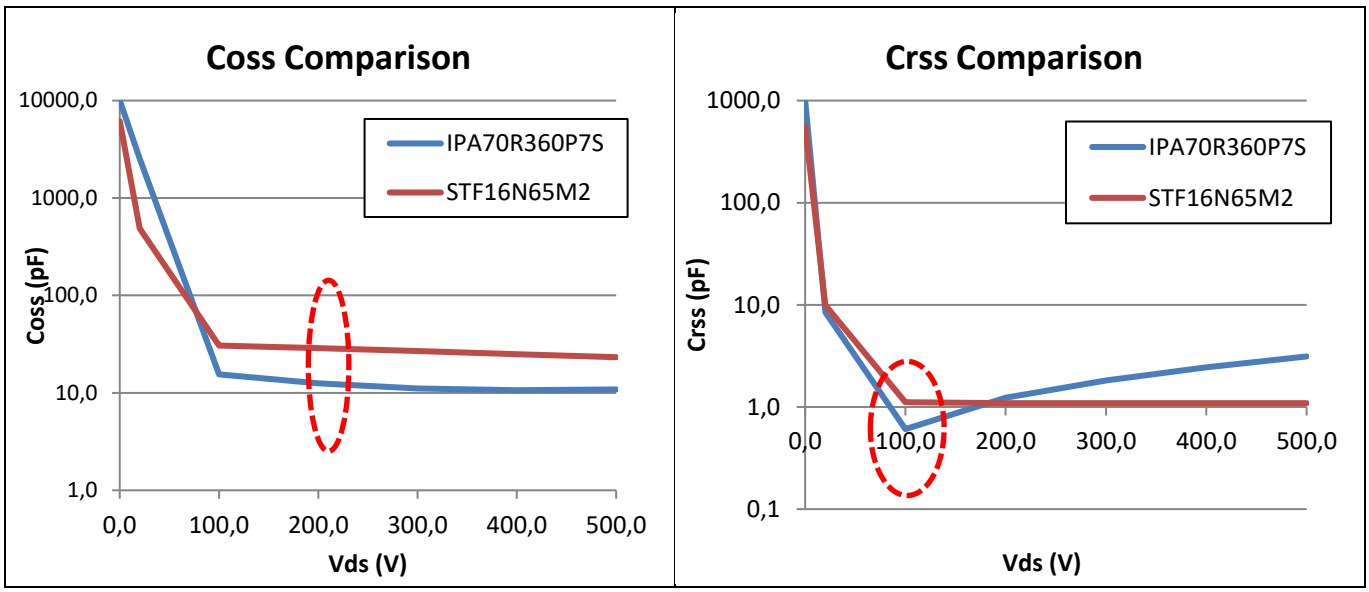

Figure 13 IPA70R360P7S and STF16N65M2 C_{oss} and C_{rss} datasheet comparisons

The information from the C_{oss} and C_{rss} curves in the datasheet graphs is taken from both the IPA70R360P7S and the STF16N65M2 datasheets.

First, we will look at the C_{oss} values. The STF16N65M2 has 28.9 pF of capacitance at 200 V. The IPA70R360P7S has 12.6 pF. The difference is then 16.3 pF of capacitance. The PCB already had a 1 kV 1206 ceramic capacitor of 47 pF drain source capacitance, so 47 pF + 16.3 pF would mean we need a 63.3 pF total drain source capacitance external to match the STF16N65M2 with a 47 pF capacitor external. The closest standard capacitance value is 68 pF, so this would be the first value to try.

Now, taking a look at the C_{rss} ratio of the devices, it can be seen that 100 V is where the P7 has the smallest C_{rss} compared to the M2 device. Here the M2 has 1.1 pF of capacitance while the P7 has 0.6 pF of capacitance at 100 V. Taking the 1.1 pF and dividing by 0.6 pF gives us 1.83. If the original design had 100 Ω for the turn-on resistor than a good guess for the new turn-on resistor to try would be 180 Ω.

From this a first guess value to slow down the MOSFET can be derived as a 68 pF C_{ds} external and a 180 Ω R_{g_on}.

3 Preventing transmission of noise

3.1 Layout practices for reducing dI/dt and dV/dt in Flyback power supplies

For EMI issues the first place to try to optimize the design is to always minimize the layout-critical dI/dt loops and the critical area of the switch node, because this will reduce the noise transmission to the outside world without reducing the system efficiency. Reducing the primary MOSFET loop can be done by adding a high-frequency, high-voltage DC capacitor (preferably a ceramic dielectric) to reduce the effective loop area. A SMD ceramic capacitor also gives the benefit of having a low series inductance and low series resistance, so it is effective to much higher frequencies than the large electrolytic capacitors used on the input of the power supply. This is shown as the C_{BP} in Figure 3.

Switching loop areas as shown in Figure 3 should be kept to a minimum. Reduce the unintended antennas in circuit boards, such as:

1. Long traces – keep the traces on high dV/dt nodes as short as possible.
2. Vias – make sure that for every noisy via going through the PCB there is a nearby ground plane via going through the PCB to keep the return path short.
3. Component leads and pins – reduce stray inductances with short leads.
4. Placement of SMD ceramic decoupling capacitors between power and ground near drivers and ICs.
5. Power planes should be backed off from the edges of the PCB.
6. Avoid traces cut within ground or power planes, which can create an unintended aperture or slot antenna.
7. Avoid loop antennas that encompass any route in which both forward and return currents are on a well-defined conducting path.
8. In single-layer designs try to keep a ground trace around the edge of the PCB as an EMI guard ring.

3.2 Heatsink grounding to input bulk capacitor return rather than chassis ground

Ground the heatsink to PCB ground/input bulk capacitor return to reduce common mode noise and radiated noise. The capacitive coupling of a TO-220FP to the heatsink is a critical loop to watch out for EMI.

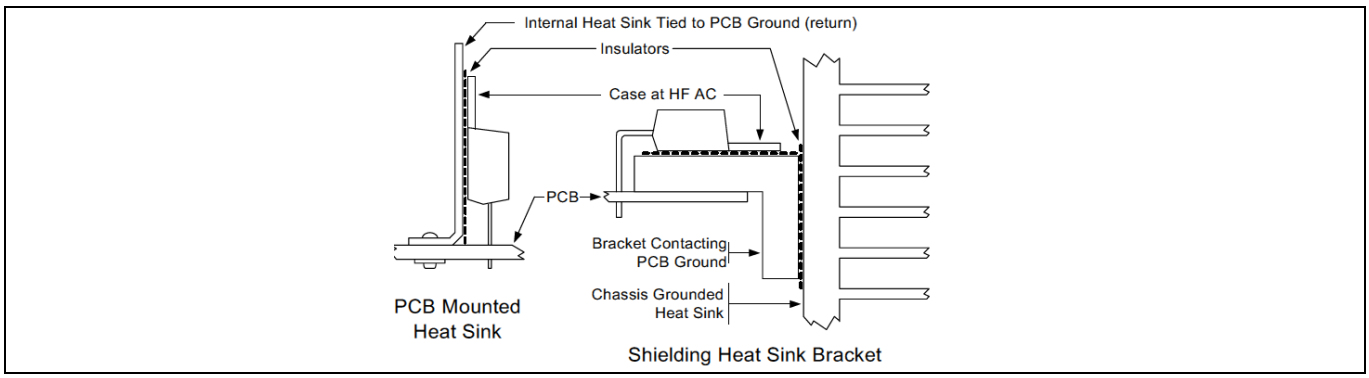

Figure 14 Two heatsink arrangements that divert capacitively coupled noise to circuit common rather than chassis ground

3.3 Y-capacitors

Apart from having the parasitic winding capacitance in a Flyback transformer as shown in Figure 9, practical transformers also have stray capacitance between the primary and secondary windings. This capacitance interacts with the switching operation of the converter. Since there is no other connection between input and output this will result in a high-frequency voltage between the input and output. The cables from the power supply are now acting as an antenna, transmitting the high frequency generated by the switching process.

To suppress the high-frequency common mode noise, it is necessary to put capacitors between the input and output side of the power supply with a capacitance substantially higher than the capacitance in the Flyback transformer. This effectively shorts out the high-frequency noise and prevents it escaping from the power supply.

When designing a Class 2 (unearthed) power supply such as a charger, there is no alternative but to connect these capacitors to the input live and/or neutral. However, short-circuit failure of these capacitors would be a serious issue. In a Class 1 power supply such as the adapter, failure of the capacitor between the mains supply and mains earth would mean a short to earth (equivalent to a failure of basic insulation). In a Class 2 PSU a failure of the capacitor is much worse; it would mean a direct and serious safety hazard to the user (equivalent to a failure of double or reinforced insulation). To prevent hazards to the user, the capacitors must be designed so that short-circuit failure is very unlikely.

Hence, special capacitors are needed for the purpose of isolating noise voltage due to transformer parasitic capacitances. These capacitors are known as “Y-capacitors” (X-capacitors, on the other hand, are used between mains live and mains neutral). There are two main sub-types of Y-capacitor, Y1 and Y2 (with Y1 being the higher-rated type).

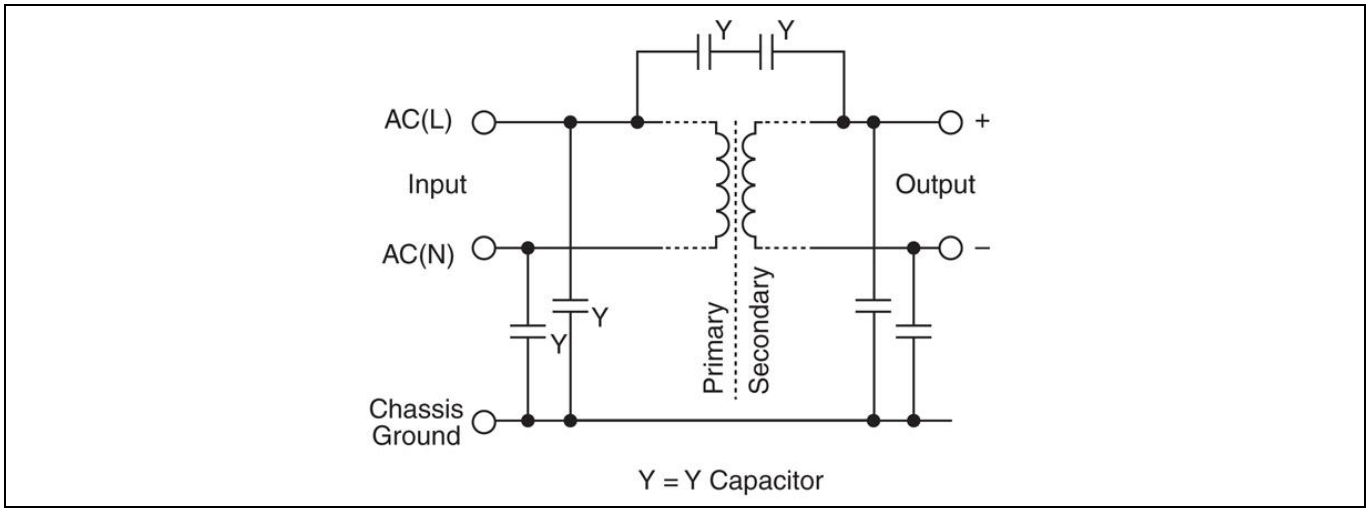

Figure 15 Using Y-capacitors to limit noise due to transformer parasitic capacitance

3.4 Transformer shielding

Transformers can be designed with a Faraday shield or copper foil between the primary and secondary windings. A Faraday shield connected to the primary and secondary grounds ensures noise voltages are safely returned to the respective grounds. It effectively works to reduce the primary to secondary capacitance mentioned in the previous section and reduce the common mode noise generated from this capacitance. More information can be obtained from application notes [3] and [4] in the reference section.

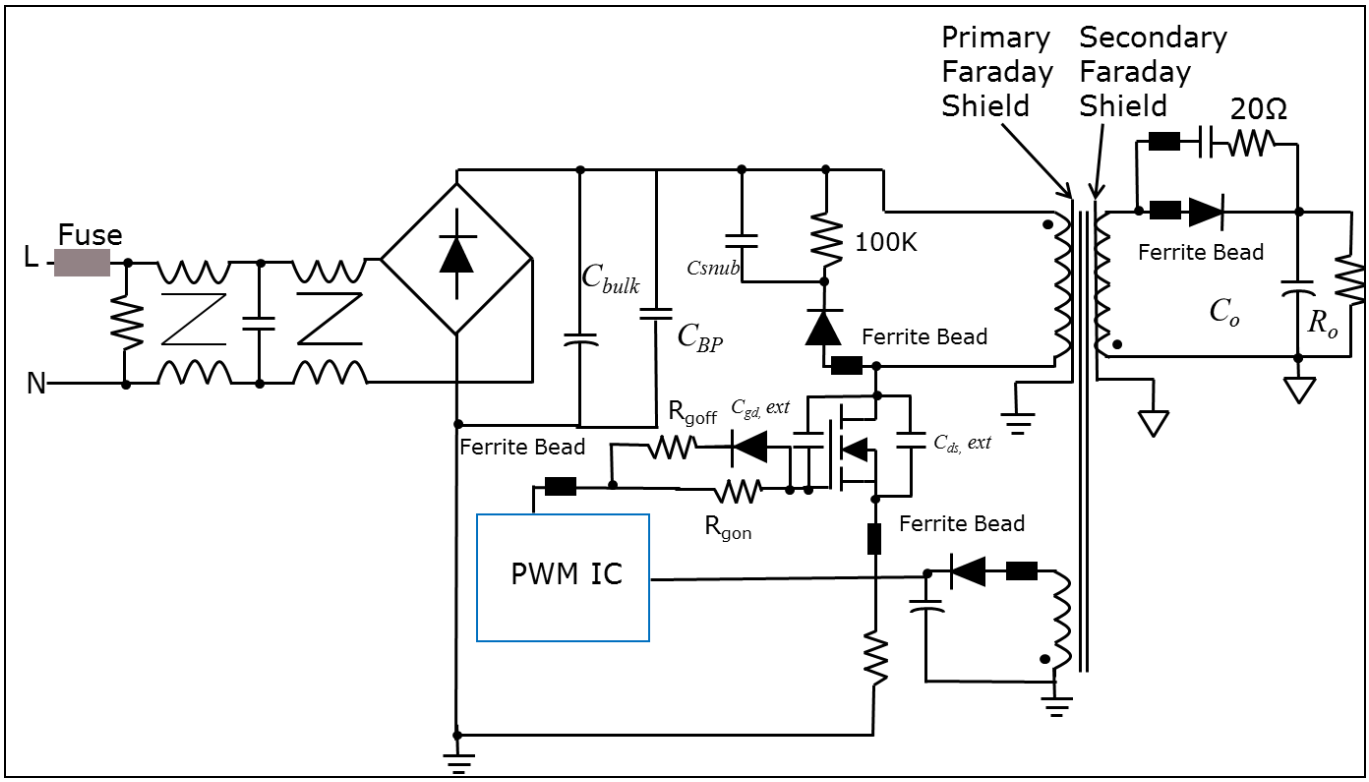

Figure 16 Transformer shielding to minimize noise coupling due to parasitic capacitances between primary and secondary

3.5 Variable- Frequency PWM controller with frequency modulation

Apart from the techniques discussed above, for Flyback converters that are controlled by a square wave with a constant frequency and duty cycle (D), the conventional technique to reduce EMI consists of using passive filters. This has limitations: size, weight, design complexity, efficiency, cost, etc. Modern Variable Frequency (VF) or frequency jittering EMI reduction techniques are available to overcome the problems faced in filter solutions. The interleaving technique is used to equally share the total power to be delivered; the general idea in VF spread spectrum signaling is shown in Figure 17. Although the spectrum distribution is different between Figures 17(a) and (b), the total energy is the same in both cases, although the peak level has reduced in Figure 17(b). Switching Frequency Modulation (SFM) is an effective method to reduce EMI in SMPS. This technique is based on the original Spread Spectrum Clock Generation (SSCG) techniques. Using SFM, there is a trade-off between the amplitude reduction of the EMI harmonics and the generation of a set of additional sideband harmonics with a smaller amplitude.

The PWM spread spectrum control principle of an SMPS is described below:

f = fs + Δf, where fs is the reference frequency of the PWM switch; Δf is the additional spread spectrum signal frequency, which is changing frequency according the time-domain characteristics of the spread spectrum signal.

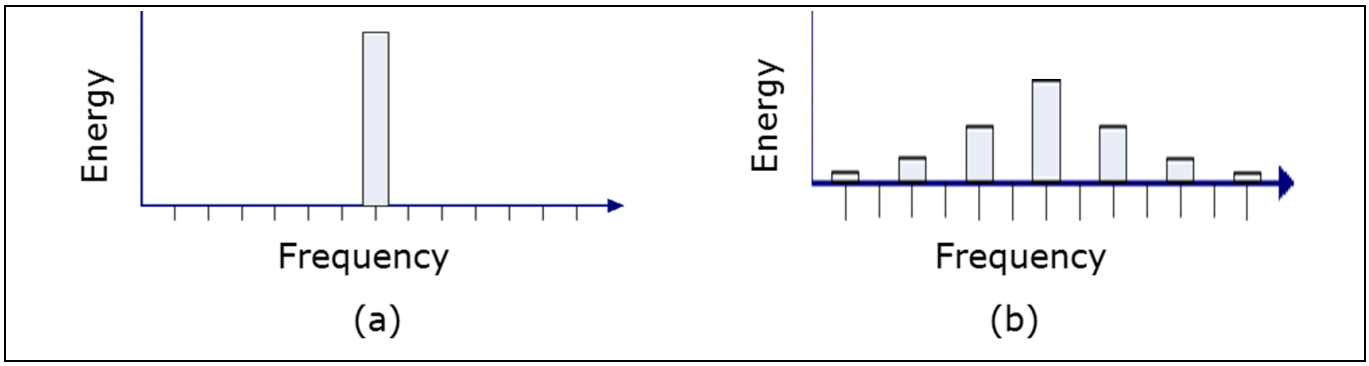

Figure 17 Spread spectrum frequency generation using VF PWM controllers

The advantage of this non-linear control design approach is the simplicity of the circuit: even basic SMPS control circuits from many IC manufacturers can be used with only a few additional passive components. The main drawback of this approach is that the designer must carefully study the circuit performance at all load conditions and parameter variations to ensure the spread spectrum operation and overall system stability in all cases.

Infineon has many PWM controllers such as the ICE5xSAG, which employ such frequency modulation techniques to reduce EMI at the controller level.

4 Practical example – 45 W adapter

For a detailed explanation of designing a 45 W adapter while meeting radiated and conducted EMI requirements and not sacrificing efficiency, the 45 W 19 V adapter reference board [5] has a very good walkthrough of the design process. In this design the focus was not to slow down the MOSFET, but instead to focus on the transformer design, high-frequency loops and line filter design, and it gives a good overview of how to approach meeting both EMI and efficiency requirements for a specific design.

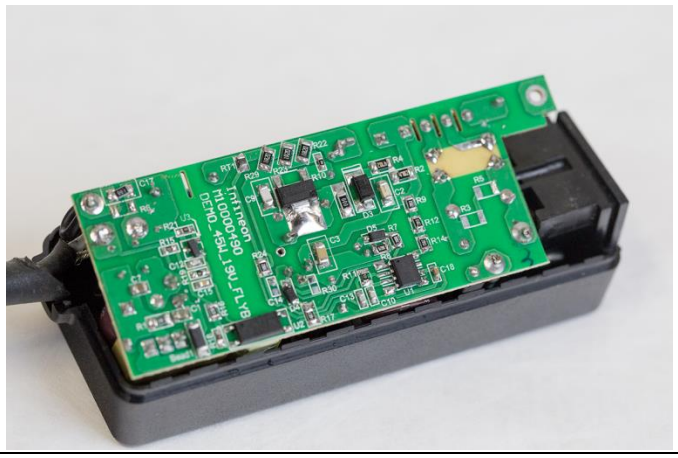

Figure 18 Bottom side of the 45 W P7 SOT-223 demo board shown inside an enclosure

Table 2 45 W NB adapter reference board specifications

Input voltage and frequency	**90 V AC (60 Hz) ~264 V AC (50 Hz)**
Output voltage, current and power	19 V/2.37 A/45 W
Active-mode four-point average efficiency (25 percent, 50 percent, 75 percent, 100 percent load) (EU CoC Version 6)	More than 88 percent
No-load power consumption	Less than 100 mW
Conducted emissions (EN 55022 Class B)	Pass with 6 dB margin for QP and average
Radiated emissions (EN 55022 Class B)	Pass with 6 dB margin for QP
PCB form factor (L × W × H)	86 × 35 × 20 mm

5 Conclusion

When designing with the latest CoolMOS™ MOSFETs, either for improving efficiency or for cost optimization, care should be taken with respect to the switching parameters of the CoolMOS™ SJ MOSFET. The difference in switching characteristics is highlighted in the EMI testing, and often the techniques discussed in this application note are required to meet the EMI requirements with a margin. The big gains in efficiency and thermal performance when using CoolMOS™ devices are often reduced by the need to meet EMI margins. It is for the power supply designer to find the optimal trade-off between efficiency and EMI to effectively reap the benefits of CoolMOS™ devices.

Apart from reducing the dI/dt and dV/dt of the CoolMOS™, the designer can also look at a system solution approach of optimizing the PCB layout, using Y-capacitors with correct grounding, shielding the switching transformer with correct grounding, grounding the heatsink and using a PWM controller with variable frequency including frequency modulation options to improve EMI while not sacrificing efficiency.

6 Appendix: Reading EMI measurement plots

The typical conducted and radiated EMI limit lines are shown in Figures 19 and 20.

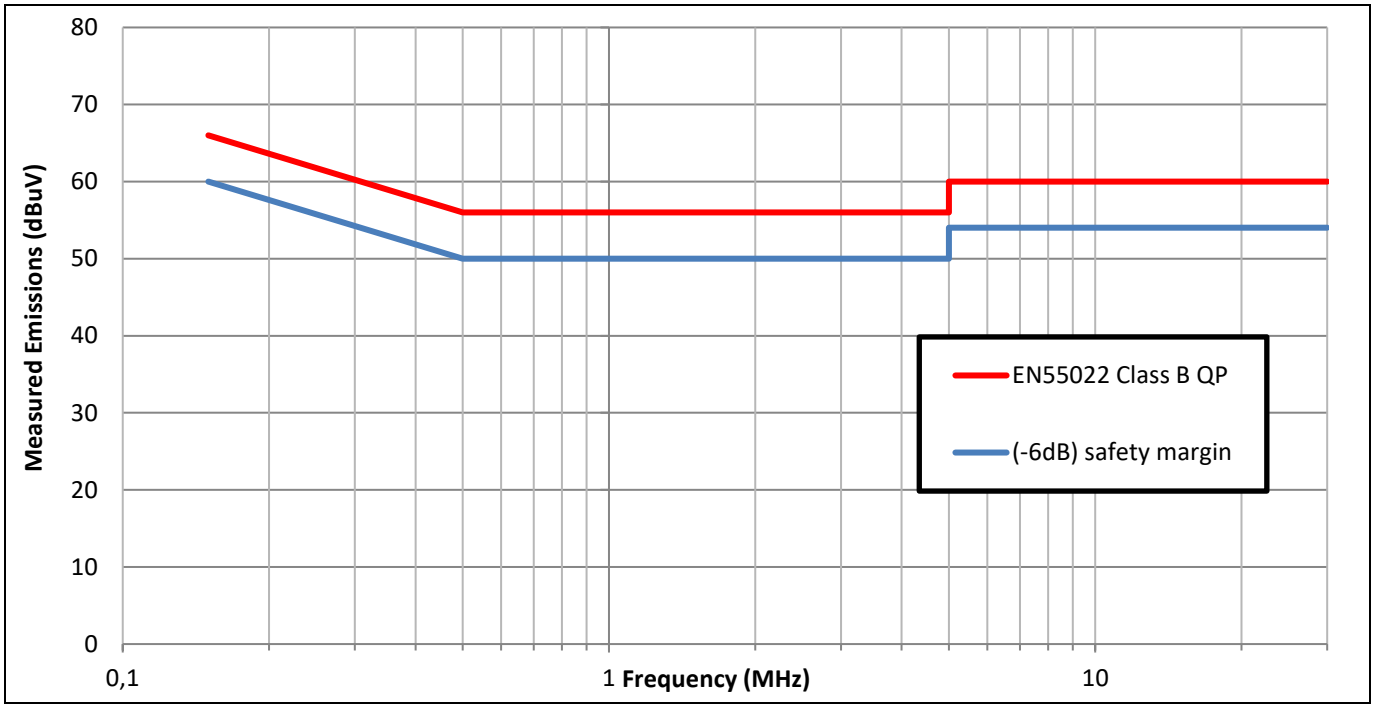

Figure 19 Conducted emission test limits – 150 kHz to 30 MHz

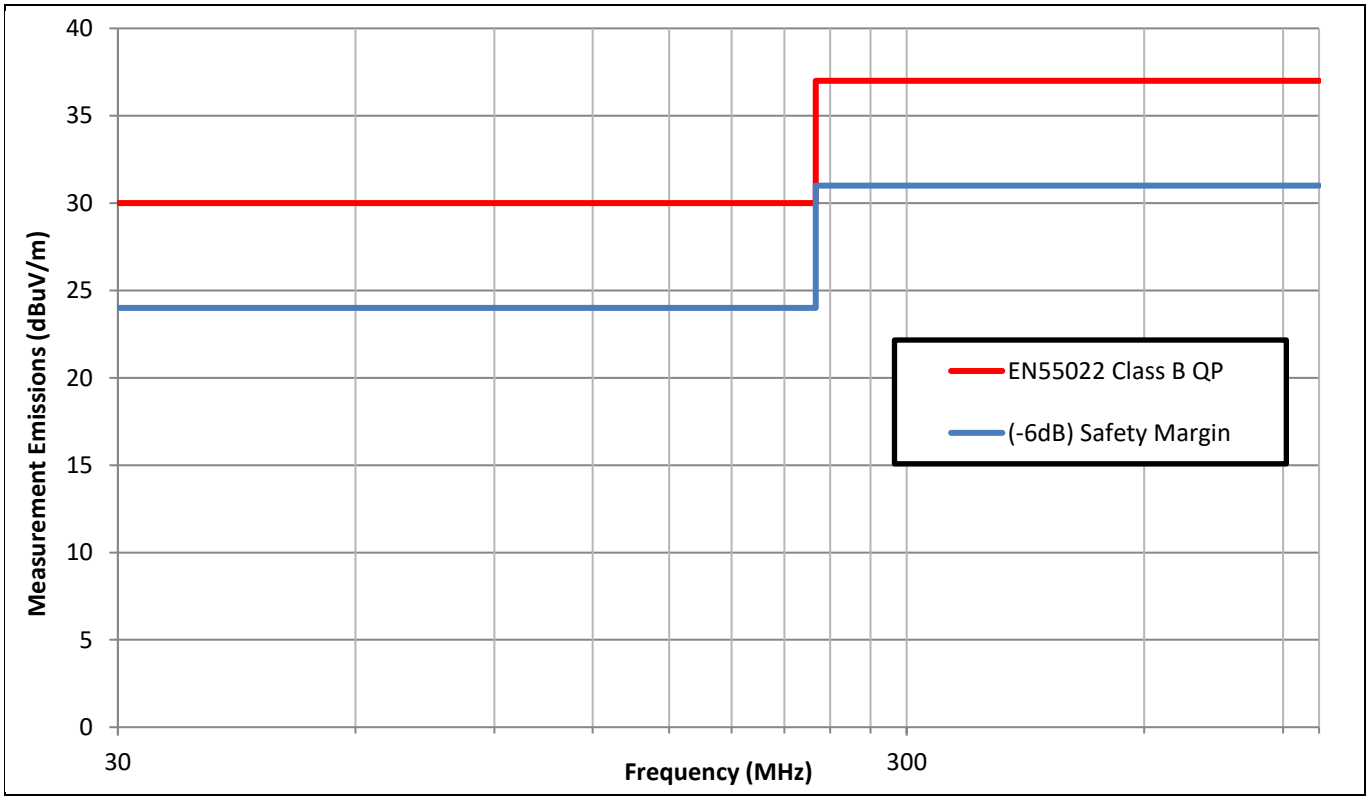

Figure 20 Radiated emission test limits – 30 MHz to 1 GHz

Appendix: Reading EMI measurement plots

Based on the detector used in the spectrum analyzer, average, Quasi-Peak (QP) or peak measurements can be obtained. Peak detection will always give the highest reading, followed by QP and then average readings. Therefore, to perform EMI scans quickly most engineers prefer peak detection and then compare the results against QP limits. If this condition is met, then in effect additional headroom (safety margin) is achieved. QP detection should only be performed when the peak detection test (with QP limits applied) marginally fails.

Typically, a -6 dB safety margin is desired to account for measurement inaccuracy, board-to-board variations, etc. Usually, if the QP limits are met the average limits (using average detection and average limits) are also met. At frequencies below approximately 5 MHz, the noise currents are predominantly differential mode, whereas at frequencies above 5 MHz the noise currents are predominantly common mode. At frequencies above 20 MHz, the conducted noise is attributed to inductive pick-up, which can be the radiation from the input or output cables.

7 References

[1] CoolMOS™ C6 – Mastering the Art of Slowness
http://www.infineon.com/dgdl/Infineon+-+Application+Note+-+PowerMOSFETs+-+600V+CoolMOS%E2%84%A2+-+C6+-+Mastering+the+Art+of+Slowness.pdf?fileId=db3a3043271faefd0127903d130171e1

[2] CoolMOS™ C7 – Mastering the Art of Quickness
http://www.infineon.com/dgdl/Infineon+-+Application+Note+-+650V+CoolMOS+C7+-+Mastering+the+Art+of+Quickness.pdf?fileId=db3a30433e5a5024013e6a966779640b

[3] Transformer construction techniques
http://www.infineon.com/dgdl/an-1024.pdf?fileId=5546d462533600a401535591115e0f6d

[4] Meeting EMI-EFT requirements on a system level
http://www.infineon.com/dgdl/AN-PS0001+Lightning+test.pdf?fileId=db3a304412b407950112b4182a8224f9

[5] 45 W 19 V adapter reference board using the 700 V CoolMOS™ P7 in SOT-223 package
https://www.infineon.com/dgdl/Infineon-Engineering_report_demo_board_DEMO_45W_19V_FLYB_P7-AN-v01_01-EN.pdf?fileId=5546d46261ff5777016242b56c745be0

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Document version	Date of release	Description of changes

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