XDPP1100 two-phase interleaved buck-boost

-48 V to 28 V 780 W digital power supply

About this document

Scope and purpose

The non-isolated -48 V to 28 V inverted buck-boost converter is often used in the telecom base station power amplifier (PA) power supply unit (PSU). This topology has inverted output, converting negative input voltage to positive output voltage. It supports both step-down (buck) and step-up (boost) voltage conversion. The buck-boost capability makes the topology suitable for PA applications where the PSU output voltage needs to be adjusted up and down based on the amplifier traffic demand.

In fifth-generation (5G) wireless communication, high-performance PSUs are required to support higher power than the fourth generation (4G). High efficiency, fast dynamic response, flexibility to adjust output voltage, and field upgrade capability are major features that are required. The XDPP1100 digital controller is designed for isolated and non-isolated DC-DC converters for telecom applications. This 780 W interleaved buck-boost converter (VD_XDP_2Ph_INV_BUCK_BOOST) utilizes the features of XDPP1100. An **extremely efficient, 97 percent peak** is achieved by an **active zero-voltage-switching (ZVS) circuit that transfers Q_{rr} charge of the SR MOSFET to the output capacitor in a lossless way, while achieving ZVS in the control MOSFET**. The hardware (HW)-based PID compensation enables fast dynamic response; the voltage adjustment is achieved by system-level PMBus communication; and the 64 kB OTP memory provides firmware (FW) and configuration upgrade capability through the I^2C protocol. This document describes the design details of the inverted buck-boost converter, and shows the performance of the evaluation board.

Intended audience

Telecom power supply designers, telecom system designers.

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1 General introduction

The input voltage of the board is -36 V to -60 V. The nominal output voltage is 28 V and can be adjusted from 20 V to 56 V. The maximum output current is 28 A, and the maximum output power is 780 W. The board is designed to operate in still air. All the switch MOSFETs are attached to a piece of heatsink for thermal distribution. An auxiliary power supply on the board provides bias voltage for gate drivers and 3.3 V V_{DD}.

A two-phase solution is selected to use a smaller inductor. The XDPP1100-Q040 controller drives two phases with 180-degree phase shift for ripple cancelation. The current balancing between the two phases is achieved by the built-in current balancing circuit of the controller. The current of each phase is sensed via the DC resistance (DCR) of the buck-boost inductor, reducing the component count and eliminating additional power loss on current shunt. The temperature compensation is built into the XDPP1100 FW ROM code, and can be enabled by configuration.

The input -48 V return is the ground reference of the control IC. To drive the control FET (bottom FET) and SR FET (top FET), Infineon isolated gate driver 2EDF7275K is used. The XDPP1100 senses the secondary voltage of the auxiliary power supply for input voltage telemetry and protection.

Test points are placed on the top side of the PCB for easy probing and debugging.

The FW patch features are described in **chapter 3**.

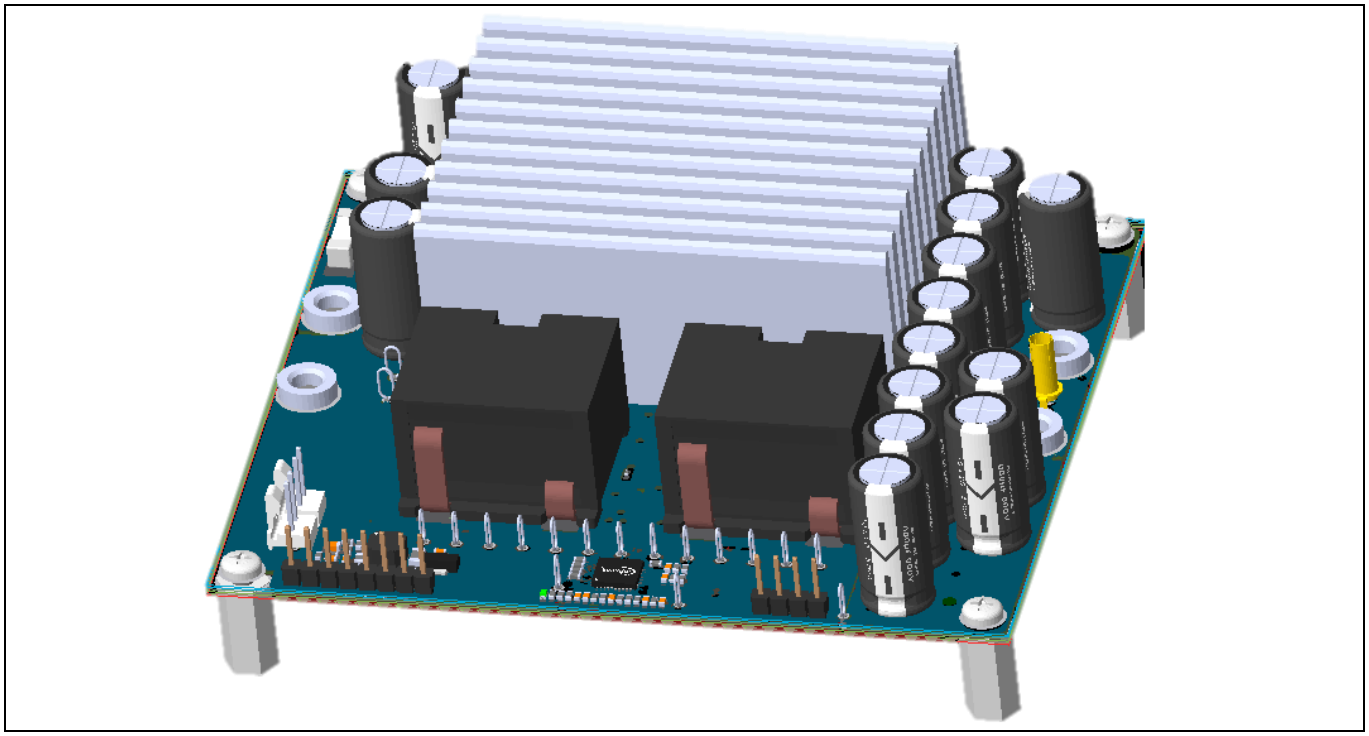


Figure 1 Board picture

The main Infineon components used in the VD_XDP_2Ph_INV_BUCK_BOOST are as follows:

- Digital controller **XDPP1100-Q040**
- OptiMOS™ 150 V 11 mΩ **BSC110N15NS5** for both high-side and low-side switches
- OptiMOS™ 150 V 30 mΩ **BSZ300N15NS5** as active clamp FET
- Isolated gate driver **2EDF7275K**

1.1 Specification

Table 1 Design specification

	Min.	Typ.	Max.	Unit
Input voltage range	-36	-48	-60	V
Input current			22.5	A
VIN_ON		33		V
VIN_OFF		30		V
Output voltage range	20	28	56	V
Output current			28	A
Output power			780	W
Output voltage ripple (peak-to-peak at full load) Measured at 20 MHz bandwidth with 2.2 µF cap			50	mV
Switching frequency		200		kHz
Efficiency at -48 V_{IN}, 28 V_{OUT}, full load		97		%
Output voltage load regulation			±2	%
Load transient (0% to 100% load, with 25%, 50%, 75% duty and 1 kHz, transition rate 5 A/us)			±1	V
Load-transient settling time		300		µs

The output voltage can be configured from 20 V to 56 V, using PMBus command VOUT_COMMAND. The maximum output power is limited to 780 W. At output voltage higher than 28 V, the rated output current reduces, as shown in **Figure 2**.

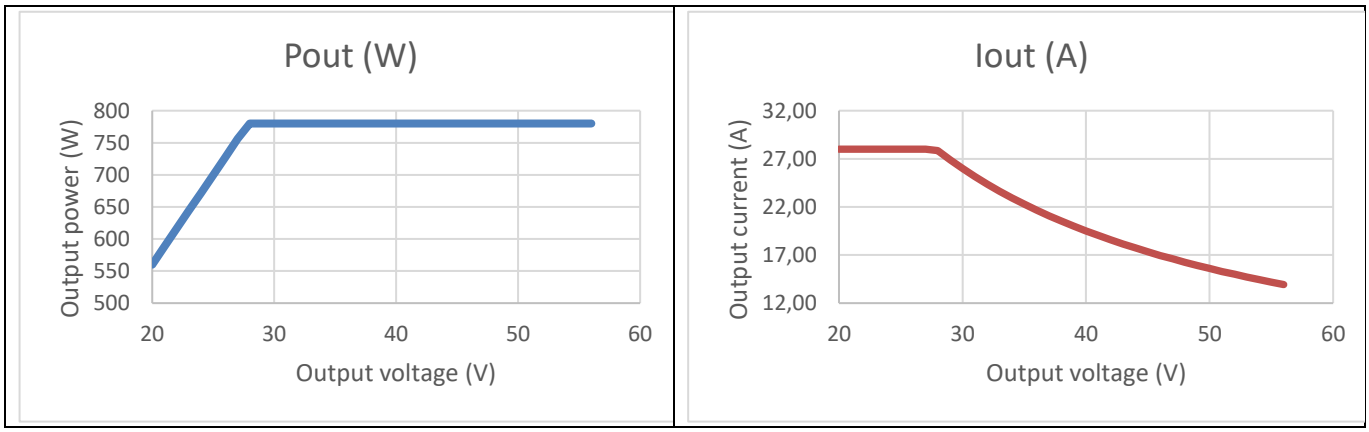


Figure 2 Rated power and rated current curve

1.2 Block diagram

The block diagram of the two-phase interleaved inverted buck-boost is shown in **Figure 3**.

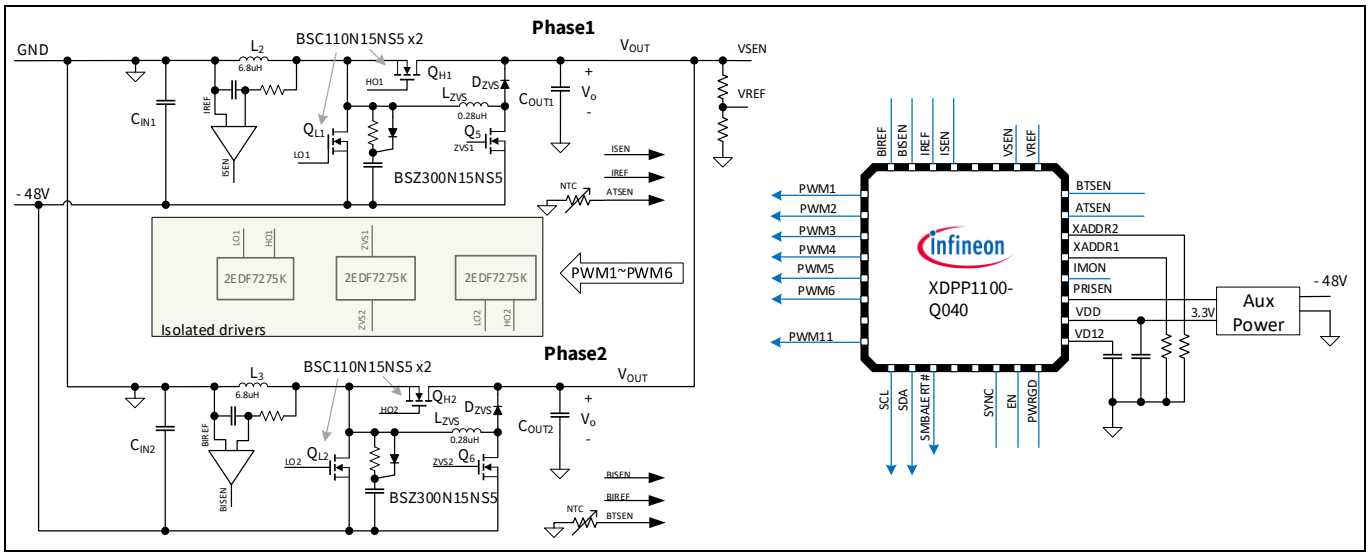


Figure 3 Block diagram of the interleaved inverted buck-boost with active ZVS

2 System and functional description

2.1 Inverted buck-boost converter

The simplified inverted buck-boost circuit is shown in **Figure 4**. Q_1 is the control FET, Q_2 is the SR FET. Q_1 and Q_2 turn on alternately.

- When Q_1 is on and Q_2 is off, the input voltage applies on the inductor L_1. Inductor current increases and energy is stored in the inductor. The inductor charging current slope is V_{IN}/L.
- When Q_1 turns off, the inductor current continuously flows in the same direction and turns on Q_2 body diode. The inductor energy delivers to the load. Q_2 is turned on to reduce the conduction loss (synchronous rectification). The output voltage applies on the inductor, and the inductor discharging current slope is V_{OUT}/L.

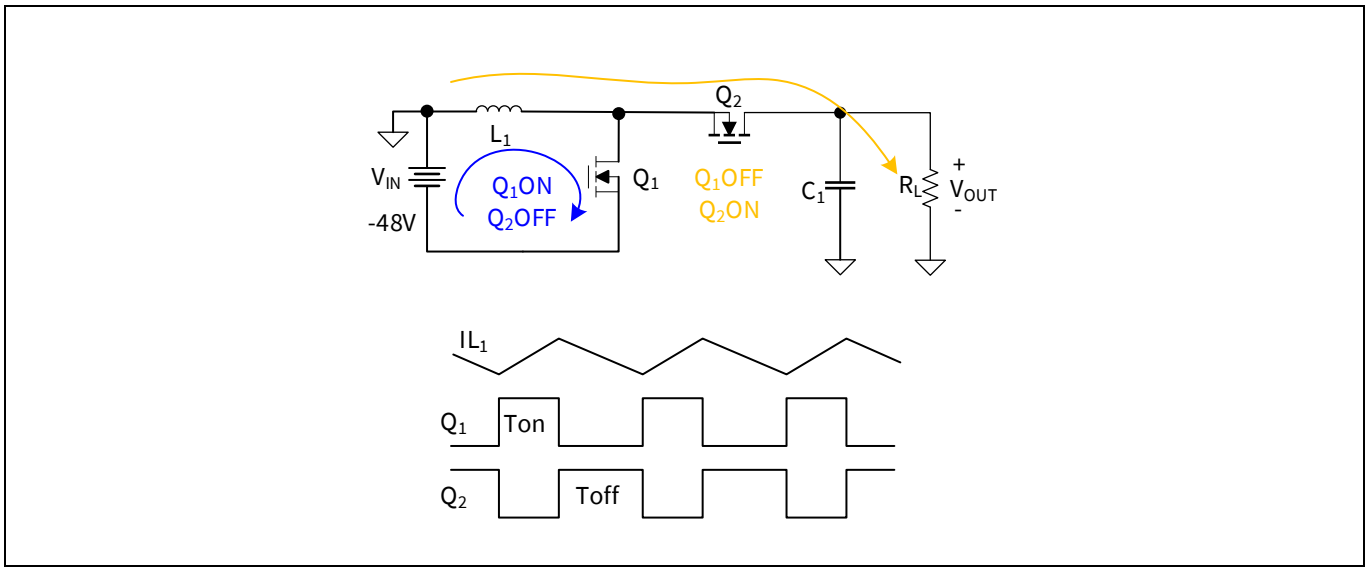


Figure 4 Inverted buck-boost converter

In steady-state, the volt-second of the inductor is balanced and we have the buck-boost equation:

$$V_{IN} \times Ton = V_{OUT} \times Toff$$
$$V_{IN} \times D = V_{OUT} \times (1 - D)$$
$$V_{OUT} = \frac{D}{1 - D} \times V_{IN}$$

D is duty-cycle, $D = T_{on}/(T_{on}+T_{off})$. The output voltage can be made to be lower or higher than the input voltage by adjusting the duty-cycle.

$$V_{OUT} = V_{IN}, @\ D = 0.5$$
$$V_{OUT} < V_{IN}, @\ D < 0.5$$
$$V_{OUT} > V_{IN}, @\ D > 0.5$$

2.2 Interleaved two-phase

The simplified interleaved buck-boost circuit is shown in **Figure 5**. The control FET Q_4 of the second phase is driven with a 180-degree shift to the control FET Q_1 of the first phase. The input current and output current are

plotted to show the relationship to the inductor current in two different conditions: at duty-cycle of less than 0.5 and at duty-cycle above 0.5.

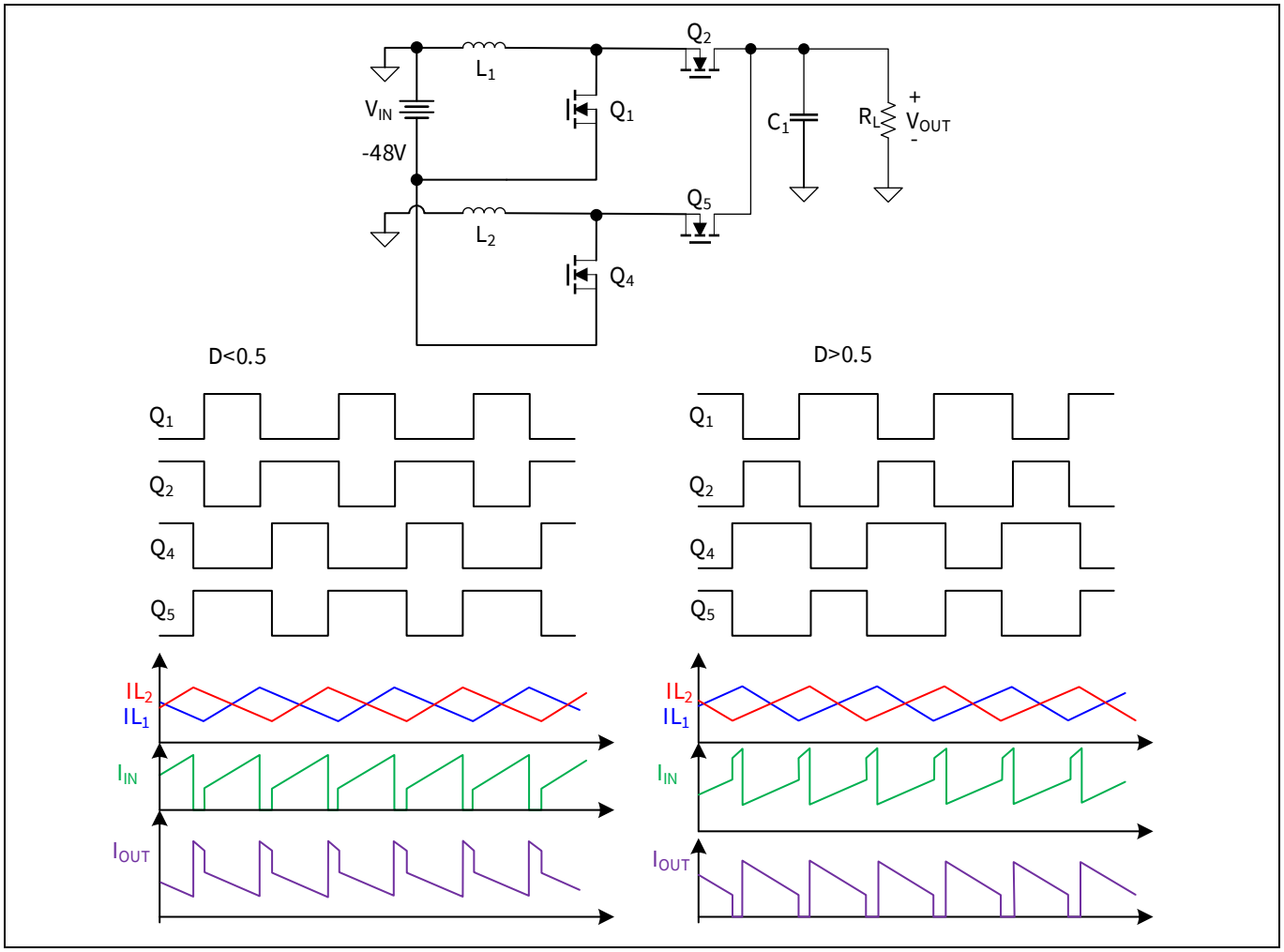


Figure 5 Interleaved buck-boost

2.3 Active ZVS circuit

The Q_2 in **Figure 4** is the synchronous rectifier (SR) MOSFET. In continuous conduction mode (CCM), where the inductor current is always above zero, the current in Q_2 always flows from source to drain. That means Q_2 stays on as long as the current flows through the body diode, no matter the Q_2 gate status. Q_2 only turns off when Q_1 turns on and negative voltage applies to the source of Q_2. This causes reverse recovery current to flow from Q_2 to Q_1, and creates high switching loss in Q_1. The loss associated with reverse recovery in a buck-boost converter can be estimated by the following equation:

$$P_{QRR} = \frac{1}{2} \times I_{rr\_pk} \times (V_{IN} + V_{OUT}) \times \frac{t_{rr_a}}{T_{SW}} + \frac{1}{4} \times I_{rr\_pk} \times (V_{IN} + V_{OUT}) \times \frac{t_{rr\_b}}{T_{SW}}$$

I_{rr_pk} is the peak reverse recovery current, t_{rr} is the reverse recovery time, T_{SW} is the switching period.

The t_{rr} in the MOSFET datasheet is specified at a certain voltage and *diF/dt*. In real applications, the *diF/dt* is determined by the external circuit and could be very different from the datasheet test condition. In this case, the power loss estimation can be done by simulation. **Figure 6** is the I_{DS} current and V_{DS} voltage of the low-side FET, simulated at 48 V input, 28 V output.

I_{rr_pk} is 65 A with 4.3 A/ns *diF/dt*, the duration of the t_{rr_a} is 15 ns, t_{rr_b} is 4 ns, total t_{rr} is 19 ns.

At 200 kHz switching frequency, the Q_{rr} loss is:

$$P_{QRR} = \frac{1}{2} \times 65\ A \times (48\ V + 28\ V) \times \frac{15\ ns}{5\ us} + \frac{1}{4} \times 65\ A \times (48\ V + 28\ V) \times \frac{4\ ns}{5\ us} = 8.4\ W$$

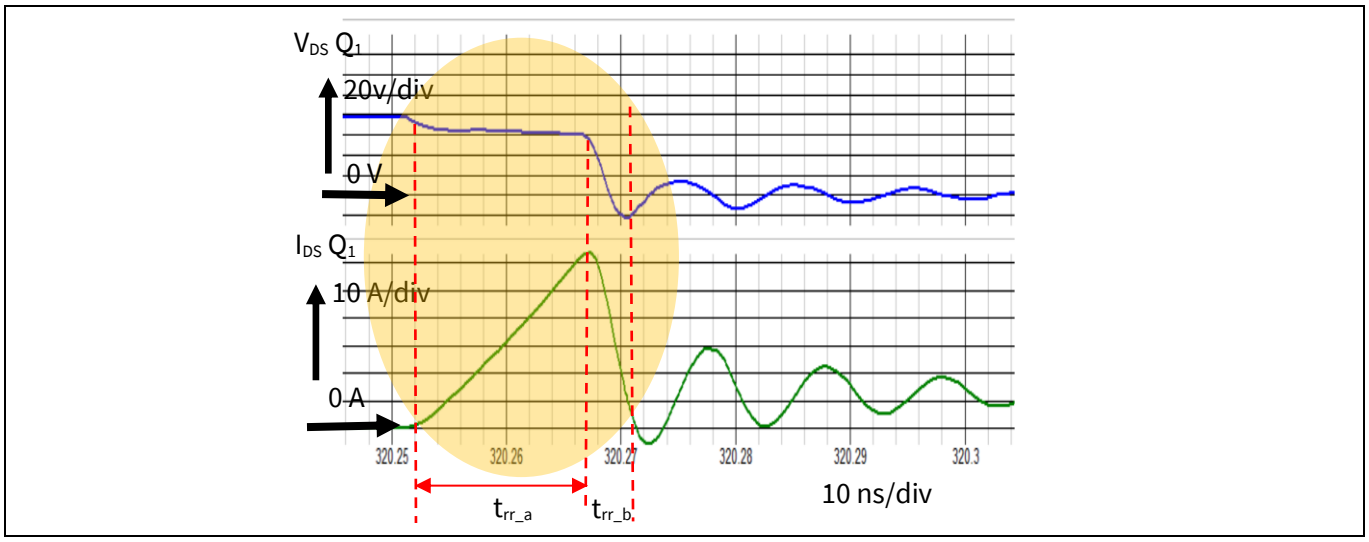


Figure 6 Simulation waveform of the low-side FET

To reduce the reverse recovery switching loss, an active ZVS circuit is introduced in this design. The schematic of the active ZVS is shown in **Figure 7**. The active ZVS circuit recycles the Q_{rr} charge back to output and provides ZVS switching to the control FET, thus increasing converter efficiency.

The following analysis focuses on the turn-off of the SR MOSFET Q_2 and the turn-on of the control MOSFET Q_1 in CCM. The current in Q_2 flows from its source to drain when Q_2 turns off.

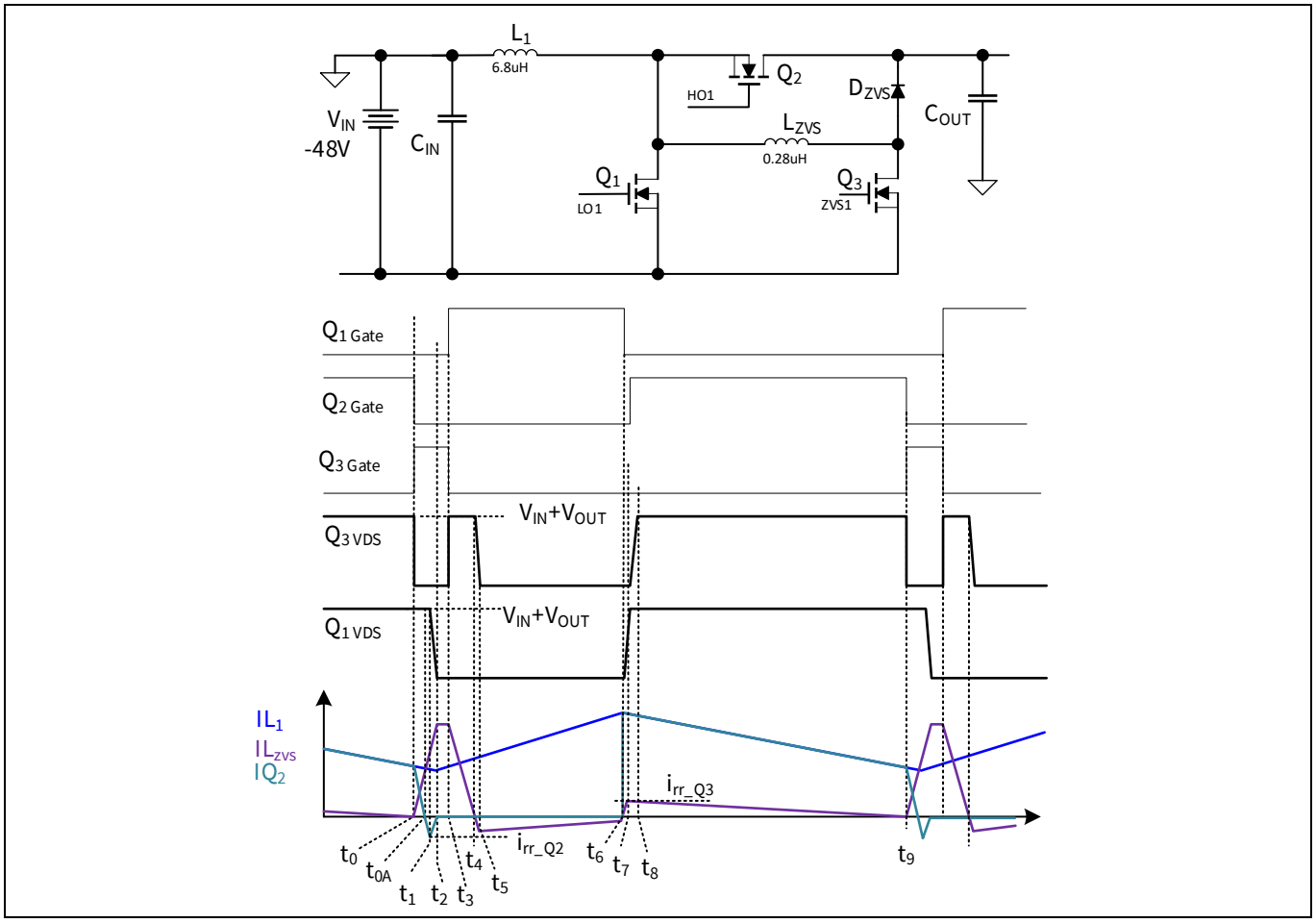


Figure 7 Buck-boost with active ZVS circuit

Mode 1:

At t_0, Q_2 turns off, and the body diode of Q_2 carries inductor L_1 current IL_1. Q_3 turns on, and the current in L_{ZVS} ramps up with a slope di/dt = $(V_{OUT} + V_{IN})/L_{ZVS}$. The current in Q_2 reduces. The total current in Q_2 and Q_3 (or L_{ZVS}) equals the inductor current IL_1. When the current in L_{ZVS} equals the IL_1, the current in the Q_2 body diode is zero. This time is labeled t_{0A}.

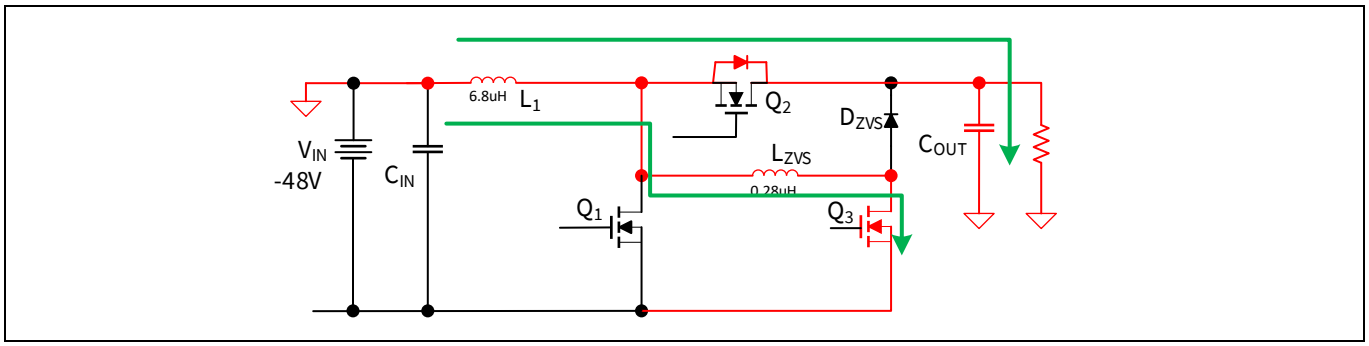


Figure 8 Mode 1

Mode 2:

After t_{0A}, L_{ZVS} current continuously increases and the current in the Q_2 body diode reverses and ramps toward I_{rr_Q2} at t_1. The Q_{rr} in the Q_2 body diode starts to deplete, the V_{DS} voltage of Q_2 begins to increase at t_1, and the V_{DS} voltage of Q_1 starts to decrease.

The current in the Q_2 body diode is completely depleted at t_2. The V_{DS} voltage of Q_2 increases to (V_{OUT} + V_{IN}). The current in L_{ZVS} charges to a peak current. When the Q_2 body diode current decays to zero, the body diode of Q_1 conducts, and brings the V_{DS} voltage of Q_1 to -0.7 V (a body diode voltage drop). The ZVS condition is achieved for Q_1. Q_1 can be turned on shortly after t_2.

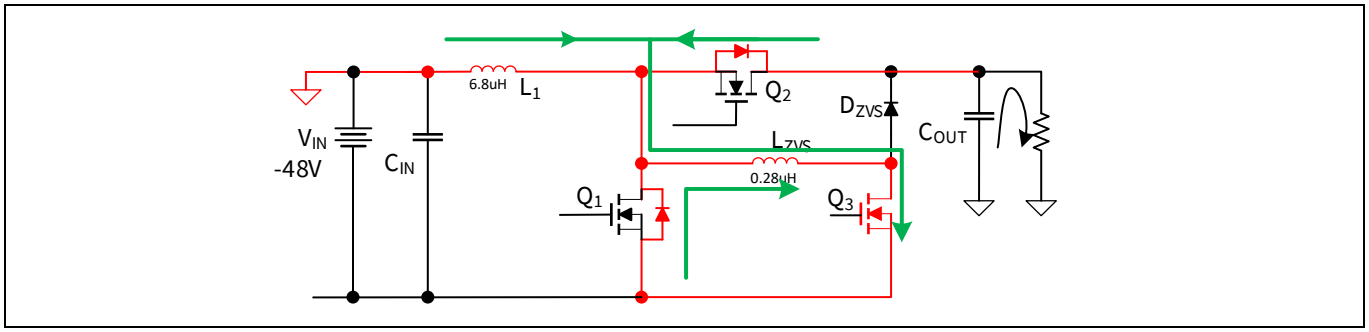


Figure 9 Mode 2

Mode 3:

At t_3, the control FET Q_1 turns on and the Q_3 turns off. The current in L_{ZVS} flows in D_{ZVS} and the charge Q_{rr} of the Q_2 body diode is converted to current in L_{ZVS} and is recycled to V_{OUT} in a non-dissipative manner. The current in L_{ZVS} decays at a slope di/dt = -(V_{OUT} + V_{IN})/L_{ZVS} to zero at t_4. The V_{DS} voltage of Q_{ZVS} is clamped to (V_{OUT} + V_{IN}) during t_3 to t_4.

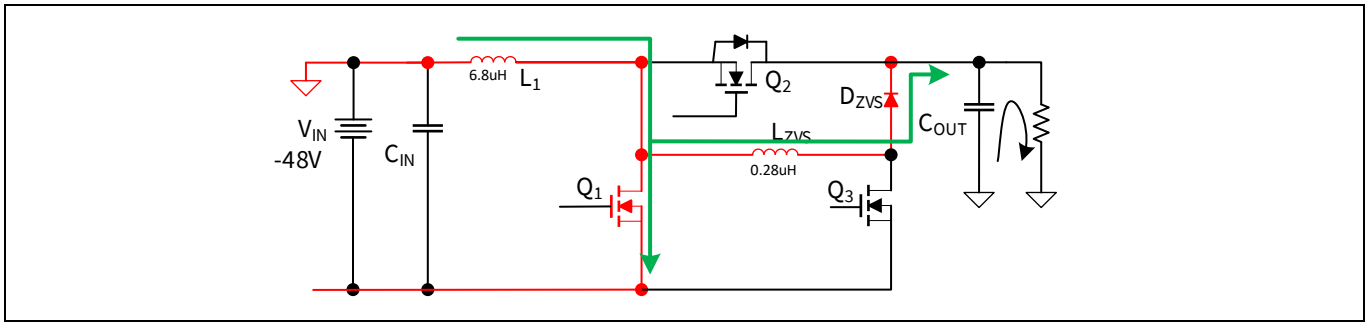


Figure 10 Mode 3

Mode 4:

At t_4 to t_5, the C_{OSS} of Q_3 discharges from (V_{OUT} + V_{IN}) to -0.7 V. The current in L_{ZVS} at t_5 is given by the following equation. At the end of the C_{OSS} discharge, the V_{DS} voltage of Q_3 is clamped to -0.7 V at t_5.

$$IL_{ZVS\_t5} = \sqrt{\frac{C_{OSS}}{L_{ZVS}}} \times (V_{OUT} + V_{IN})$$

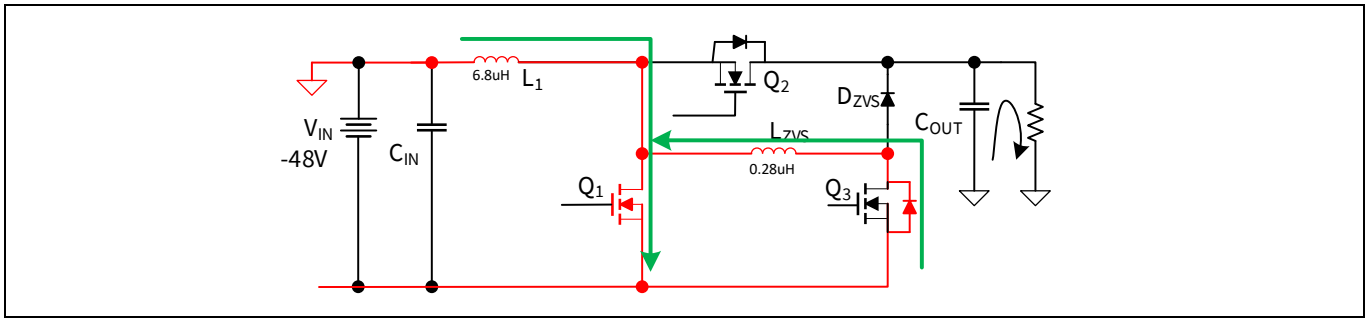


Figure 11 Modes 4 and 5

Mode 5:

From t_5 to t_6, the control FET Q_1 stays on, and the SR FET Q_2 and Q_{ZVS} stays off. The body diode of Q_3 conducts L_{ZVS} current. The L_{ZVS} current decays toward zero at a slope di/dt = 0.7 V/L_{ZVS}.

Mode 6:

At t_6, the Q_1 turns off. The current in inductor L_1 continuously flows through the body diode of Q_2 and clamps the source voltage of Q_2 at V_{OUT}. The L_{ZVS} current rises up at slope di/dt = (V_{OUT} + V_{IN})/L_{ZVS} from the initial current of -ILzvs(t_6). The current in the Q_3 body diode reaches I_{rr_Q3} at t_7. Q_2 turns on with ZVS.

At t_8, the body diode of Q_3 recovers and the reverse recovery current continues to flow in L_{ZVS} through D_{ZVS}. The current in L_{ZVS} decays at a rate of -0.7 V/L_{ZVS}.

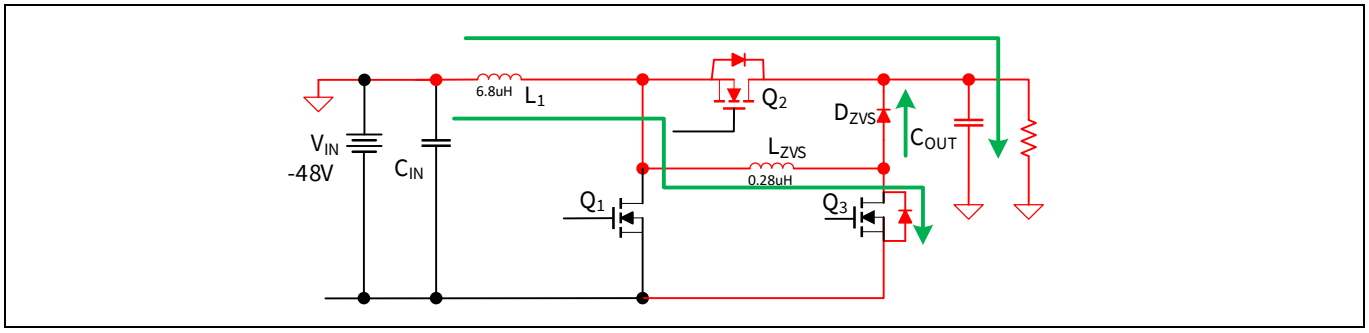


Figure 12 Mode 6

Mode 7:

At t_9, the current in L_{ZVS} decays to 0 A, and the diode D_{ZVS} turns off. The Q_2 alone conducts current and the converter is ready for the next mode 1.

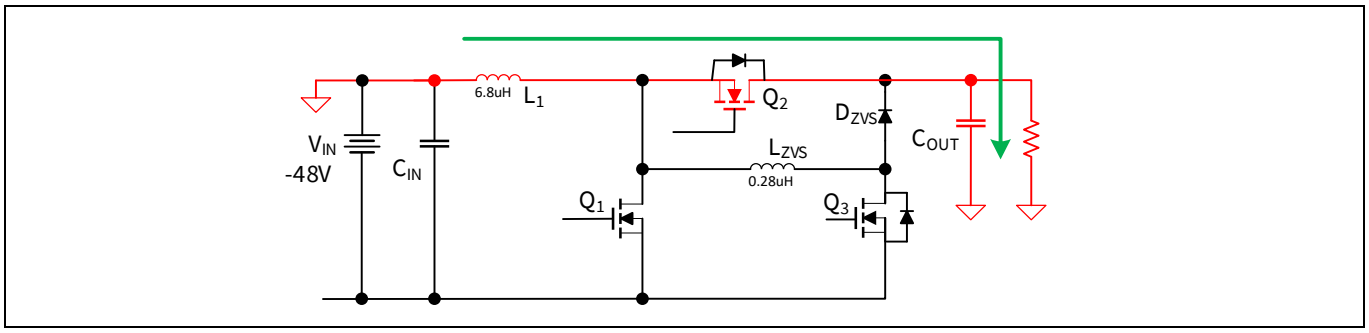


Figure 13 Mode 7

The current of each of the power devices is shown in **Figure 14**.

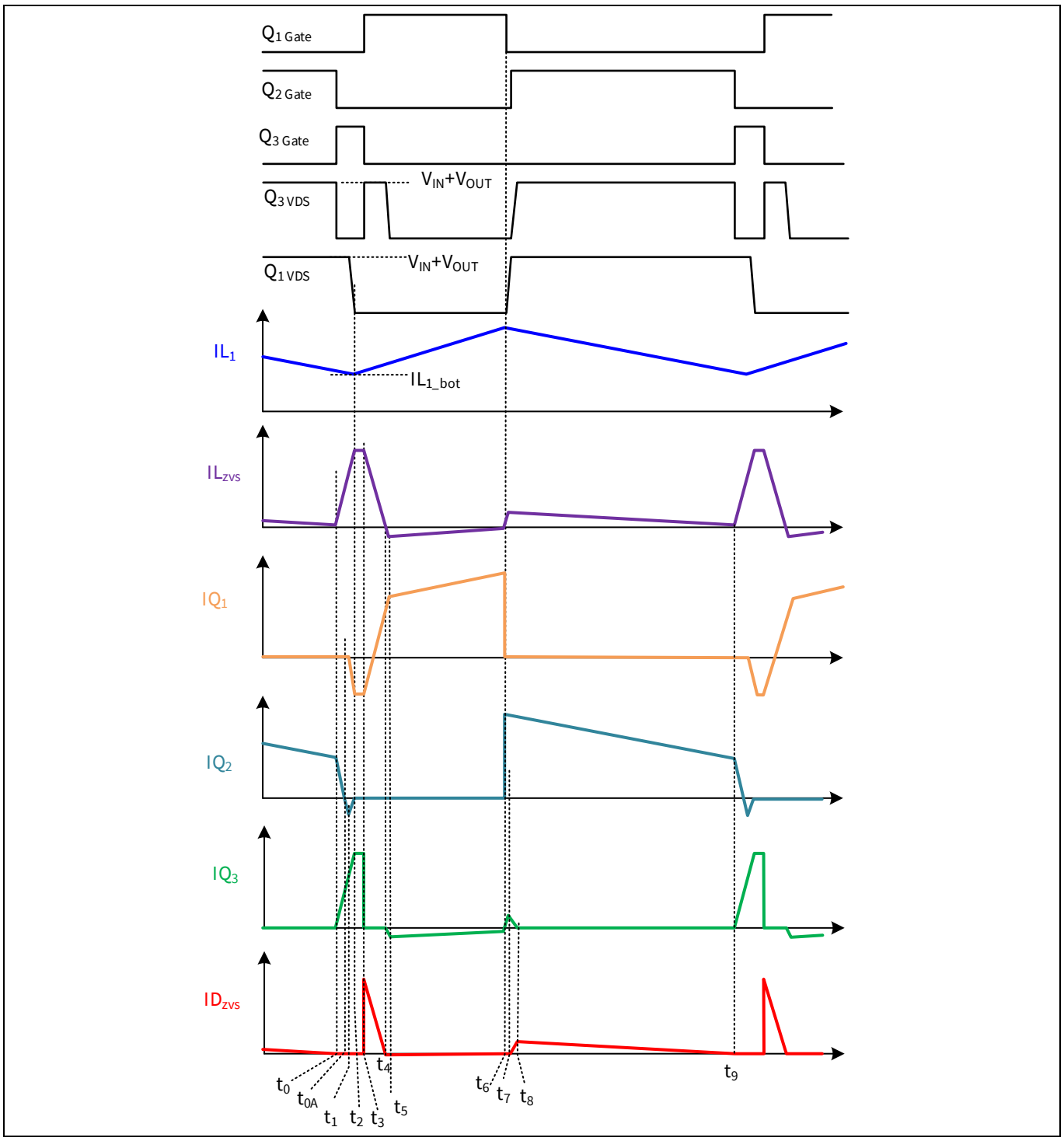


Figure 14 Current in power devices

ZVS circuit design guidelines:

- The on-time of Q_3 (Q_{ZVS}) should be set longer than the current in L_{ZVS}, increasing from 0 A to the valley of the buck-boost inductor current, which can be calculated by (L_{ZVS} * IL_{1_bot})/(V_{IN} + V_{OUT}), plus the reverse recovery time of the SR FET Q_2. The worst case happens at the low-line and full-load condition.

- The on-time of Q_3 is configured by using the XDPP1100 PWM rise/fall select registers and the dead time of the PWM. Details of the configuration are described in **chapter 7.1**. The maximum on-time of the Q_3 is limited by the maximum dead time range, 318 ns.
- If the calculated on-time of Q_3 is higher than 300 ns, it is suggested to lower the ZVS inductor value to reduce the time with higher di/dt.

The power loss of the active ZVS circuit is calculated with the following design example.

V_{IN} = -48 V, V_{OUT} = 28 V, F_{sw} = 200 kHz, T_{sw} = 5 µs, L_{ZVS} = 0.28 µH, phase current 14 A.

Q_3 (Q_{ZVS}) parameters: R_{DSon_QZVS} = 0.03 Ω, C_{oss} = 230 pF at 75 V V_{DS}, V_{DS} = 0.88 V, I_{rr_Qzvs} = 4 A

Q_3 on-time: T_{Q3_ON} = 200 ns

Q_2 parameters: t_{rr} = 45 ns (typical value at V_R = 75 V, di/dt = 100 A/ µs per **BSC110N15NS5** datasheet)

D_{ZVS} parameters: V_F = 0.8 V

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} = 0.368$$

$$IL_{1\_AV} = \frac{I_{PHASE}}{(1 - D)} = 22.2\ A$$

$$IL_{1\_bot} = IL_{1\_AV} - \frac{1}{2} \times \frac{V_{IN} \times D \times T_{SW}}{L_1} = 15.7\ A$$

$$t_{t0A-t0} = \frac{L_{ZVS} \times IL_{1\_bot}}{V_{OUT} + V_{IN}} = 58\ ns$$

$$IL_{ZVS\_t2} = \frac{(V_{OUT} + V_{IN}) \times (t_{rr} + t_{t0A-t0})}{L_{ZVS}} = 27.9\ A$$

$$I_{RMS_{QZVS}} = \sqrt{\frac{1}{3} \times \frac{(t_{rr} + t_{t0A-t0})}{T_{SW}}} \times IL_{ZVS\_t2} + \sqrt{\frac{(T_{Q3_{ON}} - t_{rr} - t_{t0A-t0})}{T_{SW}}} \times IL_{ZVS\_t2} = 6.2\ A$$

$$IL_{ZVS\_t5} = \sqrt{\frac{C_{OSS}}{L_{ZVS}}} \times (V_{OUT} + V_{IN}) = 2.2\ A$$

$$t_{t6-t5} = \frac{L_{ZVS} \times IL_{ZVS\_t5}}{V_{SD}} = 0.7\ us$$

$$t_{t4-t3} = \frac{L_{ZVS} \times IL_{ZVS\_t2}}{V_{OUT} + V_{IN}} = 0.103\ us$$

$$t_{t9-t8} = \frac{L_{ZVS} \times I_{rr\_QZVS}}{V_F} = 1.4\ us$$

$$PQ_{ZVS_{cond}} = I^2_{RMS\_QZVS} \times R_{DSON\_QZVS} = 1.15\ W$$

$$PQ_{ZVS_{bodydiode}} = \frac{1}{2} IL_{ZVS\_t5} \times V_{SD} \times \frac{t_{t6-t5}}{Tsw} = 0.13\ W$$

$$PQzvs_{total} = PQ_{ZVS_{cond}} + PQ_{ZVS_{bodydiode}} = 1.28\ W$$

$$PDzvs = 0.5 \times IL_{ZVS\_t2} \times V_F \times \frac{t_{t4-t3}}{Tsw} + 0.5 \times I_{rr\_Qzvs} \times V_F \times \frac{t_{t9-t8}}{Tsw} = 0.68\ W$$

The total power loss of the active ZVS circuit is around 2 W.

2.4 ZVS enable/disable

At light load the current in the buck-boost inductor is in “discontinuous mode”, or in other words, the current in the SR FETs goes negative and flows from drain to source at the end of the SR conduction time. Active ZVS is not desirable in this condition. Disabling the active ZVS at light load gives higher efficiency. See **Table 2** for a comparison of the efficiency at different input voltages and output loads.

Table 2 Efficiency with active ZVS and without active ZVS

I_{OUT} (A)	42 V DC with ZVS	42 V DC without ZVS	48 V DC with ZVS	48 V DC without ZVS	57 V DC with ZVS	57 V DC without ZVS
2.5	91.10%	92.16%	87.49%	91.31%	89.10%	90.12%
5	95.15%	95.92%	94.58%	95.72%	93.86%	95.10%
10	96.96%	95.80%	96.70%	95.31%	96.25%	94.63%

A FW patch disables ZVS (PWM3 and PWM4 are turned off) if the output current is lower than the set threshold. The configuration instruction is described in **chapter 3.4**.

2.5 DCR current sense

DCR current sense (CS) is often used in high-current applications. It uses the DCR of the inductor as an inherent shunt resistor, eliminating the cost and additional power loss of the shunt resistor. This design puts the IC reference ground to the return of the -48 V input, making it convenient to sense output voltage with positive polarity. It is also easy to implement the DCR CS circuit, as one end of the inductor is grounded. The DCR sensing circuit is shown in **Figure 15**.

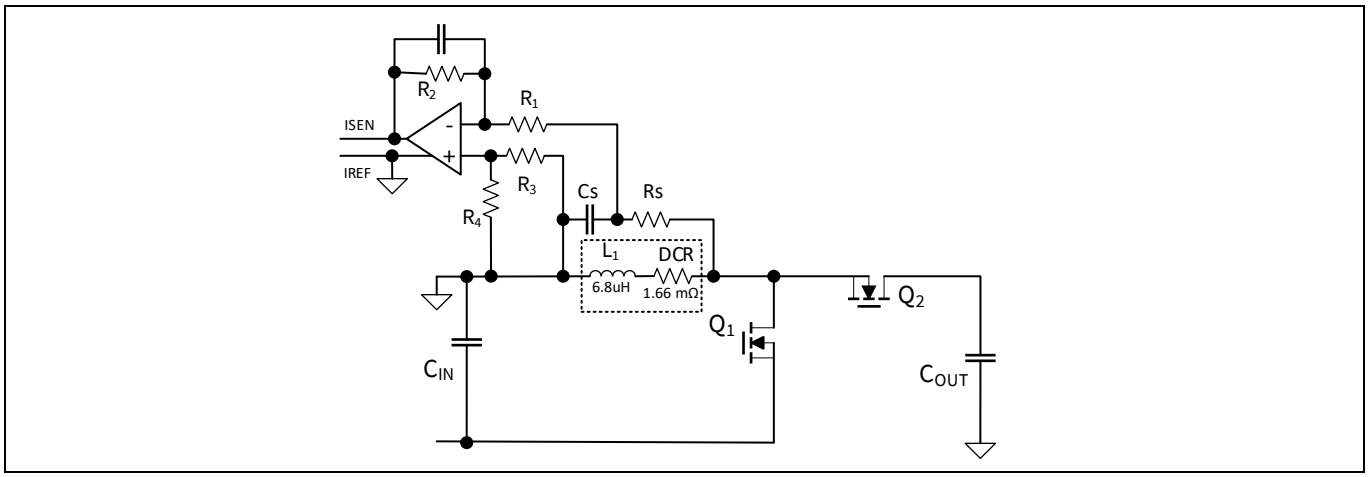


Figure 15 DCR current sense circuit

The ripple voltage across the reactive impedance of the inductor can be canceled using a low-pass filter if the time constant of the RC filter equals L/R_{DCR}.

$$Rs \times Cs = \frac{L_1}{R_{DCR}}$$

With the matching time constant, the voltage across the capacitor C_S equals the voltage drop on the DCR. Thus by sensing the voltage of capacitor C_S, the circuit knows the inductor current value.

$$VC_S = I_{L1} \times R_{DCR}$$

An op-amp is used to increase the signal from tens of millivolts to hundreds of millivolts and feed to the CS ADC input of the XDPP1100. With the amplifier, the R_S should be selected based on the trade-off between the power loss on the resistor and the offset error introduced by the input bias current of the amplifier. A smaller R_S would have less offset error, but higher power loss. The inductor of this design is 6.8 µH with 1.66 mΩ DCR. So, choose C_S = 0.1 µF, R_S = 40.2 kΩ for the CS RC filter. Because the voltage across the RC filter is mainly dropped on the R_S resistor, the power loss of R_S (P_{RS}) can be estimated based on the following equations. The maximum power loss happens at 60 V input and 56 V output:

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}}$$

$$P_{RS\_max} = \frac{V_{IN\_max}^2}{Rs} \times D + \frac{V_{OUT\_max}^2}{Rs} \times (1 - D) = 84\ mW$$

The gain of the op-amp is designed to use the full scale of the ADC input (395 mV) at the maximum inductor current, which happens at the minimum input 36 V and the nominal output voltage 28 V. Each phase takes half of the load, and the inductor current is calculated as follows:

$$D = \frac{V_{OUT\_nom}}{V_{IN\_min} + V_{OUT\_nom}} = \frac{28}{36 + 28} = 0.4375$$

$$I_{L1} = \frac{0.5\ I_{OUT\_max}}{(1 - D)} = \frac{14\ A}{(1 - 0.4375)} = 24.9\ A$$

$$\Delta I_{L1} = \frac{V_{IN} \times D}{L_1 \times Fsw} = \frac{36\ V \times 0.4375}{6.8\ uH \times 200\ kHz} = 11.6\ A$$

$$I_{L1\_pk} = I_{L1} + \frac{\Delta I_{L1}}{2} = 30.7\ A$$

The inductor temperature could reach 90°C at full load without airflow. The temperature drift of the DCR can be estimated using the temperature coefficient of copper, which is 0.393 percent/°C. Considering 25 percent temperature drift of the DCR and 10 percent margin for the overcurrent limit, the gain of the op-amp can be computed by the equation below:

$$Gain_{opamp} = \frac{395\ mV}{I_{L1\_pk} \times 1.1 \times R_{DCR} \times 1.25} = 5.6$$

In **Figure 15**, R1 = R3 = 100 kΩ, R2 = R4 = 560 kΩ for gain 5.6.

The XDPP1100 PMBus command MFR_IOUT_APC configures the CS gain in amperes per code (APC). The CS ADC LSB is 1.45 mV, thus the IOUT_APC is calculated by the following equation. Because the DCR of the inductor is a parasitic parameter, it usually has large tolerance. To have accurate CS, the MFR_IOUT_APC should be tuned on each board. Take the calculated value as a reference and trim the number in the system test. The phase 1 CS should be configured by PMBus loop 0 MFR_IOUT_APC, and the phase 2 current should be configured by PMBus loop 1 MFR_IOUT_APC.

$$IOUT\_APC = \frac{1.45\ mV}{R_{DCR} \times Gain_{opamp}} = \frac{1.45\ mV}{1.66\ mohm\ \times 5.6} = 0.16\ A$$

To exclude the temperature drift error for accurate current telemetry, temperature compensation should be enabled by setting the PMBus command FW_CONFIG_REGULATION bit [9], EN_IOUT_APC_TEMP_COMP.

2.6 Output current telemetry correction

Because the HW senses inductor current, a FW patch is implemented to compute the output current based on the inductor current and duty-cycle. The patch has the following equation:

$$Output\ Current = (1 - Duty\ Cycle\ \pm Deadtime) \times Inductor\ Current$$

The sign of the dead time depends on whether the dead time is applied to the rising edge of PWM or the falling edge of PWM. If the dead time is at the rising edge of PWM, the sign is negative. If the dead time is applied at the falling edge of PWM, the sign in the equation is positive. The FW gets the dead time parameter from PMBus command PWM_DEADTIME.

Please note that the above correction only changes I_{OUT} telemetry. The overcurrent fault limits IOUT_OC_FAULT_LIMIT and MFR_IOUT_OC_FAST_FAULT_LIMIT are still applied to inductor current, thus the I_{OUT} OC fault thresholds should be set accordingly, i.e., higher than the actual I_{OUT} OC fault limit with a factor of 1/(1-D).

2.7 Input voltage sense

The input voltage is negative with reference to the XDPP1100 ground, and it can't be directly sensed using a resistor divider. To avoid adding a voltage sense (VS) amplifier to the circuit, the design uses the secondary winding of the auxiliary power supply to sense input voltage. The schematic is shown in **Figure 16**. The auxiliary transformer T1 has a 1:1 turns ratio.

During primary on-time, the high-side switch of U8 is on and the SW pin and pin 2 of T1 are connected to V48RTN. This creates a voltage drop on the T1 primary winding, equal to V_{IN} – (12 V_P). The secondary winding of T1 has the same voltage, as the turns ratio is 1:1. D1 conducts, and the voltage on C90 equals V_{IN} – (12 V_P) + (12 V_S).

When the primary high-side turns off and the low-side turns on, the SW pin of U8 is connected to -VN (i.e., -V_{IN}). The T1 primary winding voltage equals 12 V_P with the dot name (pin 1) that has high potential. At the secondary side, D1 turns off, D6 turns on and the C92 voltage equals 12 V_P; i.e., the 12 V_S equals 12 V_P. If we ignore the forward voltage drop of D1 and D6, the voltage on capacitor C90 equals the input voltage V_{IN}.

A resistor divider R74, R75 is used to scale down the input voltage and send it to the PRISEN pin. The PRISEN ADC input voltage range is 0 V to 1.2 V, thus the resistor divider is selected to have a scale of R75/(R74 + R75) = 0.0156. This makes the PRISEN voltage 0.56 V to 0.94 V when V_{IN} is -36 V to -60 V.

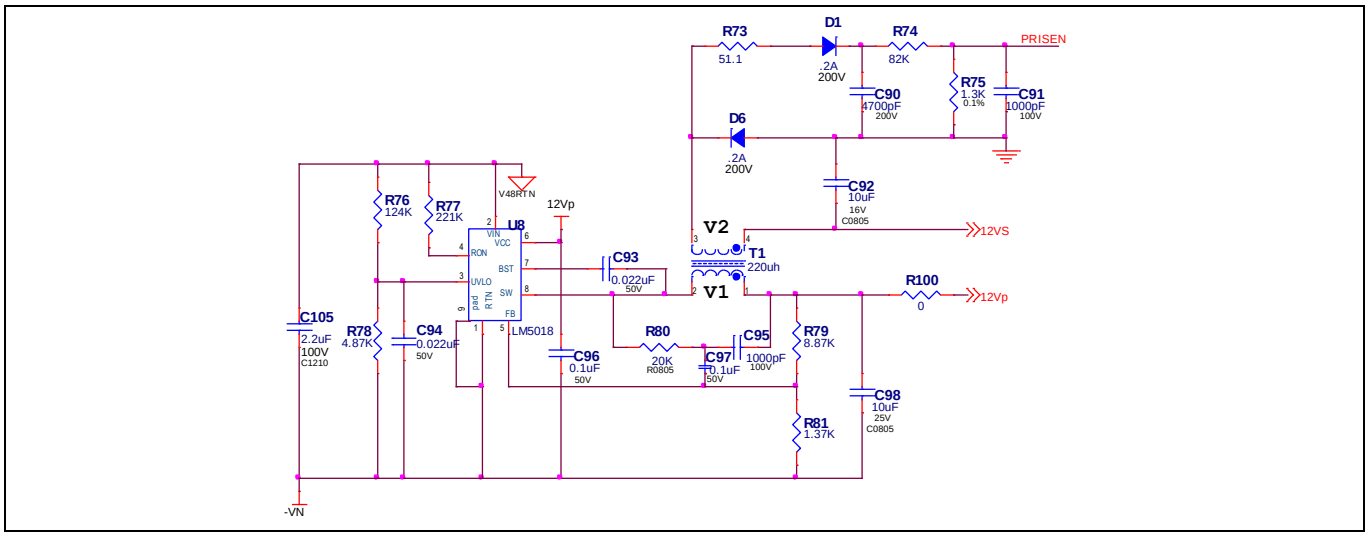


Figure 16 Auxiliary power supply and input voltage sense

The input voltage sense gain is configured by the **vin_pwl_slope** register. The **vin_pwl_slope** can be calculated by the following equation:

$$vin\_pwl\_slope = \frac{1.2\times2^5}{PRISEN\_SCALE} = \frac{1.2\times2^5}{0.0156} = 2462$$

The V_{IN} telemetry offset can be configured by **vin_trim** register.

Setting register **tlm0_vin_src_sel** = 3 would select the PRISEN as the input voltage telemetry source.

2.8 Loop feedback and PID compensation

The XDPP1100 GUI provides design support to estimate the gain and phase of the loop. **Figure 17** shows the PID bode plot tool. Please note, for inverted buck-boost, the V_{OUT} and I_{OUT} must have a negative sign for the correct result. The PID was configured to have stable operation during load transient.

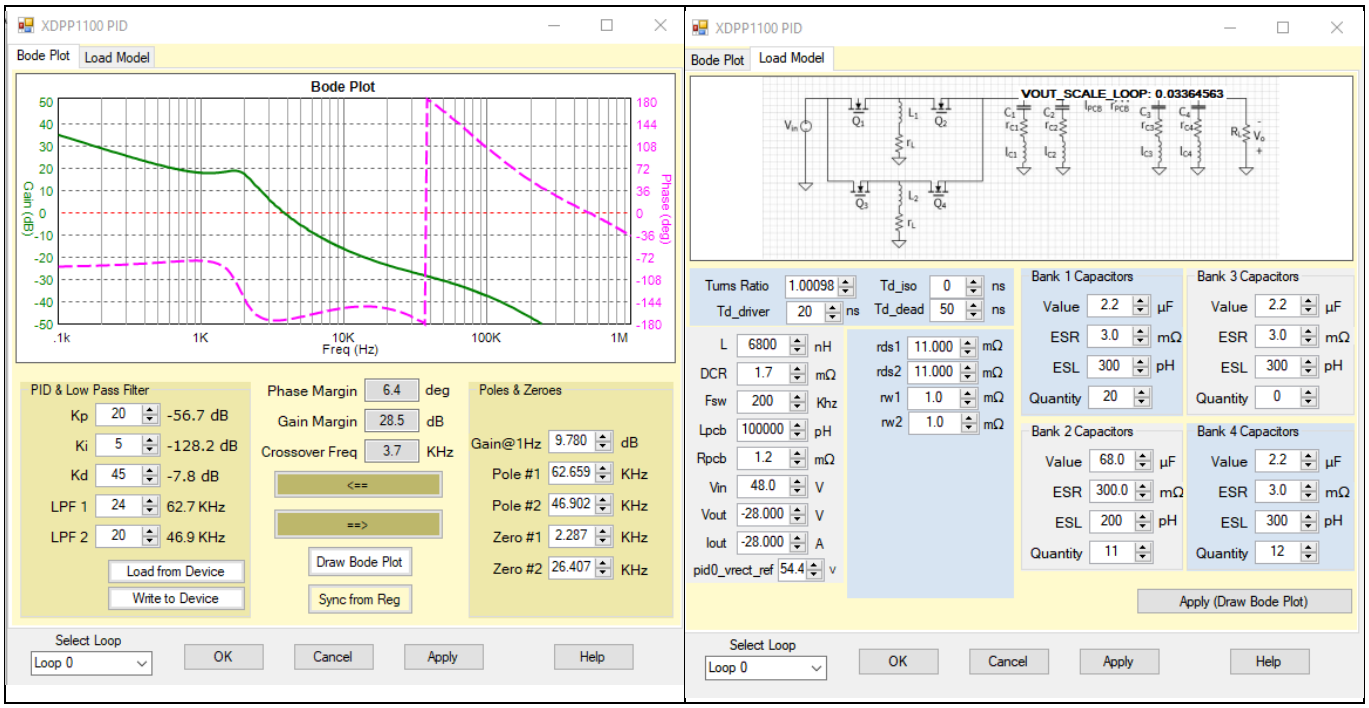


Figure 17 PID configuration

An external RC (R20, C71) is added for additional pole and zero. This circuit is used to reduce gain and increase phase margin.

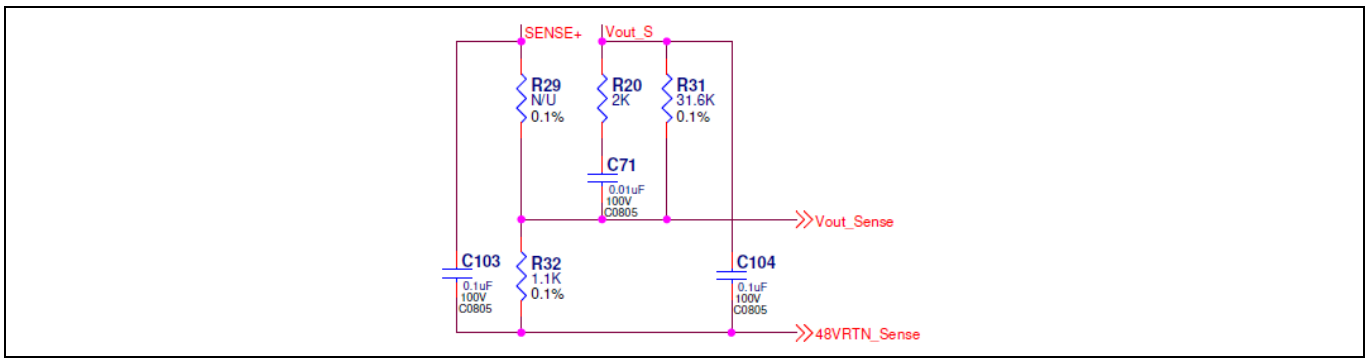


Figure 18 External RC pole/zero

$$f_{zero} = \frac{1}{2\pi \times (R20 + R31) \times C71} = 473\ Hz$$

$$f_{pole} = \frac{1}{2\pi \times R20 \times C71} = 7.95\ kHz$$

2.9 Feed-forward compensation

The XDPP1100 doesn't have a HW feed-forward circuit for the buck-boost topology. Thus a FW patch implements a feed-forward feature to support inverting buck-boost topology. The feed-forward duty-cycle is computed per the following equation:

$$D\_VFF = \frac{V_{OUT}}{V_{IN} + V_{OUT}}$$

The calculated D_VFF is then assigned to the feed-forward override register **pid0_ff_override** for feed-forward compensation. The FW override should be enabled by setting register **pid0_ff_override_sel** = 1. During input voltage transient, the variation of V_{IN} is detected, and the FW directly changes duty-cycle before the feedback loop response to the input transient.

This feed-forward feature is executed every eighth switching cycle. Setting a higher IRQ rate could result in a faster feed-forward response. But at a higher IRQ rate, the FW might overload the CPU and reset. It is not recommended to set the interrupt higher than every four switching cycles.

$$Feed\ Forward\ Frequency = Switching\ Frequency/8$$

To enable the buck-boost feed-forward feature, set the patched command "MFR_EN_BUCK_BOOST_FEED_FORWARD" to 1.

2.10 Interleave current balancing

In this demo board design, phase 1 current is sensed by the ISEN/IREF pair of ADC inputs and phase 2 current is sensed by the BISEN/BIREF ADC pair. Both ISEN and BISEN signals are converted from analog to digital and processed by the ISP digital processor of the XDPP1100. Both phase currents are cycle-averaged and sent to the current balancing block.

Figure 19 is the block diagram of the current balancing circuit (ibal) of the XDPP1100. It subtracts phase 1 current from phase 2 to obtain the current difference between phase 1 and phase 2. The result is filtered and clamped then sent to phase 1 to adjust duty-cycle in every switching frequency cycle. If phase 1 current is lower than phase 2 current, the ibal_duty_adj_o is positive, and it increases the duty-cycle of phase 1 until phase 1 current is equal to phase 2. Vice-versa, if phase 1 current is higher than phase 2, phase 1 duty-cycle is reduced to reduce the phase current until it equals phase 2 current.

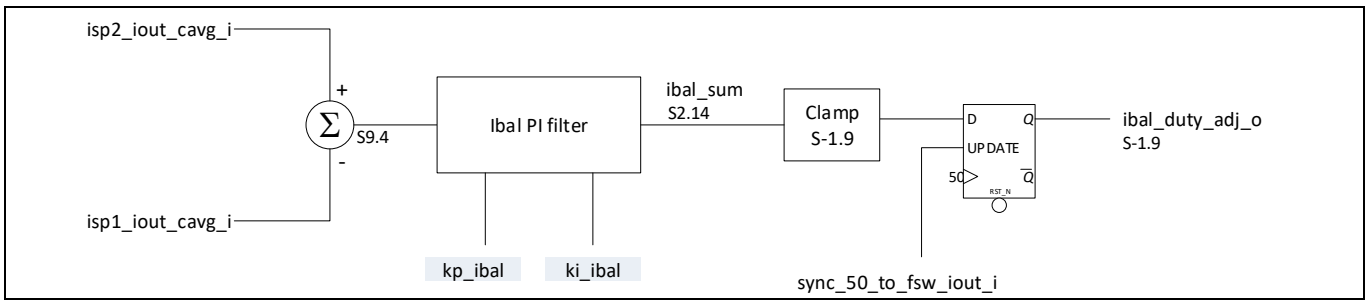


Figure 19 Current balancing block diagram

The ibal PI filter is configured by registers **kp_ibal** and **ki_ibal**.

Table 3 Current balancing PI filter registers

Register	Description	Equation
kp_ibal	Current balancing PI filter proportional coefficient index	kp_exp = kp_ibal [5:3] kp_man = 8 + kp_ibal [2:0] kp = kp_man * 2^(kp_exp – 14)
ki_ibal	Current balancing PI filter integral coefficient index	ki_exp = ki_ibal [5:3] ki_man = 8 + ki_ibal [2:0] ki = ki_man * 2^(ki_exp – 20)

The magnitude response of the PI filter is defined by:

$$\sqrt{kp^2 + \left(\frac{ki}{2\pi \cdot Tsw \cdot f}\right)^2} \quad (8.1)$$

Here, T_{SW} is the converter switching period.

The current balancing circuit is enabled by the FW when converter topology is interleaved topology and the bit [8] of PMBus command FW_CONFIG_REGULATION, INTERLEAVE_ENABLE is set to 1.

A dead band can be set to disable current balancing when the total output current of the two phases is less than the threshold **ibal_en_thresh**. This threshold helps to avoid bad balancing when the CS accuracy is low at light load, which is usually caused by offset error or due to the board's lack of capability to sense negative current.

Table 4 Ibal_en_thresh configuration table

Value	Current balancing enable threshold
0, 1	Always enabled for interleaved topology
2	3 A
3	5 A

In this design, the **kp_ibal** = 20, **ki_ibal** = 16. With 200 kHz switching frequency, the ibal PI filter magnitude is plotted as shown in **Figure 20**. The **ibal_en_thresh** = 2 for 3 A current balancing threshold.

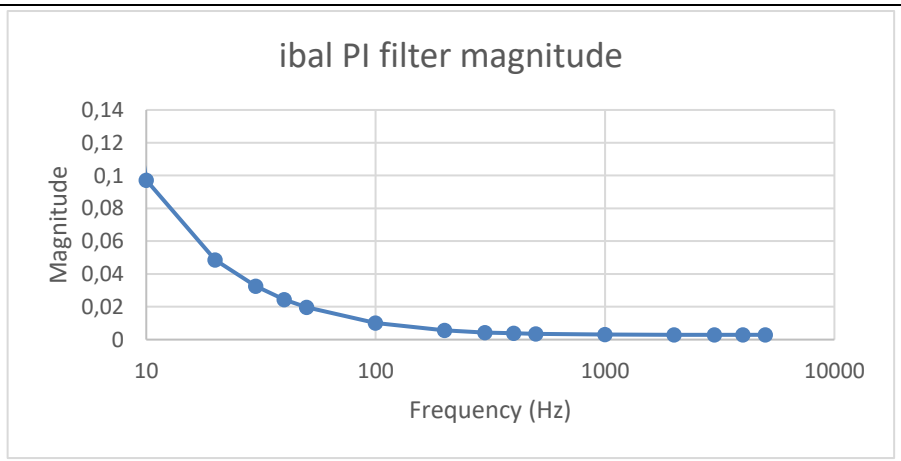


Figure 20 The ibal PI filter

3 FW patch features

The following functions are implemented in the FW patch.

- I_{OUT} telemetry correction
- Efficiency table feature
- Feed-forward of buck-boost
- ZVS enable/disable

3.1 I_{OUT} telemetry correction

This feature allows the user to get the output current telemetry from the combination ISEN + BISEN inductor current, and adjusts it based on dead time and duty-cycle values, according to the following equation. For further explanation see **chapter 2.6**.

$$Output\ Current = (1 - Duty\ Cycle\ \pm Deadtime) * Inductor\ Current$$

3.2 Efficiency table feature

This feature improves measurement accuracy of the input current and input power telemetry based on pre-programmed power efficiencies for different ranges.

To reflect more accurate readings on the input current telemetry, the following equation is used:

$$Input\ Current\ Corrected = \ Input\ Current\ /\ Efficiency\ LUT\ value$$

where *Efficiency LUT value* is selected from the efficiency look-up table (LUT) based on the output current and the input voltage of operation. In the default buck-boost project, the following efficiency LUT is programmed:

Table 5 Efficiency look-up table

Output current / Input voltage	5 A	10 A	15 A	25 A
36 V DC	95.62%	97.32%	97.74%	97.60%
48 V DC	94.57%	96.75%	97.39%	97.52%
60 V DC	93.98%	96.38%	97.16%	97.39%

The input current and input power correction happen with every telemetry interrupt iteration.

The LUT hysteresis is 1 V for the input voltage and 0.75 A for the output current, respectively.

Example

If the output current is 10 A and the input voltage is 42 V, the efficiency LUT value is 97.32 percent.

3.3 Feed-forward of buck-boost

This is a FW-based feed-forward feature to support inverting buck-boost topology. The feed-forward duty-cycle is computed per the following equation:

$$D\_VFF = \frac{V_{OUT}}{V_{IN} + V_{OUT}}$$

This feed-forward feature is executed every eighth regulation frequency switch, or:

$$Feed\ Forward\ Frequency = Regulation\ Frequency/8$$

To enable the buck-boost feed-forward feature, set the patched command "MFR_EN_BUCK_BOOST_FEED_FORWARD" to 1.

3.4 ZVS enable/disable

The ZVS patch feature disables ZVS once the output load is below the ZVS disable threshold. The user can configure the ZVS threshold with the (0xB2) MFR_ZVS_DISABLE_THRESHOLD PMBus command. Its format is the same as (0x8C) READ_IOUT with its READ_IOUT_EXP exponent value. The default value is 0.

Note that once READ_IOUT_EXP is updated, the user should rewrite MFR_ZVS_DISABLE_THRESHOLD with a new value according to a new READ_IOUT_EXP.

A hysteresis of 1 A is implemented to avoid ZVS jittering.

Example

If READ_IOUT_EXP is "-3" and the user wants to have 6 A ZVS threshold level, set MFR_ZVS_DISABLE_THRESHOLD to "0xE830".

4 Test setup

The input/output and I²C dongle connection is shown in **Figure 21**. When testing the board without a heatsink, a fan is required.

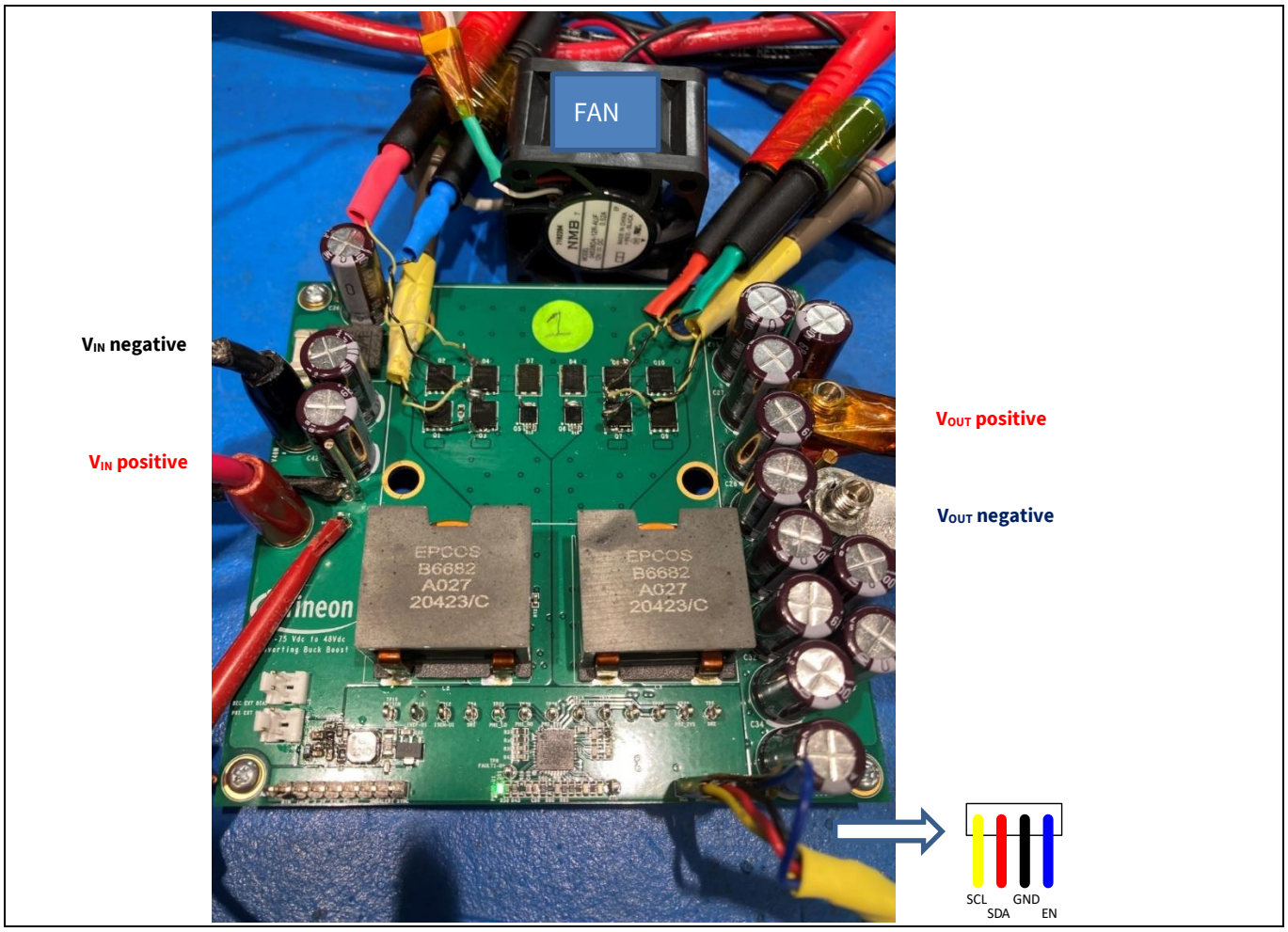


Figure 21 Test setup

5 Experimental results

The unit was tested at 36 V DC, 48 V DC and 56 V DC input voltages at the nominal 28 V DC output.

5.1 Efficiency

Table 6 36 V V_{IN}

V_{IN}	P_{IN}	V_{OUT}	I_{OUT}	P_{OUT}	Efficiency
36.00	5.76	28.082	0.000	0.00	
36.00	146.52	28.076	4.990	140.10	95.92
36.01	287.68	28.075	9.972	279.96	97.32
36.01	429.71	28.079	14.957	419.98	97.74
36.00	572.72	28.072	19.944	559.87	97.76
36.01	716.24	28.067	24.907	699.07	97.60
36.00	803.05	28.056	27.892	782.54	97.45

Table 7 48 V V_{IN}

V_{IN}	P_{IN}	V_{OUT}	I_{OUT}	P_{OUT}	Efficiency
48.00	7.39	28.078	0.001	0.03	
48.01	147.68	28.073	4.975	139.66	95.72
48.01	289.64	28.071	9.983	279.55	96.75
48.01	431.18	28.073	14.96	456.19	97.39
48.00	573.98	28.068	19.945	559.82	97.53
48.00	716.06	28.064	24.883	698.32	97.52
48.00	802.80	28.063	27.878	782.34	97.45

Table 8 56 V V_{IN}

V_{IN}	P_{IN}	V_{OUT}	I_{OUT}	P_{OUT}	Efficiency
56.00	8.34	28.08	0.002	0.06	
56.00	148.51	28.082	4.970	139.57	95.10
56.00	289.74	28.078	9.946	279.26	96.38
56.00	432.04	28.075	14.951	419.75	97.16
56.01	574.83	28.07	19.941	559.74	97.38
56.01	717.43	28.06	24.901	698.72	97.39
56.00	803.60	28.055	27.891	782.48	97.37

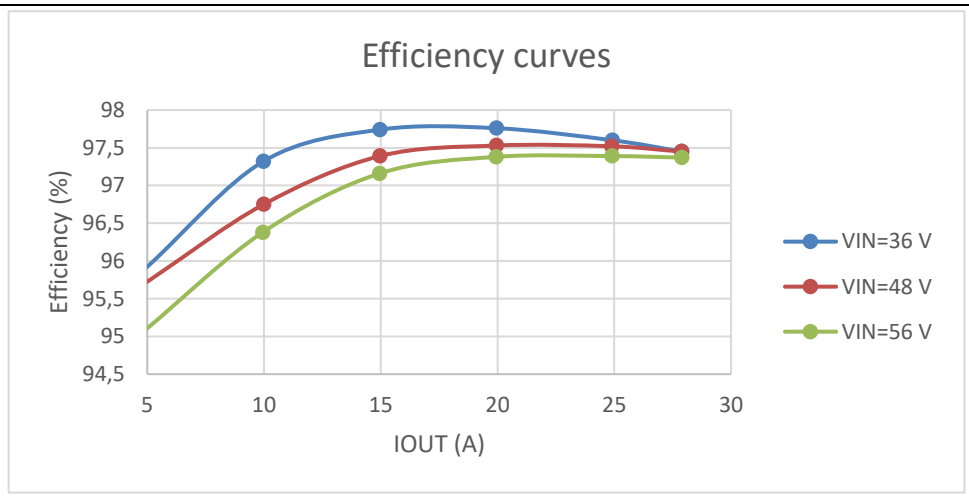
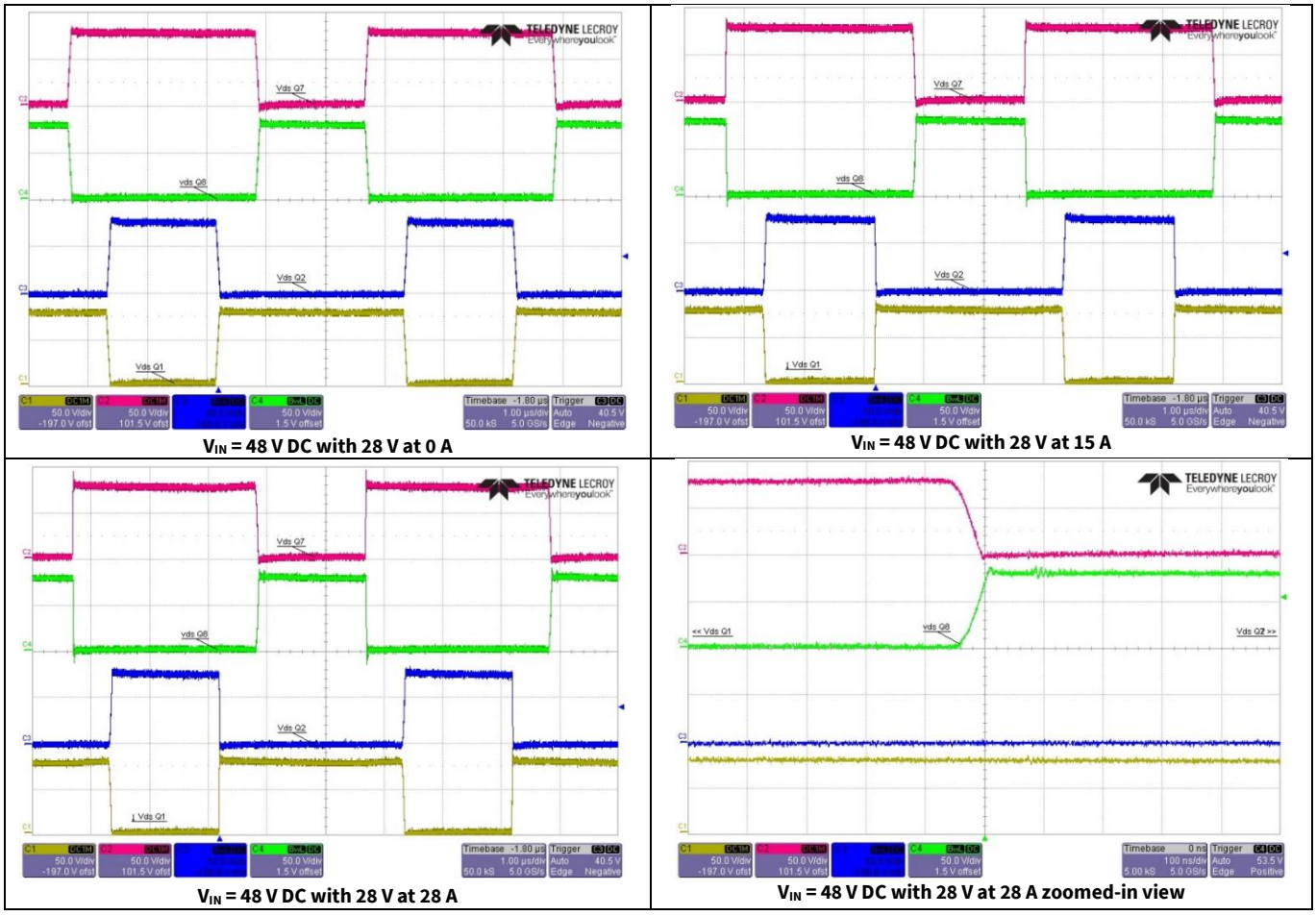


Figure 22 Efficiency curves

5.2 Steady-state waveforms

The switching waveforms of the buck-boost converter are shown in **Figure 23** and **Figure 24**. The part designator refers to the schematic shown in **Figure 38**.

Ch.1 = V_{DS} Q1 bottom-side FET, Ch.2 = V_{DS} Q7 bottom-side FET, Ch.3 = V_{DS} Q2 top-side FET, Ch.4 = V_{DS} Q8 top-side FET



V_{IN} = 48 V DC with 28 V at 0 A

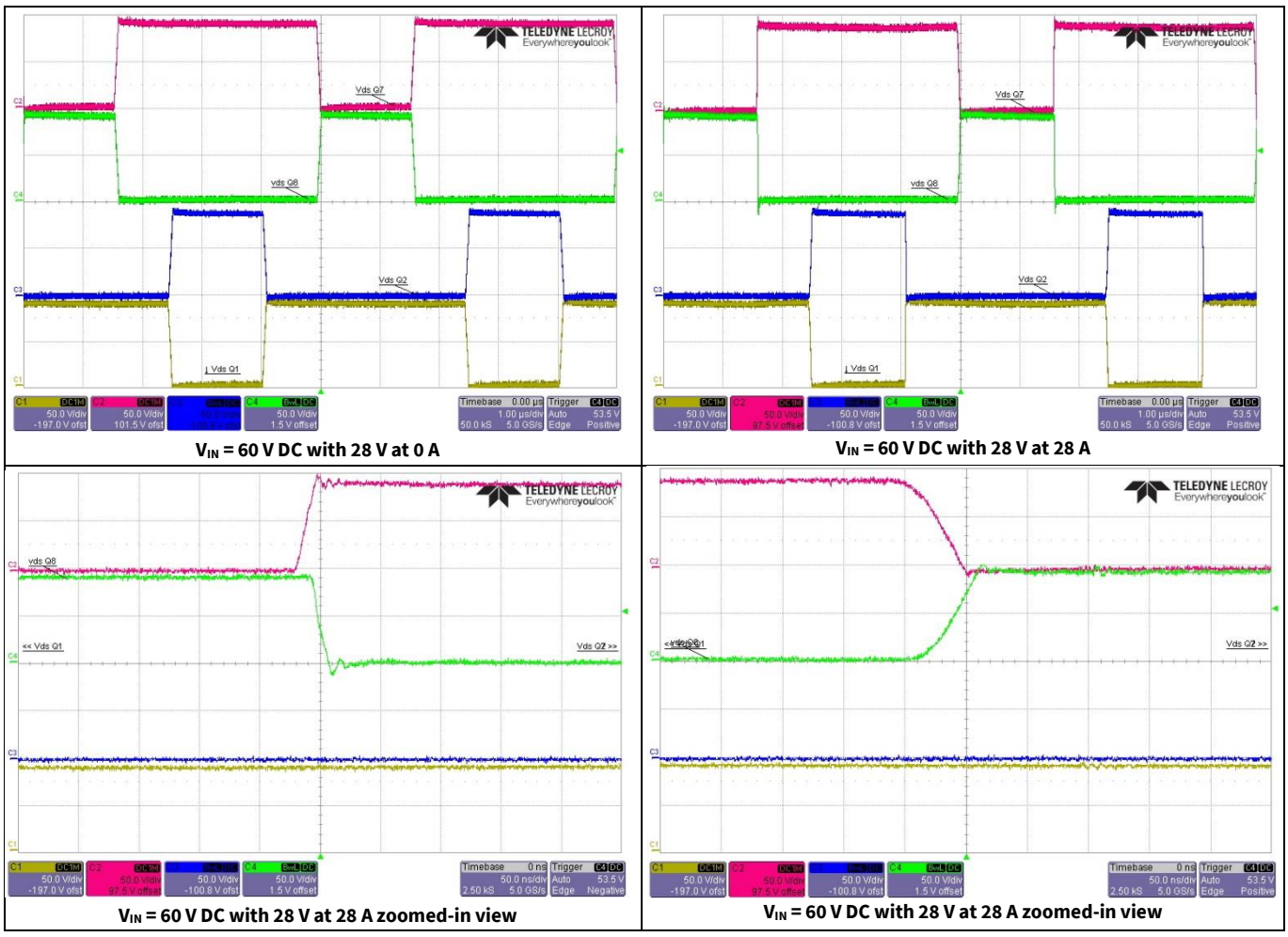
V_{IN} = 48 V DC with 28 V at 15 A

V_{IN} = 48 V DC with 28 V at 28 A

V_{IN} = 48 V DC with 28 V at 28 A zoomed-in view

Figure 23 Switching waveforms at 48 V input

Ch.1 = V_{DS} Q1 bottom-side FET, Ch.2 = V_{DS} Q7 bottom-side FET, Ch.3 = V_{DS} Q2 top-side FET, Ch.4 = V_{DS} Q8 top-side FET



V_{IN} = 60 V DC with 28 V at 0 A

V_{IN} = 60 V DC with 28 V at 28 A

V_{IN} = 60 V DC with 28 V at 28 A zoomed-in view

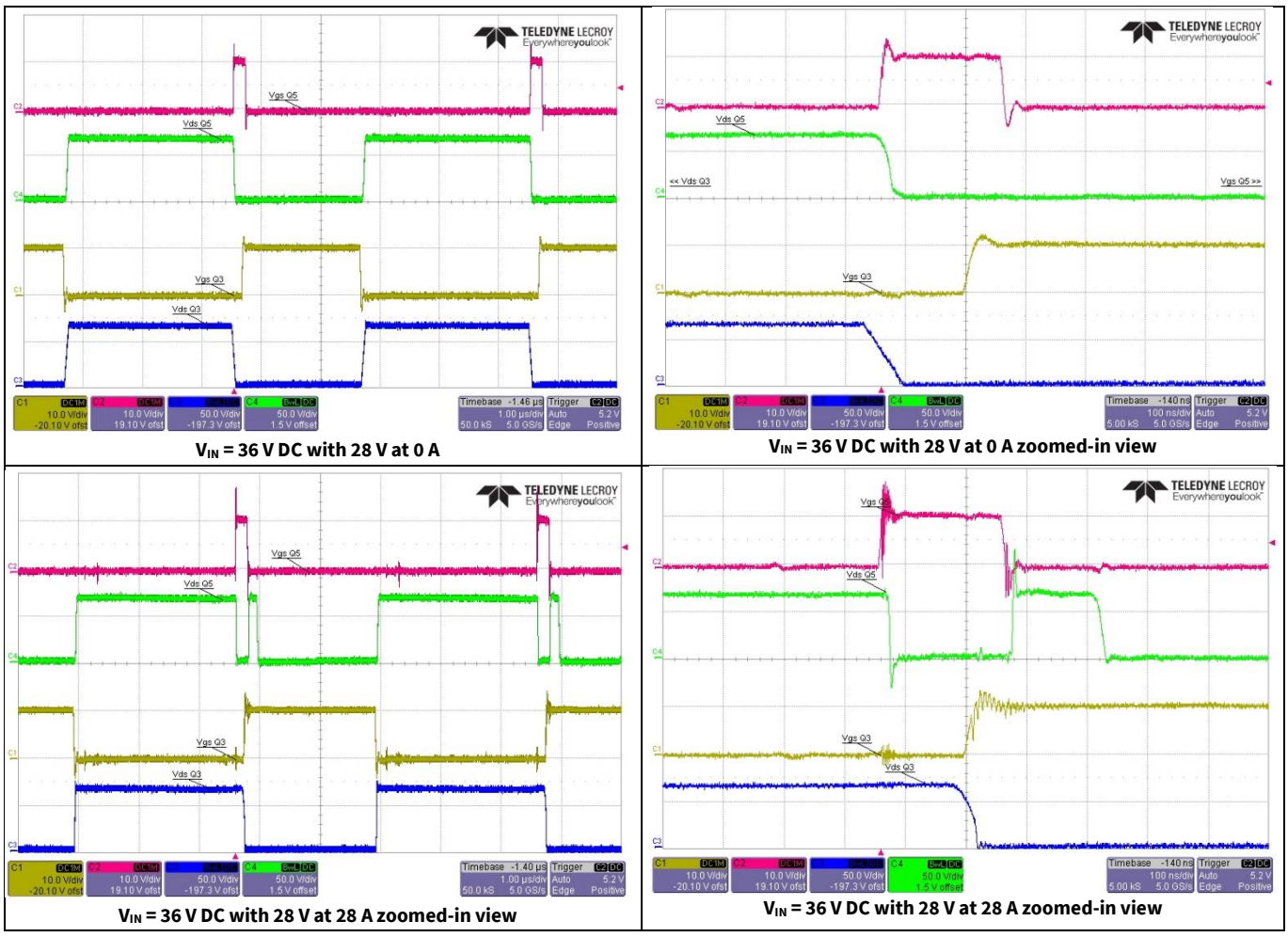
V_{IN} = 60 V DC with 28 V at 28 A zoomed-in view

Figure 24 Switching waveforms at 60 V input

The zoomed-in waveforms show the ZVS switching when the top-side FET (SR FET) turns off.

Figure 25 to **Figure 27** show the timing of the ZVS FET and the bottom-side FET (control FET).

Ch.1 = V_{GS} Q3 bottom-side FET, Ch.2 = V_{GS} Q5 ZVS FET, Ch.3 = V_{DS} Q3 bottom-side FET, Ch.4 = V_{DS} Q5 ZFS FET



V_{IN} = 36 V DC with 28 V at 0 A

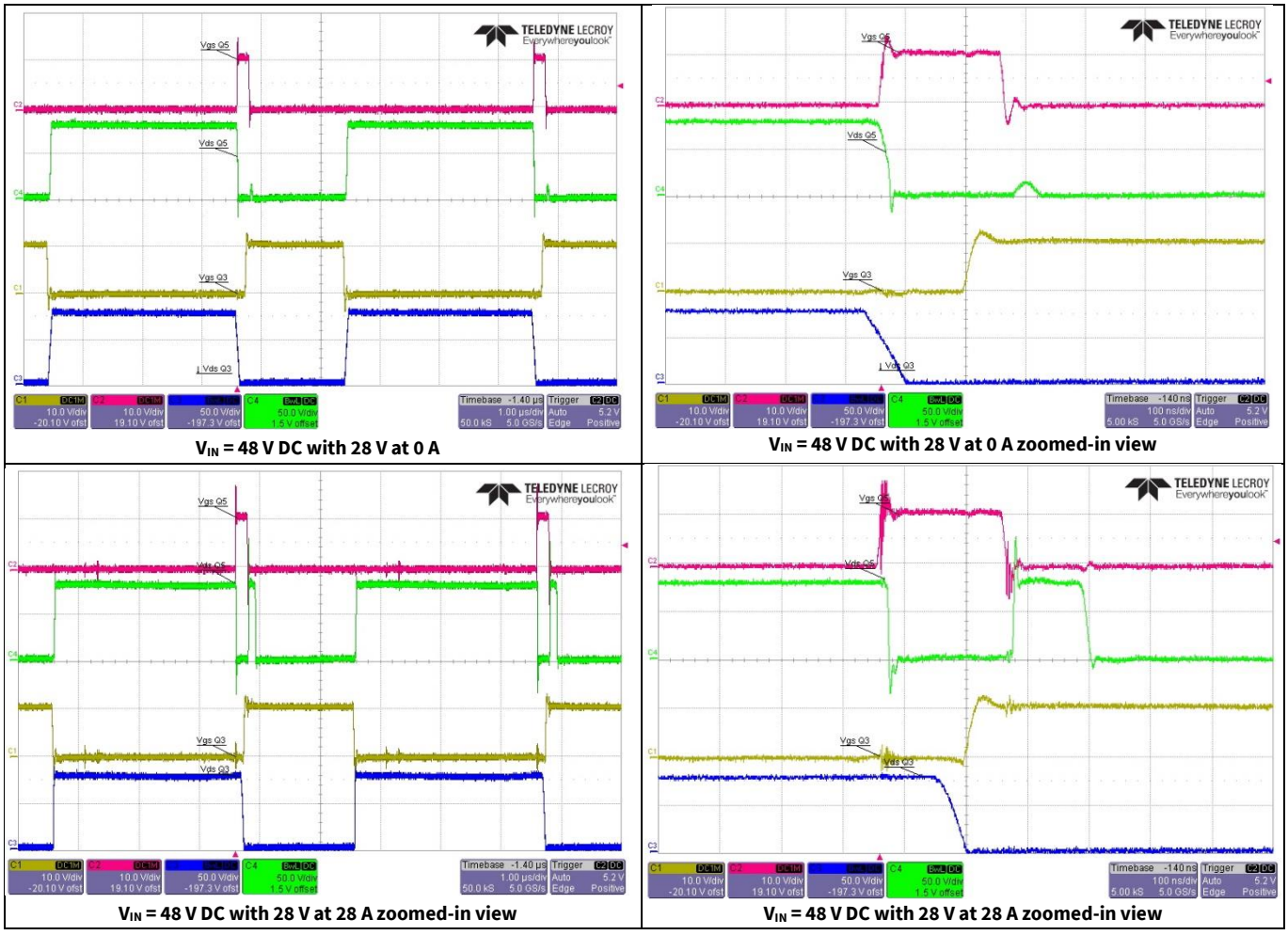
V_{IN} = 36 V DC with 28 V at 0 A zoomed-in view

V_{IN} = 36 V DC with 28 V at 28 A zoomed-in view

V_{IN} = 36 V DC with 28 V at 28 A zoomed-in view

Figure 25 Switching waveforms at 36 V input

Ch.1 = V_{GS} Q3 bottom-side FET, Ch.2 = V_{GS} Q5 ZVS FET, Ch.3 = V_{DS} Q3 bottom-side FET, Ch.4 = V_{DS} Q5 ZFS FET



V_{IN} = 48 V DC with 28 V at 0 A

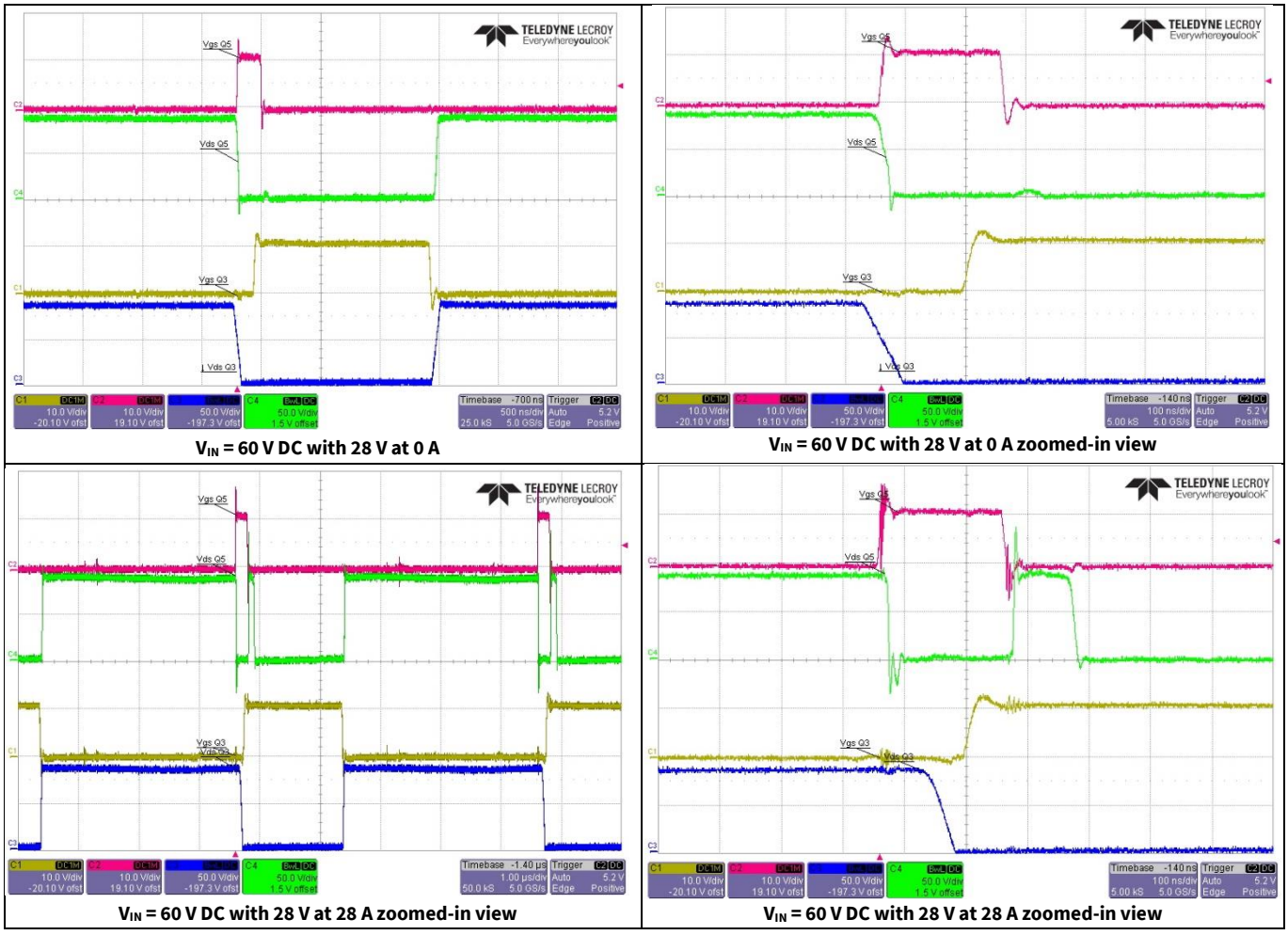
V_{IN} = 48 V DC with 28 V at 0 A zoomed-in view

V_{IN} = 48 V DC with 28 V at 28 A zoomed-in view

V_{IN} = 48 V DC with 28 V at 28 A zoomed-in view

Figure 26 Switching waveforms at 48 V input

Ch.1 = V_{GS} Q3 bottom-side FET, Ch.2 = V_{GS} Q5 ZVS FET, Ch.3 = V_{DS} Q3 bottom-side FET, Ch.4 = V_{DS} Q5 ZFS FET



V_{IN} = 60 V DC with 28 V at 0 A

V_{IN} = 60 V DC with 28 V at 0 A zoomed-in view

V_{IN} = 60 V DC with 28 V at 28 A zoomed-in view

V_{IN} = 60 V DC with 28 V at 28 A zoomed-in view

Figure 27 Switching waveforms at 60 V input

5.3 Start-up waveforms

Start-up waveforms at different input voltages and at no load and full load are shown in **Figure 28**.

Ch.1 = V_{OUT} (5 V/div, DC coupled)

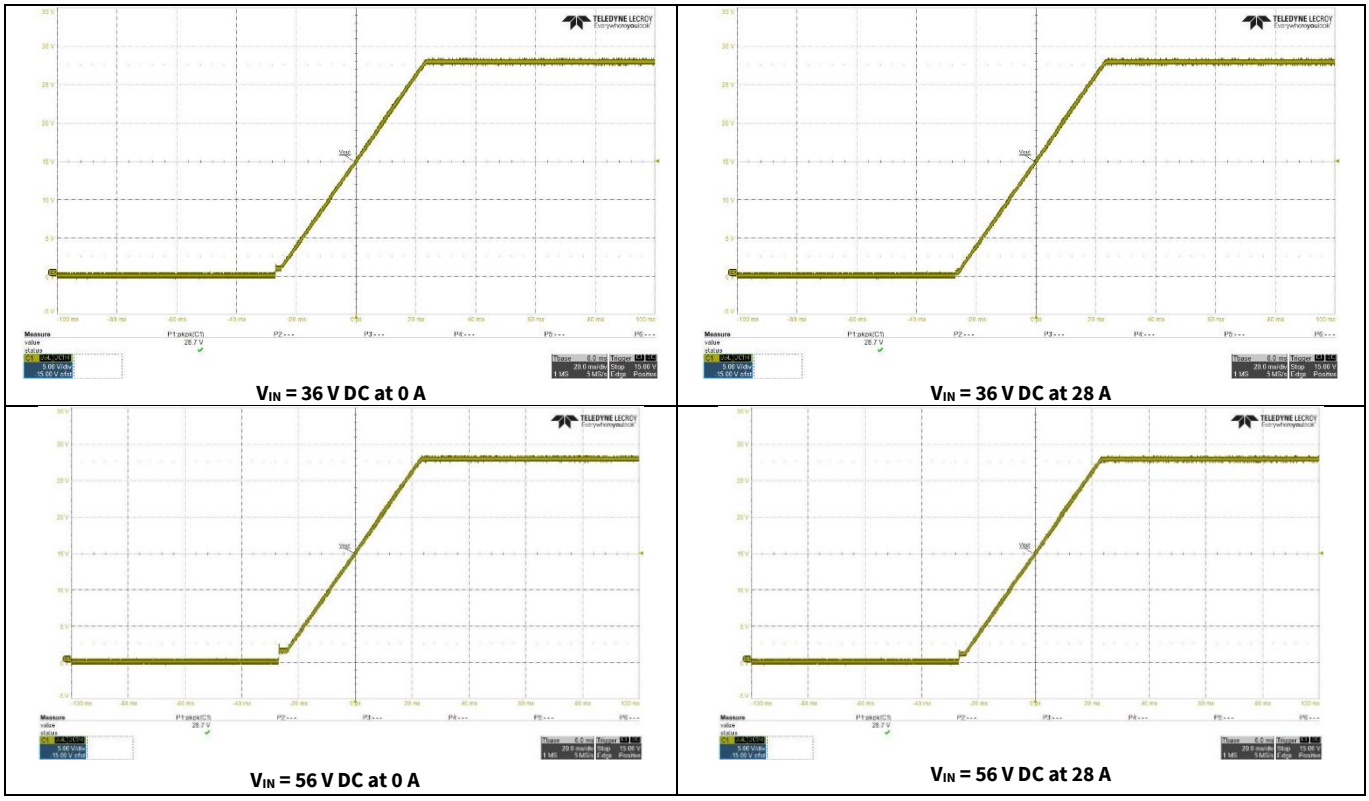


Figure 28 Start-up waveforms

5.4 Output PARD

Output periodic and random deviation (PARD) ripple waveforms are shown in **Figure 29**.

Ch.1 = V_{OUT} (20 mV/div, AC coupled)

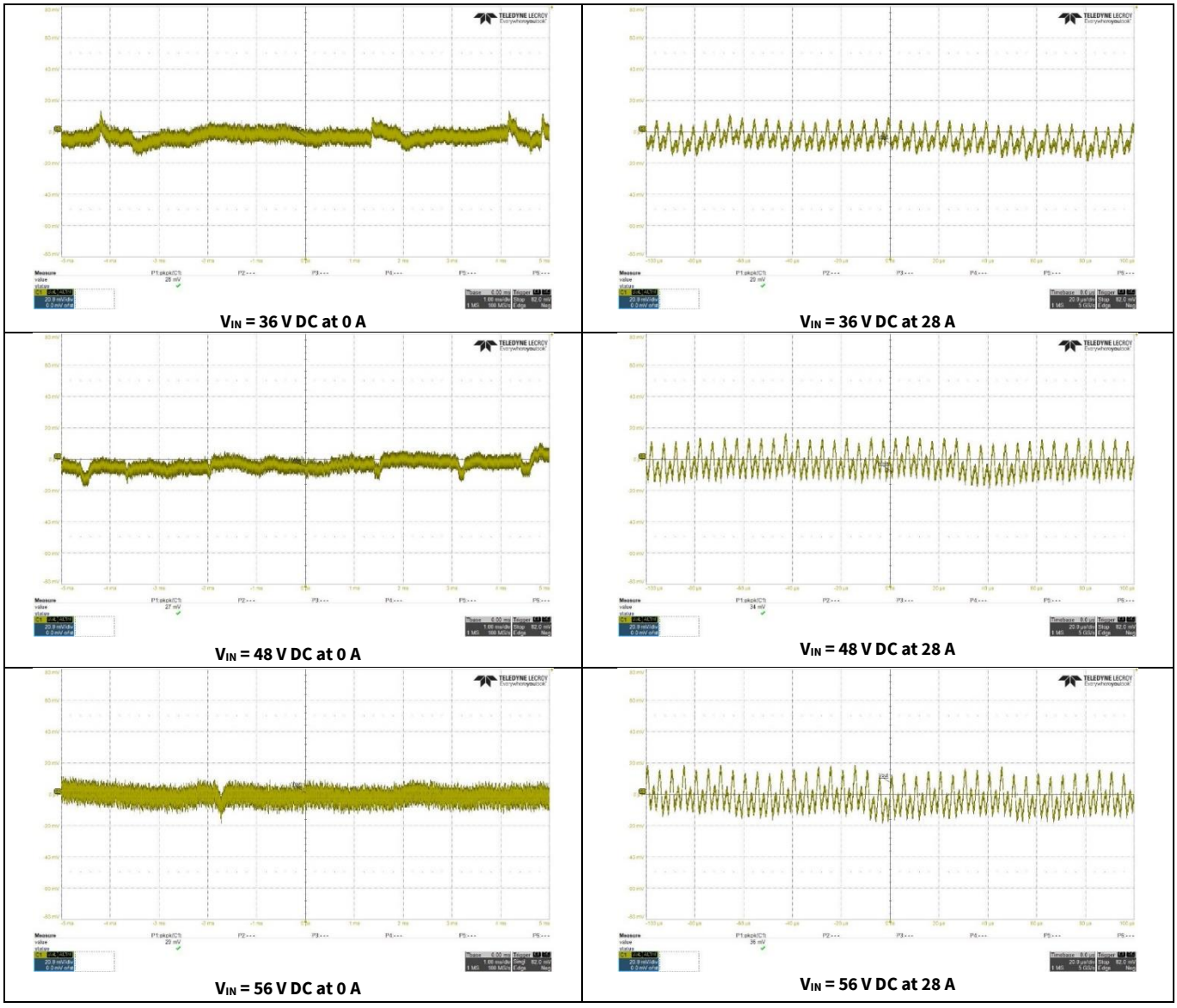
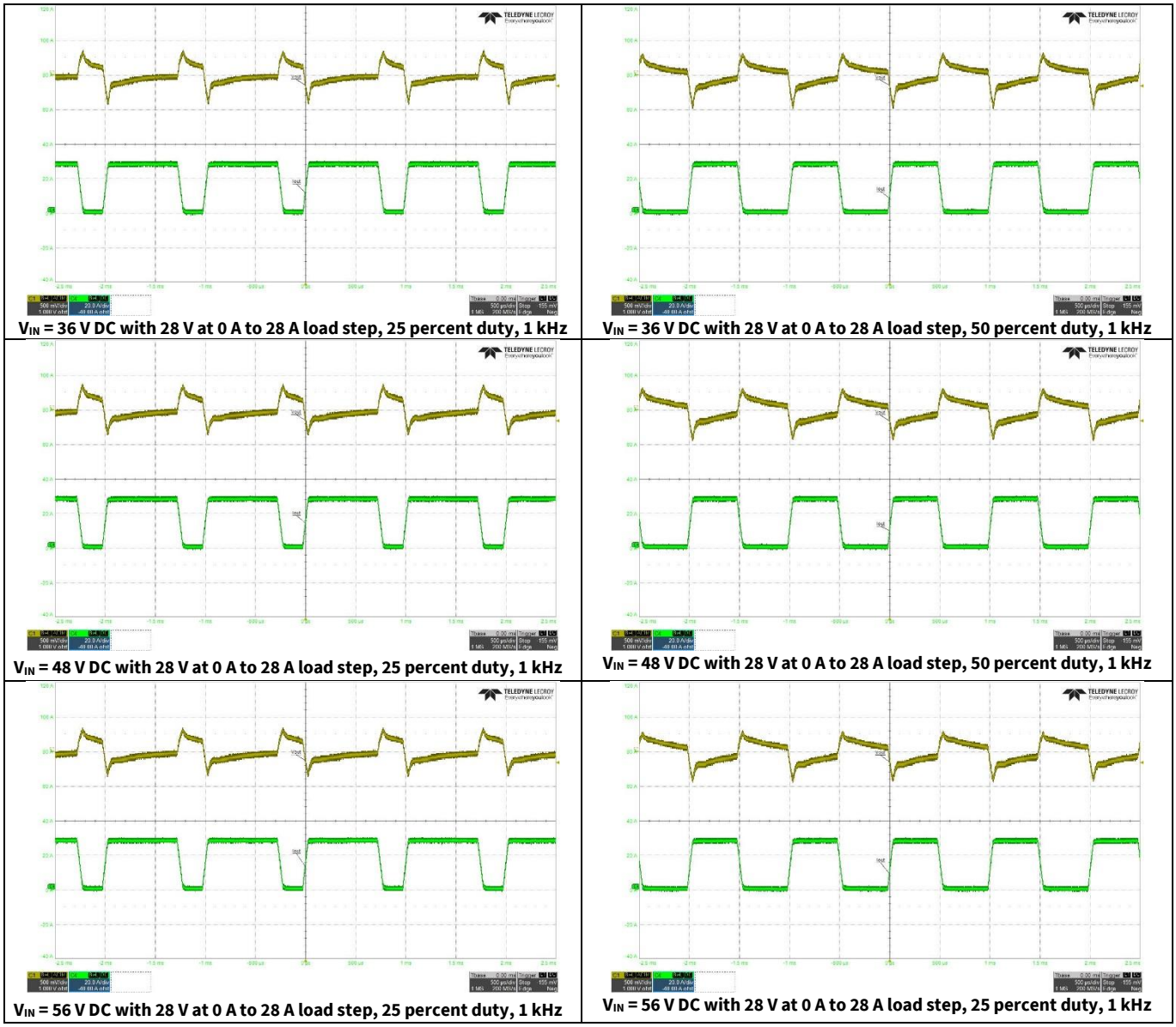


Figure 29 Output PARD

5.5 Load-transient response

Ch.1 = V_{OUT} (500 mV/div, AC coupled), Ch.4 = output current (20 A/div)



V_{IN} = 36 V DC with 28 V at 0 A to 28 A load step, 25 percent duty, 1 kHz

V_{IN} = 36 V DC with 28 V at 0 A to 28 A load step, 50 percent duty, 1 kHz

V_{IN} = 48 V DC with 28 V at 0 A to 28 A load step, 25 percent duty, 1 kHz

V_{IN} = 48 V DC with 28 V at 0 A to 28 A load step, 50 percent duty, 1 kHz

V_{IN} = 56 V DC with 28 V at 0 A to 28 A load step, 25 percent duty, 1 kHz

V_{IN} = 56 V DC with 28 V at 0 A to 28 A load step, 25 percent duty, 1 kHz

Figure 30 Load-transient waveforms

5.6 Input voltage transient response

Ch.1 = V_{OUT} (200 mV/div, AC coupled), Ch.3 = input voltage (20 V/div)

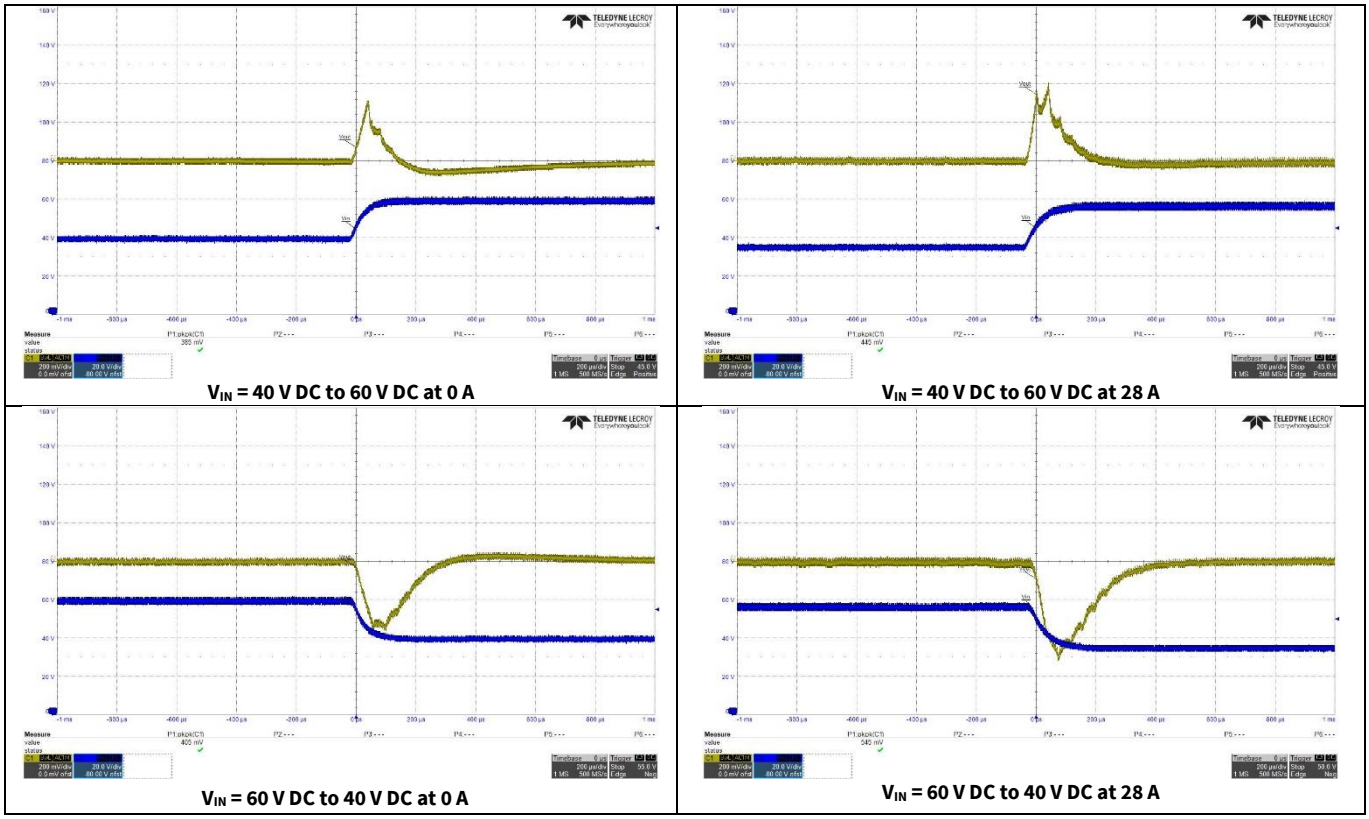


Figure 31 Line-transient waveforms

5.7 Current balancing

Phase 1 and phase 2 current are measured at different I_{OUT} to check the current balancing performance. The inductor current of each phase is probed, and the averages of inductor currents are listed in **Table 9**. The output current of each phase is calculated per inductor current and duty-cycle. The current balancing error is less than 5 percent at 10 A and above. A higher error rate at light load is expected due to CS accuracy being worse at light load. The current balancing is disabled when output current is less than 3 A, configured by register **ibal_en_thresh** = 2.

Table 9 Current balance at 48 V input

Total load current (A)	Phase 1 inductor (A)	Phase 2 inductor (A)	Phase 1 output (A)	Phase 2 output (A)	Balance error (%)
5 (4.98 A)	3.33	4.2	2.10	2.65	-11.6 %
10 (10.01 A)	7.08	7.88	4.47	4.98	-5.3 %
15 (15 A)	10.78	11.44	6.81	7.23	-3.0 %
20 (19.98 A)	14.71	14.97	9.29	9.45	-0.9 %
25 (25.07 A)	18.31	18.81	11.56	11.88	-1.3 %
28 (28.03 A)	20.76	20.6	13.11	13.01	0.4 %

5.8 Overcurrent protection

The XDPP1100 has three levels of overcurrent protection (OCP). The cycle-averaged and filtered I_{OUT} OCP, cycle-averaged but non-filtered I_{OUT} OC FAST (fast OCP), and short-circuit protection (SCP). The IOUT_OC and IOUT_OC_FAST can be configured in the design tool “Fault Protections”, as shown in **Figure 32**. The threshold should be calculated based on input inductor current at the worst case at 36 V input and 28 V/28 A output.

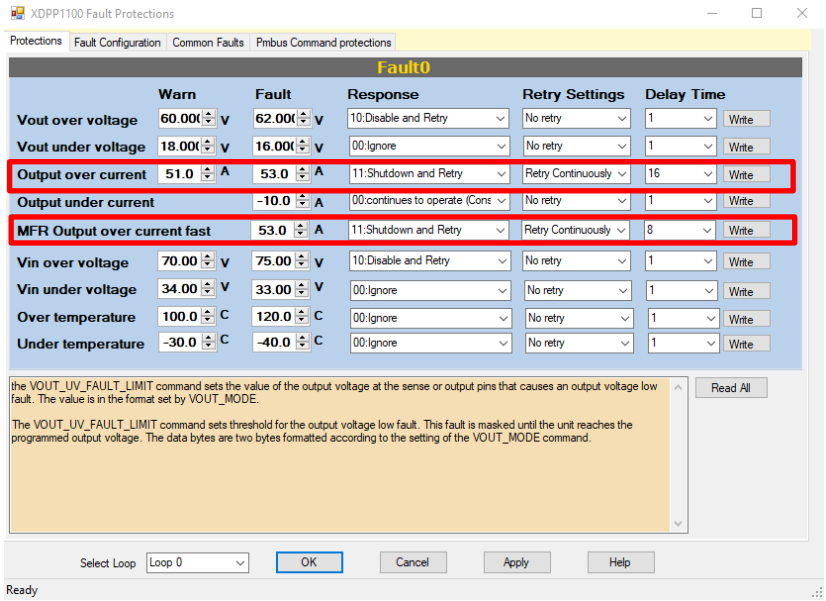


Figure 32 Fault protection

The SCP is the fastest over current protection, which responds to the instantaneous current of each phase, including ripple and spike. The SCP is configured in the “common fault” tab of the fault protection. The threshold is current **per phase** in amps. To enable common fault shutdown, check the common fault box in the “common fault shutdown configuration” section.

This protection can be disabled by setting the threshold value to 0.

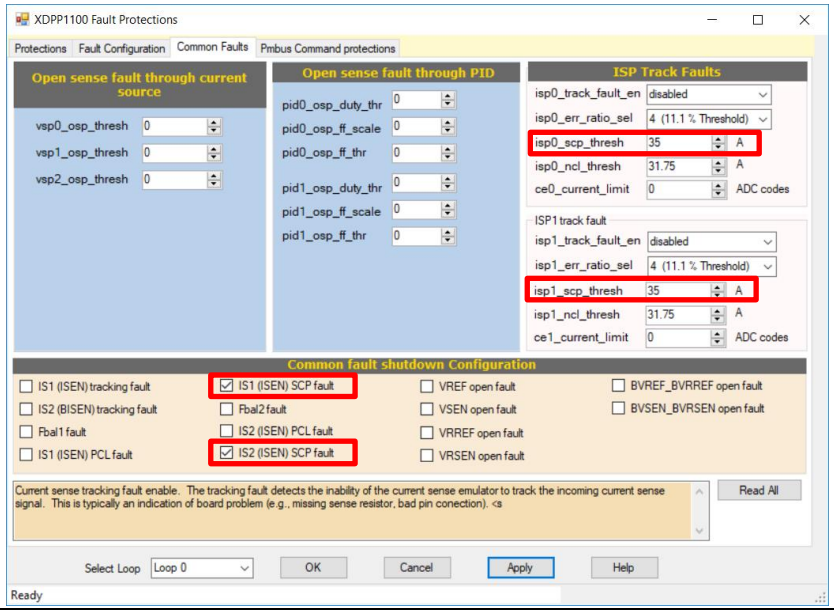
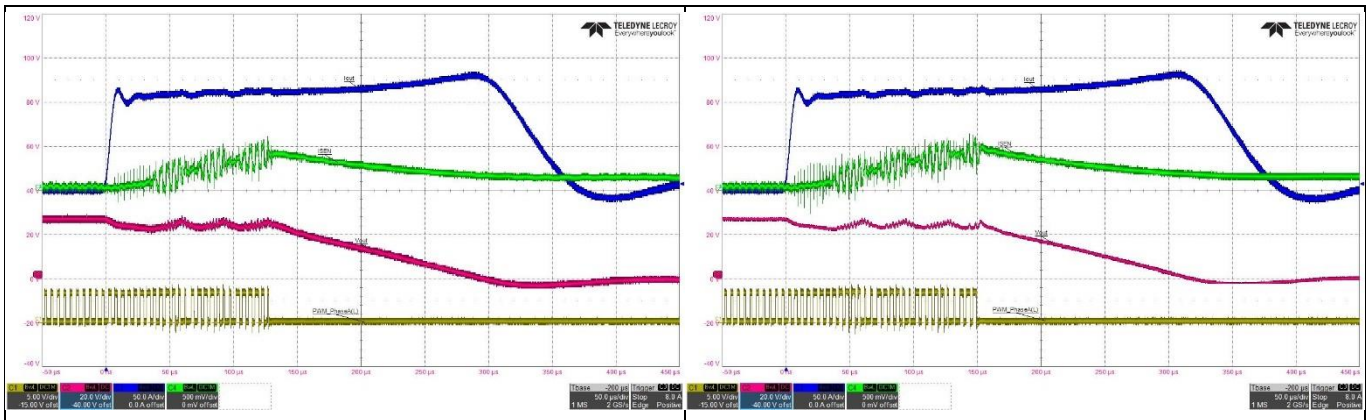


Figure 33 Common fault configuration – SCP

Figure 34 shows the output SCP waveform, in response to MFR_IOUT_OC_FAST_FAULT. The short-circuit is performed by e-load, applied at 0 A initial output current, which is the worst case as the inductor current needs time to build up. The ISEN is the input of the CS ADC of the controller. It shows that shutdown delay is due to the ISEN taking 130 µs before reaching the protection threshold. The fault0_mfr_iout_oc_fast_cnt sets the number of consecutive switching cycles (T_{SW}) the cycle-averaged current must exceed the fault threshold by in order to assert a fault. The fault count reduces the sensitivity of the OCP protection and adds additional delays to the shutdown response.

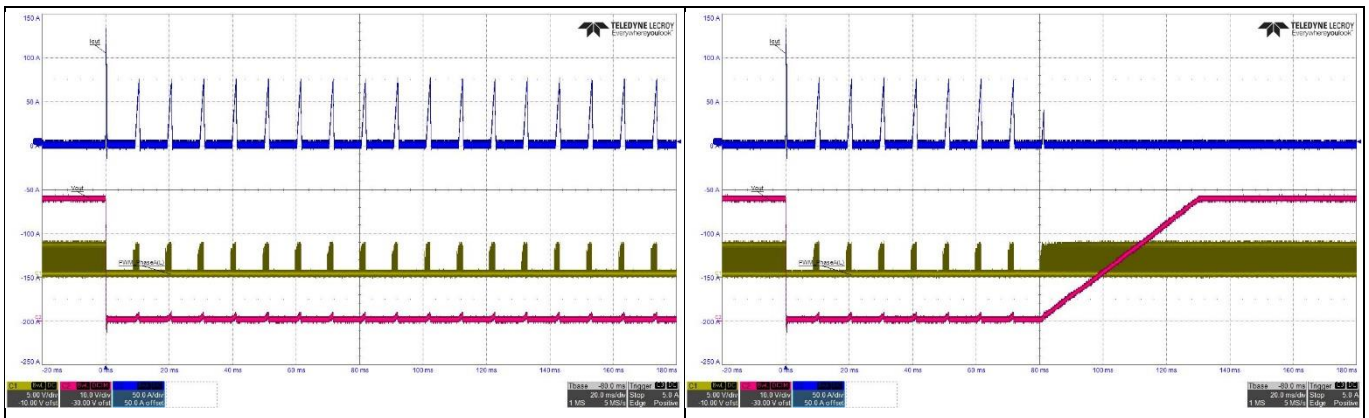
Ch.1 = PH1_LO phase 1 bottom-side FET PWM, Ch.2 = V_{OUT} (20 V/div), Ch.3 = I_{OUT} (50 A/div), Ch.4 = ISEN (500 mV/div)



fault0_mfr_iout_oc_fast_cnt =0 | fault0_mfr_iout_oc_fast_cnt = 4

Figure 34 OCP waveforms

Figure 35 shows the power supply response when the MFR_IOUT_OC_FAST_FAULT_RESPONSE is set to “shutdown and retry continuously”, and retry delay time is 8 ms.



Output hiccup when the short-circuit persisted | Output resumed when the short-circuit was removed

Figure 35 Overcurrent fault response

5.9 Thermal images

Thermal data was taken with a heatsink installed at no airflow. The unit was allowed 30 minutes to reach thermal stability before measurements were recorded. The thermal testing was done at 36 V DC, 48 V DC and 60 V DC inputs, but only the 60 V result is shown because it is the highest. The thermocouple probes are shown in **Figure 36**. The measured thermal image is shown in **Figure 37**.

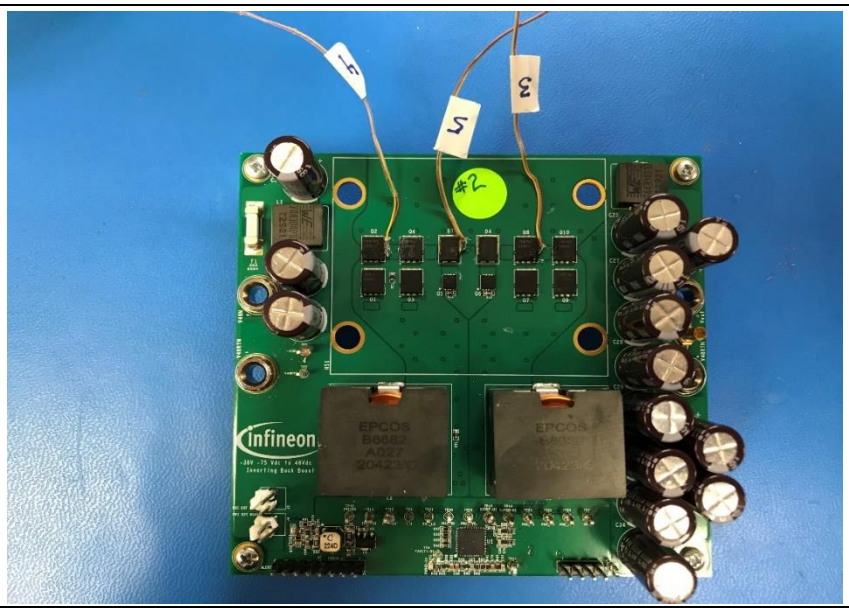


Figure 36 Thermocouple placement

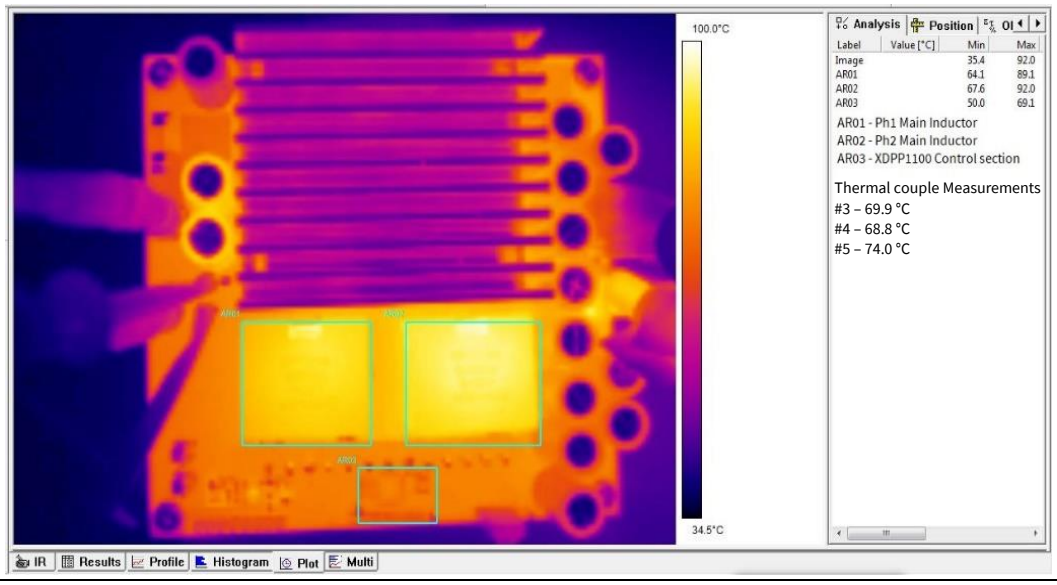


Figure 37 Thermal testing done at 60 V DC input with 28 V at 28 A output and no airflow

6 Schematic

6.1 Power stage schematic

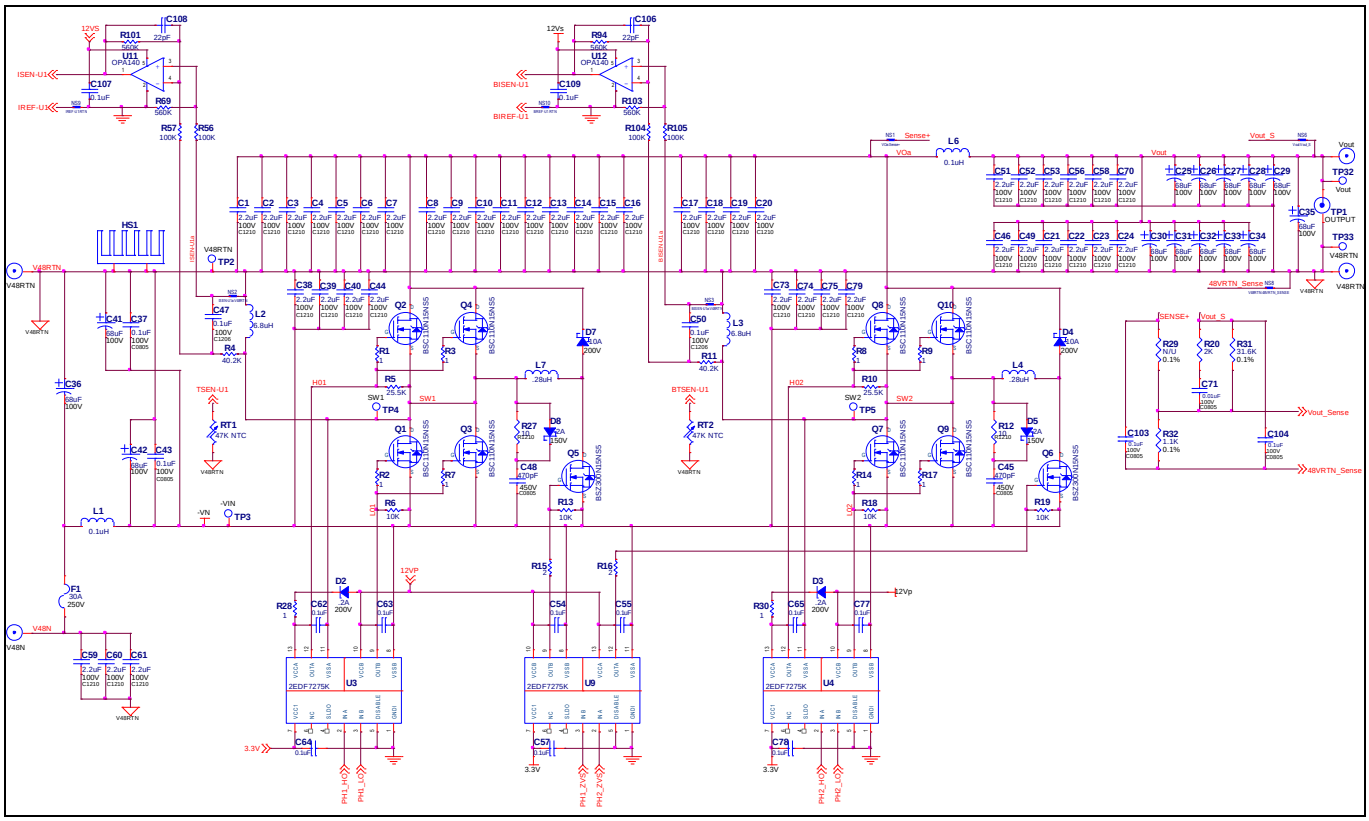


Figure 38 Power stage of the demo board

6.2 Control circuit schematic

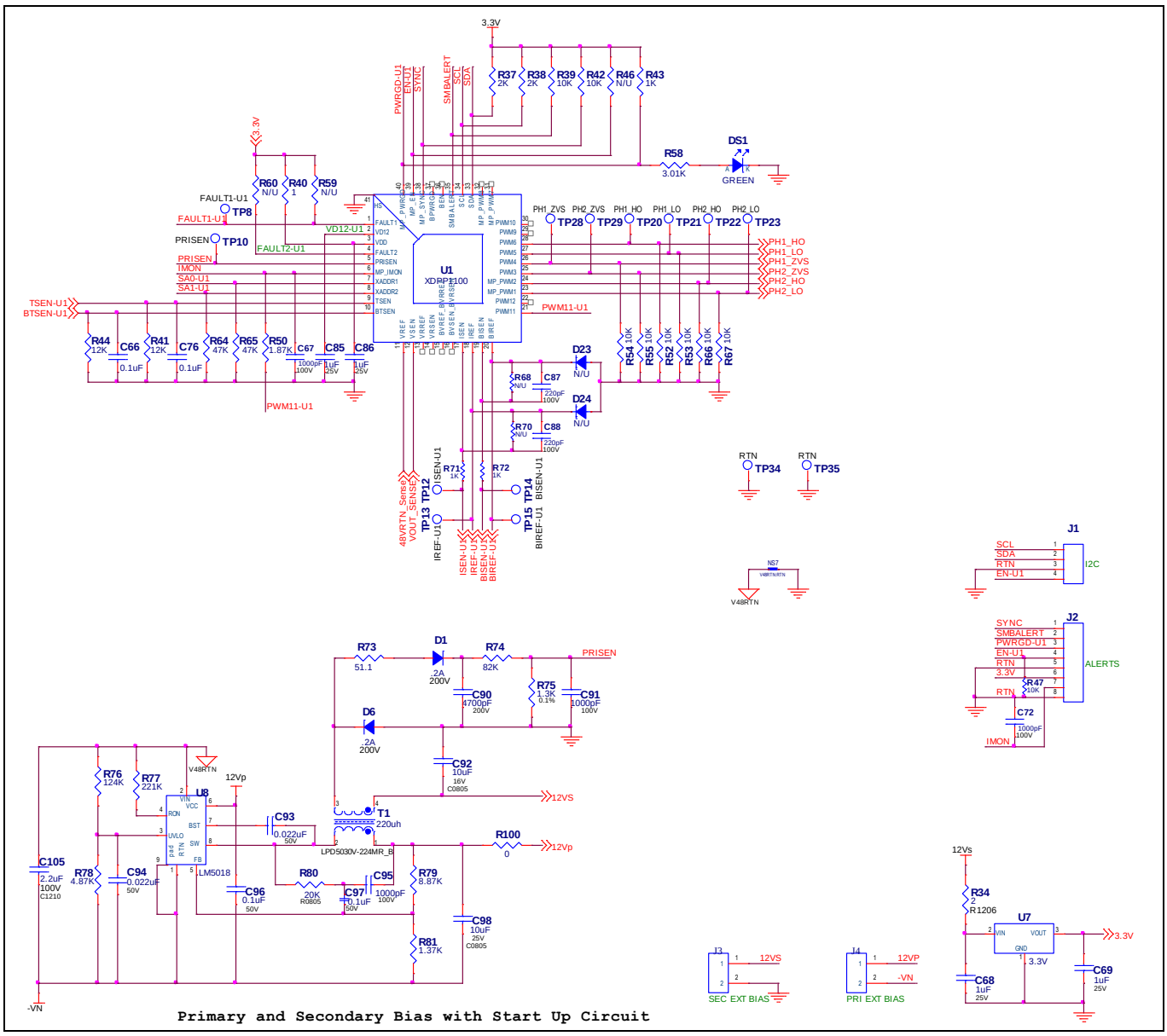


Figure 39 Control circuit of the demo board

6.3 Bill of materials

Table 10 Bill of materials

Item	Qty.	Ref.	Manufacturer	Part number
1	1	BRD1		P100124 A
2	44	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C38, C39, C40, C44, C46, C49, C51, C52, C53, C56, C58, C59, C60, C61, C70, C73, C74, C75, C79, C105	TDK	C3225X7R2A225K230AM
3	14	C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C41, C42	Nichicon	UPW2A680MPD
4	4	C37, C43, C103, C104	TDK	C2012X7R2A104K125AA
5	2	C45, C48	TDK	C2012C0G2W471K060AA
6	2	C47, C50	TDK	C3216C0G2A104J160AE
7	15	C54, C55, C57, C62, C63, C64, C65, C66, C76, C77, C78, C96, C97, C107, C109	TDK	C1608X7R1H104K080AA
8	4	C67, C72, C91, C95	TDK	C1608C0G2A102J080AA
9	4	C68, C69, C85, C86	TDK	C1608X7R1E105K080AB
10	1	C71	TDK	C2012C0G2A103K125AA
11	2	C87, C88	TDK	C1608C0G2A221K080AA
12	1	C90	Kemet	C0603C472K2RACTU
13	1	C92	Samsung	CL21B106KOQNNNE
14	2	C93, C94	TDK	C1608X7R1H223K080AA
15	1	C98	TDK	C2012X5R1E106K125AB
16	2	C106, C108	TDK	C1608C0G1H220J080AA
17	1	DS1	Würth	150060GS75000
18	4	D1, D2, D3, D6	ON Semiconductor	BAS20HT1G
19	2	D4, D7	Vishay	V10P20-M3/87A
20	2	D5, D8	STMicroelectronics	STPS2150A
21	2	D23, D24	NXP	Not Used
22	1	F1	Bel Fuse	0678H9300-02
23	1	HS1		H100023-3
24	1	J1	Würth	61300411121
25	1	J2	Würth	61300811121
26	2	J3, J4	TE Connect	640456-2
27	2	L1, L6	Würth	744304010
28	2	L2, L3	TDK	B82559B6682A027
29	2	L4, L7	Coilcraft	XEL6030-281MEB
30	8	Q1, Q2, Q3, Q4, Q7, Q8, Q9, Q10	Infineon	BSC110N15NS5ATMA1

Item	Qty.	Ref.	Manufacturer	Part number
31	2	Q5, Q6	Infineon	BSZ300N15NS5ATMA1
32	2	RT1, RT2	Murata	NCP15WB473F03RC
33	11	R1, R2, R3, R7, R8, R9, R14, R17, R28, R30, R40	Panasonic	ERJ-3RQF1R0V
34	2	R4, R11	Panasonic	ERJ-3EKF4022V
35	15	R5, R6, R10, R13, R18, R19, R39, R42, R47, R52, R53, R54, R55, R66, R67	Panasonic	ERJ-3EKF1002V
36	2	R12, R27	Panasonic	ERJ-14NF10R0U
37	2	R15, R16	Panasonic	ERJ-3BQF2R0V
38	3	R20, R37, R38	Panasonic	ERJ-3EKF2001V
39	1	R29	Panasonic	Not Used
40	1	R31	Panasonic	ERA-3AEB3162V
41	1	R32	Panasonic	ERA-3AEB112V
42	1	R34	Panasonic	ERJ-8RQF2R0V
43	2	R41, R44	Panasonic	ERJ-3EKF1202V
44	3	R43, R71, R72	Panasonic	ERJ-3EKF1001V
45	5	R46, R59, R60, R68, R70	Panasonic	Not Used
46	1	R50	Panasonic	ERJ-3EKF1871V
47	4	R56, R57, R104, R105	Panasonic	ERJ-3EKF1003V
48	1	R58	Panasonic	ERJ-3EKF3011V
49	2	R64, R65	Panasonic	ERJ-3EKF4702V
50	4	R69, R94, R101, R103	Panasonic	ERJ-3EKF5603V
51	1	R73	Panasonic	ERJ-3EKF51R1V
52	1	R74	Panasonic	ERJ-3EKF8202V
53	1	R75	Panasonic	ERA-3AEB132V
54	1	R76	Panasonic	ERJ-3EKF1243V
55	1	R77	Panasonic	ERJ-3EKF2213V
56	1	R78	Panasonic	ERJ-3EKF4871V
57	1	R79	Panasonic	ERJ-3EKF8871V
58	1	R80	Panasonic	ERJ-6ENF2002V
59	1	R81	Panasonic	ERJ-3EKF1371V
60	1	R100	Panasonic	ERJ-3GEY0R00V
61	1	TP1	Cinch Connectivity	129-0701-202
62	20	TP2, TP3, TP4, TP5, TP8, TP10, TP12, TP13, TP14, TP15, TP20, TP21, TP22, TP23, TP28, TP29, TP32, TP33, TP34, TP35	Keystone	5020
63	1	T1	Coilcraft	LPD5030V-224MR_B
64	1	U1	Infineon	XDPP1100-Q040K64
65	3	U3, U4, U9	Infineon	2EDF7275KXUMA1
66	1	U7	STMicroelectronics	LDK320ADU33R
67	1	U8	Texas Instruments	LM5018SD/NOPB
68	2	U11, U12	Texas Instruments	OPA140AIDBVT

Item	Qty.	Ref.	Manufacturer	Part number
69	4	1, 2, 3, 4	Keystone	575-4
70	1	BRD1		P100124 A
71	44	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C38, C39, C40, C44, C46, C49, C51, C52, C53, C56, C58, C59, C60, C61, C70, C73, C74, C75, C79, C105	TDK	C3225X7R2A225K230AM
72	14	C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C41, C42	Nichicon	UPW2A680MPD
73	4	C37, C43, C103, C104	TDK	C2012X7R2A104K125AA

7 XDPP1100 configuration guide

The inverted buck-boost converter can be configured using GUI design tools, following the steps from 1 to 6 for the topology, and system settings for start-up and shutdown, PID compensation, fault and protections, basic configuration for input voltage/current and output current telemetry setup, and advanced features of feed-forward and current balancing.

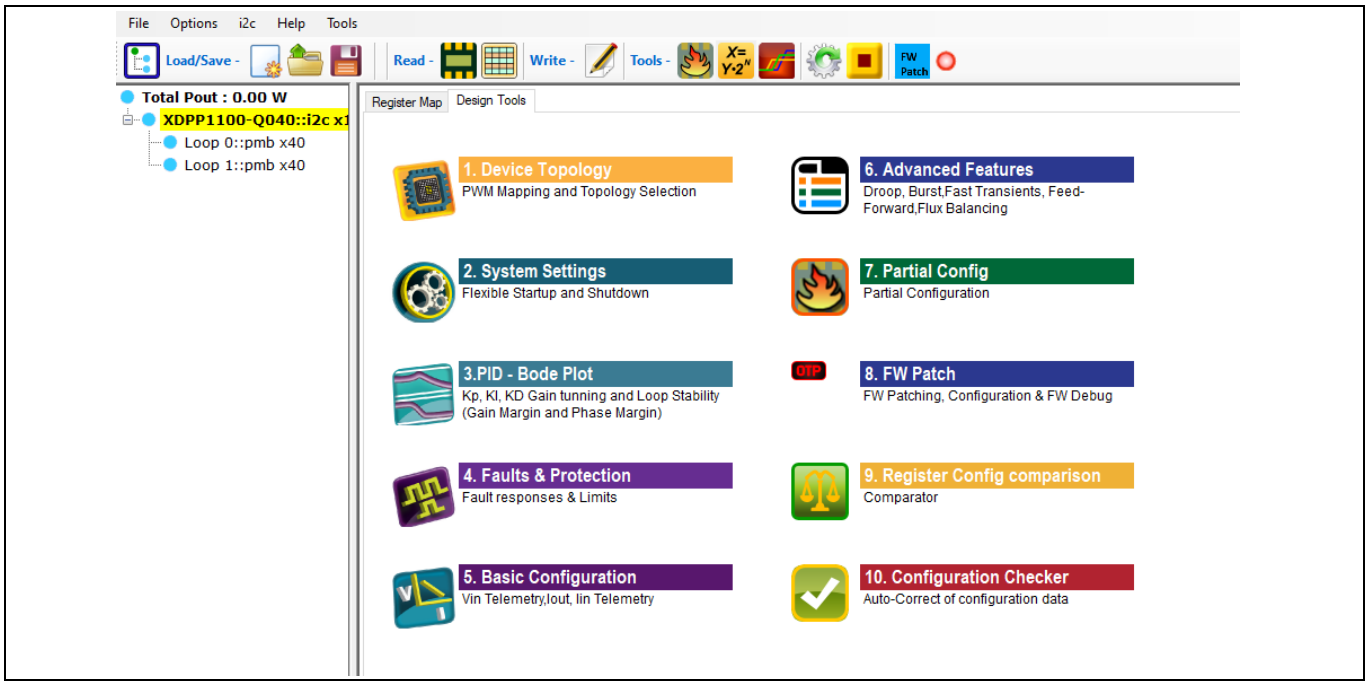


Figure 40 XDPP1100 GUI design tools

7.1 Configuring the active ZVS

The demo board implements an active clamp circuit to achieve ZVS. The ZVS MOSFET is driven by PWM4 (phase 1) and PWM3 (phase 2). As the ZVS is not part of the standard topology, it must be manually configured in the register map, per **Table 11**.

Table 11 PWM3, PWM4 config

Register	Config value	Comments
pwm3_fall_sel	6, t1 delay	PWM3 is turned off at t1 delay (delay time is 10 ns)
pwm3_rise_sel	0, t1	PWM3 is turned on at t1 (which is the falling edge of Q4, pwm2)
pwm4_fall_sel	6, t1 delay	PWM4 is turned off at t1 delay (delay time is 10 ns)
pwm4_rise_sel	0, t1	PWM4 is turned on at t1 (which is the falling edge of Q2, pwm6)
pwm3_loop_map	3	PWM3 is the ZVS control of loop 0, phase 2
pwm4_loop_map	1	PWM4 is the ZVS control of loop 0, phase 1
pwm3_ppen	1	Set CMOS output
pwm4_ppen	1	Set CMOS output

In addition to the register, PMBus command FW_CONFIG_PWM should also be updated to activate PWM3 and PWM4 as shown in **Figure 41**. This configures PWM1 and PWM5 as control PWM, PWM2 and PWM6 as SR output, and PWM3 and PWM4 are added as the control switch.

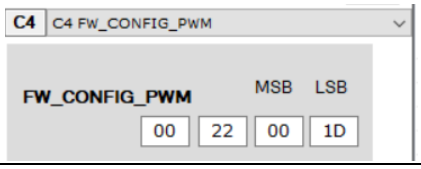


Figure 41 FW_CONFIG_PWM

Table 12 FW_CONFIG_PWM

Command	New value	Comments
FW_CONFIG_PWM	00 22 00 1D	The 00 1D means primary (control) FETs are driven by PWM1, PWM3, PWM4, PWM5 The 00 22 means SR FETs are driven by PWM2, PWM6

The ZVS PWM will turn on at t1 and turn off at t1_delay. The t1 and t1_delay has 10 ns time difference. So the internal pulse width of PWM3 and PWM4 is only 10 ns. To have the desired pulse width, the user should add delay to the rising and falling edge to PWM3 and PWM4 by configuring the dead time.

PWM dead time can be set by PMBus command 0xCF PWM_DEADTIME. The dead times of the PWM rising and falling edge can be set separately. The dead time adds delay to the rising edge or the falling edge of PWM and is always positive. The maximum dead time can be set to 318.75 ns with a resolution of 1.25 ns.

For example, setting the rise delay of PWM3 to 50 ns will turn on PWM3 50 ns after t1 crossing. As PWM2 is turned off right at t1 (it has 0 ns delay), the dead time between the PWM2 falling edge and PWM3 rising edge is 50 ns. Setting the falling edge dead time of PWM3 to 240 ns will turn off PWM3 240 ns after t1_delay crossing. As the t1_delay is 10 ns after t1, the PWM3 pulse width can be calculated by 10 ns + 240 ns – 50 ns = 200 ns.

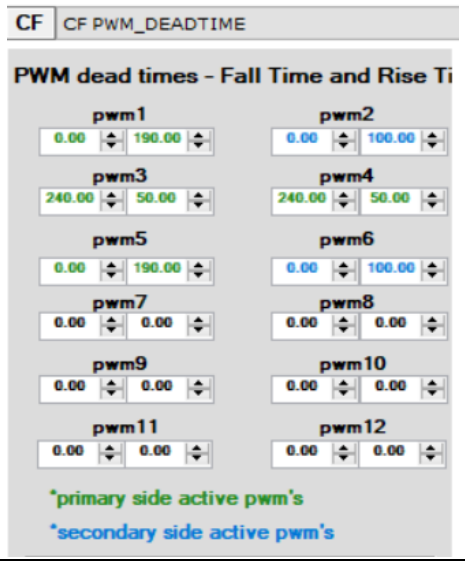


Figure 42 Dead time configuration

In the XDPP1100 GUI, the active primary and secondary PWMs of this loop will be highlighted in green and blue, respectively. Writing inactive PWMs is not allowed in the GUI to prevent accidental setting of the dead time of the other loop.

7.2 Configuring the patched MFR command

Make sure the XDPP1100 has the buck-boost FW patch before configuring the patched MFR command. If there is no active patch in the device, use the XDPP1100 GUI FW patch tool to load the FW patch and save the patch to OTP or to RAM.

7.2.1 Loading the PMBus spreadsheet

To enable the configuration of the patched command, go to the “MFR Commands” tab in the PMBus configuration section and load the PMBus Excel file. Each FW patch project will have its own PMBus Excel file including the patched commands. In the Excel file, the patched PMBus command will have column F “MFR” labeled “y”, and column G “Loop 0 support” or column L “Loop 1 support” also labeled “y”. Click the “Load PMBus Spread sheet” button and open the PMBus Excel file that comes with the patch. The GUI will update the command list and the patched command can be configured through the Read/Write button.

Please note that if the patch is not stored in OTP or RAM, the MFR PMBus command will show an invalid message when performing a Read or Write. The patched PMBus commands are only valid with an active FW patch.

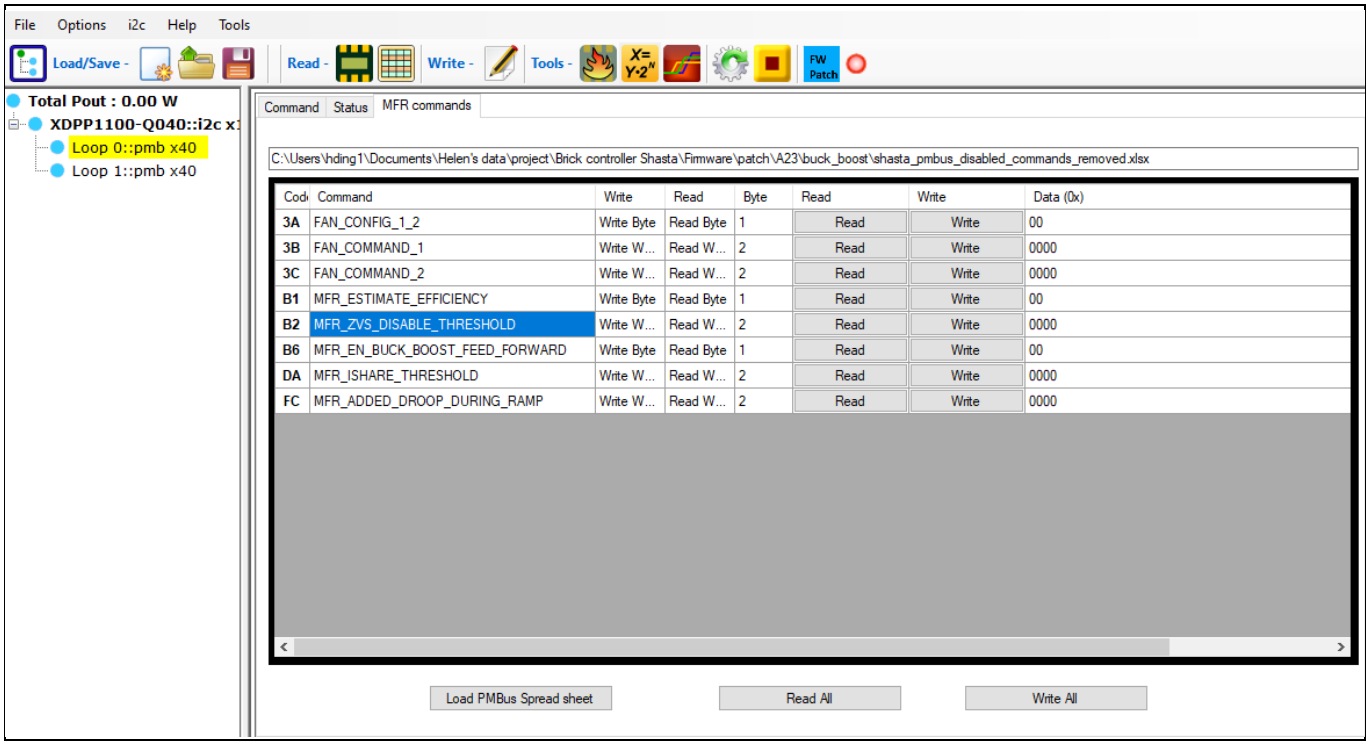


Figure 43 Patched MFR commands

Table 13 Buck-boost patched MFR commands

Command	Value	Comments
MFR_ZVS_DISABLE_THRESHOLD	E830	Sets the ZVS disable threshold to 6 A
MFR_EN_BUCK_BOOST_FEED_FORWARD	1	Enables the feed-forward feature for buck-boost topology

8 Definitions

Table 14 Definitions of acronyms, symbols and terms

Acronym, symbol or term	Definition
ADC	Analog-to-digital converter
BOM	Bill of materials
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
DE	Diode emulation
F_{SW}	Switching frequency of converter
FW	Firmware
GUI	Graphical user interface
HW	Hardware
LSB	Least significant bit
N_p	Number of turns of the transformer primary winding
N_s	Number of turns of the transformer secondary winding
NTC	Negative temperature coefficient
OCP	Overcurrent protection
OTP	One-time programmable memory
OTP	Overtemperature protection
OVP	Overvoltage protection
PA	Power amplifier
PCB	Printed circuit board
PCMC	Peak current mode control
PID	Proportional, integral, derivative coefficient
PSU	Power supply unit
PWM	Pulse width modulation
$R_{DS(on)}$	MOSFET on-state resistance
SCP	Short-circuit protection
SR	Synchronous rectification
T_{SW}	Switching period of converter
V_{IN}	Input voltage
VMC	Voltage mode control
V_{OUT}	Output voltage

[1] **XDPP1100 Datasheet**

[2] **XDPP1100 GUI Installation and User Guide**

Revision history

Document version	Date of release	Description of changes
V 1.0	2021-09-20	Initial release

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