Advantages of Infineon's high-voltage gate driver ICs (HVICs) based on its silicon-on-insulator (SOI) technology

About this document

Scope and purpose

Gate drivers are an important building block in any power conversion or motor control application. They enable a micro-controller or digital signal processor (DSP) to efficiently turn on and turn off a semiconductor switch such as an IGBT or a MOSFET. High-voltage integrated-circuit (HVIC) based gate drivers are popular due to their simplicity in driving a half bridge stage, and have been used in power supplies and motor drives for a long time. International Rectifier (IR) was the leading manufacturer of HVIC gate drivers based on junction isolation technology since the late 90's. With the acquisition of IR in 2015, Infineon Technologies has worked on improving some key aspects of HVIC gate drivers by moving them to Infineon's silicon-on-insulator (SOI) technology. Most popular IR gate drivers such as IR(S)2106, IR(S)2108, IR(S)2109, IR(S)21091, IR(S)2181, IR(S)2183 and IR(S)2184 family are part of the initial transfer to the SOI technology-based family of low current (+ 290 mA/- 700 mA) gate drivers 2ED2106, 2ED2108, 2ED2109, 2ED21091 and to the family of high current (+ 2.5 A / - 2.5 A) gate drivers 2ED2181, 2ED2182, 2ED2183, 2ED2184 from Infineon. It will increase the already existing portfolio of SOI-based gate drivers including 2ED2304S06F, 2EDL05N06, 6EDL04N02PR, 2EDL23N06, 6EDL04N06. This application note details the benefits of Infineon's SOI technology and the improvement it provides to HVIC gate drivers which in turn benefit designers working on power conversion and motor control applications.

Intended audience

Motor control and power supply designers who work on major home appliances, battery-powered systems, electric vehicles, industrial power supplies and similar applications.

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1 Introduction

A simple and cost-effective way to drive a MOSFET or IGBT in a half-bridge or high-side configuration is to use a gate drive transformer as shown in Figure 1. For this basic configuration to provide an optimal gate drive, and enable operation over wide duty cycles, additional circuitry is required as well as design expertise for the complex calculations. Significant parasitics create less than ideal operation with fast switching waveforms imposing a well controlled design and manufacturing of the gate drive transformer itself.

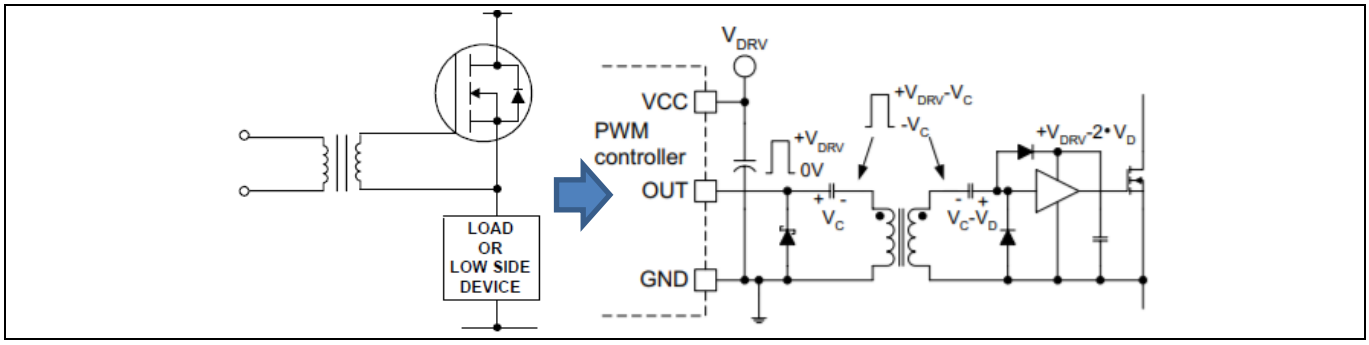


Figure 1 Basic transformer coupled gate drive and its equivalent for optimal gate drive

There are other techniques such as optocoupled floating gate drives which overcome some of the problems associated with the gate drive transformer. This technique needs a separate floating or isolated power supply adding cost, and it inherits the drawbacks of optocouplers such as noise sensitivity and low bandwidth.

During the 1990s, International Rectifier introduced the now widely popular bootstrap-based high-voltage IC (HVIC)-based gate drivers. These ICs are simple, inexpensive and come with an integrated level-shift technology which facilitated the designer's job to drive a half-bridge or high-side MOSFET with ease.

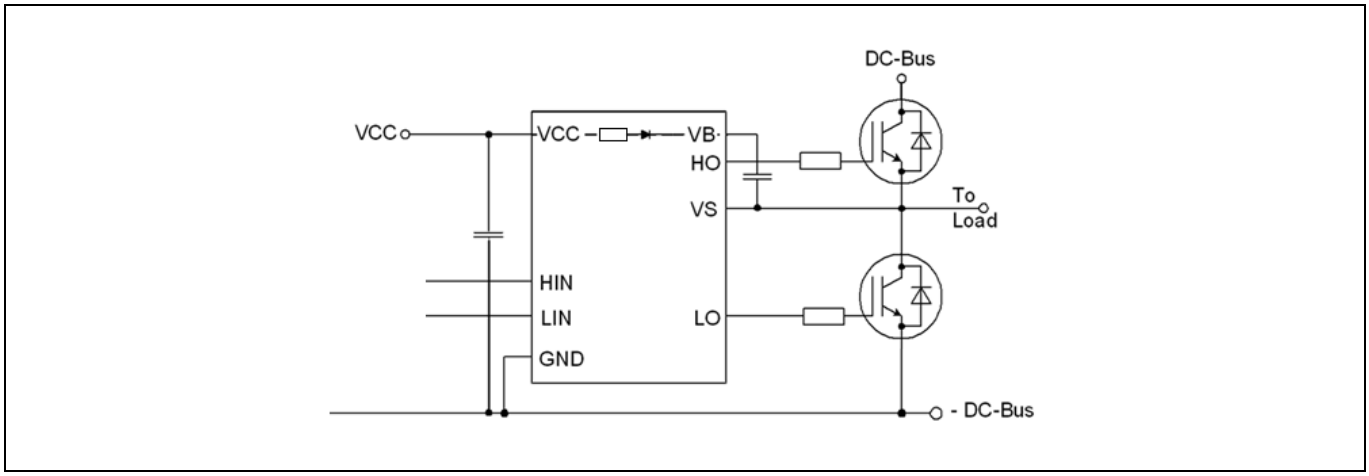


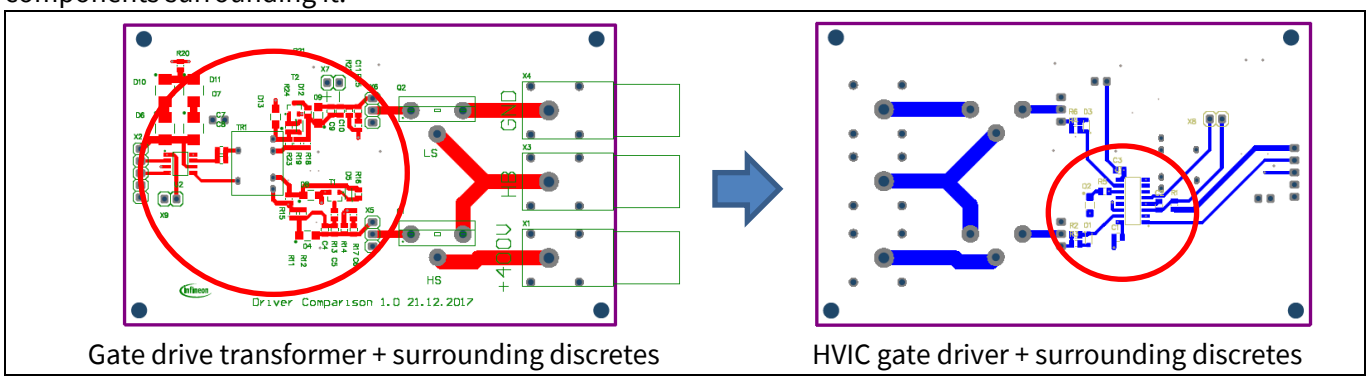
Figure 2 A typical HVIC half-bridge gate driver

Table 1 provides a summary of the comparison between HVIC and gate drive transformer approach.

Table 1

Parameters	HVIC	Gate drive transformer
Ease of design	Yes. Most features implemented inside the IC	No, every feature needs to be designed separately with external components
Noise sensitivity	Low, based on optimal PCB layout	Low
High sink current	Yes. Built-in	Needs separate turn-off circuitry
Magnetic core saturation	Not applicable	Yes. Volt-sec balance of the transformer must be met
Leakage inductance effects	Not applicable	Yes. Transformer construction must be optimal
Isolation lifetime	Not applicable	Varies based on materials used
Ease of layout	Yes. Low components	No. Many discrete components
PCB area including number of layers	Low	High
Assembly type	Pick 'n place	Manual
Component height	Low (~2.5 mm)	High (~15 mm)
Cost (including surrounding discretes)	Low	High

A simple comparison of PCB layout between the two approaches is provided in Figure 3 below. It clearly shows that the HVIC-based gate drive is simple, occupies less space and is more reliable considering the less number of components surrounding it.



Gate drive transformer + surrounding discretes | HVIC gate driver + surrounding discretes

Figure 3 PCB area comparison between transformer-based gate drive and its equivalent HVIC-based gate drive

With the HVIC solution, a high-side isolation of up to 1200 V is reached within the silicon. A matched propagation delay and shoot-through prevention logic between high side and low side drive prevents cross conduction leading to shoot-through failures. The negative voltage robustness of these parts is key to survive negative transients due to the half-bridge operation. The application notes [3] to [7] mentioned in the References section at the end of this document help in understanding the working of the HVIC.

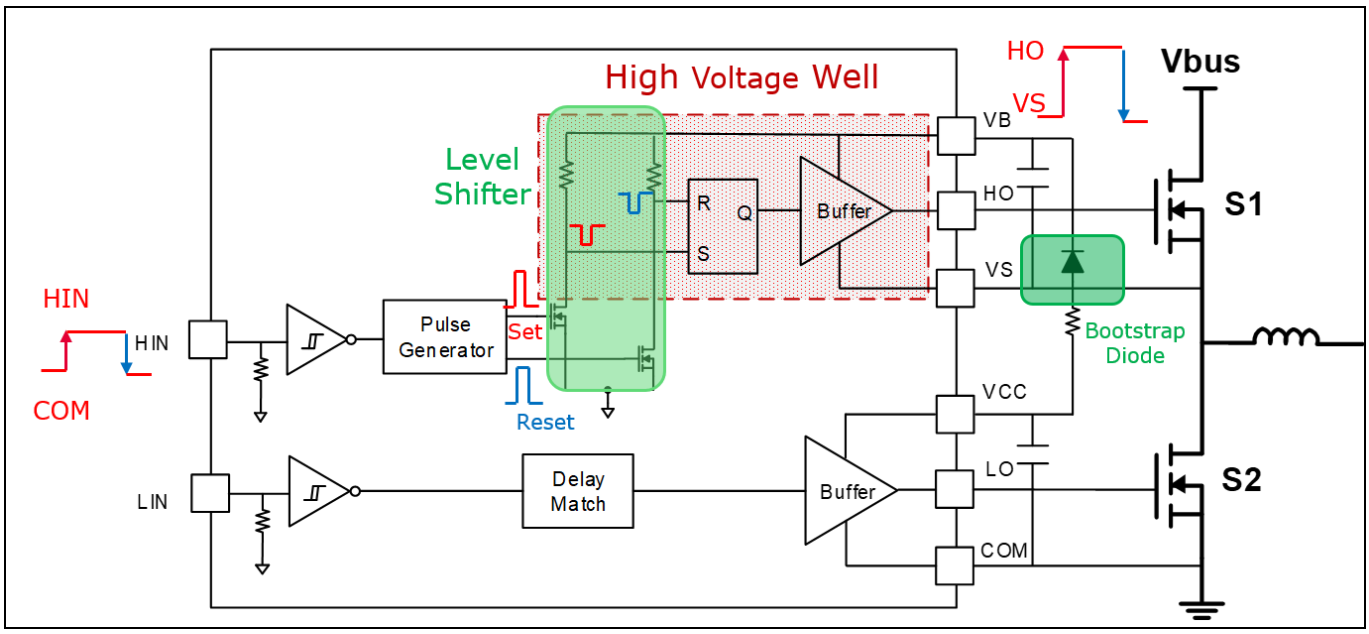


Figure 4 Functional block diagram of a HVIC half-bridge gate driver

To summarize, looking at Figure 4, a pulse generator generates set and reset pulse on each edge from HIN input. The level shifter shifts these GND-referenced pulses to VS node-referenced pulses. A Set-Reset flip flop latches the pulse information from the level shifter to provide a clean, error-free pulse to the pre-driver stage. To compensate the delays involved in pulse transfer, level shifter and SR flip flop stages, a delay match block is added to the low-side driver. It is good to note that the HVIC does not need a secondary isolated power supply for high side. The bootstrap configuration supplies the required power to the high-side stage.

2 Advantages of Infineon's SOI technology

Infineon's silicon-on-insulator (SOI) technology is well-established and has proven benefits in HVIC gate driver. The application notes [8] to [10] mentioned in the References section at the end of this document help in understanding the basic SOI structure, its benefits and unique advantages of Infineon's SOI.

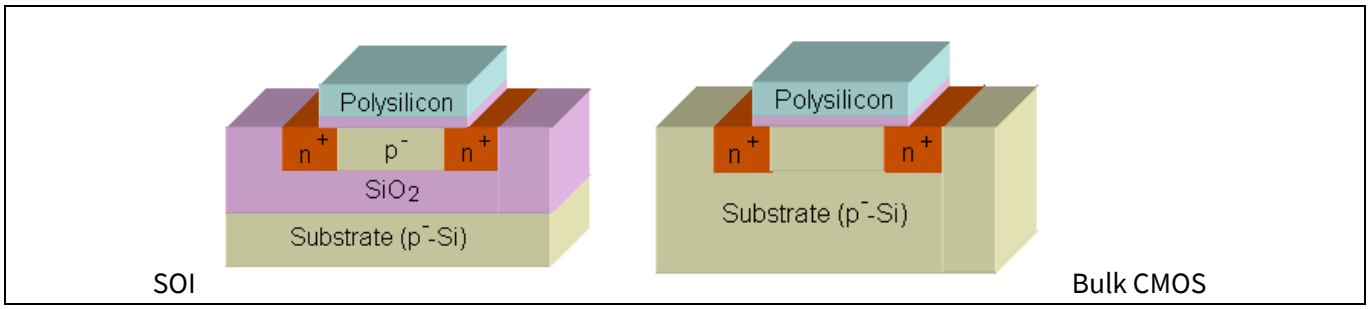


Figure 5 Basic silicon-on-insulator structure (on left) as compared to bulk CMOS structure (on right)

As seen in left of Figure 5, with Infineon's SOI structure there is no latch-up possible because of the dielectric isolation to all sides of the current path of all sections. The leakage current is also very low. Since there is no isolation of the substrate in the bulk CMOS structure to the right of Figure 5, latch-up can occur through the bottom of the device.

Infineon's SOI has superior negative VS transient immunity (up to -100 V for 300 ns) to prevent latch-up. The common mode transient immunity (CMTI) is typically 50 V/ns and a PN-based bootstrap diode (typically 40 Ω) with fast recovery is integrated to charge the bootstrap capacitor.

The main benefits of Infineon's SOI technology is summarized in Figure 6. Each of these benefits is explained in detail in the subsequent sections of this application note.

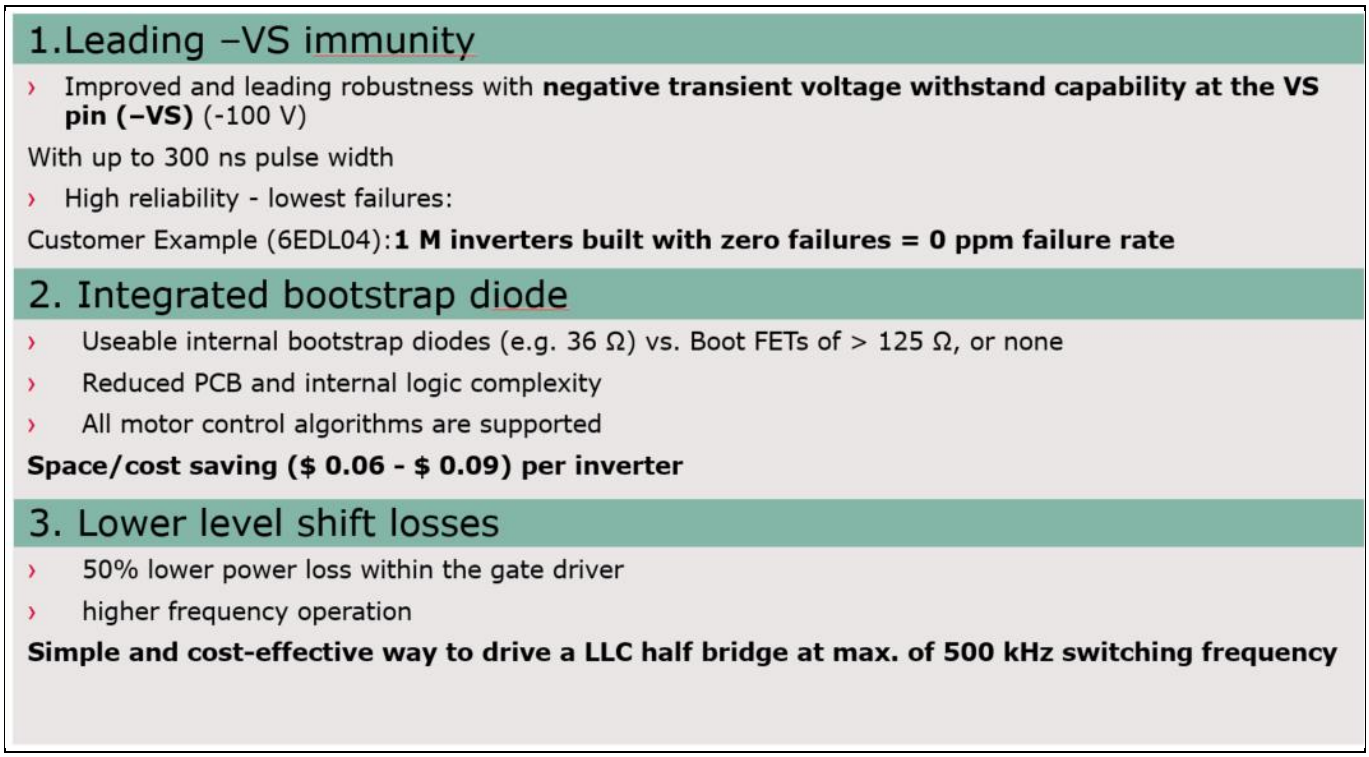


Figure 6 Summary of three key benefits of Infineon's SOI technology

3 Industry's leading, most reliable and robust negative voltage -VS transient protection

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical three-phase inverter circuit is shown in Figure 7; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 8 and 9) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1} swings from the positive DC bus voltage to the negative DC bus voltage.

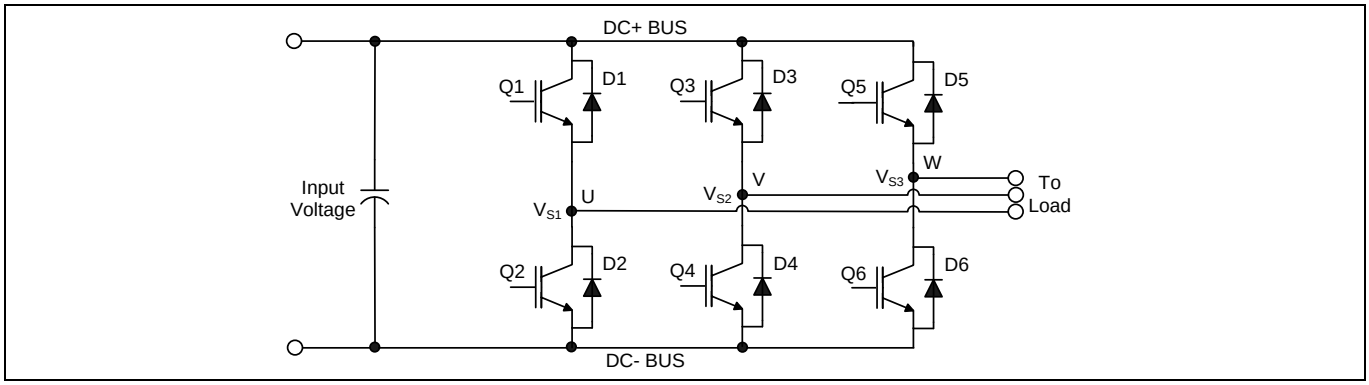


Figure 7 Three-phase inverter

Also when the V phase current flows from the inductive load back to the inverter (see Figure 8), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node V_{S2} swings from the positive DC bus voltage to the negative DC bus voltage.

However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called negative V_S transient.

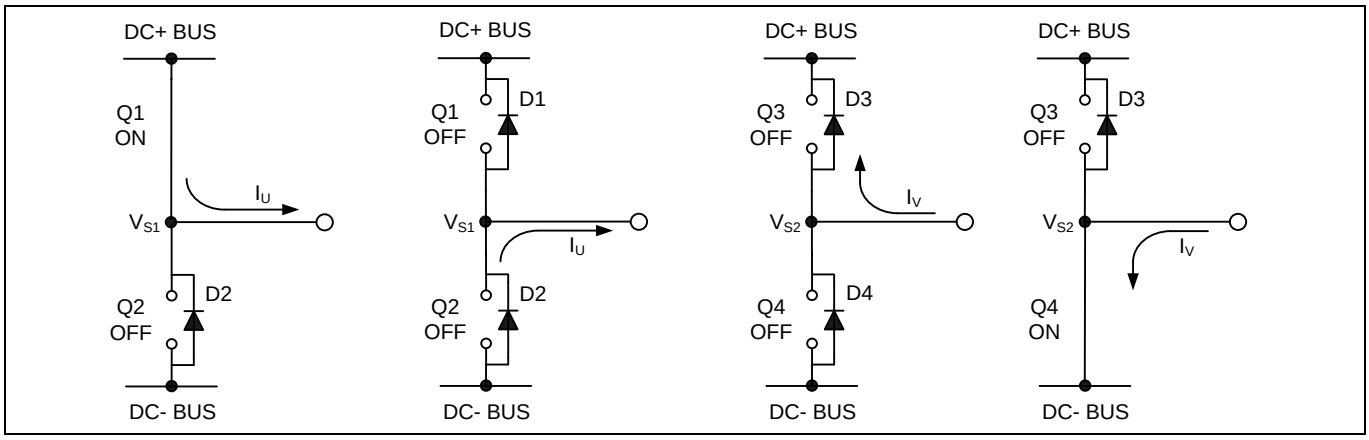


Figure 8 Switching cycle of the three-phase inverter

The circuit shown in Figure 9 depicts one leg of the three-phase inverter; Figure 9 shows a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage including the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side

freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC bus (which is connected to the COM pin of the HVIC) to the load, and a negative voltage between V_{S1} and the DC bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

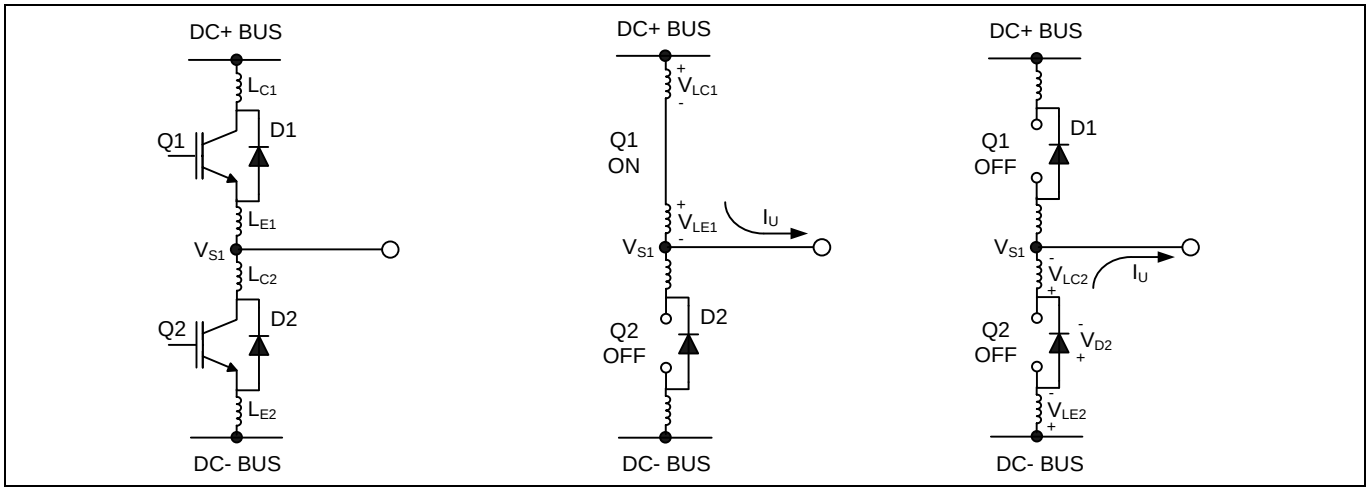


Figure 9 Negative voltage – VS transient generation

To check the performance of the new SOI-based gate drivers, the typical test setup used in the system verification lab at Infineon is shown in Figure 10. The characteristic –VS waveform is also shown next to the schematics.

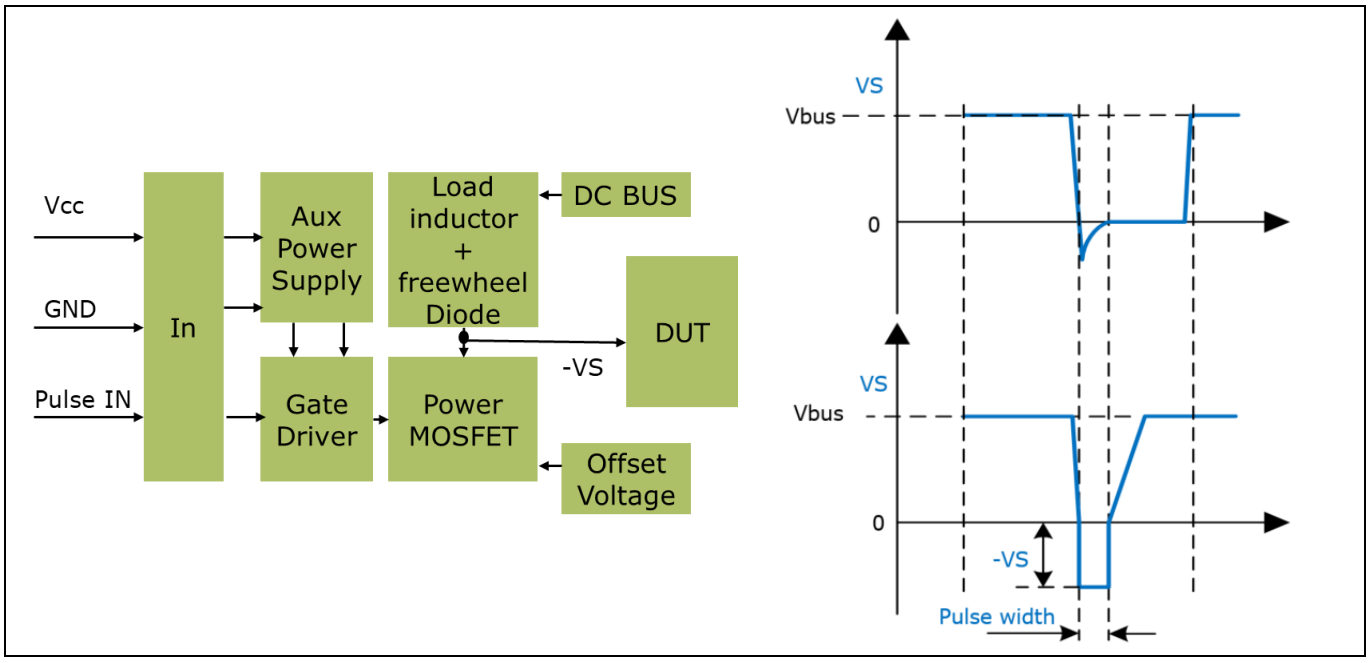


Figure 10 Basic block diagram of –VS testing setup

The pulse generator provides the pulse, whose width (of VS voltage) can be changed from 100 ns to 1 us. With the BUS voltage of IC under test at 400 V, different VS offset voltages are applied. Example: with pulse width of 100 ns and VS offset = –50 V, the I_{Vcc} and waveform of HO/LO are monitored. If I_{VCC} does not increase and no HO/LO triggering from "LOW" / "HIGH" to "HIGH" / "LOW" is seen, the IC is considered robust for that VS offset voltage and pulse width. On further increasing minus VS or pulse width or both, if I_{Vcc} increases or HO/LO triggers from "LOW" / "HIGH" to "HIGH" / "LOW", the device under test has failed. This test is repeated for multiple devices from different production lots, and a safe operating area with maximum VS and pulse width limits is obtained.

After complete system verification in the lab for each family of SOI gate drivers, the negative transient SOA (NTSOA) curve is plotted and provided in the device datasheets. A typical NTSOA curve is shown in Figure 11.

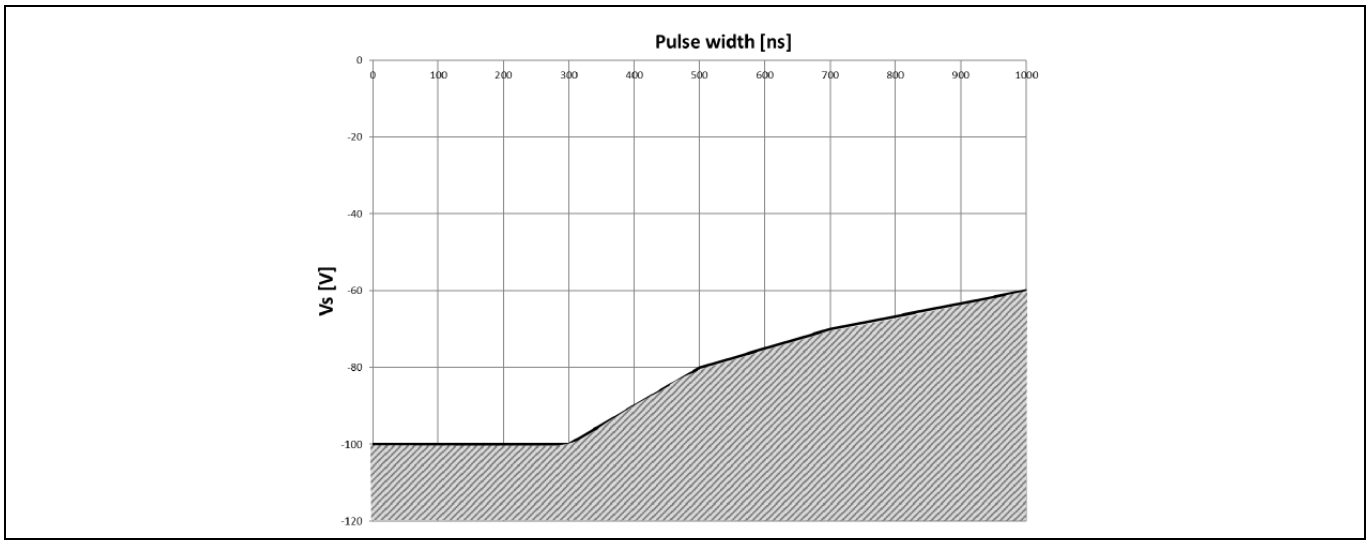


Figure 11 Example of a negative transient safe operating area (NTSOA) graph shown in all SOI-based gate driver device datasheets

Although Infineon SOI-based high voltage gate driver ICs are able to handle negative VS transients of varying duration and amplitude, it is still highly recommended that the circuit designer always limits the negative VS transients as much as possible using careful PCB layout and component selection.

Power-stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase-voltage negative transients. In order to avoid such conditions, it is recommended to:

1) Minimize the high-side emitter to low-side collector distance, and

2) Minimize the low-side emitter to negative bus rail stray inductance.

However, if negative VS spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the VS pin and the switch node (see Figure 12a), and in some cases using a clamping diode between COM and V_S (see Figure 12b).

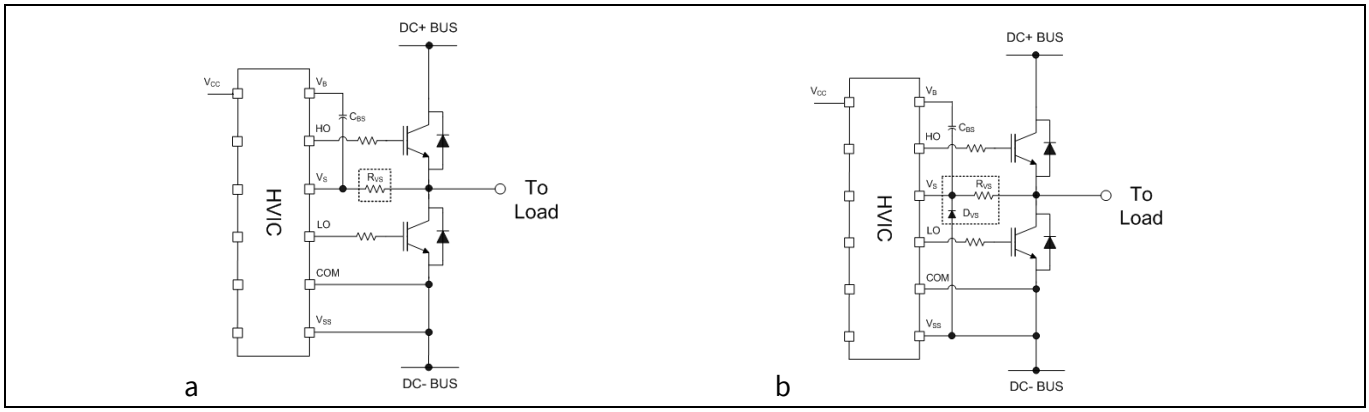


Figure 12 V_S resistor and clamping diode

4 Integrated bootstrap diode in SOI-based HVIC gate drivers

For a HVIC, the power for high-side internal circuitry and drive is provided by a low-cost technique commonly known as bootstrapping. This method has the advantage of being simple, but may force some limitations on duty cycle and on-time, since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.

Typical components of a bootstrap power supply are shown in Figure 13. The bootstrap diode should be a fast recovery diode (typical trr < 100 ns) and have a voltage rating higher than the bus voltage. Bootstrap resistor R_{boot} is typically of low ohmic value (< 50 Ω) and is used to limit the initial charging current of the bootstrap capacitor. C_{boot}, the bootstrap charging capacitor charges when the low-side switch is ON and the high-side switch is OFF. It discharges when the low-side switch is OFF and the high side switch is ON. It should be large enough to hold the voltage above the undervoltage lockout threshold of the high-side circuitry (VBS > Vbs_UVLO-). The calculation of the bootstrap capacitor is explained in the respective device datasheet and is also available in the online tool on Infineon's website.

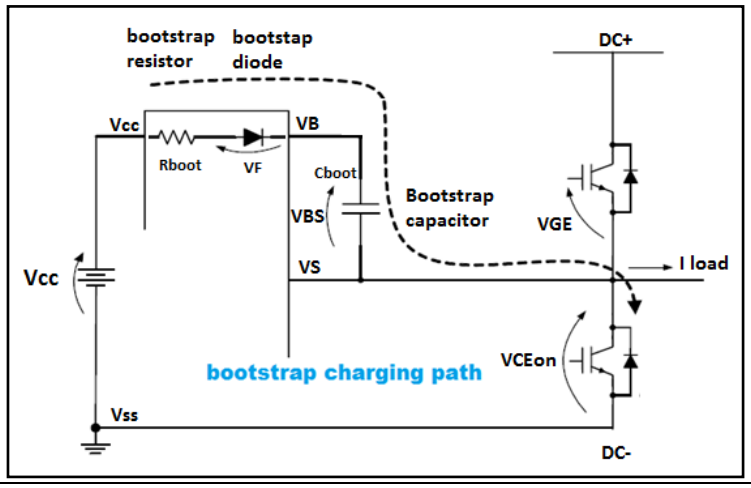


Figure 13 Bootstrap power supply components

The new SOI family of parts have the bootstrap diode and resistor monolithically integrated as shown in Figure 14. This saves cost to customers with a reduction in bill of material and precious PCB board area, especially in three-phase designs.

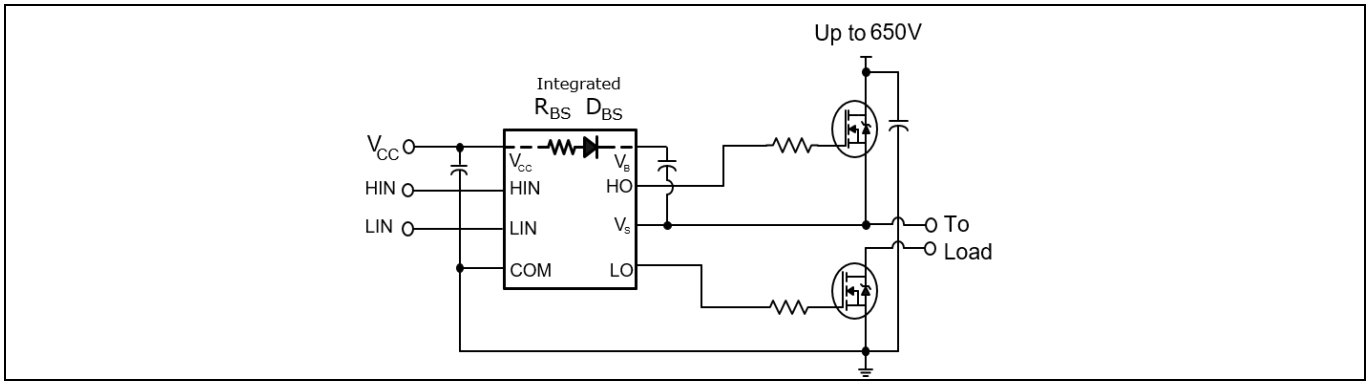


Figure 14 Bootstrap diode is monolithically integrated

The integrated diode is an ultra-fast bootstrap diode along with a resistor (different resistor value for different gate drivers) which helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The resistor value is 25 Ω for the 2ED218x family. The low ohmic current limiting resistor provides essential

advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 2ED218x family allows faster recharching of the bootstrap capacitor during periods of small duty cycles on the low-aside transistor.

The bootstrap diode is usable for all types of power electronic converters. The bootstrap diode is a real pn diode and is temperature-robust. It can be used at high temperatures with a low duty cycle of the low-side transistor. The bootstrap diode of the 2ED218x family works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal motor drives control. The typical recovery response (< 50 ns) of the integrated diode is shown in Figure 15.

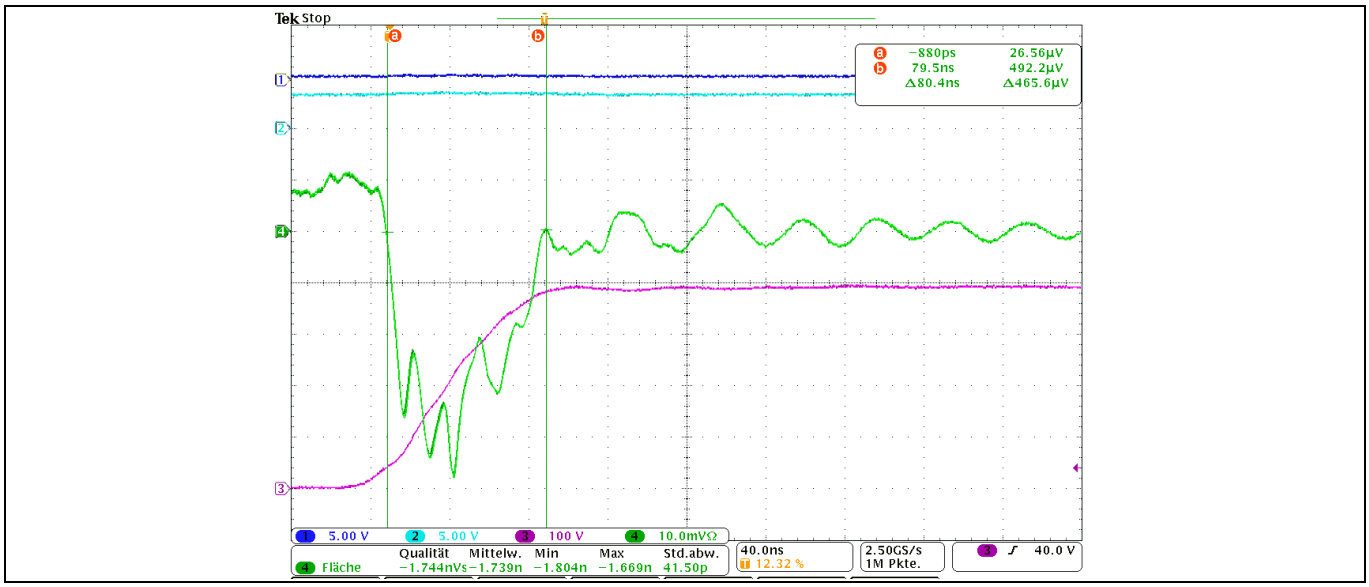


Figure 15 Less than 50 ns fast recovery response of integrated bootstrap diode

5 Lower switching losses enabling high-frequency operation

The power dissipated by the driver IC is a combination of several sources. All these sources are listed in Figure 16.

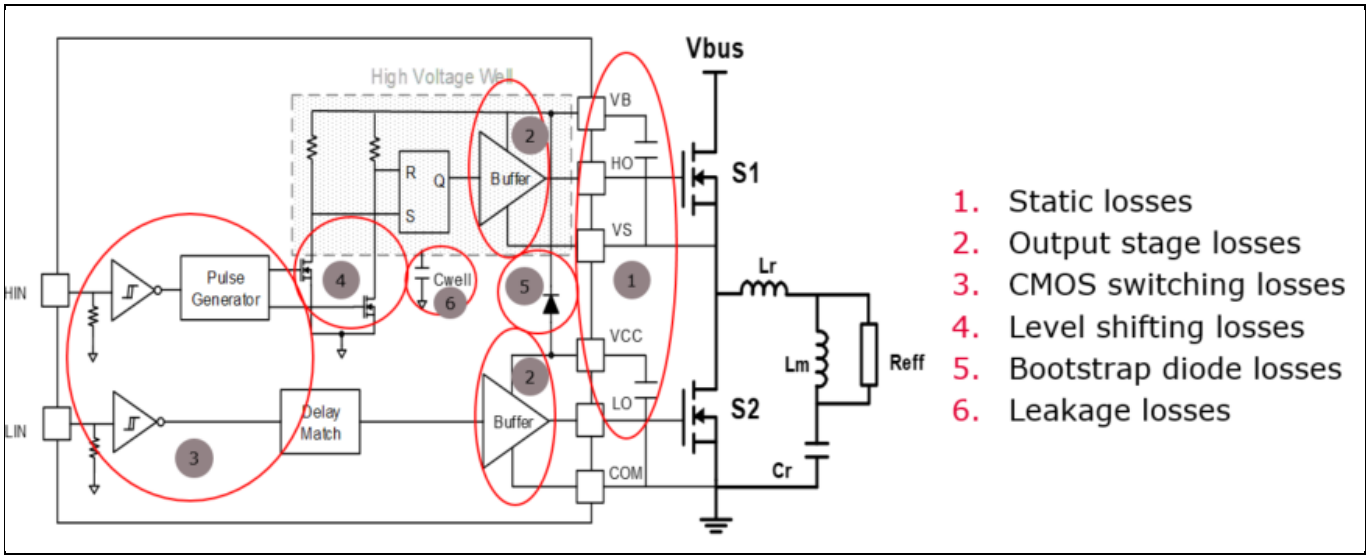


Figure 16 Different power losses within the HVIC gate driver

The output stage is the major contributor for the power dissipation of the gate driver IC. The external gate resistors also contribute to the power disspation of the gate driver IC. The bigger the external gate resistor, the smaller the power dissipation in the gate driver. Within the gate driver IC, the different losses include:

1. Static losses: are calculated at given supply voltage and quiescent / bootstrap charging currents.

Static losses in the low side = V_{cc} x I_{Qcc}
Static losses in the high side = V_{cc} x I_{QBS}
Static losses at input stage = ½* V_{cc} x V_{cc} / R_{pullup}

2. **Output stage losses:** are calculated by means of the total gate charge of the power MOSFET or IGBT. It drives Q_{gtot}, the supply voltage V_{CC}, the switching frequency f_P, and the external gate resistor R_{gon} and R_{goff}. Different cases for turn-on and turn-off must be considered, because many designs use different resistors for turn-on and turn-off. This leads to a specific distribution of losses in respect to the external gate resistor $R_{gon/off}$, ext and the internal resistances (R_{on_int} and R_{off_int}) of the output section.

Turn on losses: $Pdon = \frac{2}{2} \times Q_{gtot} \times V_{cc} \times f_p \times \frac{Ron\_int}{Ron\_int+Rgon\_ext}$

Turn off losses: $Pdoff = \frac{2}{2} \times Q_{gtot} \times V_{cc} \times f_p \times \frac{Roff\_int}{Roff\_int+Rgoff\_ext}$

3. **CMOS losses**: are calculated at given switching frequency and supply voltages.

CMOS losses = Q_{COMS} x V_{CC} x fp

Junction capacitance switching losses = 0.5 x CJ x V_{bus}^2 x f

4. **Level shift losses**: are calculated at given switching frequency and supply voltages.

Loss per level shifter (ON) = (V_{bus}+V_{cc}) x I_{LSON} x t_{ON} x fp

Loss per level shifter (ON) = (V_{bus}+V_{cc}) x I_{LSOFF} x t_{OFF} x fp

5. **Bootstrap diode losses**: are calculated at given switching frequency and supply voltages.

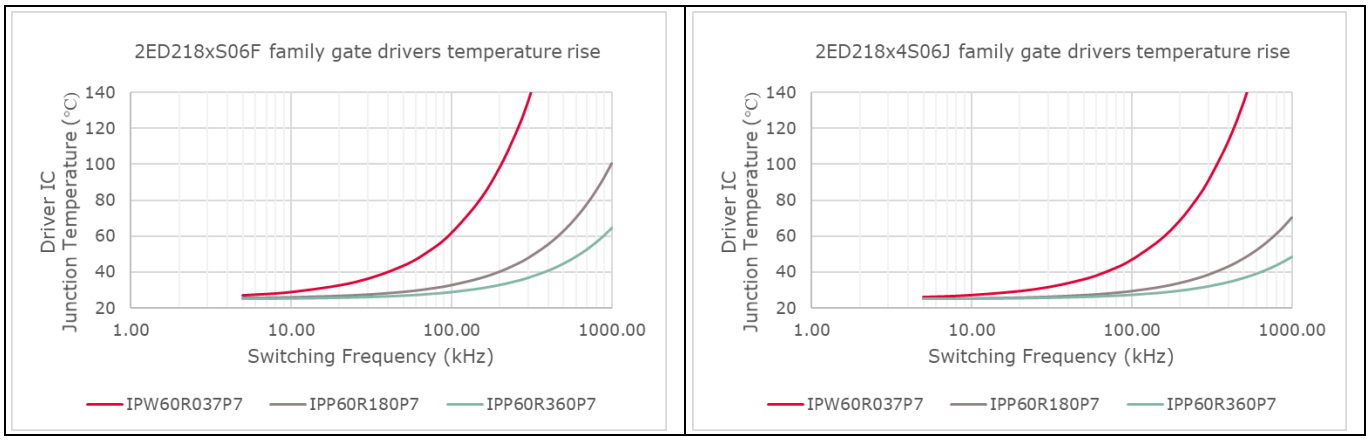
Dynamic losses in boot diode = EB x fp x 2 x [I_{QBS}+ (Q_{gtot}*fp)] / 10E-3 x Vbus /400

Static losses in boot diode = 0.5 x (V_{TH}+ 2 x [I_{QBS}+ (Q_{gtot}*fp)] x R_D) x 2 x [I_{QBS}+ (Q_{gtot}*fp)]

6. **Leakage losses**: are calculated at given switching frequency and supply voltages.

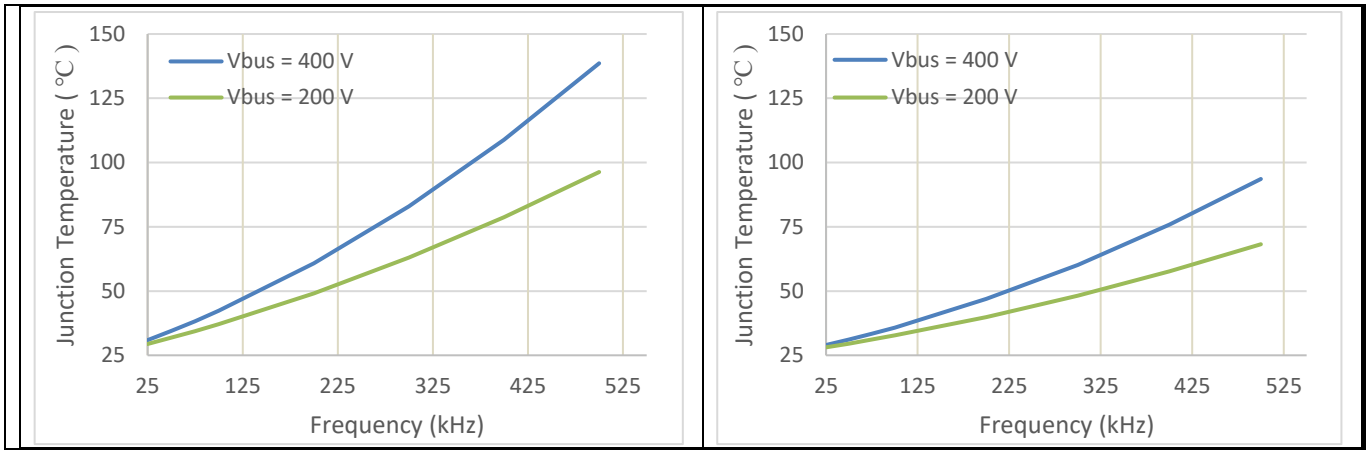
Leakage loss = I_{LEAK} x V_{bus}

All these losses within the gate driver IC are added together producing the results below, which estimate the gate driver IC temperature rise when switching a given MOSFET or IGBT at different switching frequencies.



*Assumptions for above curves: T_a = 25 °C, V_{BUS} = 400 V, V_{CC} = 12 V, R_{gon} = 10 Ω, R_{goff} = 1 Ω

Figure 17 2ED2182 Maximum switching frequencies for different CoolMOS™ P7 MOSFETs



*Assumptions for above curves: LLC topology, power switch = IPP60R600P6, T_a = 25 °C, V_{BUS} = 400 V, V_{CC} = 12 V, R_{gon} = 3.9 Ω, R_{goff} = 1 Ω

Figure 18 2ED2108 Maximum switching frequencies for different bus voltages for given CoolMOS™

Lower switching losses enabling high-frequency operation

The 2ED218x and 2ED210x families are capable of switching at higher frequencies as compared to standard half-bridge or high side / low side gate drivers. They are available in two packages, the PG-DSO-8 and the PG-DSO-14. It is essential to ensure that the component is not thermally overloaded when operating at higher frequencies. This can be checked by means of the thermal resistance junction-to-ambient, and the calculation or measurement of the dissipated power. The thermal resistance is given in the datasheet (section 4) and refers to a specific layout. Changes of this layout may lead to an increased thermal resistance, which will reduce the total dissipated power of the driver IC. One should therefore do temperature measurements in order to avoid thermal overload under application-relevant conditions of ambient temperature and housing.

The maximum chip temperature T_J can be calculated with

$T_J = \mathrm{Pd} \cdot Rth_{JA} + T_{A\_max}$, where T_{A_max} is the maximum ambient temperature.

Below Figure 19 shows the impact of lower power dissipation while switching at high switching frequencies. A comparison of Infineon's new SOI technology vs. legacy bulk CMOS-based gate drivers shows the lower losses in SOI-based gate driver leading to high-frequency switching capability.

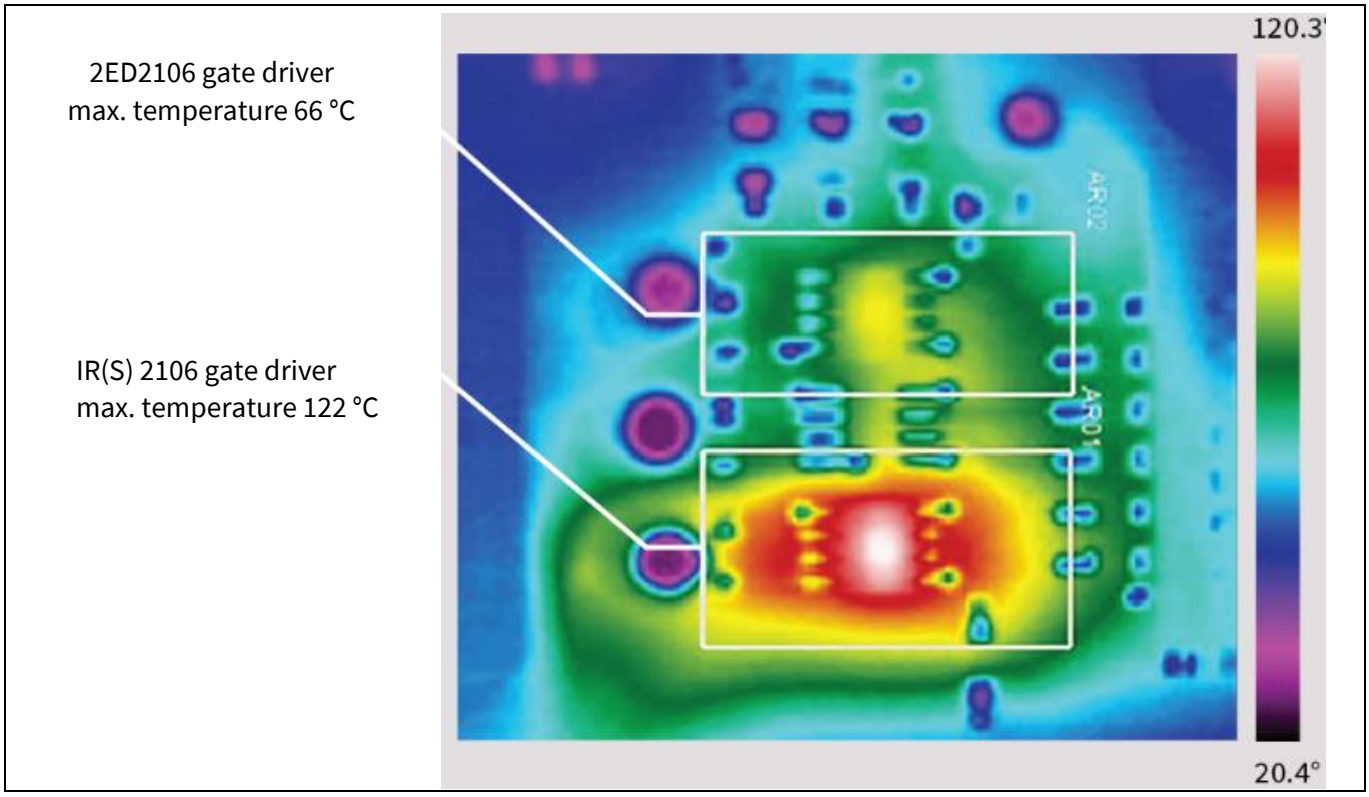


Figure 19 2ED218x gate driver is operating at almost half the temperature of IR(S) 218x while switching at 300 kHz

6 Programmable dead time in 2ED21xxxJ (14-pin variants only)

14-pin, half-bridge, SOI-based gate driver variants provide greater design flexibility with a programmable dead-time feature. This inserts a time period (a minimum dead time), in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT; external dead times larger than DT are not modified by the gate driver.

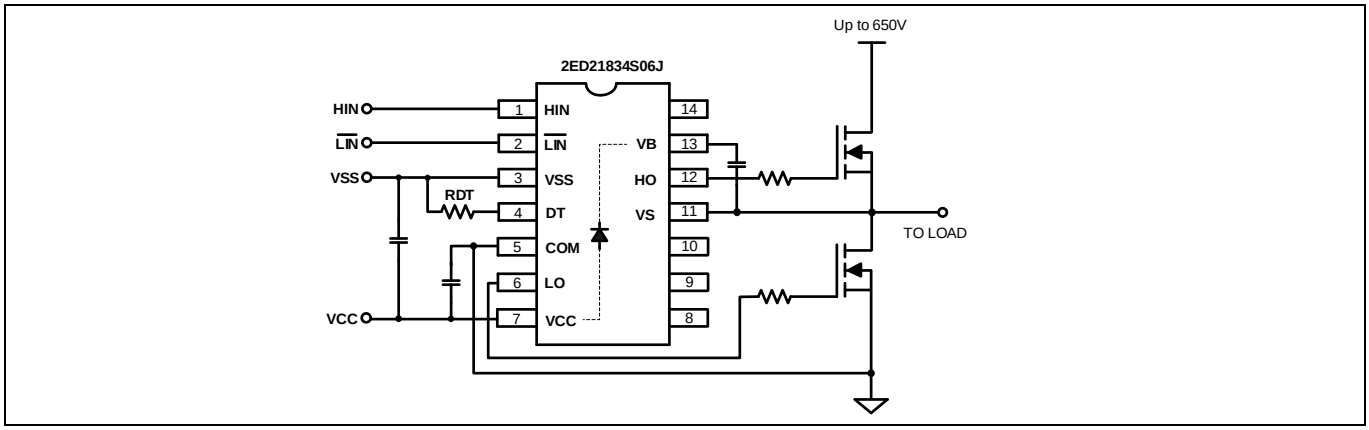


Figure 20 14-pin half-bridge variants having adjustable dead-time feature settable with a resistor

Figure 21 shows the linear relationship between the resistor (RDT) and dead time. Based on the end application, designers can choose to add the external resistor to increase the dead time.

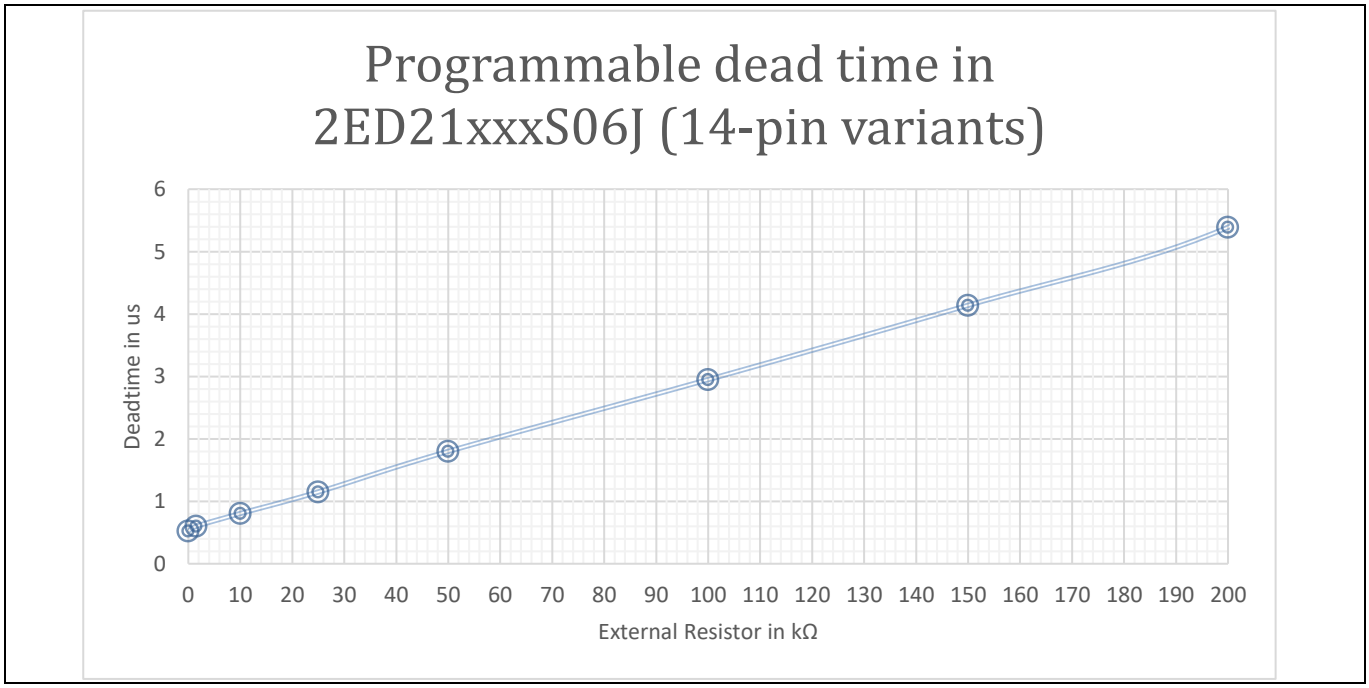


Figure 21 Variation of dead time vs. external resistor

7 Pin-to-pin compatibility with legacy IR gate drivers

As mentioned at the beginning of this application note, International Rectifier (IR) was the pioneer in HVIC gate drivers during the 1990's. IR HVIC gate drivers were used across motor control and power conversion applications owing to the simple, robust and cost-effective designs they enabled. From major home applicances such as refrigerators and washing machines to battery powered systems such as power tools, all use IR HVIC gate drivers.

With the benefits of Infineon's silicon-on-insulator (SOI) technology explained in the prior sections, it makes sense to improve the most popular IR HVIC gate driver designs and move them on to SOI. IR gate drivers such as IR(S)2108, IR(S)2109, IR(S)21091, IR(S)2106, IR(S)2181, IR(S)2183 and IR(S)2184 family are now moved to SOI-technology based 2ED2106, 2ED2108, 2ED2109, 2ED21091,2ED2181, 2ED2182, 2ED2183, 2ED2184 family of gate drivers from Infineon. All three variants will co-exisit, and it is up to the customer to choose the optimal technology based on the application needs. 2ED2182 is a new variant that does not have a backward compatible IR(S) 2182. Also, 2ED21091 has different logic for deadtime / shutdown feature as compared to IR(S) 21091

Legacy IR parts starting with IR2x or IRS2x provide robust and cost-effective solutions to motor control applications operating at low switching frequencies of 25 kHz and below. Infineon SOI-based HVIC gate drivers starting with 2ED2x nomenclature provide efficient and cost-effective solutions to power conversion applications operating at high switching frequencies of 100 kHz to 500 kHz.

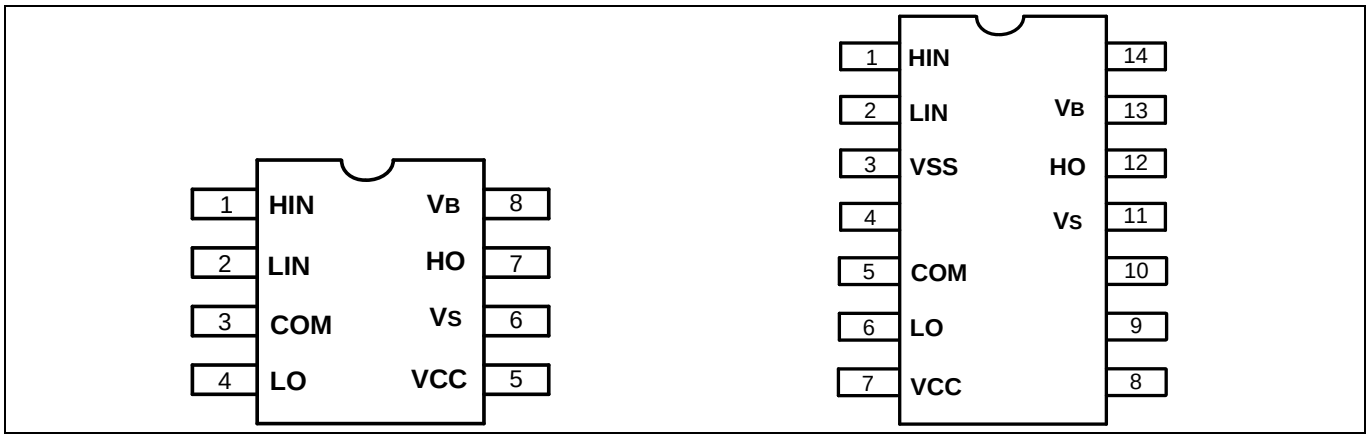


Figure 22 Example of 2ED2181 shown above has same pin-out as IR2181, IRS2181. There is same pin-out between IR218x, IRS218x and 2ED218x equivalent devices.

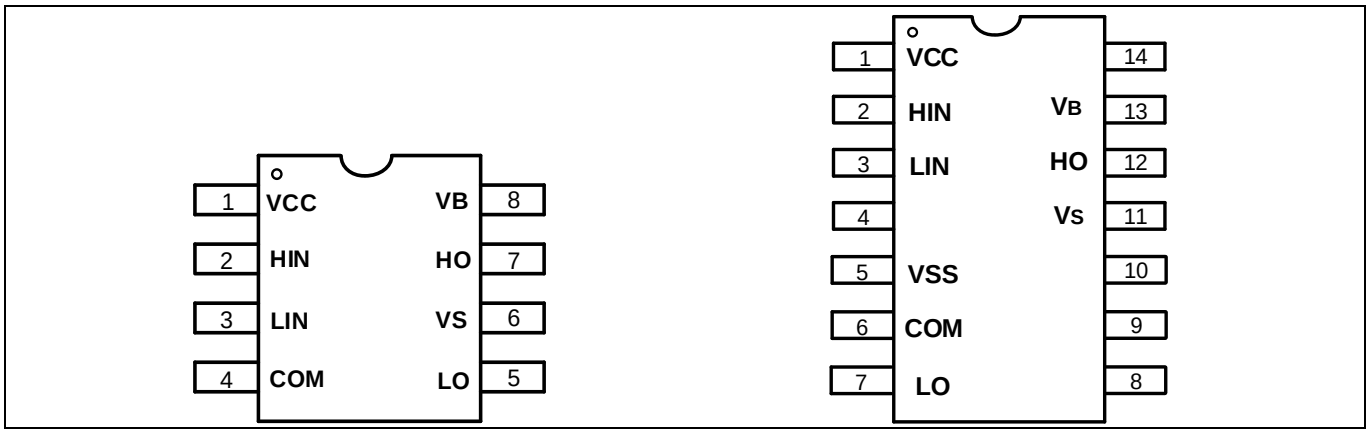


Figure 23 Example of 2ED2106 shown above has same pin-out as IR2106 / IRS2106. There is same pin-out between IR210x, IRS210x and 2ED210x equivalent devices

Summary of the product family moved to SOI technology

Table 2 Infineons's SOI-based high-current family of HVIC gate drivers

Part no.	Package	Drive current source / sink	Input logic	Cross conduction prevention logic	Dead time	Ground pins	t_{ON} / t_{OFF}
2ED2181S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, LIN	No	None	COM	200 ns
2ED21814S06J	DSO – 14	+ 2.5 A / - 2.5 A				VSS / COM	
2ED2182S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, LIN	Yes	Internal 400 ns	COM	
2ED21824S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	
2ED2183S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, $\overline{LIN}$	Yes	Internal 400 ns	COM	
2ED21834S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	
2ED2184S06F	DSO – 8	+ 2.5 A / - 2.5 A	IN, $\overline{SD}$	Yes	Internal 400 ns	COM	
2ED21844S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	

Table 3 Infineons's SOI based high current family of HVIC gate drivers

Part no.	Package	Drive current source / sink	Input logic	Cross conduction prevention logic	Dead time	Ground pins	t_{ON} / t_{OFF}
2ED2106S06F	DSO – 8	+ 290 mA / - 700 mA	HIN, LIN	No	None	COM	200 ns
2ED21064S06J	DSO – 14	+ 290 mA / - 700 mA				VSS / COM	
2ED2108S06F	DSO – 8	+ 290 mA / - 700 mA	HIN, $\overline{LIN}$	Yes	Internal 540 ns	COM	
2ED21084S06J	DSO – 14	+ 290 mA / - 700 mA			Programmable 540 ns - 5000 ns	VSS / COM	
2ED2109S06F	DSO – 8	+ 290 mA / - 700 mA	IN, $\overline{SD}$	Yes	Internal 540 ns	COM	
2ED21094S06J	DSO – 14	+ 290 mA / - 700 mA			Programmable 540 ns - 5000 ns	VSS / COM	
2ED21091S06F	DSO – 8	+ 290 mA / - 700 mA	IN, DT / SD	Yes	Internal 540 ns	COM	

Hence, customers now have a wide selection of high current and low current, 650 V gate-driver options with different input logic capability to make their power conversion and motor control designs simple, cost-effective, rugged and reliable.

8 Summary of benefits of SOI-based HVIC gate drivers

The basics of HVIC gate driver working and silicon-on-insulator (SOI) technology were covered at the beginning of this application note. It was followed by detailed explanations of the benefits of Infineons's SOI-based technology high-voltage gate drivers to customers. They are summarized as shown in Table 4 below.

Table 4

Features of Infineon's high voltage level-shift gate drivers based on SOI technology	Benefits to customers in different applications
Highest negative VS (- VS) Robustness	Provides best reliability in any application and hence lower field failures leading to lower maintenance costs
Integrated bootstrap diode	Reduction in external component count leading to lower bill of material (BOM), higher reliability and lower production costs
Lower level shift losses	Ability to switch at higher switching frequencies with low temperature rise on the gate driver IC leading to cheaper gate drive option for driving half bridges in LLC or similar topologies
Additional integrated functions	Faster or redundant system level protection providing reduction in external component count leading to lower BOM, higher reliability and lower production costs
Pin-to-pin compatibility with popular junction isolation parts from International Rectifier (IR)	Drop in replacement of gate drivers in existing designs, which bring additional benefits as above to the overall design

A summary of the pin-to-pin equivalents between legacy IR gate drivers and Infineon's new SOI gate drivers are shown in Figure 24. The benefits of SOI technology as discussed throughout this application note are also summarized.

SOI sales part number	Equivalent IR21xxSPBF / IR21xx4SPBF or IRS21xxSPBF / IRS21xx4SPBF		SOI vs. JI advantages Notes / comments
2ED2182S06F 2ED21824S06J	New SOI only Gate Driver No Equivalent IR or IRS versions		Same footprint, form, and electrical characteristics as IR(S)2183(4)SPBF but with HIN, LIN inputs
2ED2181S06F	IR2181SPBF	IRS2181SPBF	• pin to pin footprint, form, fit, functionally and electrically compatible with IR and IRS series of drivers • SOI vs. JI gate driver advantages • VS node breakdown voltage = **650V** vs. 600V • VB node breakdown voltage = **675V** vs. 625V • Integrated bootstrap diode for **reduced BOM cost** • Industry's **Best in Class negative VS transient immunity (-100V)** for highest robustness / reliability with reduced development costs / number of PCB spins • 50% lower level shift losses for higher switching frequencies for expanded applications and markets • Latch up immune due to silicon on insulator substrate • **> 28% increased UVLO hysteresis range** for improved noise immunity (0.9V vs. 0.7V) • **Higher typical current drive of 2.5A / 2.5A** vs. 1.9A / 2.3A for high current versions enable increase switch device flexibility • **Logic operation up to -11V on VS Node** for increased noise immunity
2ED21814S06J	IR21814SPBF	IRS21814SPBF	
2ED2183S06F	IR2183SPBF	IRS2183SPBF	
2ED21834S06J	IR21834SPBF	IRS21834SPBF	
2ED2184S06F	IR2184SPBF	IRS2184SPBF	
2ED21834S06J	IR218344SPBF	IRS21834SPBF	
2ED2106S06F	IR2106SPBF	IRS2106SPBF	
2ED21064S06J	IR21064SPBF	IRS21064SPBF	
2ED2108S06F	IR2108SPBF	IRS2108SPBF	
2ED21084S06J	IR21084SPBF	IRS21084SPBF	
2ED2109S06F	IR2109SPBF	IRS2109SPBF	
2ED21094S06J	IR21094SPBF	IRS21094SPBF	
2ED21091S06F	IR21091SPBF	IRS21091SPBF	

Figure 24 Summary of pin-to-pin equivalents between new SOI-based gate drivers and legacy IR / IRS gate drivers

With the aforementioned, it is clear that there are substantial benefits to customers from Infineon's SOI-based HVIC gate drivers. Based on the final application, the benefit is added robustness in the case of motor control designs, and lower power loss in the case of power supply designs. Integrated bootstrap components improve reliability and reduce overall cost followed by the pin-pin compatibility with legacy IR parts.

Infineon's wide range of high-voltage CoolMOS™ super-junction MOSFETs, low-voltage OptiMOS™, high-voltage RCD, TrenchSTOP™ series IGBTs and EasyPACK™, EconoPACK™ power modules can now be driven with a robust and efficient SOI-based HVIC gate driver leading to a best-in-class power conversion and motor control product with highest quality standard.

9 References

[1] Infineon Technologies Gate Driver ICs Product Selection Guide

[2] Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs

[3] Understanding HVIC Datasheet Specifications

[4] Using Monolithic High Voltage Gate Drivers

[5] Managing Transients in Control IC Driven Power Stages

[6] Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

[7] HV Floating MOS-Gate Driver ICs

[8] Robustness of level shifter gate driver ICs concerning negative voltages

[9] 6ED family - 2nd generation Technical Description

[10] 2EDL family Technical Description

[11] Obtaining information about junction temperature by using the thermal coefficient Ψth(j-top)

9.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

Revision history

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