Introduction to Infineon's simulation models for IGBTs and silicon diodes in discrete packages

About this document

Scope and purpose

This document introduces and describes Infineon's simulation models for discrete IGBTs and silicon diodes.

Intended audience

The intended audience for this document is research and development teams, and engineers who want to perform an initial evaluation of Infineon's discrete IGBTs and silicon diodes through electrical and thermal simulations.

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1 Disclaimer

Models provided by Infineon are not warranted as fully representing all the specifications and operating characteristics of the semiconductor products to which the model relates. The models describe the characteristics of typical devices. In all cases, the current datasheet information for a given device provides the only guaranteed performance specifications that can be used as a design guideline. Although models can be a useful tool in evaluating device performance, they cannot model exact device behavior and characteristics under all conditions, nor are they intended to replace experimental tests for the final verification of the application system. Infineon therefore does not assume any liability arising from the improper use of these models. Infineon reserves the right to modify models without prior notice.

2 Introduction

Circuit simulation is a safe and efficient way for researcher and engineers to verify the performance of the selected device in an application and understand its behavior. Infineon offers simulation models such as SPICE (Simulation Program with Integrated Circuit Emphasis) and PLECS® (Piecewise Linear Electrical Eircuit Simulation) for its discrete IGBTs, CoolSiC™ MOSFETs, and diodes. These simulation models provide insights into device behavior and performance during the design phase or troubleshooting. This helps designers find valuable solutions for their application before the physical designs are created.

Simulation models are useful for virtual prototyping. This saves costs and time during the development process and helps developers design, optimize, and test electronic circuits using simulation software.

SPICE simulation models of Infineon's power devices provide a detailed, transient switching waveform that helps users understand device behavior. These models can be used to:

- Thoroughly evaluate the device behavior (both static and dynamic characteristics) in simulation and compare different devices to find the most suitable one as per application requirements
- Evaluate and optimize system-level performance by comparing and evaluating different devices in the system level simulation
- Design application parameters (such as selecting an appropriate switching frequency or dead-time) and compare the switching losses of different components
- Replicate external circuit effects such as commutation loop design, gate driver design, and various parasitic elements
- Enable detailed analysis of resonant or soft-switching topologies, and typical hard-switching converters

Circuit simulation in SPICE helps in determining switching losses by considering the physical behavior of the switching process, therefore SPICE simulation requires a very small time step (in nanoseconds).

Unlike SPICE, PLECS uses ideal switches and does not include physical models of components, therefore, transient waveforms cannot be observed during the switching operation. However, PLECS has a thermal modeling domain that estimates device switching and conduction losses, and consequently calculates junction temperatures of the device [6].

Estimating power dissipation and junction temperatures of power semiconductors is essential for reliable operation of power converters. Thermal management is an important aspect of power electronic systems. It is gaining more importance with the increasing requirement for compact packages and higher power density. PLECS enables users to incorporate thermal design into the electrical design at an early stage and provides a cooling solution suitable for the application [6]. PLECS simulation models address the power loss estimation by using specially defined device models that include switching losses obtained from measurements and use lookup tables to define losses as a function of voltage, current, junction temperature, and other user-defined variables such as gate resistance. This method does not require small time steps and provides high computational speed while accurately predicting power dissipation and junction temperature to achieve optimized power and thermal management.

This application note explains the PLECS and SPICE simulation models of Infineon's discrete IGBTs as well as their calibration and accuracy. It also describes in detail how to use SPICE simulation models in offline simulation tools such as LTspice® and SIMetrix.

3 Infineon SPICE models for IGBTs and power silicon diodes

3.1 Model library files

The models for Infineon IGBTs and power silicon diodes are evaluated with the SIMetrix circuit simulator. The models are tested, verified, and provided in PSpice® simulation code. All power device models are grouped in dedicated library (.lib) files according to their voltage class and product technology. These .lib files are compatible with all SPICE simulators available on the market such as SIMetrix, LTspice®, PSpice®, and OrCAD®. SPICE models for all discrete products of Infineon are available on Infineon's website [1] and their respective product pages. The model folder published on the website contains the .lib file of the device model and the .sxslb file, which is the IGBT symbol file for the SIMetrix graphical user interface.

3.1.1 Library implementation in SIMetrix

Before setting up a simulation, a model must be integrated in the simulator tool. This section illustrates the installation process of the simulation model files in SIMetrix. The simulation model folder can be downloaded from Infineon's website as a zip file. After unzipping the file, users can install the model using the steps described in the following sections:

- Installing the model
- Associating the model with a symbol

3.1.1.1 Installing the model

SIMetrix provides two ways to install the model – the "drag-and-drop" method and the "local installation" method.

To install a model using the drag-and-drop method, users can follow these steps (Figure 1):

1. Open Windows Explorer and locate the device models.
2. Select the files to be installed (files with extensions .lib and .sxslb**.**)
3. Ensure that the SIMetrix command shell is in focus. If this is not the case, select a schematic or graph and press the spacebar.
4. Drag and drop the files from Windows Explorer into the command shell. A message box will pop up to individually process the files.
5. Click **Ok** to confirm and install the simulation model.

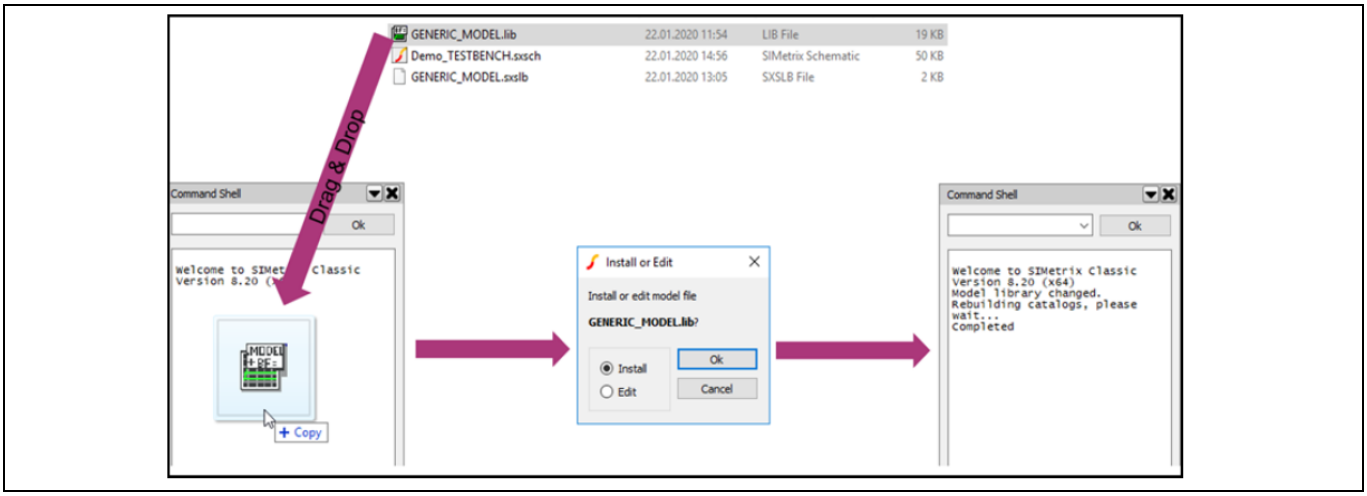


Figure 1 Installing a model in SIMetrix using the drag-and-drop method

In the local installation method, a model can be enabled (for a certain schematic) by including a reference in the Command Window. To include the model in the schematic, users can follow these steps (Figure 2):

1. Open the schematic sheet and press F11 on the keyboard to toggle to the Command Window.
2. Type .include, .inc, .library, or .lib commands followed by the name of the library file. If the model library file (.lib) is not in the same folder as the schematic, type the full path to the file.

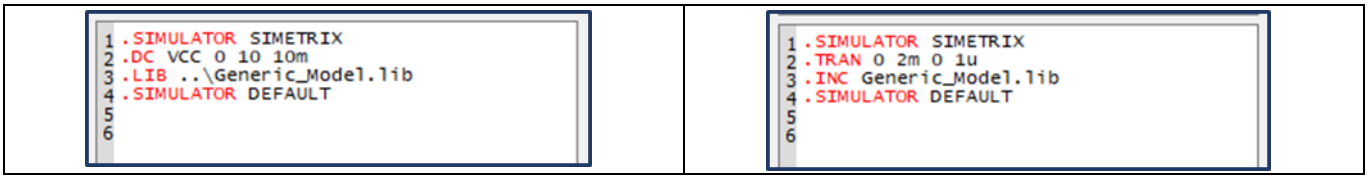


Figure 2 Installing a model in SIMetrix using the local installation method

3.1.1.2 Associating the model with a symbol

Once the simulation model is installed, the relevant part can be placed on the schematic. If the model has been installed using the drag-and-drop method, users can follow these steps:

1. Go to **Place** → **From Model Library** to associate a symbol to a newly installed library (Figure 3a.)
2. The newly installed part is available in the Recently Added Models section. Select the part. If a related symbol had been assigned, a preview of the symbol appears in the preview window (Figure 3b.)
3. If a symbol has not been assigned, the simulator displays a warning that a symbol cannot be found. In this case, to generate a standard symbol for the model, click **Place** (Figure 3c) and then click **Auto Create Symbol** (Figure 3d.)
4. If the part is to be placed in the "Unassigned" category, click OK (Figure 3e) and select **Yes, leave at "Unassigned"** (Figure 3f), otherwise select a suitable category or create a new one to place the part .

The symbol is now ready to be placed in the schematic.

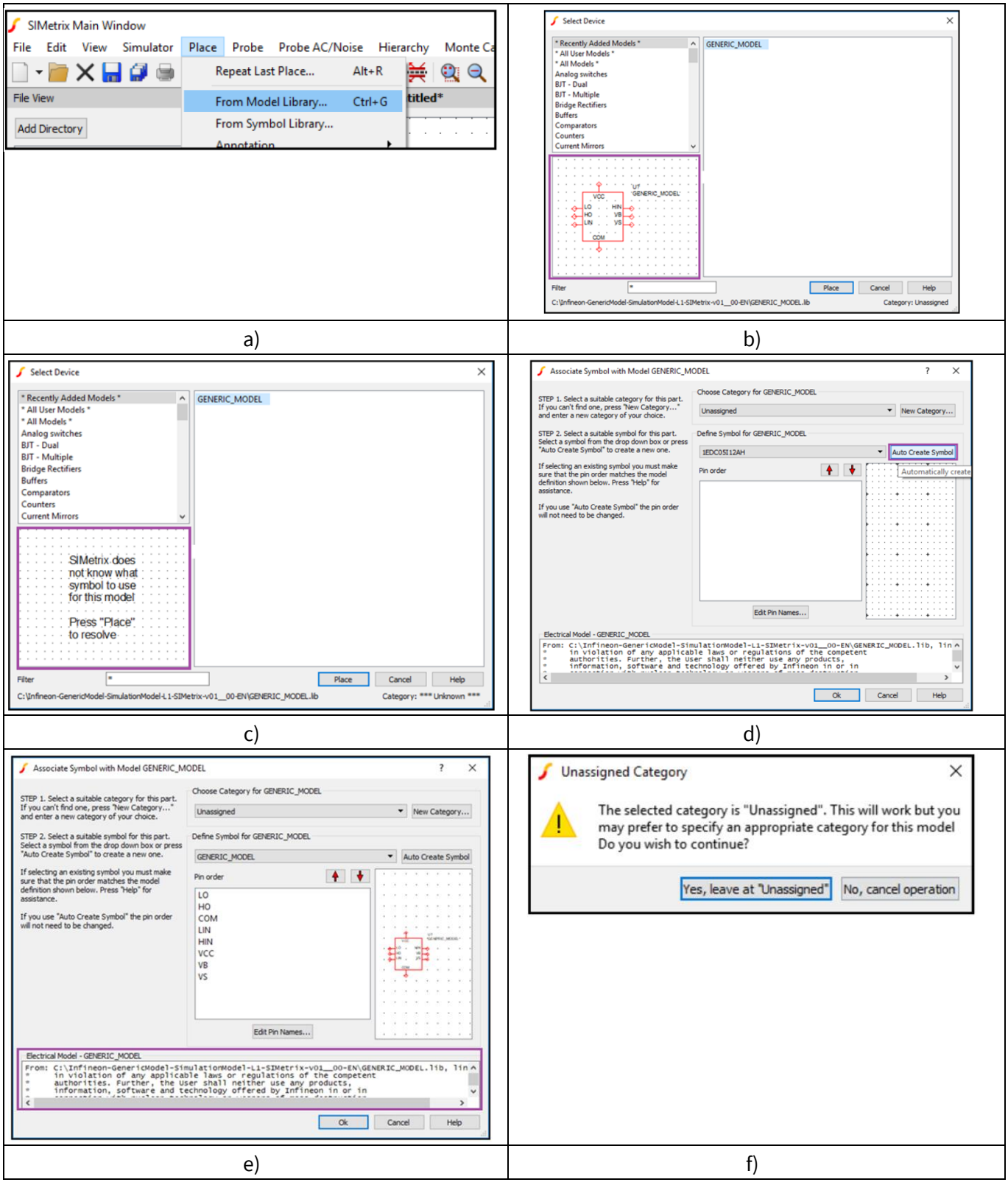


Figure 3 Associating installed models with symbols in SIMetrix

To associate the symbol with a model that has been included in the simulation through the local installation method, users can follow these steps (Figure 4):

1. Click **Place** → **From Symbol Library…**.

2. Select an appropriate symbol (for e.g. Semiconductors, IGBT). Note that the number of pins in the symbol must be the same as indicated in the model file .lib file.
3. Place the symbol within your user-defined schematic.
4. Combine the locally installed library with the placed symbol.
5. Define MODEL as X to use an arbitrary sub-circuit.
6. Define VALUE as the model name you want to use. The model names can be retrieved from the library file (e.g., IKW50N65H5_L1).

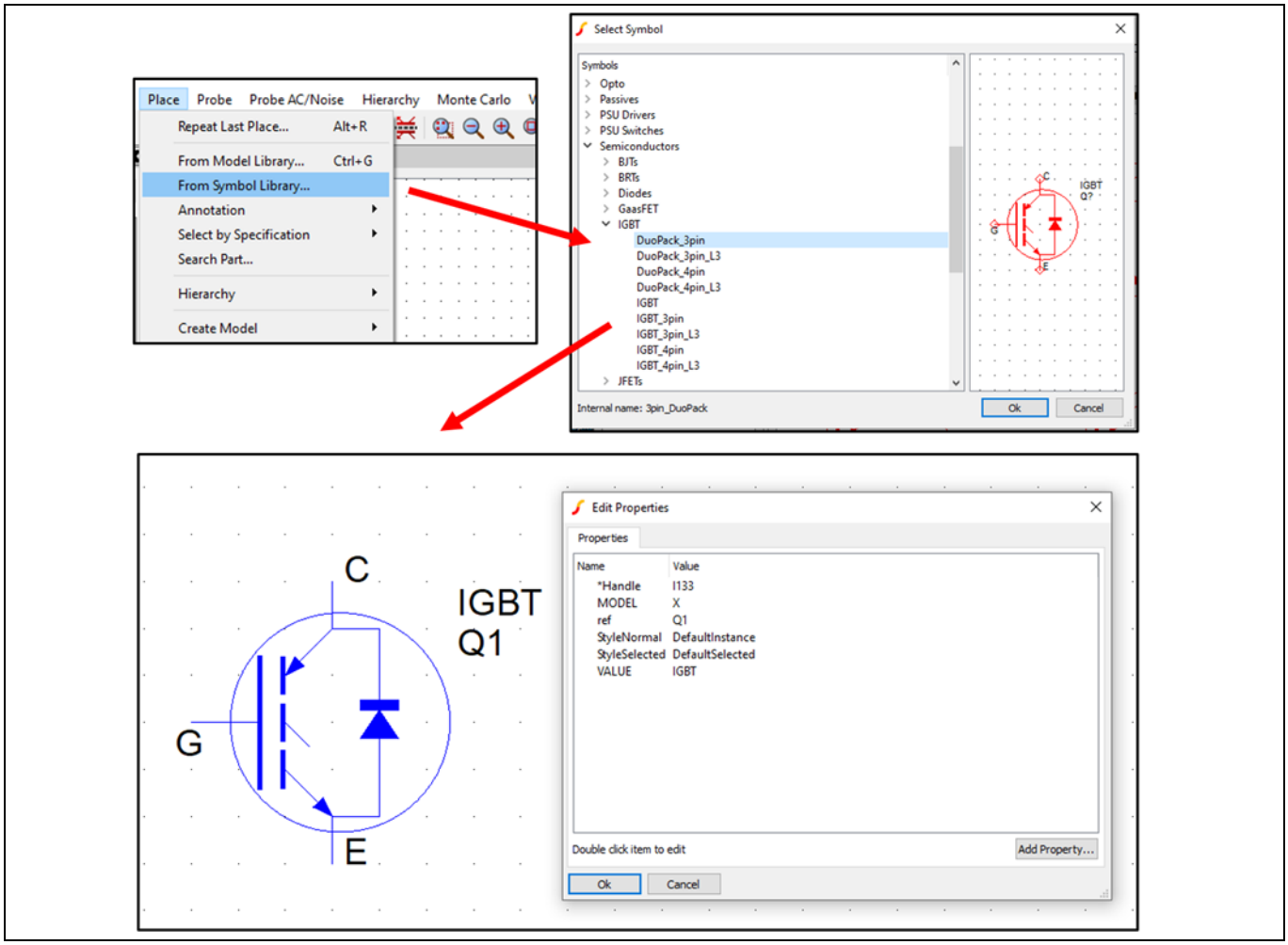


Figure 4 Associating locally installed model with a symbol

3.1.2 Library implementation in LTspice®

This section explains the installation method for the simulation model files in LTspice®. All simulation models are installed using a two-step procedure:

1. Installing the model
2. Associating the model with a symbol

3.1.2.1 Installing the model

In LTspice®, an external model can be easily enabled in the schematic file. This can be done by using one of the inclusion SPICE commands: .include, .inc, .library, or .lib, followed by the library name (Figure 5.) If the model library file (.lib) is not placed in the same folder of the schematic, the full path to the file must be used.

Alternatively, the path to the model file can be added permanently to the simulator default searching paths. This can be done in the Control Panel of the software by adding the path in the "Sym. & Lib. Search Path" section of the "Library Search Path" area.

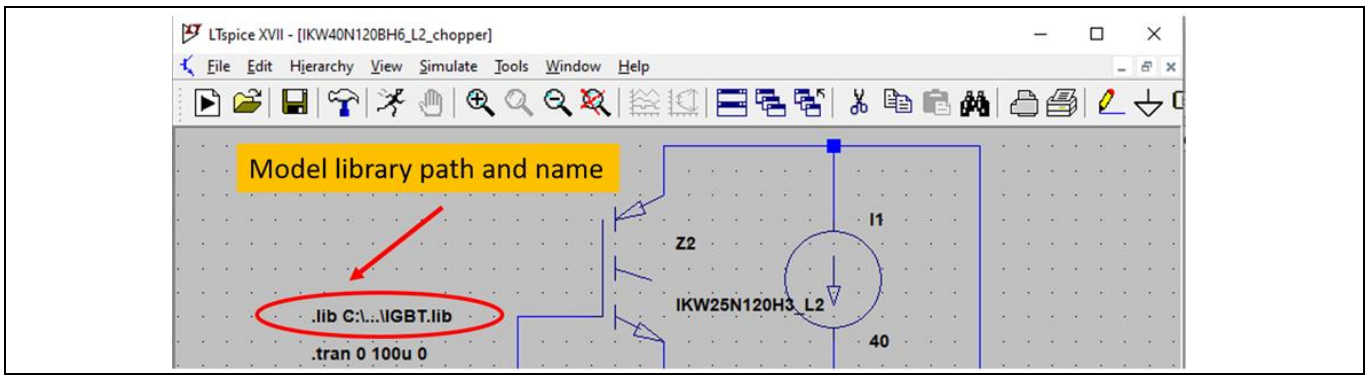


Figure 5 Including a model library in LTspice® schematic

3.1.2.2 Associating the model with symbol

A symbol file for LTspice® has the extension .asy. The symbol can be used in the software only if it is in the included search paths of the software. This can be done by adding it in the "Sym. & Lib. Search Path" section of the "Symbol Search Path" area.

Alternatively, the software can be used to automatically create a symbol for the specific model. To do so, users can follow these steps (Figure 6):

1. Open the library file with LTspice®.
2. Right-click on the .SUBCKT line of the desired device and then click **Create Symbol.**
3. Click **Yes** in the window that opens. A general, editable symbol is generated with the same number of pins and pin names as defined in the source model file. Any parameter that may be needed by the model is also visible (for e.g. parameter TJ.)

The generated symbols can be found in the AutoGenerated folder[1].

[1] The "AutoGenerated" models can be accessed directly by the software clicking on "Edit" menu and then "Component".

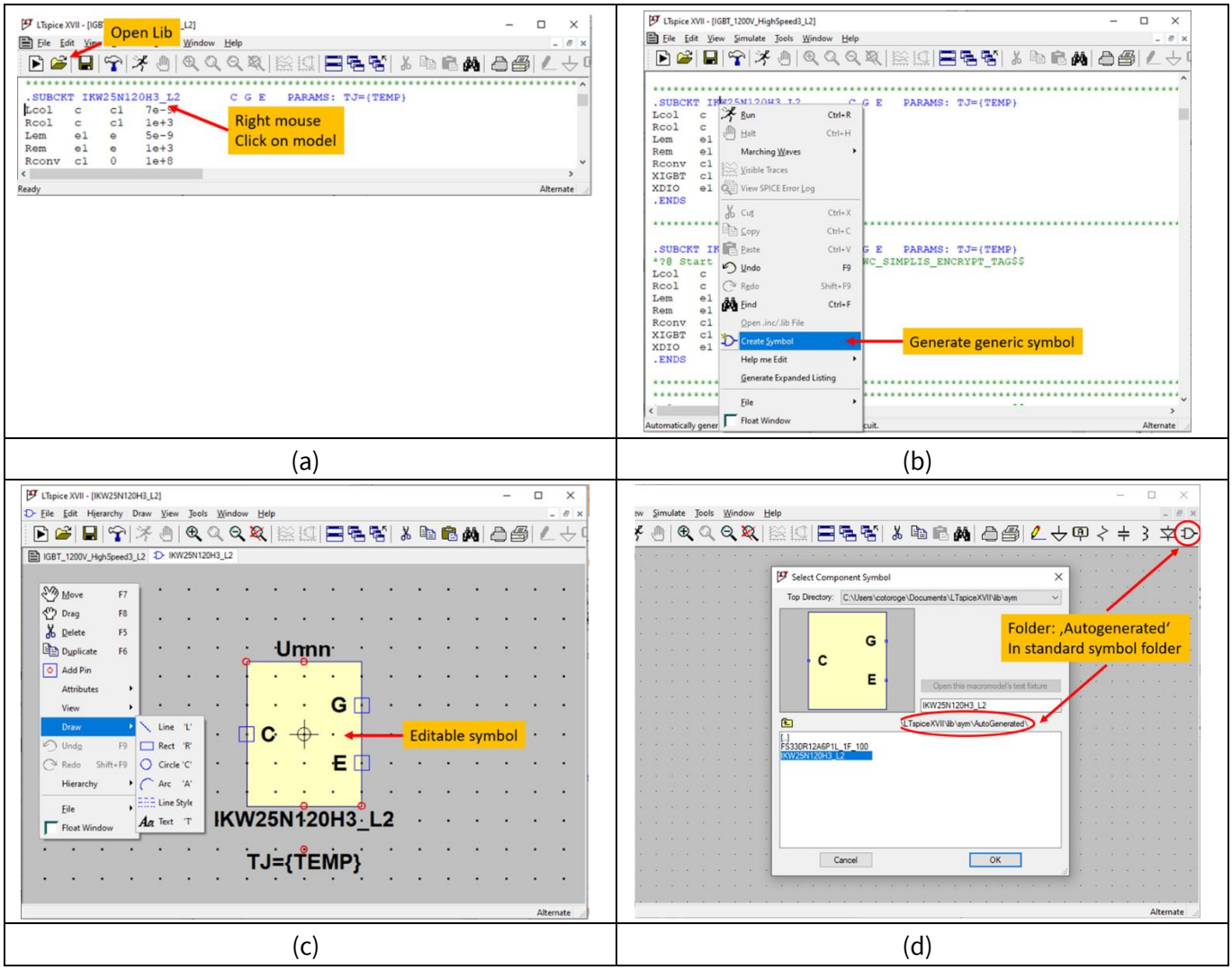


Figure 6 Creating a generic symbol for a model in LTspice®

3.2 Modelling levels

Infineon provides up to three different types of models for IGBTs and power silicon diode devices. The differences among the models lies in the implementation of the electrical characteristics of the device and the definition of the dynamic temperature dependence. The nomenclature of the models is the device name with a suffix identifying the level (Table 1):

Table 1 Modelling level nomenclature

Suffix	Model Level	Terminals
_L1	1	For IGBTs: C, G, E (K) For diodes: A, C
_L2	2	
_ L3[1]	3	For IGBTs: C, G, E (K), tc, tj, (tjd) For diodes: A, C, tc, tj

[1] Due to the high modelling effort, level 3 models of IGBTs and diodes are provided only upon request.

For e.g., Level 1 model of the IKW50N65F5 has the model name IKW50N65F5_L1.

Pin naming is defined as follows:

```
* PINS:
* ------------------------------------------------------------------------
* | PIN | DESCRIPTION
* ------------------------------------------------------------------------
* | C   | IGBT collector for single devices and DuoPacks
* ------------------------------------------------------------------------
* | G   | IGBT gate for single devices and DuoPacks
* ------------------------------------------------------------------------
* | E   | IGBT emitter for single devices and DuoPacks
* ------------------------------------------------------------------------
* | K   | IGBT Kelvin emitter sense for single devices and DuoPacks
* ------------------------------------------------------------------------
* | A   | diode anode for single devices
* ------------------------------------------------------------------------
* | C   | diode cathode for single devices
* ------------------------------------------------------------------------
* | tc  | case temperature
* ------------------------------------------------------------------------
* | tj  | junction temperature for IGBTs or single diodes
* ------------------------------------------------------------------------
* | tjd | junction temperature for diodes within a DuoPack
```

The following sub-sections explain the different levels and their distinctions in detail.

3.2.1 Level 1 (behavioral modelling approach) [2]

Level 1 model is based on a behavioral description of the electrical characteristics of the device [1]. The calibration is done with respect to the latest datasheet content. The transient calibration is based on the Dynamic test circuit given in the latest datasheet. In this datatsheet, parasitic elements and nominal condition values are also specified in the table, Switching characteristics, inductive load.

The diode and the IGBT model consist of two interdependent sub circuits – the main circuit that describes the outer electrical characteristics of the device, and an auxiliary circuit that is used to calculate the amount of stored charge as the result of a bipolar effect. The usage of Level 1 compact models is restricted to a temperature range between 25°C and the maximum allowed junction temperature stated in the corresponding datasheet. The static temperature of the model can be set using the SPICE command, .TEMP, in the simulator interface.

3.2.2 Level 2 (physics-based modelling approach) [3] , [4]

Level 2 compact models are based on the discretization of device-physic equations to one-dimension current flow (Figure 7). This simplification is done to achieve acceptable runtimes and model development cycles. Model

parameters are based on technological data and device physics. Additionally, the model is calibrated against the measured characteristic curves (output, transfer, and gate-charge curves) of the device. Level 2 compact models can also model second-order effects of the devices (for e.g. sharp tail current cut-off, diode reverse recovery snap-off, etc.) to a limited extent.

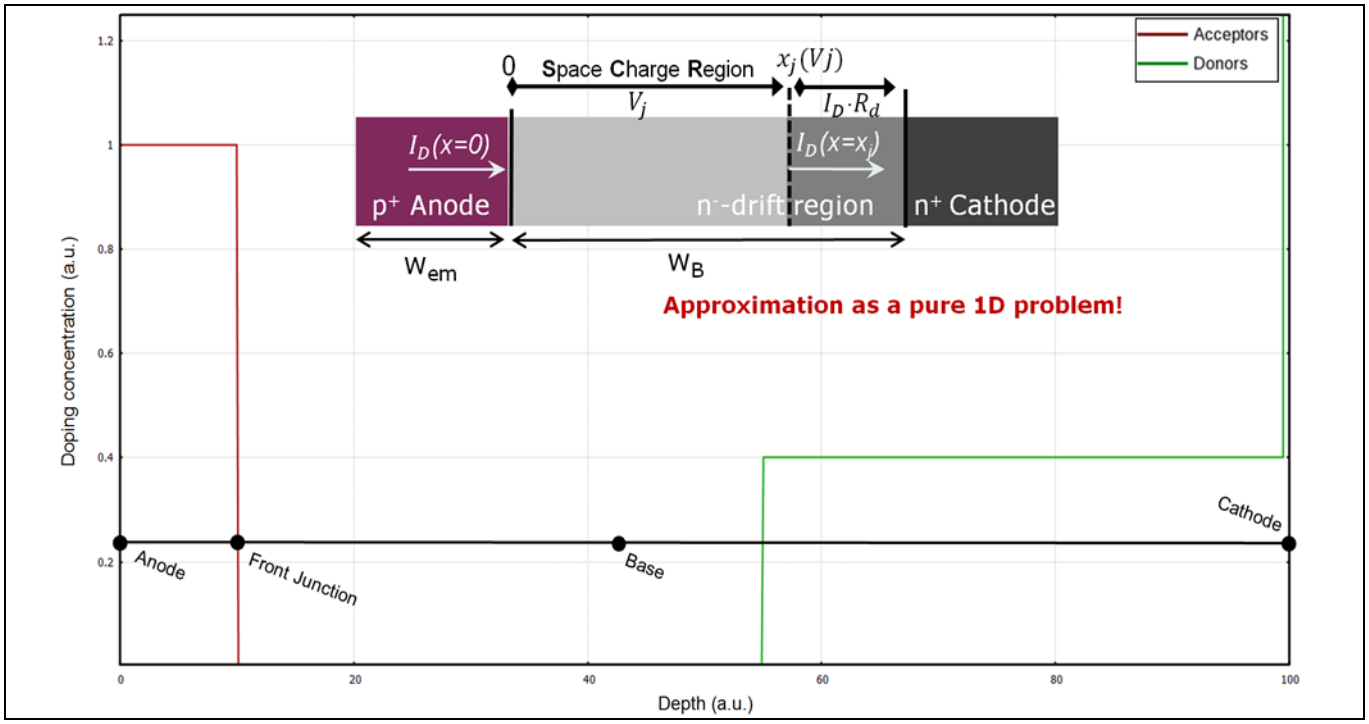
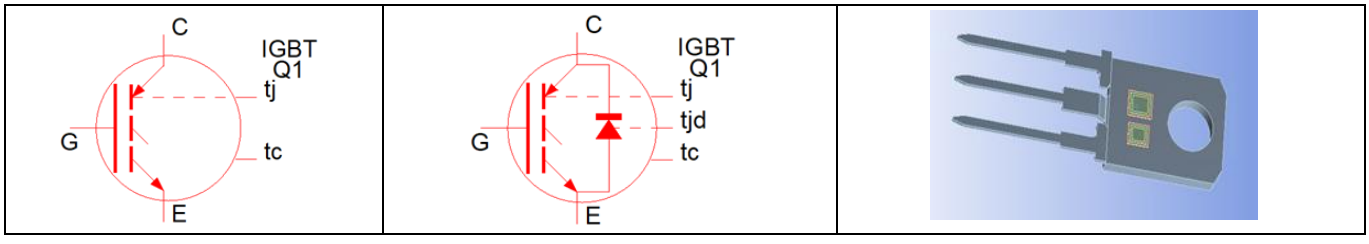


Figure 7 Vertical doping profile of a typical pin diode along with the basic nodes used to describe the diode behavior

3.2.3 Level 3 (coupled electro-thermal modelling)

To compute self-heating dynamically, the electrical model (Level 1 or Level 2) is coupled with a thermal model of the mounted device, including the package, in what is called a Level 3 model. Therefore, Level 3 compact models include a suitably dimensioned Cauer RC network describing the thermal path from the IGBT/diode junction (located inside the chips) to the back side of the lead frame (corresponding to the case). To achieve self-heating, the instantaneous power dissipation in the transistor is continuously calculated and a current proportional to this power is fed into the equivalent thermal network. Level 3 models must be used only for transient analysis, except short circuit.

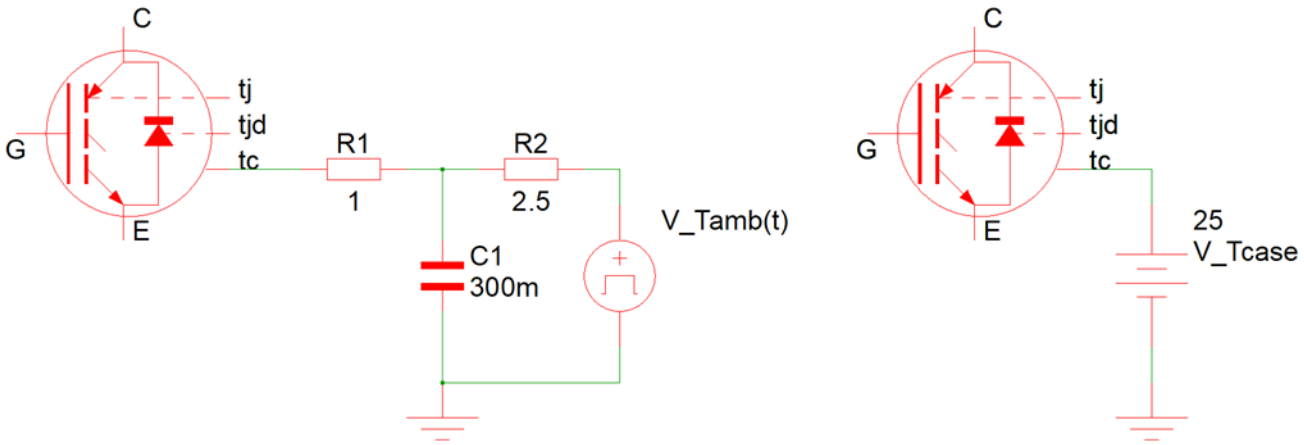
The voltage at nodes tj and tjd contain information about time-dependent junction temperature of the IGBT and the diode, respectively. This in turn is fed back directly to the corresponding temperature-dependent electrical model. The Level 3 model symbol is extended by thermal nodes with junction temperatures and case temperature, 5 pins in single-packed IGBT, and 6 pins in a co-packed IGBT (Figure 8)



Single-packed IGBT with thermal nodes	Co-packed IGBT and diode with thermal nodes	3D geometry of a co-packed IGBT and diode (leadframe is in grey and chip is in green)

Figure 8 Schematic symbols of Level 3 IGBT models for electro-thermal calculation

The temperature connections work as voltage nodes and are electrically separated from the electrical device model. Therefore, a potential difference of 1 V refers to a temperature difference of 1°C. The additional thermal nodes tj and tjd enable the user to easily monitor the simulated junction temperature of the IGBT and the diode, respectively. Usually, these nodes should not be connected, however, if the initial temperature of the device has to be different from the thermal equilibrium, a small capacitor (typically 1 pF) can be connected between these nodes and the thermal ground. The initial temperature can then be set on the capacitor through the .IC SPICE instruction. The small capacitor does not alter the thermal network and is only used to force the initial temperature. The thermal node tc contains information about the case temperature, which is the temperature on the back side of the lead frame. In the model, it can be constant or time dependent. The node tc must always be connected to a reference voltage/temperature, either directly (to simulate a constant case temperature) or through an external thermal RC network (for e.g. when the case is connected to a thermal pad and to a heat sink). The reference temperature can also be time dependent if it represents the temperature of a heat sink.



(a) Connection through additional thermal network	(b) Connection to a fixed reference temperature

Figure 9 Connecting external thermal networks to devices modelled after the Level 3 approach

Figure 9 shows an example of a simulation with external heat sink. In image (a), R1 can refer, for e.g., to the thermal resistance of the interface between the case of the device and heat sink (e.g. a thermal pad). In this case, C1 and R2 model the transient thermal behavior of the heat sink, representing its thermal capacitance and thermal resistance to the environment, respectively. The voltage source connected to R2 describes the time-dependent ambient temperature behavior of the simulation. An alternative connection method is shown in image (b), where the case of the package is fixed to 25°C. In such a connection, by changing the value of the source it is possible to exploit the variations of the device parameters (for e.g. V_{CEsat} , and V_F) with temperature, to replicate the information shown in the datasheet graphs. This possibility is also offered by Level 1 and Level 2 models through the TEMP parameter.

3.3 IGBT models for 4-pin devices

Some of the IGBT portfolios offered by Infineon include a four-pin package that has an additional emitter pin connection for fast and efficient switching. These products feature a separate connection for the gate-driving

return path, called the Kelvin emitter (K)[1]. The 4-pin device models require a dedicated symbol with an additional pin, compared to the standard 3-pin symbol of an IGBT. These models include an internal parasitic emitter inductance of the bond wires and the emitter pin of the package up to the ideal solder point. According to the datasheet specification, this point is defined as 4.5 milimeter from the mold of the package given in the 3-pin configuration. In the 4-pin model, a separate, internal parasitic inductance is included that corresponds to the contribution of the Kelvin emitter bond wire and pin.

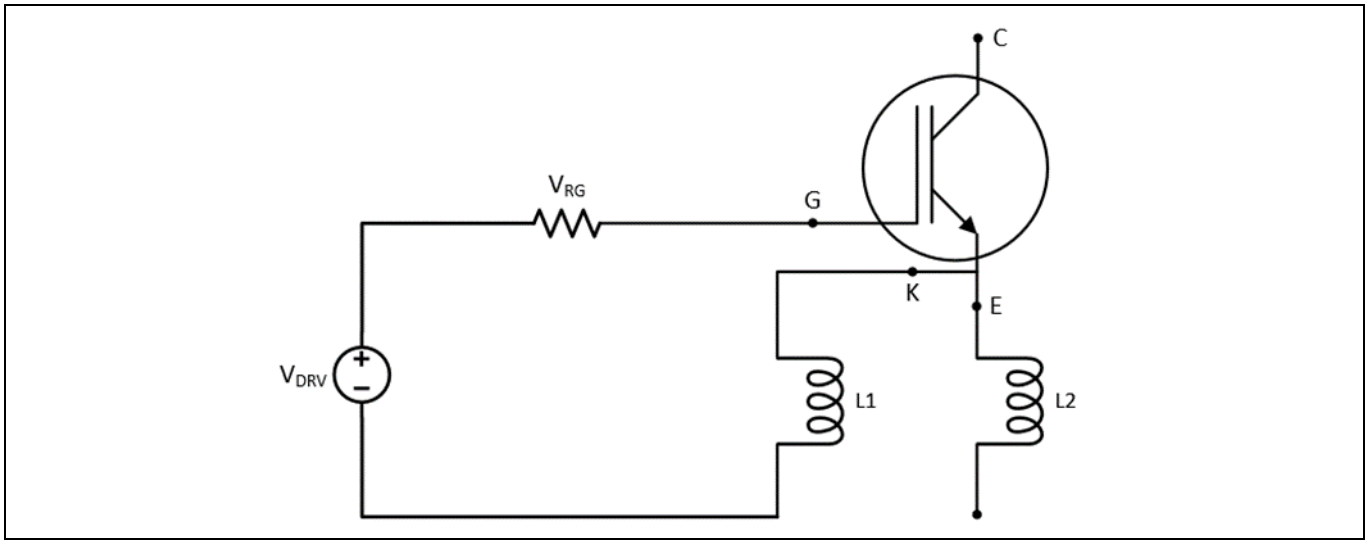


Figure 10 Simulation circuit for 4-pin IGBT devices

In addition to the parasitic inductance of the package, the PCB (printed circuit board) layout contributes to the increase in the overall parasitic inductance of the gate loop. The simulation schematic should, therefore, consider this additional contribution by including an external parasitic inductance as shown in Figure 10. As a first order of approximation for the stray inductance, a value of 1 nH per milimeter of the trace length can be used. Alternatively, a more precise value of stray inductance can be determined by performing a 3D simulation of the PCB geometry.

3.4 Typical simulation parameters

The following settings have been found to be helpful for simulation with the indicated circuit simulator tools:

Table 2 Simulator settings for SIMetrix, OrCAD® PSpice®, LTspice®

OPTION	Level 1	Level 2
Method	Gear	Gear
AbsTol	1e-9	1e-9
VnTol	1e-6	1e-6
RelTol	1e-3	1e-3
ITL1	200	200
ITL2	200	200
ITL4	25	50

[1] For further information, the users can refer to the dedicated application note: "TRENCHSTOP™ 5 IGBT in a Kevin Emitter Configuration".

OPTION	Level 1	Level 2
POINTTOL (only Simetrix)	-	1
CONV (only Simetrix)[1]	-	> 1

In OrCAD® PSpice®, it is also recommended that **Enable Advanced Convergence Algorithms** be selected (see Figure 11.)

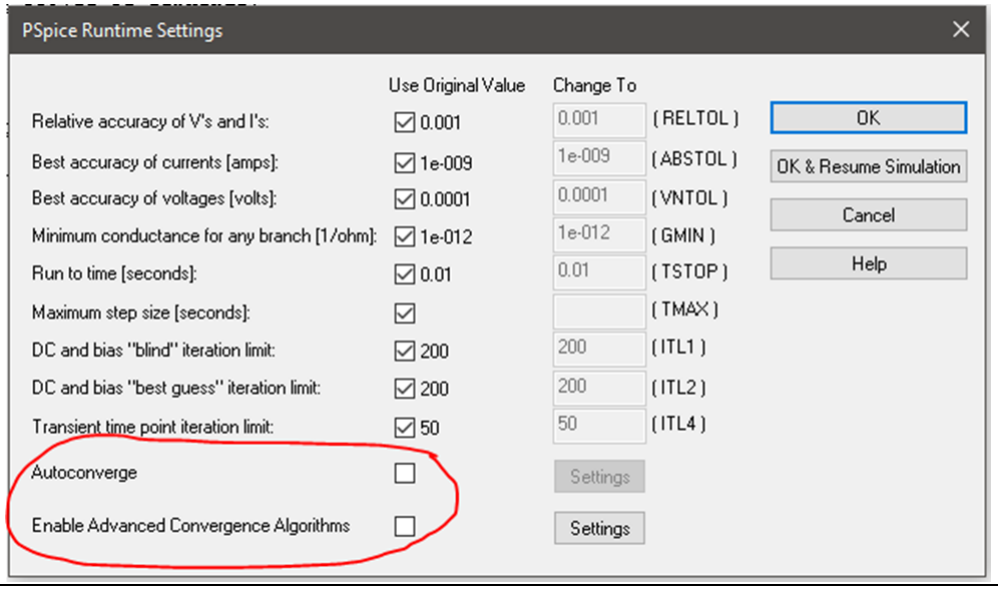


Figure 11 OrCAD® PSpice® runtime settings

In many cases, it is necessary to limit the step size for transient analyses. As a typical power electronic circuit contains elements with different time scales, the automatic step control of the simulators can sometimes disregard essential fast time-scale information that eventually leads to convergence problems. In the latter case, limiting the maximum step size to a value of 1 ns can resolve the issues.

In cases where the time to be simulated, TSTOP, is relatively large (typically if thermal phenomena are of main interest) and sharp gradients occur (for e.g. in the startup phase of the system), the required simulation time might be too long. In such cases, it is helpful to start the first simulation with a shorter simulation time and save the simulation status. Then a second simulation can be started from the saved state with a relaxed timestep.

3.5 Transient simulation results

This section highlights the differences between Level 1 and Level 2 models in terms of transient turn-on and turn-off curves in a standard double-pulse test circuit, using IKW25N120H3 IGBT model as an example.

3.5.1 Level 1 vs. Level 2 calibration

The following are used for calibrating a Level 1 IGBT model:

Transfer curves at 25°C and T_{jmax}

Output curves for different V_{GE} values at 25°C and T_{jmax}

Gate-charge curves at 20% and 80% V_{CE}

[1] Only if convergence fails.

Capacitance as a function of V_{CE}

Switching energies and switching times at 25°C and T_{jmax}, both at nominal values of gate resistance, load current, and DC-link voltage

The following are used for calibrating a Level 1 diode model:

V_F curves at 25°C and T_{jmax}

Q_{rr} and I_{rr} values at 25°C and T_{jmax}

In contrast, Level 2 models are calibrated using only the gate-charge and static characteristic curves.

Figure 12 to Figure 16 show that the calibrated static and gate-charge curves are very similar for both Level 1 and Level 2 models.

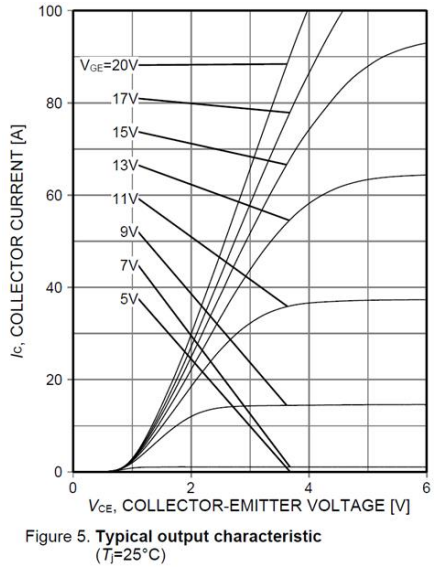
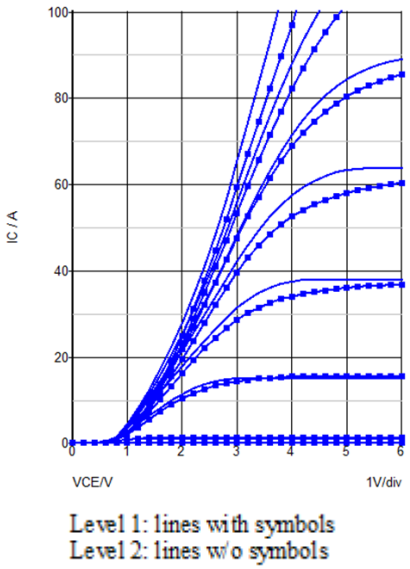


Figure 5. **Typical output characteristic** (T_j=25°C)



(a) Datasheet	(b) Simulation

Figure 12 Output characteristics at T_j = 25°C of KW25N120H3

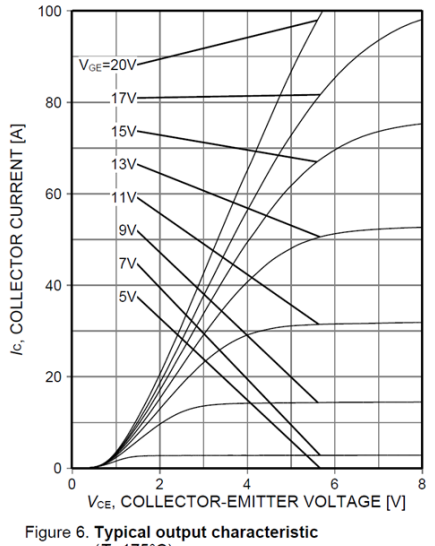
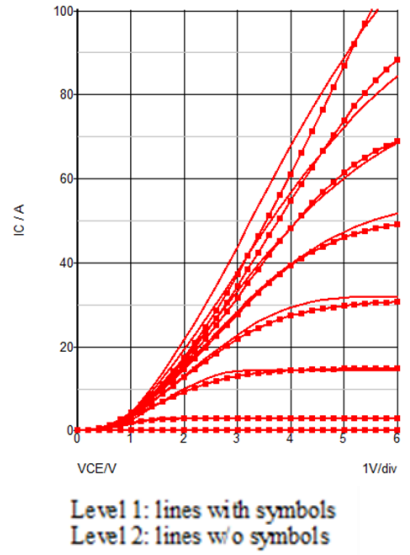


Figure 6. **Typical output characteristic** (T_j=175°C)



(a) Datasheet	(b) Simulation

Figure 13 Output characteristics at T_j = 175°C of KW25N120H3

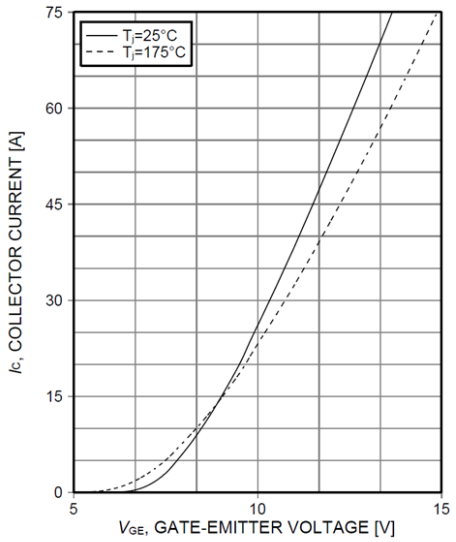
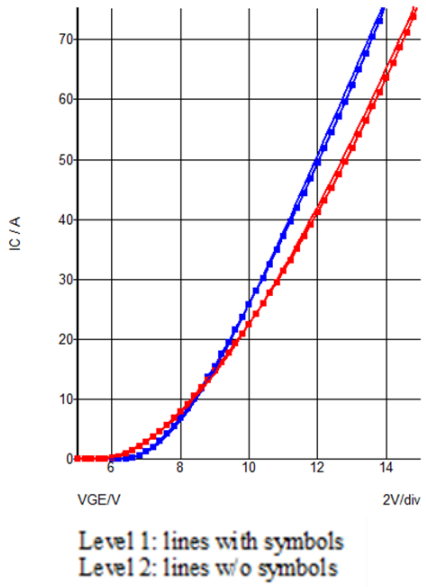


Figure 7. **Typical transfer characteristic** (V_{CE}=20V)



(a) Datasheet	(b) Simulation

Figure 14 Transfer characteristics at V_{CE} = 20 V of KW25N120H3

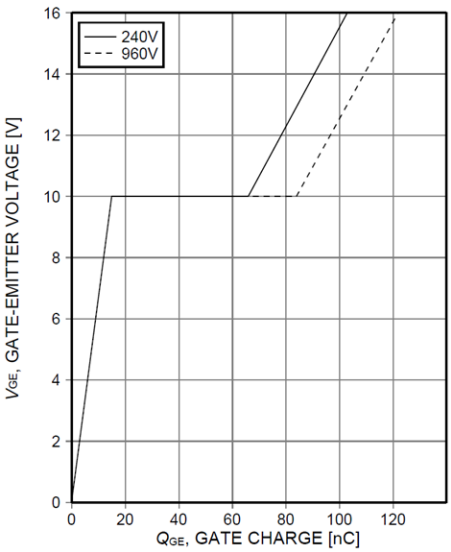
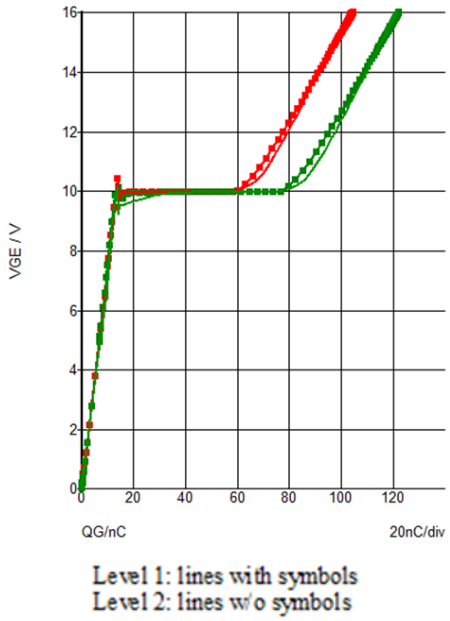


Figure 17. **Typical gate charge** (I_C=25A)



(a) Datasheet	(b) Simulation

Figure 15 Gate charge characteristics at I_C = 25 A of KW25N120H3

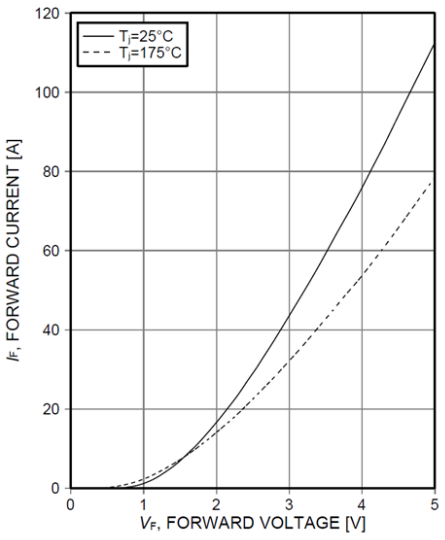
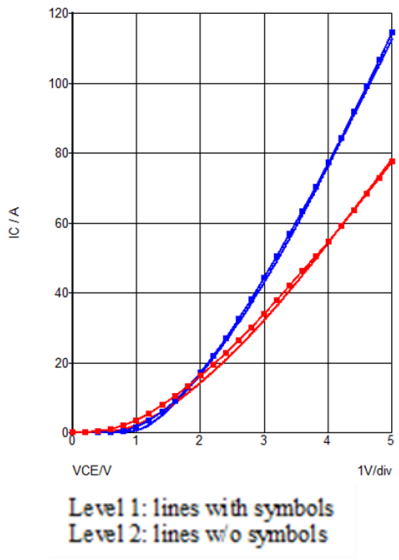


Figure 27. **Typical diode forward current as a function of forward voltage**

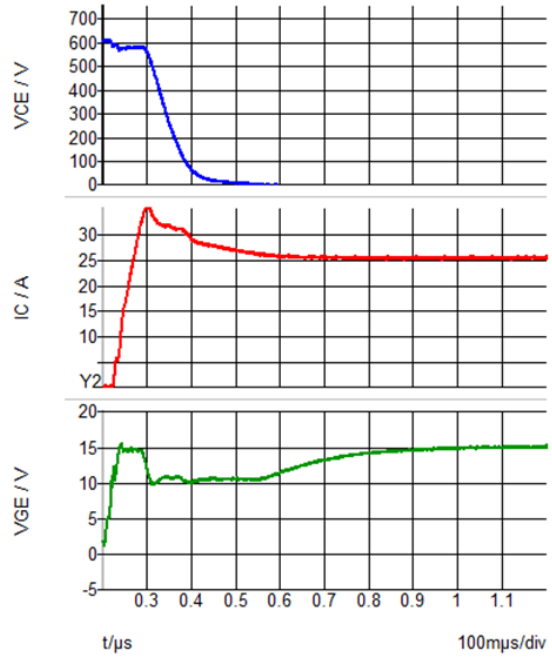


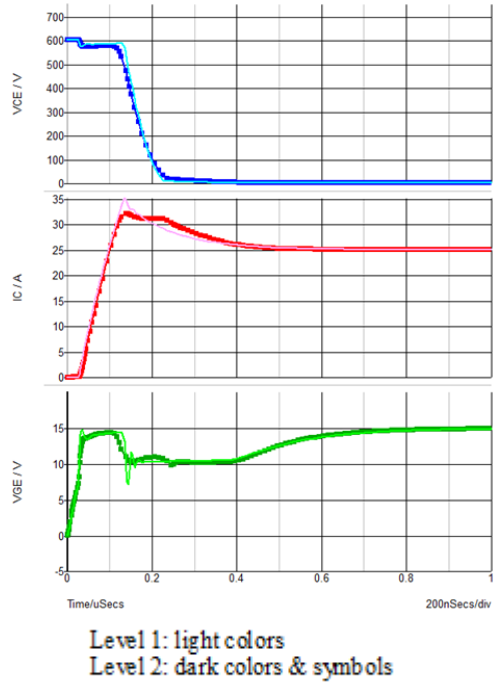
(a) Datasheet | (b) Simulation

Figure 16 Diode output characteristics of KW25N120H3

3.5.2 Level 1 vs. Level 2 transient behavior

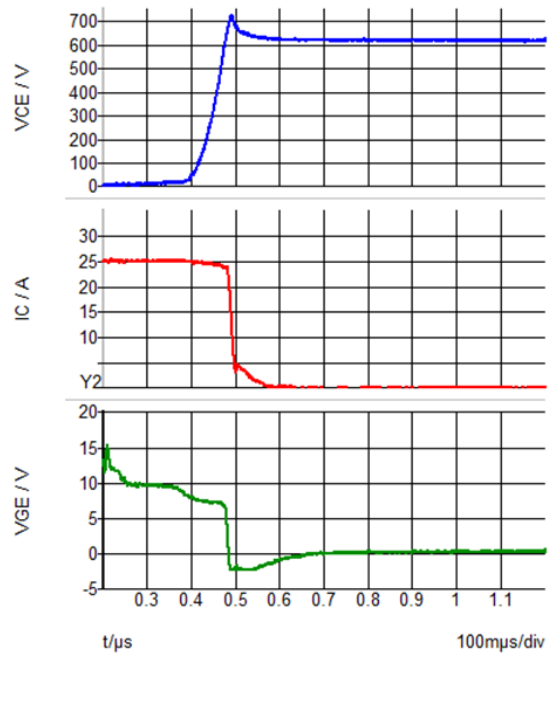
This section discusses precision of the compact models in terms of the switching characteristics of the IGBT and the power diode. It also illustrates the differences between closely calibrated behavioral (Level 1) and physics-based (Level 2) models, in representing the behavior of the device.



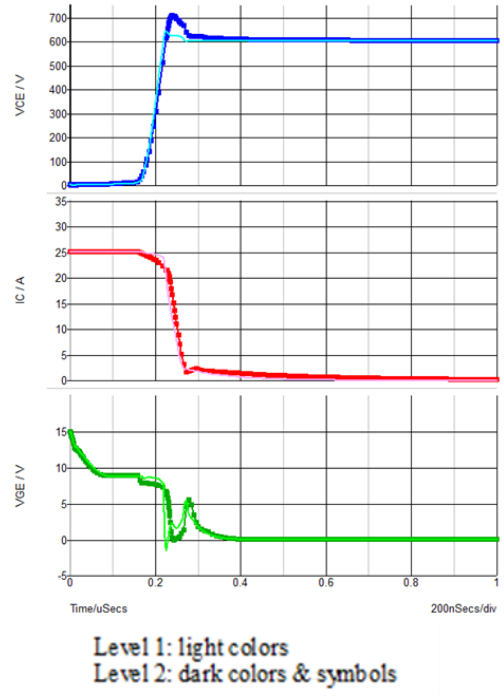


(a) Measurement | (b) Simulation

Figure 17 Turn-on transient curves of IKW25N120H3 for nominal switching conditions (T_j = 25°C, V_{CC} = 600 V, I_C = 25 A, R_G = 20 Ω)



(a) Measurement

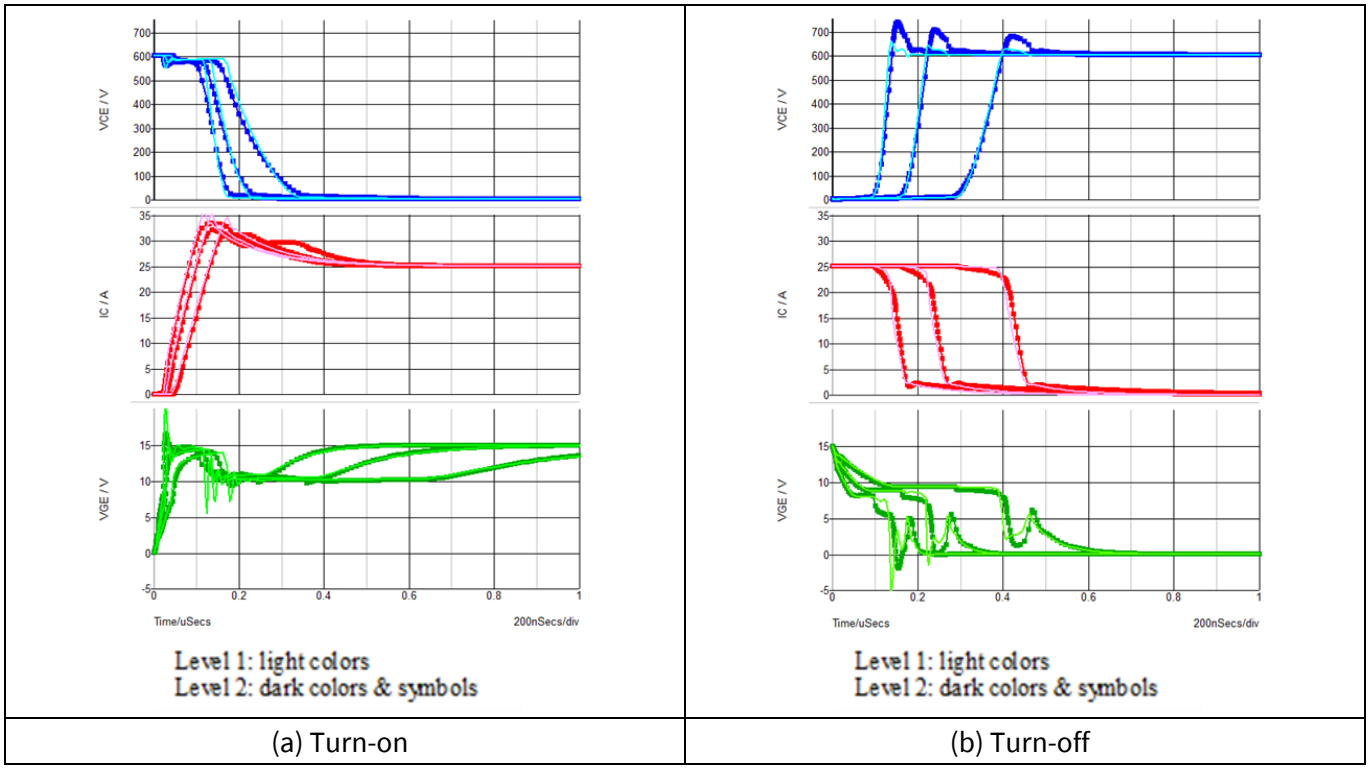


(b) Simulation

Figure 18 Turn-off transient curves of IKW25N120H3 for nominal switching conditions (T_j = 25°C, V_{CC} = 600 V, I_C = 25 A, R_G = 20 Ω)

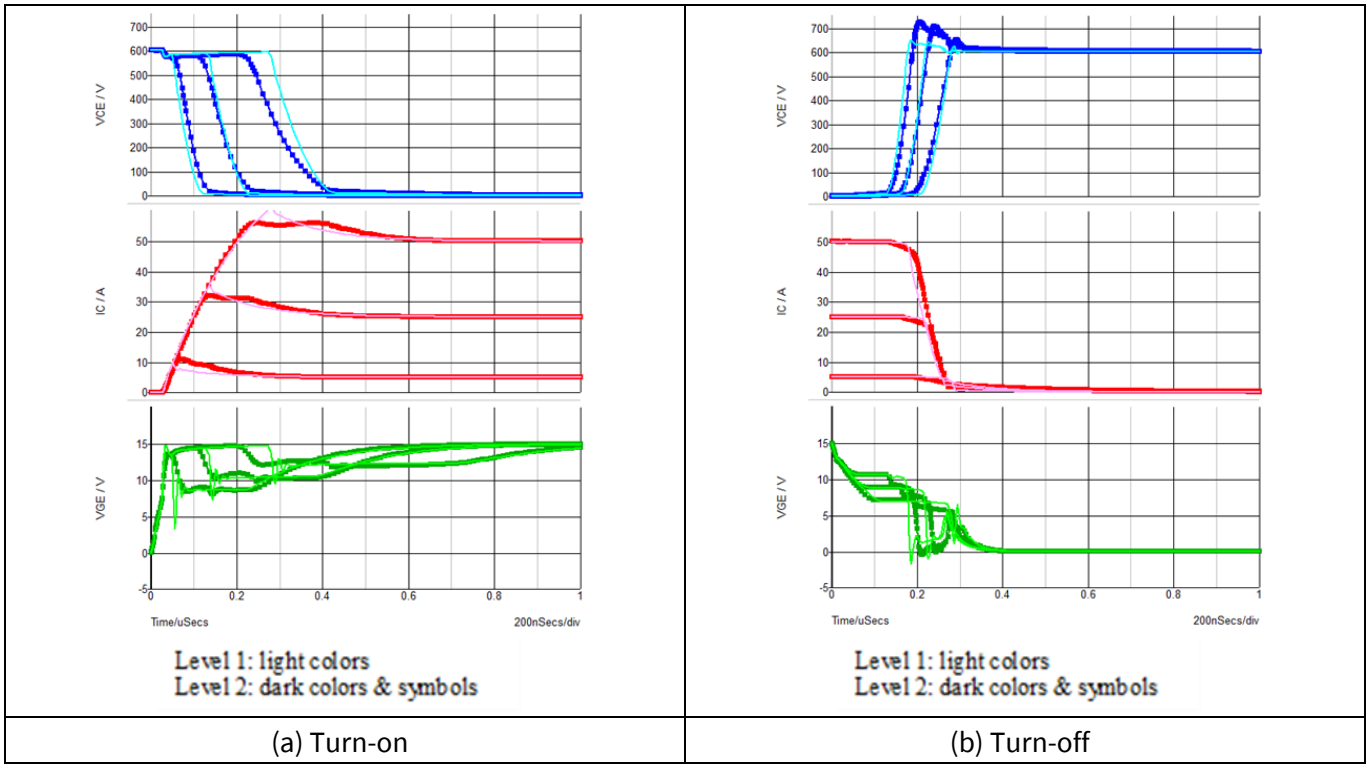
Figure 17 and Figure 18 depict the waveforms during the turn-on and turn-off switching events at nominal operating conditions as obtained by measurement and simulation, respectively. From the comparison it can be concluded that both Level 1 and Level 2 models represent the transient behavior of the IGBT with good accuracy. The most pronounced difference seen from the experimental results is the shape of the collector current at turn-off. The differences between Level 1 and Level 2 are mainly visible in the reverse-recovery current at turn-on and the overvoltage peak at turn-off. The Level 2 modelling approach gives the closest results with respect to the experimental waveforms, as it considers 1D physical effects and the real vertical design of the power diode. In contrast, the Level 1 behavioral model represents the reverse-recovery current by an exponential decay function, which is not always accurate. Also, Level 1 does not model the forward-recovery effect of the diode, which is partially responsible for the overvoltage peak at turn-off.

Figure 19 and Figure 20 show the simulated curves with the variation of the gate resistance and the load current, respectively. The difference between Level 1 and Level 2 models is very small at nominal operating conditions. However, at 50 A load current (twice the nominal current) the deviations become more significant, affecting the accuracy of the turn-on energy losses. This is shown in Figure 21 that depicts the overlay of the load-current dependency of the switching energy losses, as given in the datasheet, with the values extracted from the simulated transient curves. As the behavioral Level 1 model is calibrated on the switching energies for nominal conditions, E_{on} and E_{off} match quite well to the datasheet values at 25 A. Whereas, for the Level 2 model the deviation is less than 30%. The Level 2 model, calibrated only on static characteristics and gate-charge curves, predicts the transient behavior of the device quite well as it is based on semiconductor physics. Its benefit becomes clear when the load current is 50 A. As the Level 1 model is not calibrated for this operation, its error is higher than 30% while the error of the Level 2 model is lower than 10%.



(a) Turn-on | (b) Turn-off

Figure 19 Simulated transient curves of IKW25N120H3 for nominal switching conditions (T_j = 25°C, V_{cc} = 600 V, I_C = 25 A) with gate resistance variation



(a) Turn-on | (b) Turn-off

Figure 20 Simulated transient curves of IKW25N120H3 for nominal switching conditions (T_j = 25°C, V_{cc} = 600 V, R_G = 20 Ω) with load current variation

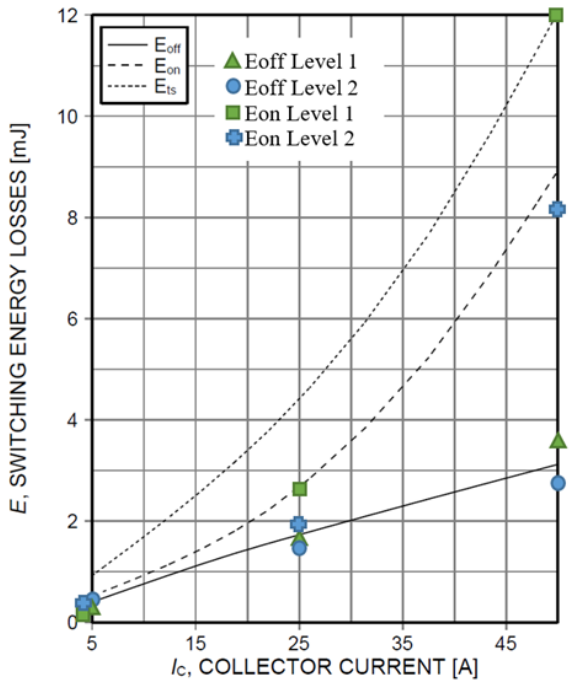


Figure 13. **Typical switching energy losses as a function of collector current**
(ind. load, T_j=175°C, V_{CE}=600V, V_{GE}=15/0V, r_G=23Ω, test circuit in Fig. E)

Figure 21 Comparison of datasheet and simulation current dependency of switching energy losses for IKW25N120H3 (T_j = 25°C, V_{CC} = 600 V, R_G = 23 Ω, V_{GE} = 15/0 V)

In conclusion, both Level 1 and Level 2 compact models for the IGBT are useful simulation tools to perform electrical simulations where the electrical behavior of the device is represented with a decent accuracy.

Level 1 models provide faster computation speed and reasonable accuracy within the calibrated range.

Level 2 models provide a more precise representation of the switching transients over a wide range of operating points but these can result in slower simulation times and convergence instability.

4 Infineon PLECS models for IGBTs and power silicon diodes

PLECS® is a modeling and simulation tool that enables simulation of complete systems, including power sources, power converters, and loads. PLECS software is integrated with a wide component library that includes electrical, magnetic, thermal, and mechanical components to simulate power conversion systems and their controls. Power electronics circuits are captured through a schematic editor in a way that is easy to use for the user. The schematics can be drawn easily by selecting the components and connecting them by wire connections [5].

4.1 Model library files

PLECS uses a library of thermal models for semiconductor devices. Infineon provides PLECS-compatible thermal models based on the values of product datasheets. The PLECS model can be considered as an electronic version of the product datasheet, where the most important electrical and thermal parameters of semiconductors are presented. It is, therefore, possible to easily model the power dissipation of a specific device by using generic electrical switch models available in the PLECS library [5].

4.1.1 Model categories

The PLECs model of Infineon's discrete IGBTs and diodes contains information from the product datasheet that is required for calculating power dissipation and junction temperature. The models use XML format to describe the behavior of each chip in the product. For products that contain two chips, for e.g. IGBTs with antiparallel diode, two PLECS models are created – one for the IGBT and one for the diode. The model file is named as:

<part number>_<type>.xml

For e.g., in the case of the IGBT, **IKD06N65ET6**, the model file name for the IGBT part will be IKD06N65ET6_igbt.xml and the model file name for its co-packed diode will be IKD06N65ET6_diode.xml. Please note that the dynamic parameters given in the datasheet for co-packed or reverse conducting IGBT are always measured with the same part number on the low and the high side. Figure 22 shows an IGBT characterized by using its own co-packed diode on the high side.

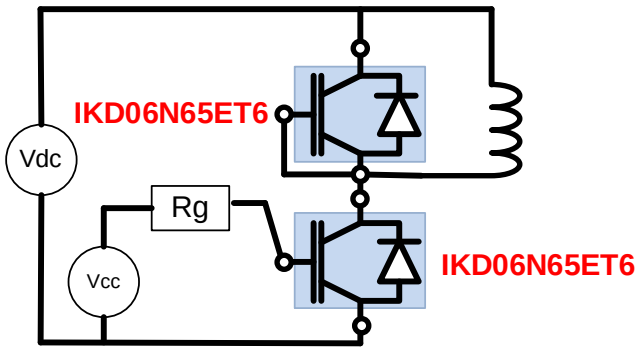


Figure 22 Measurement board setup for co-packed IGBTs

For products that contain only a single IGBT die, the model is named as <part number>_igbt.xml, for e.g. **IGD06N65T6**_igbt.xml. In this case (Figure 23), the diode used on the high side to characterize the IGBT is usually mentioned in the datasheet table.

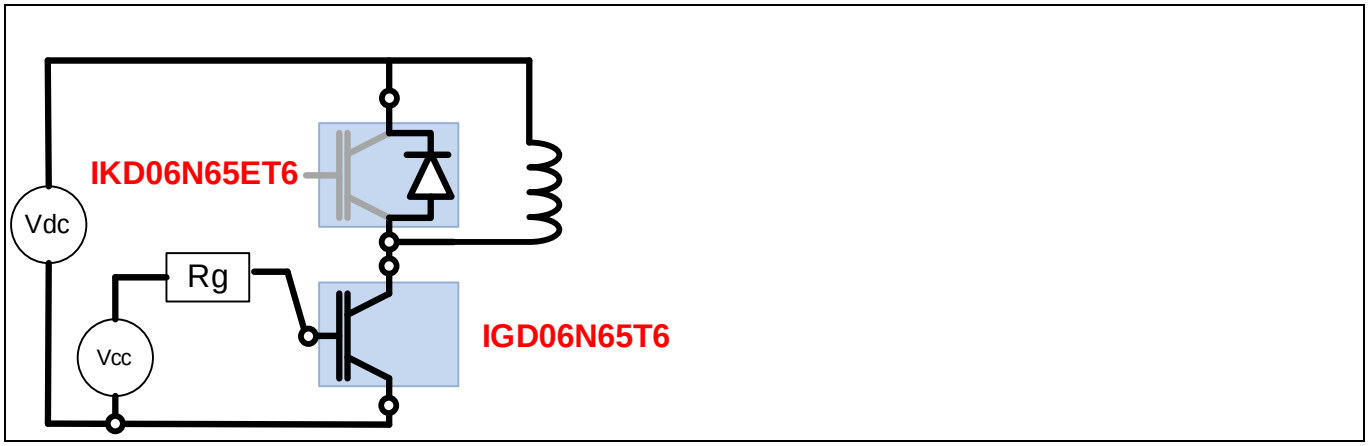
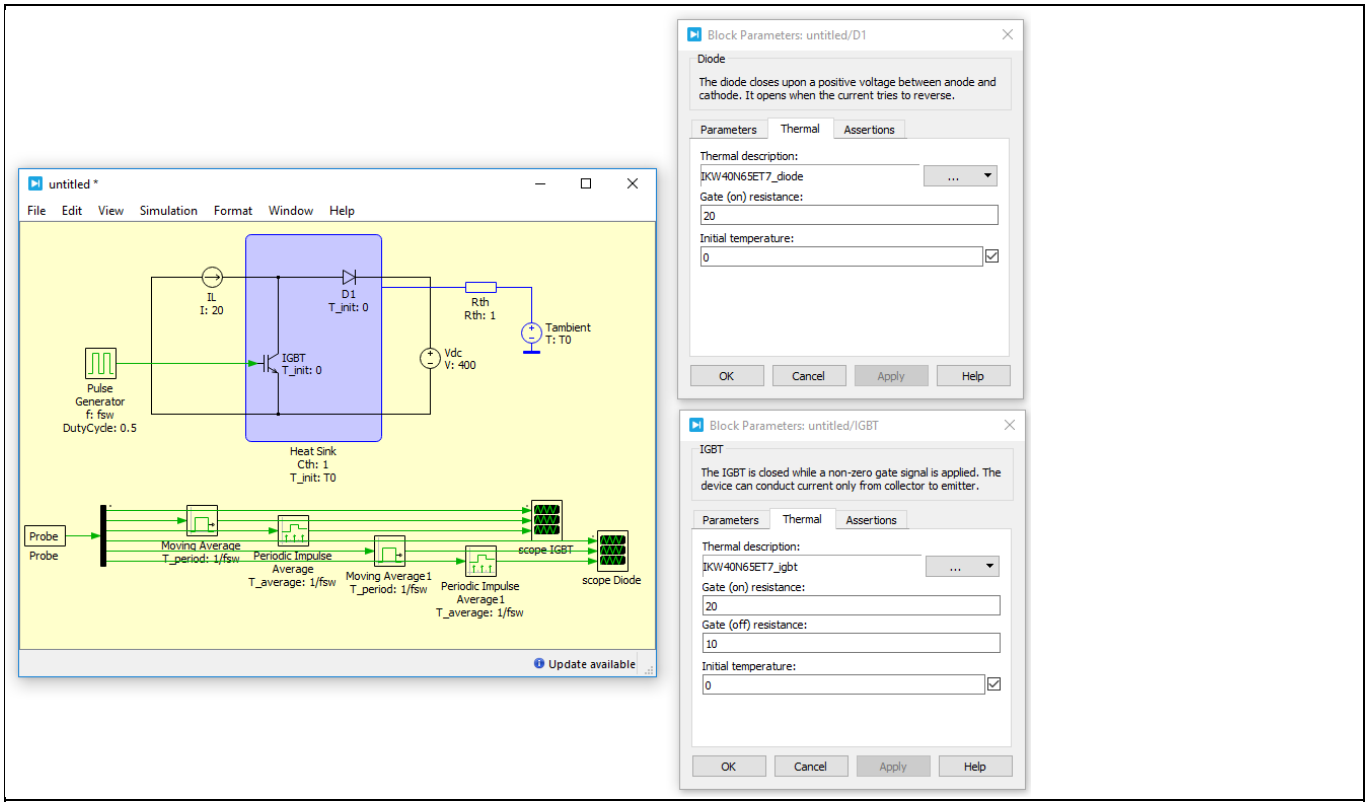
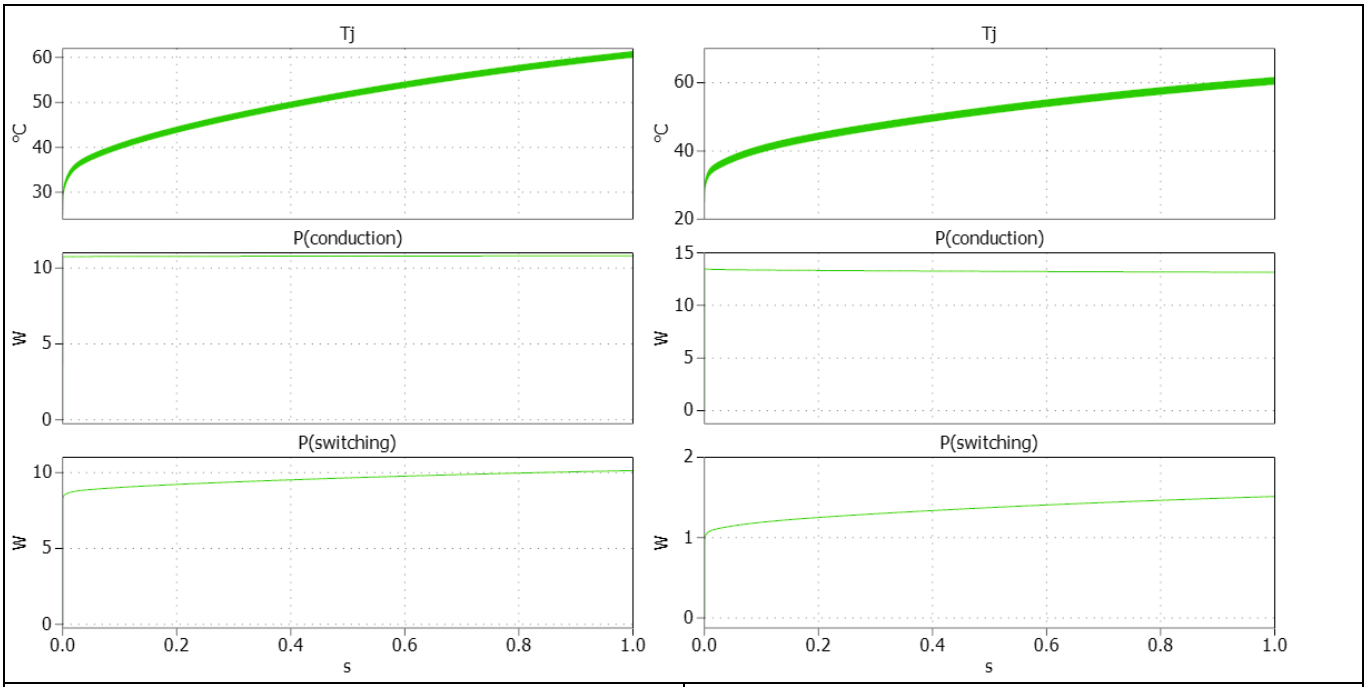


Figure 23 Measurement board setup for a single IGBTs without antiparallel diode

Figure 24 shows the PLECS simulation for a simple boost topology using the IGBT and diode PLECS models for the part, IKW40N65ET7. The switching frequency is 10 kHz and initial system temperature is 25°C.



(a) Schematics of the boost converter



(b) IGBT power dissipation and junction temperature

(c) Diode power dissipation and junction temperature

Figure 24 PLECS simulation for the boost topology

In addition to these regular models that are available for all Infineon discrete devices, there are two other categories of models that have been developed specifically for the requirements of a particular application. These models are the PFC (Power Factor Correction) models and the soft-switching models.

4.1.1.1 PFC models

The PFC models contain data that is based partly on information from the product datasheet and partly on dedicated measurement values. These thermal models are created to simulate losses in applications such as boost PFC converters, where the complementary switch is a separate stand-alone diode. These models are called PFC models because the devices characterized in this category are tailored for PFC applications.

Depending on the requirements of the application (for e.g. switching frequency, EMI (electromagnetic interference) or switching losses), the standalone diode can be a silicon diode, such as the Rapid I or Rapid II diode, or a SiC diode. Switching losses in hard switching circuit topologies are highly dependent on diode reverse recovery performance. Therefore, these special models include switching losses measured specifically for a particular IGBT-diode combination and provide a more realistic result. This is in contrast to the regular models that are based entirely on the content available in the product datasheet. As explained earlier, the switching loss values given in the datasheet for a co-packed and reverse conducting IGBT are measured against its own anti-parallel diode. If the anti-parallel diode is not optimized for reverse recovery performance, it can worsen the turn-on switching energy loss of the IGBT.

An IGBT-diode combination is indicated in the nomenclature of the model. The name of the model includes the IGBT part number and the diode part number that was used in the measurement of the Dynamic switching transient test circuit. For each IGBT-diode pair, there are two models – one for the IGBT and one for the diode. For any given pair, the models are named as follows:

- Diode: IGBT part number**o**diode part number_diode.xml
- IGBT: IGBT part number**o**diode part number_igbt.xml

The IGBT and diode names are separated by the letter "o". For e.g., the IKWH30N65WR6oIDW30C65D1_igbt model includes the switching losses of the IGBT IKWH30N65WR6 that are measured against the diode IDW30C65D1; and vice versa for the switching losses of the diode IDW30C65D1 in the model IKWH30N65WR6oIDW30C65D1_diode.

4.1.1.2 Soft-switching models

For induction-heating applications, circuits with resonant topologies such as a single-ended parallel resonant circuit and a half-bridge resonant circuit are used. Infineon offers a wide range of discrete IGBTs in both high voltage and low voltage classes, optimized for best performance in these applications. Resonant topologies, because of their mode of operation, offer the advantage of soft switching that eliminates turn-on losses because the device is turned on when the voltage across it is zero. The only switching loss that occurs in the device is during the turn-off transient.

Achieving soft-switching operation in turn-off is also possible, but it comes at the cost of additional electrical components such as a resonant capacitance. The resonant capacitance causes the device to slow down its switching speed and the resulting turn-off losses depend on the value of the snubber capacitance. Infineon's soft-switching models define the dependence of E_{off} on snubber capacitance, other electrical parameters, and the junction temperature of the device. Figure 25 shows the E_{off} values as a function of device current at various values of resonant capacitance. This is also given in the device datasheet.

For the half-bridge resonant topology, a 650 V reverse conducting devices can be used. For single-ended parallel resonant topology, devices with a voltage class of 1100 V and above are used. Infineon offers soft-switching PLECS-compatible models tailored to Induction heating application, for all these devices.

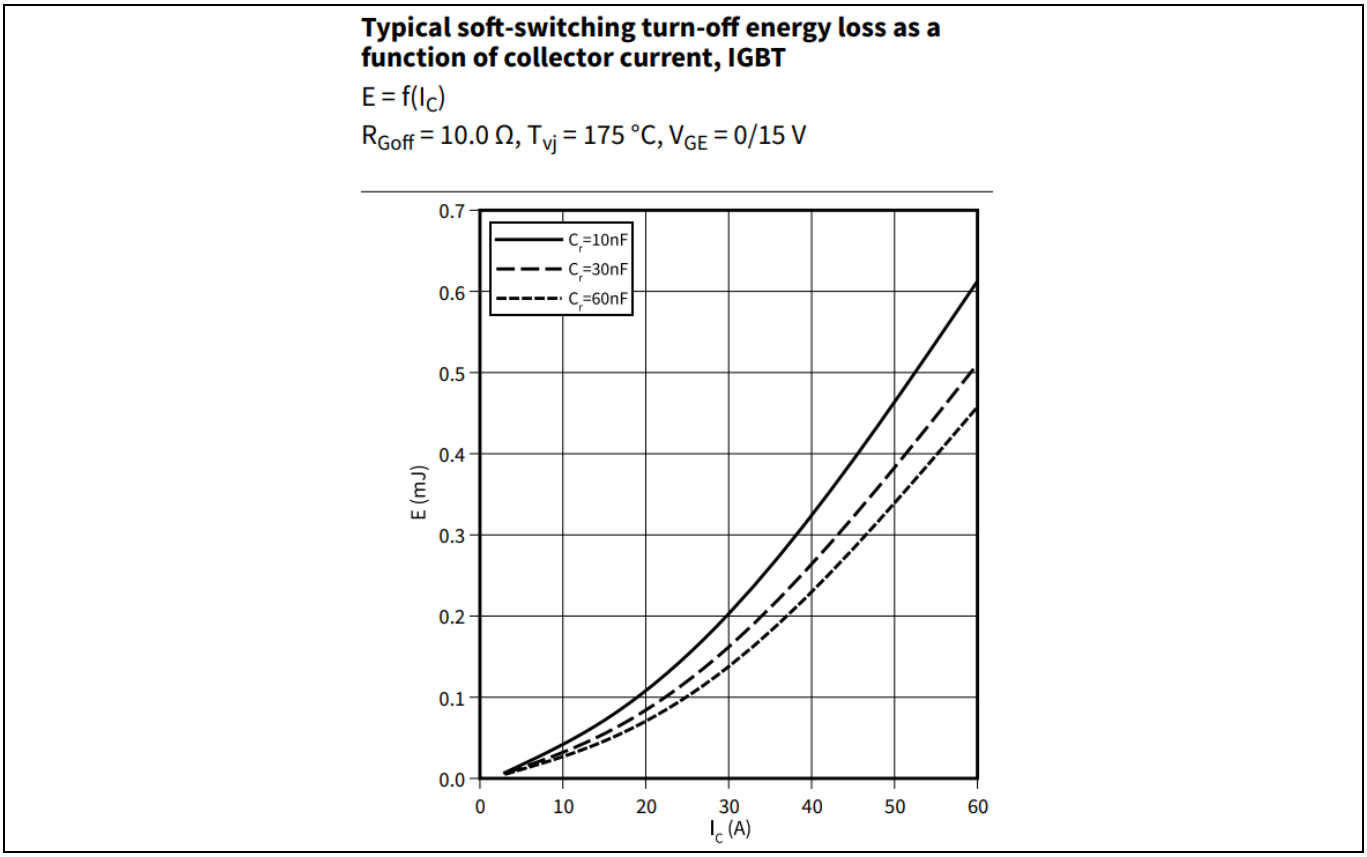


Figure 25 E_{off} losses of IHW30N65R6

4.1.2 Library implementation in PLECS

Infineon's PLECS models are provided in a zip file containing all the devices that are based on a specific technology. To use the models, users have to unzip the file and copy the .xml files in the PLECS search path for thermal libraries, as shown in Figure 26 [6].

To install simulation models from the product website, users can follow these steps:

1. Extract the models downloaded from the website in the appropriate folder.
2. Open **Files** → **PLECS Preferences…**. Under the Thermal tab, click **Rescan** to refresh the library (Figure 26.) Restarting PLECS will have the same effect.

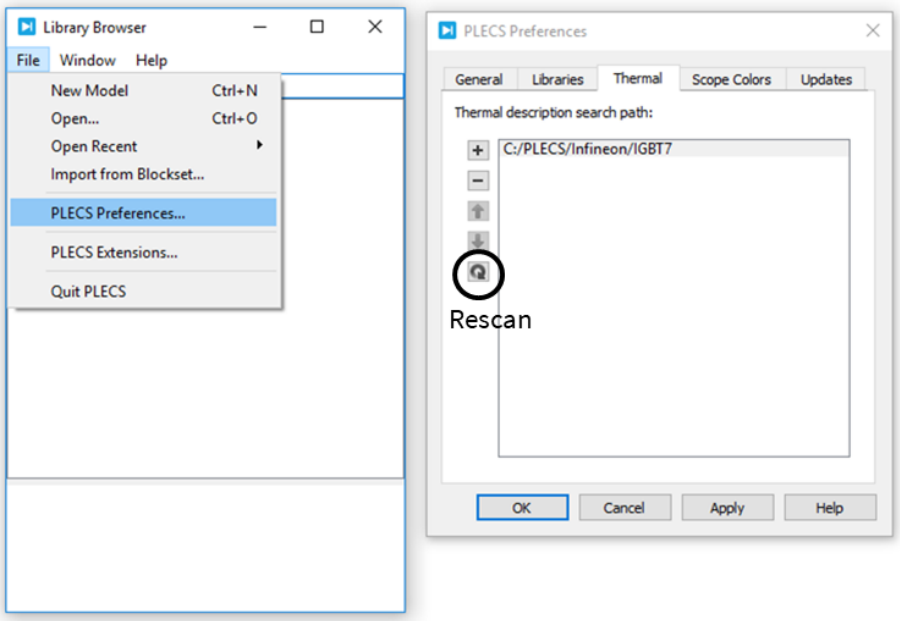


Figure 26 PLECS models' folder selection

3. From the library browser, choose the appropriate power semiconductor that needs to be simulated (IGBT, diode, MOSFET, etc.) For an IGBT with an anti-parallel diode, select the IGBT and the diode symbols separately. Do NOT choose the "IGBT with Diode" symbol. This is because PLECS assigns the junction temperature to the symbol, and to simulate the junction temperature behavior of the IGBT and diode separately, two symbols are needed. In any case, the IGBT and diode models from Infineon are provided in two different .xml files[1].

In the context menu of the symbol, open the **Parameters** menu and select **Thermal**. For the Thermal description choose the preferred model **From Library…**. Only models that are valid for the specific device (for e.g. IGBT or diode) are listed in the menu (Figure 27.)

[1] To distinguish between IGBT and diode models, refer to section 4.1.1.

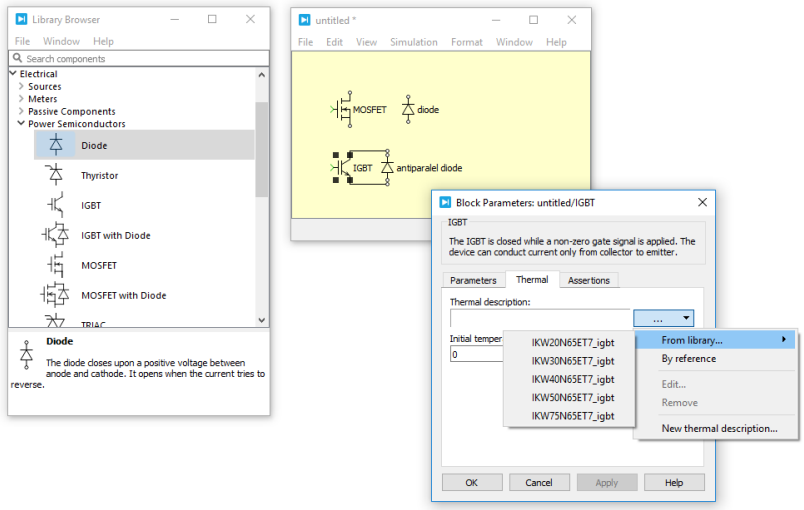
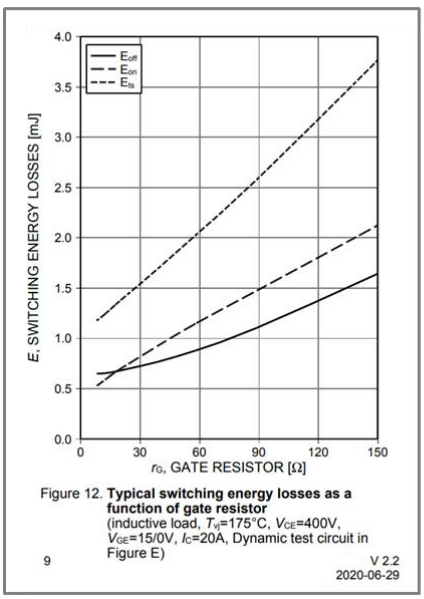


Figure 27 Model selection

Depending on the model, different parameters can appear after the model is chosen. For e.g., for the IGBT model of the IKW20N65ET7, two additional parameters appear: Gate (on) resistance and Gate (off) resistance. This means that the model implements the dependence of the switching losses on gate resistance. The additional parameters are needed to calculate the losses correctly and cannot be left empty. The range of these parameters is, in principle, unlimited but the proper behavior of the model is calibrated based on the datasheet values. Which means, using parameter values outside the range provided in the datasheet charts can result in inaccurate results. For e.g., the range of values for the gate resistances of IKW20N65ET7, for which the model is calibrated, is between 8 Ω and 150 Ω, as shown in Figure 28.



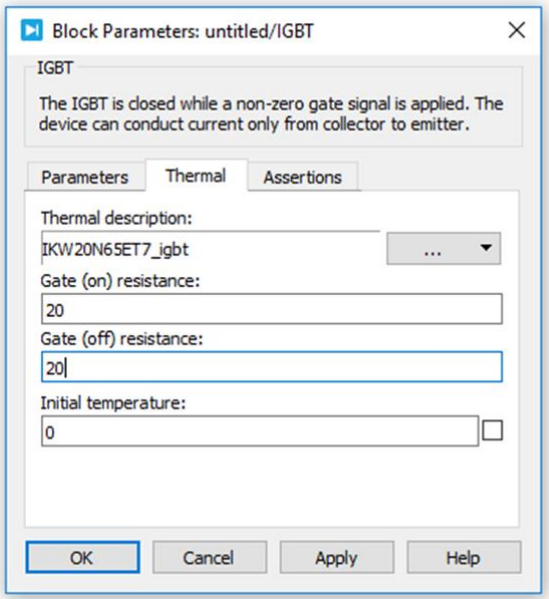


Figure 28 R_g dependent PLECS model for the IGBT

5 Conclusion

Infineon provides several simulation models for the silicon IGBTs and power diodes.

If the main purpose of the simulation is to estimate power losses and the junction temperature behavior in a system-level simulation, the usage of PLECS models is recommended due to low computation times. This is particularly true for long simulations (in the range of several minutes).

If the main purpose of the simulation is to understand the switching behavior of the device and the inherent effects (for e.g. reverse-recovery, Miller plateau, gate charge, etc.), any one of the following SPICE models is recommended:

- Level 1 models offer fast computational times and good accuracy within the calibrated conditions. It is the best choice whenever SPICE simulations have to be run according to the test conditions in the datasheet. With Level 1 models, longer simulation runs (of 10 seconds or more) can be performed with acceptable computational times
- Level 2 models offer slower computation times but give more accurate results over a wider range of conditions. These models should be used if simulations have to be performed with test conditions that are not covered by the datasheet (for e.g. different R_{gs}, different stray inductances, different supply voltages, etc.) With Level 2 models, short simulations (of up to 10 seconds) are preferable due to longer computational efforts

6 Contact address

For questions related to simulation models, users can contact Infineon's local sales offices or send an email to support@infineon.com.

7 References

[1] https://www.infineon.com/cms/en/product/power/igbt/?redirId=54367#!simulation

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[3] R. Kraus, K. Hoffmann, An Analytical Model of IGBTs with Low Emitter Efficiency, IEEE 1993

[4] R. Kraus, P. Tuerkes, J. Sigg, Physics-based Models of power semiconductor devices for the circuit simulator PSPICE, IEEE 1998

[5] https://www.plexim.com/products/plecs

[6] https://www.plexim.com/sites/default/files/plecsmanual.pdf

Revision history

Document version	Date of release	Description of changes
1.0	12-10-2020	First version
1.1	19-03-2021	Added PLECS models section
1.2	05-04-2022	Added the sub-sections: PFC and soft switching models

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