EiceDRIVER™ F3 – Single-channel enhanced isolated gate driver family with short-circuit protection

Technical description - 1ED332xMC12N

About this document

Scope and purpose

This document gives an overview of the basic behavior and application-related considerations of the 1ED332xMC12N family listed in Table 1, and describes, in particular, the dimensioning of external components that are used in a typical application.

Table 1 EiceDRIVER™ 1ED332xMC12N (F3) product family

Product name	Gate driver current (typ.)	Outputs	UVLO	Fault switch-off
1ED3320MC12N	+3.3 A / -6 A	OUTH/OUTL	12 V	Soft-off
1ED3321MC12N	+6 A / -8.5 A	OUTH/OUTL	12 V	Soft-off
1ED3322MC12N	+6 A / -8.5 A	OUTH/OUTL	13.6 V	Hard-off
1ED3323MC12N	+6 A / -8.5 A	OUT	13.6 V	Hard-off

Intended audience

The intended audience for this document are hardware design engineers of power electronic systems.

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1 Introduction

The 1ED332xMC12N family is a group of enhanced, galvanically isolated, single-channel driver ICs in a DSO-16 300 mil package. These driver ICs provide typical peak output currents of up to 8.5 A. The 1ED332xMC12N family includes a combination of features aimed to address the market, including soft-off and hard-off fault turn-offs, IGBT and SiC undervoltage lockout (UVLO) settings, two different output current strengths, and two different output configurations.

The 1ED3323MC12N is designed to be a direct replacement for the Infineon EiceDRIVER™ 1ED020I12-F2 and comes with a much stronger output stage.

The input logic terminals of 1ED332xMC12N operate safely with supply voltages of 3.3 V and 5 V. All input structures have threshold levels proportional to the supply voltage.

A wide range of output-side supply voltages (up to 40 V) can be configured for positive and negative voltages as long as the absolute maximum of 40 V is not exceeded. All driver ICs have output sections with active shutdown.

Data transfer across the isolation barrier is achieved by the coreless transformer technology.

Note: For easy evaluation and better understanding of the Infineon EiceDRIVER™ 1ED332xMC12N gate driver IC family, the Eval-1ED3321MC12N evaluation board can be used.

2 Input side

The input side of the gate driver IC contains two inputs *IN+* and *IN-* for the control signals, two power terminals *VCC1* and *GND1* for the reference and supply of the input chip, an *RDY* output for internal state feedback, a */FLT* output for fault state feedback, and a */RST* input for resetting the fault state.

Its input features also include undervoltage lockout of input supply, pull-up and pull-down resistors of logic inputs and outputs, and signal filtering.

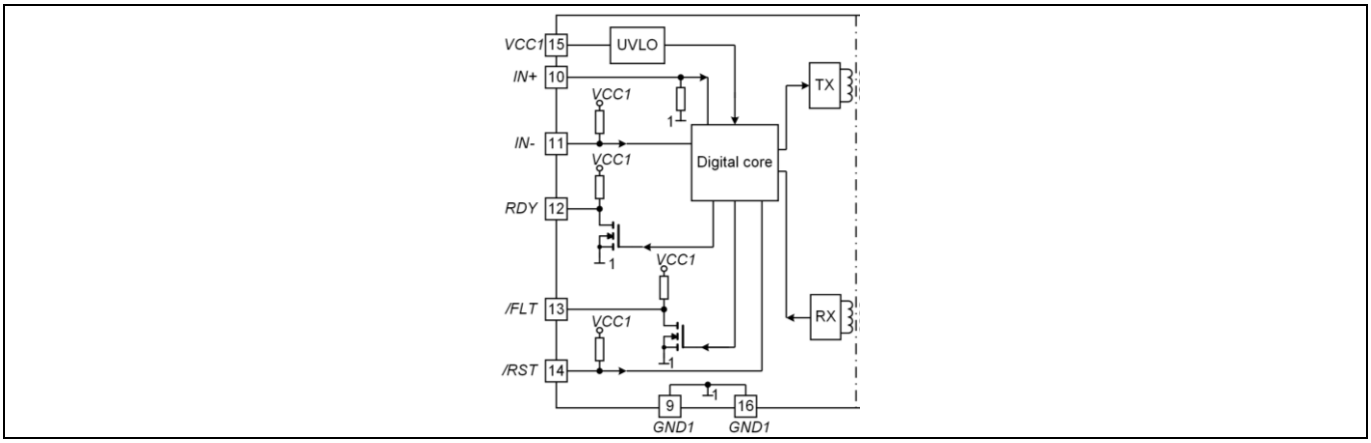

Figure 1 Block diagram of the input side

2.1 Input side power supply

The supply voltage on the input side can range from V_{VCC1} = 3.3 V to 7 V. This provides margins for spikes and coupling on the supply rail in non-optimal layouts with respect to the standard supply voltage of 3.3 V. Operation outside the absolute maximum voltage ratings may result in internal IC damage, and is prohibited.

The supply voltage should be blocked by a suitable low-impedance capacitor and a low-impedance layout to the origins of the supply voltage. The capacitor should be placed in immediate proximity to the driver IC. This will stabilize the supply conditions of the IC's input side. The highlighted loop in the Figure 2 showns the supply stray inductance that should be minimized as much as possible.

A 1 µF decoupling capacitor is generally suitable for most operations.

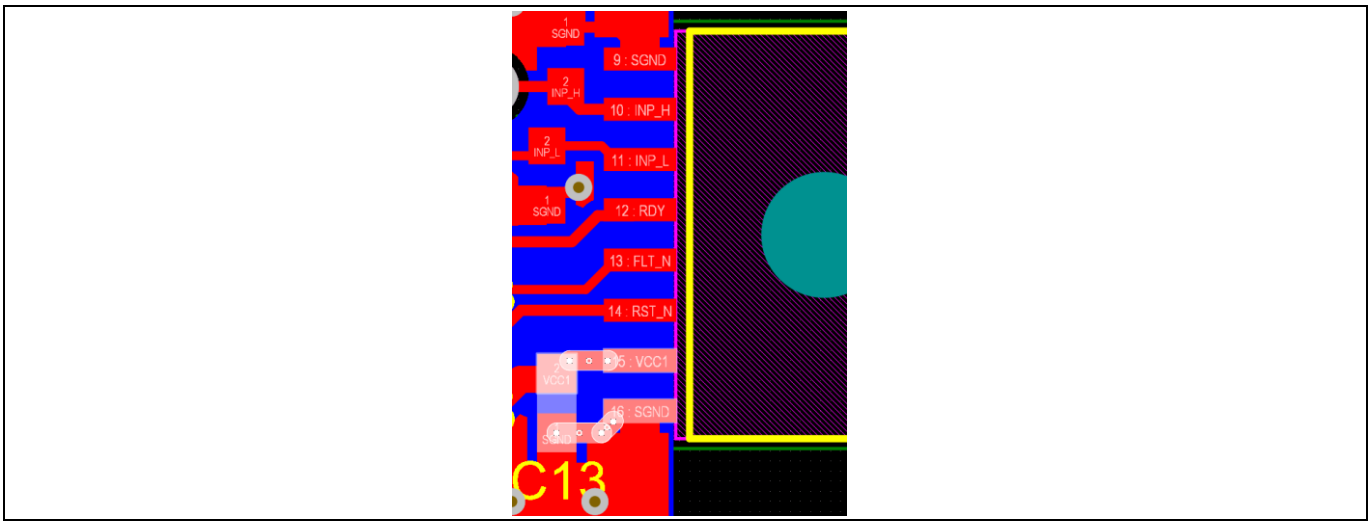

Figure 2 Good layout practices for supply capacitor at terminal *VCC1*

2.2 Pull-up and pull-down resistors for the input side signals

The input pull-up or pull-down resistors ensure an off state in case the corresponding input is not connected. These resistors have a minimum value of 25 kΩ. Even with the maximum allowed voltage at VCC1 pin, the input current due to these resistors stays below 1 mA.

For the input pins, *IN+* and *IN-*, the pull-up and pull-down resistors are designed such that they can be connected to an external supply or ground potential for permanent activation of the individual driver input.

For the status output pins, */FLT* and *RDY*, the resistors are used to ensure that the open drain outputs return to high when the gate driver is in a normal operation mode. When operating in harsh environments, use of external pull-up resistors (e.g. 4.7 kΩ) is recommended for increased application safety. Similarly, for the */RST* input, the pull-up resistor ensures that it can be driven by an open drain signal.

2.3 Input side filtering

RC filters are a common way to suppress or reduce cross talk and parasitic coupling effects. However, external RC filters are imprecise and their tolerance is unsymmetrical as depicted in Figure 3.This can make the calculation of deadtime for half-bridge-based power converters more difficult, especially if the time constant is large.

The Infineon EiceDRIVER™ 1ED3332xMC12N IC family offers integrated noise filters with symmetric tolerance and high precision. The integrated noise filters help reduce the external RC filter to a minimum, thus reducing the tolerances to a minimum. The performance of this combined solution is often superior compared to gate driver ICs without integrated noise suppression filters.

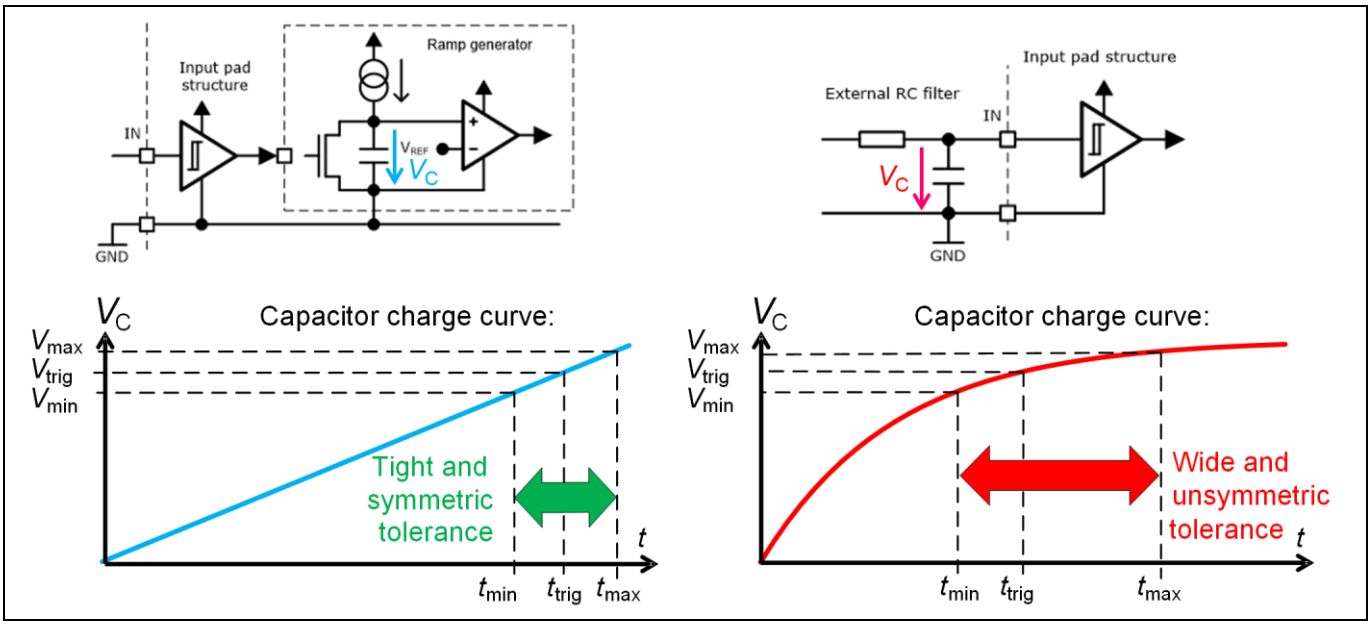

Figure 3 Tolerance of integrated filters (left) and external filters (right) for noise suppression

The input section of the driver IC filters all the input signals to suppress short pulses triggered by external influences.

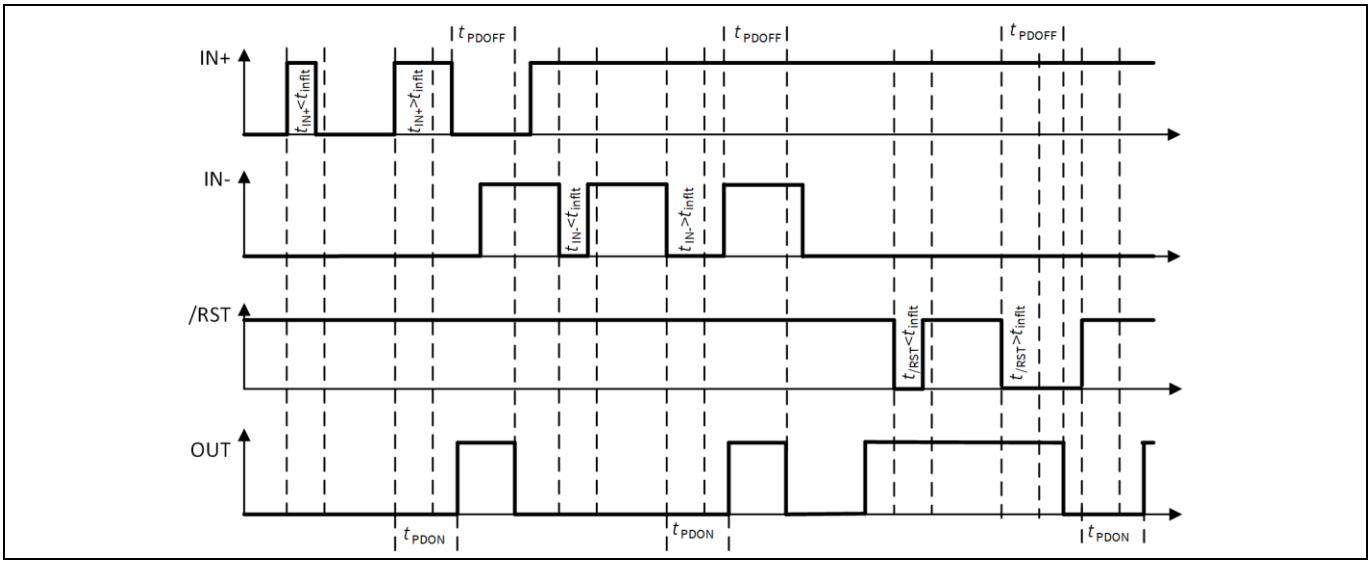

Figure 4 Input pulse suppression and turn-on/turn-off propagation delay

Every pulse at *IN+* shorter than the input pulse suppression time for pin *IN+* (t_{inflt}) is filtered and not transmitted to the output chip. Longer pulses are sent to the output with the propagation delay t_{PDON} and t_{PDOFF} as shown in Figure 4. This same behavior is implemented at *IN-* and */RST* inputs.

2.4 Application usage of *IN+* and *IN-*

The inverting (*IN-*) and non-inverting (*IN+*) input pins offer multiple possibilities to connect PWM input and logic signals for various control and protection uses.

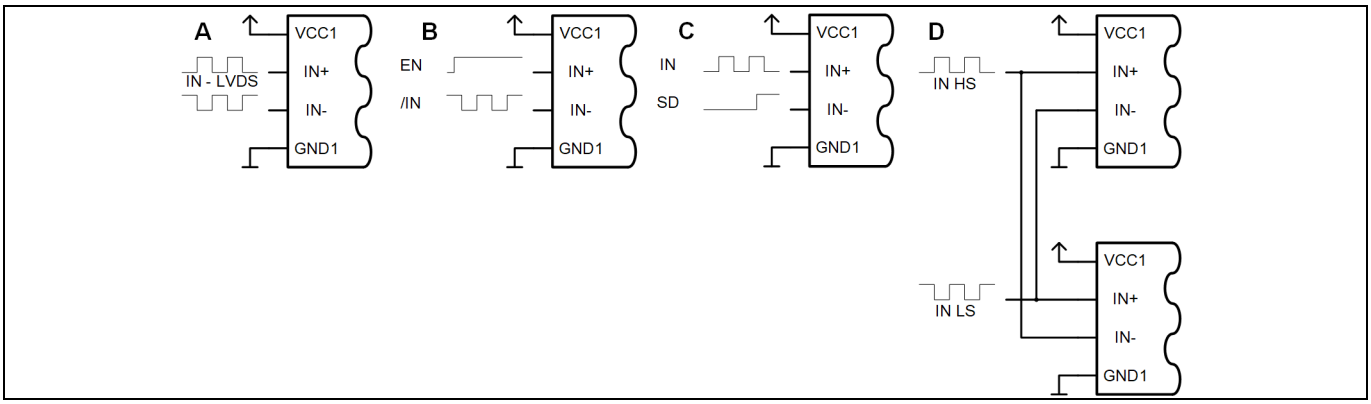

Figure 5 Input *IN+* and *IN-* usage

Apart from using both inputs with a differential signal (A) (*VCC1* and *GND1* levels), using only one input signal for actual switch control leaves the second input available for functions like Enable (B), Shutdown (C) or Interlock (D).

A) Differential signal

Applying a logic-level differential signal on both *IN+* and *IN-* with the positive level of *VCC1* pin and the negative level of *GND1* pin improves common-mode noise rejection.

B) Enable

Using the *IN+* pin as enable signal leaves the *IN-* to control the output PWM with an inverted logic input signal. The enable signal can then be shared between gate driver ICs of a complete inverter to start operation with a single control signal.

C) Shutdown

Using the *IN-* pin as shutdown signal leaves the *IN+* to control the output PWM with a non-inverted logic input signal. The shutdown signal can then be shared between gate driver ICs of a complete inverter to interrupt operation with a single control signal.

D) Interlock

Interlocking is often used in half-bridge configurations to avoid a shoot-through current from a high-voltage DC bus supply. Connecting together the following input signal pins of the top and bottom driver ICs inhibits a static turn-on for both channels at the same time:

- Top driver non-inverting input (*IN+*) with the bottom driver inverting input (*IN-*)
- Bottom driver non-inverting input (*IN+*) with the top driver inverting input (*IN-*)

Dynamic turn-on and turn-off characteristics of gate drivers and power switches can often lead to a short term shoot-through. To avoid overlapping turn-on times at the power switches, a proper deadtime setting for PWM generation at the microcontroller is recommended.

2.5 State feedback and reset signals

The gate driver comes with two state feedback outputs: *RDY* and */FLT* plus a reset input /RST.

RDY is an open-drain ready status output. It is used to signal the correct operation of the gate driver IC. When *RDY* is high, both input and output sides of the gate driver IC supply voltages are above the UVLO level, and internal communication between the two chips works correctly. During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the driven transistor is switched off and the *RDY* output reports an internal error.

/FLT is an open-drain fault reporting output used to signal a desaturation (DESAT) fault of the power transistor that is being driven. */FLT* is actively pulled low if desaturation has occurred.

/RST is an open-drain input that has the following two functions:

- Function 1: Enables or shuts down the gate driver IC. The outputs of the gate driver IC are actively pulled low when */RST* is low. The integrated filter ensures that the gate driver IC is robust against glitches.
- Function 2: Resets the DESAT fault state of the gate driver IC. For the gate driver IC to reset the DESAT fault state, signaled by the */FLT* output, the */RST* pin has to be pulled low for a time t_{RST}.

3 Output features

This section describes the gate driver output section of all the EiceDRIVER™ 1ED332xMC12N family variants.

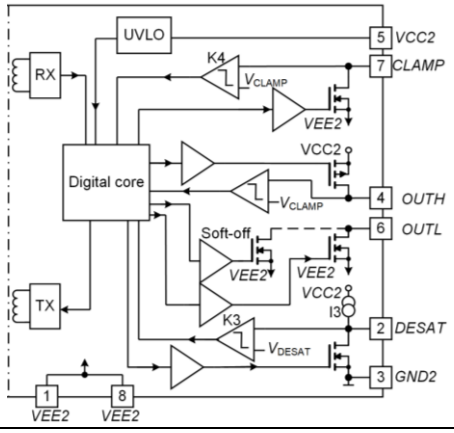

Figure 6 Block diagram of the output side

3.1 Output side power supply

The output supply range has a positive absolute maximum rating of 40 V for all variants. The gate driver ICs are therefore capable of providing a bipolar gate voltage to a connected power switch.

The undervoltage lockout thresholds of different gate driver variants are optimized to be used with IGBTs, Si MOSFETs, or SiC MOSFETs. All variants provide unlimited functionality for use with both IGBTs and MOSFETs.

Table 2 Output undervoltage lockout threshold levels

Parameter	Symbol	Value	Unit
1ED3320, 1ED3321, 1ED3323 maximum turn-on level	V_{UVLOH2}	12.6	V
1ED3322 maximum turn-on level	V_{UVLOH2}	14.2	V
1ED3320, 1ED3321, 1ED3323 minimum turn-off level	V_{UVLOL2}	10.4	V
1ED3322 minimum turn-off level	V_{UVLOL2}	11.9	V

The 1ED332xMC12N driver is designed to support two different supply configurations - bipolar supply and unipolar supply.

For example: as shown in Figure 7, for an IGBT operation, in a bipolar supply configuration the driver is typically supplied with a positive voltage of 15 V at *VCC2* and a negative voltage of -8 V at *VEE2*. The negative supply prevents a dynamic turn-on during fast dV/dt transients. If an appropriate negative supply voltage is used, connecting CLAMP to IGBT gate becomes redundant but it is still recommended.

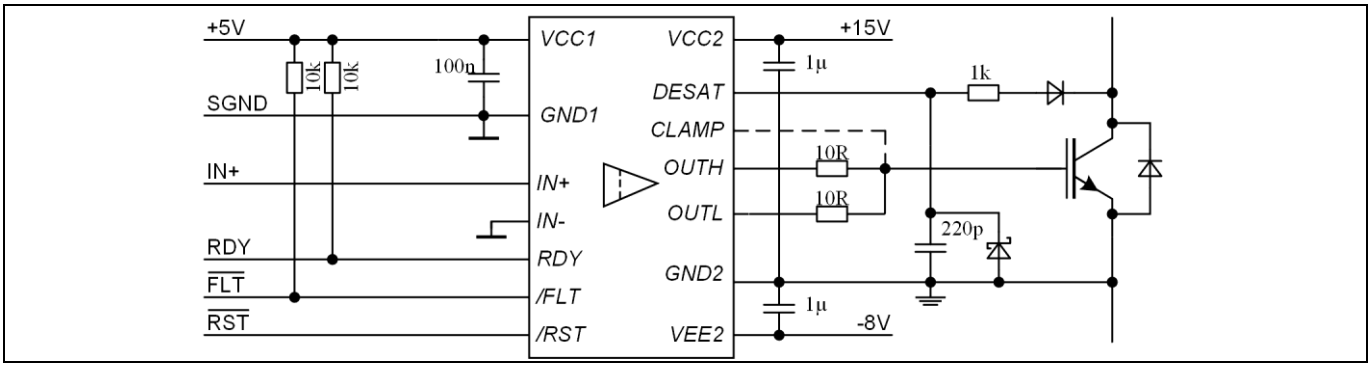

Figure 7 Application example of bipolar supply

In a unipolar supply configuration, the driver is typically supplied with a positive voltage of 15 V at *VCC2*. *VEE2* has to be connected to *GND2*.

To avoid erratic turn-on of the IGBT due to fast dV/dt, the active Miller clamp function can be used. As shown in Figure 8, the CLAMP output is directly connected to the IGBT gate.

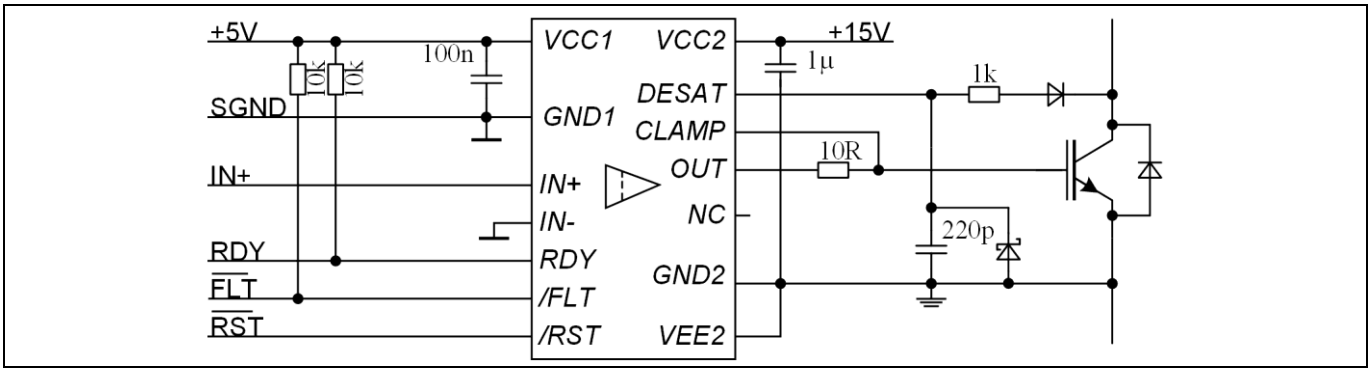

Figure 8 Application example of unipolar supply

3.2 Output terminals *OUTH* and *OUTL* or *OUT*

With separated outputs for current sourcing and sinking in a gate driver IC, individual gate resistors can be used for turning a power switch on and off. To maintain footprint compatibility with the Infineon EiceDRIVER™ 1ED020I12-F2, the 1ED3323MC12N has only one output pin, *OUT*, that both sources and sinks current.

The driver IC's output section at output terminal(s) provides a rail-to-rail output. This feature enables tight control of the gate voltage during the on state. It ensures that even during short-circuits the gate voltage does not increase above the *VCC2* supply voltage. Due to the low internal R_{DSon} of the IC, the switching behavior of the power transistor is mainly dominated by the gate resistors. This generates a low internal voltage drop, reducing the power that is dissipated by the driver IC.

The active shutdown feature of output(s) ensures a safe off state of the power transistor in case the output side is not connected to a power supply or an undervoltage lockout is in effect. The transistor's gate is clamped at terminal *OUT*/*OUTL* to *VEE2*.

3.3 Short circuit clamping

During a short-circuit, the power transistor gate voltage tends to rise because of the feedback via the Miller capacitance. An additional internal protection circuit connected to *OUT* or *OUTH* and *CLAMP* limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10 µs can be fed back to the supply through one of these paths. If higher currents are expected or a tighter clamping is desired, external Schottky diodes have to be added.

3.4 Active Miller clamp terminal - *CLAMP*

The active Miller clamping function reduces the risk of a parasitic turn-on during a high dV/dt transition at the connected IGBT or power transistor.

Displacement currents through the intrinsic gate collector, C_{GC}, and gate emitter, C_{GE}, capacitances can lead to a voltageincrease at V_{GE}. When the voltage reaches the IGBT threshold, the power switch is dynamically turned on. It stays on until the regular discharge path through R_G reduces the gate voltage. For example, in a half-bridge configuration, the switched off IGBT tends to dynamically turn on during the turn-on phase of the opposite IGBT.

The implemented CLAMP function of this gate driver IC monitors the gate voltage during the clamp inactive state. It activates an additional discharge path between *CLAMP* and *VEE2* as soon as the gate voltage drops below 2 V (related to *VEE2*). The clamping circuit stays active until the gate driver is turned on again. To achieve the most effective clamping results, the circuit layout between the gate and *CLAMP* pin has to be optimized for lowest possible inductance.

Figure 9 shows a simplified block diagram snippet with only the CLAMP function and the connection to an IGBT.

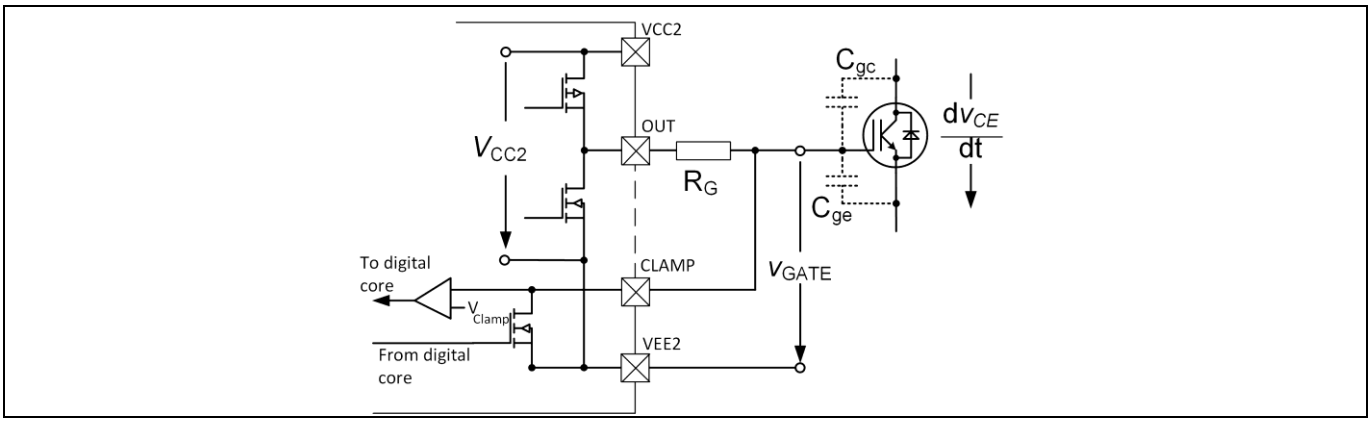

Figure 9 Simplified output block diagram showing only the CLAMP function and connection to an IGBT

3.5 Short-circuit protection – DESAT

A desaturation protection ensures the protection of the IGBT during a short-circuit (i.e. current larger than 5 times the rated value, not for over-current). The *DESAT* pin of the EiceDRIVER™ 1ED332xMC12N family monitors the collector-emitter voltage, V_{CE} of the IGBT to detect desaturation caused by short-circuits. When the *DESAT* voltage rises and reaches a defined value, the output of the driver chip is driven low and the */FLT* output is activated.

A programmable blanking time, $t_{DESATBLANK}$ is used to provide enough time for the IGBT saturation during a normal turn-on operation. This blanking time is provided through a highly precise internal current source and an external capacitor.

As shown inFigure 10, fault detection circuit monitors the IGBT's emitter to collector voltage, V_{CE}. A high current in IGBT might cause the transistor to desaturate. This condition results in an increase of V_{CE}. Due to the presence of diode, D_{DESAT}, after the leading-edge blanking time, $t_{DESATleb}$ elapses, an internal current source, I_{DESATC} (500 µA) starts charging up the external capacitor, C_{DESAT}. When the *DESAT* voltage at C_{DESAT} rises and reaches the DESAT reference level, $V_{DESATth}$ (9 V), the gate is turned off by the digital core of the output section.

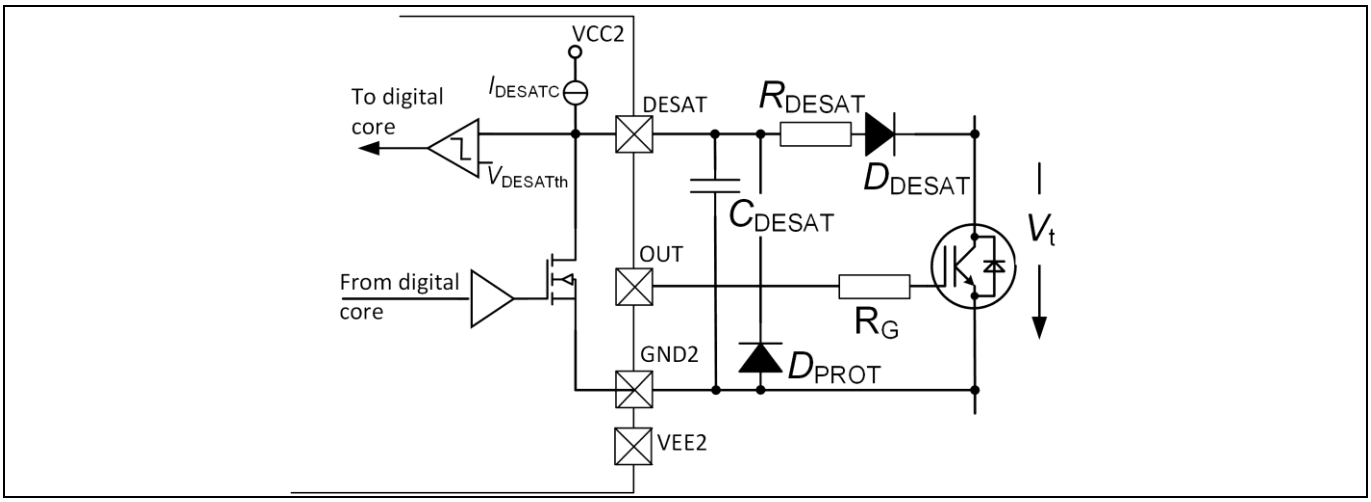

Figure 10 DESAT circuit snippet

It is recommended to use a protective diode, D_{Prot} at *DESAT-GND2* to limit the amount of negative voltage to the *DESAT* input. It is not allowed to go below -0.3 V according to the absolute maximum ratings. The diode, D_{DESAT} should be chosen based on the IGBT collector-emitter's absolute maximum ratings, low stray capacitance, and low recovery current (to minimize noise coupling and switching delays).

Depending on the EiceDRIVER™ 1ED332xMC12N variant used, this could be a hard-off or a soft-off.

As shown in Figure 11, if the hard-off variant is used, the gate is switched off faster during a normal operation.

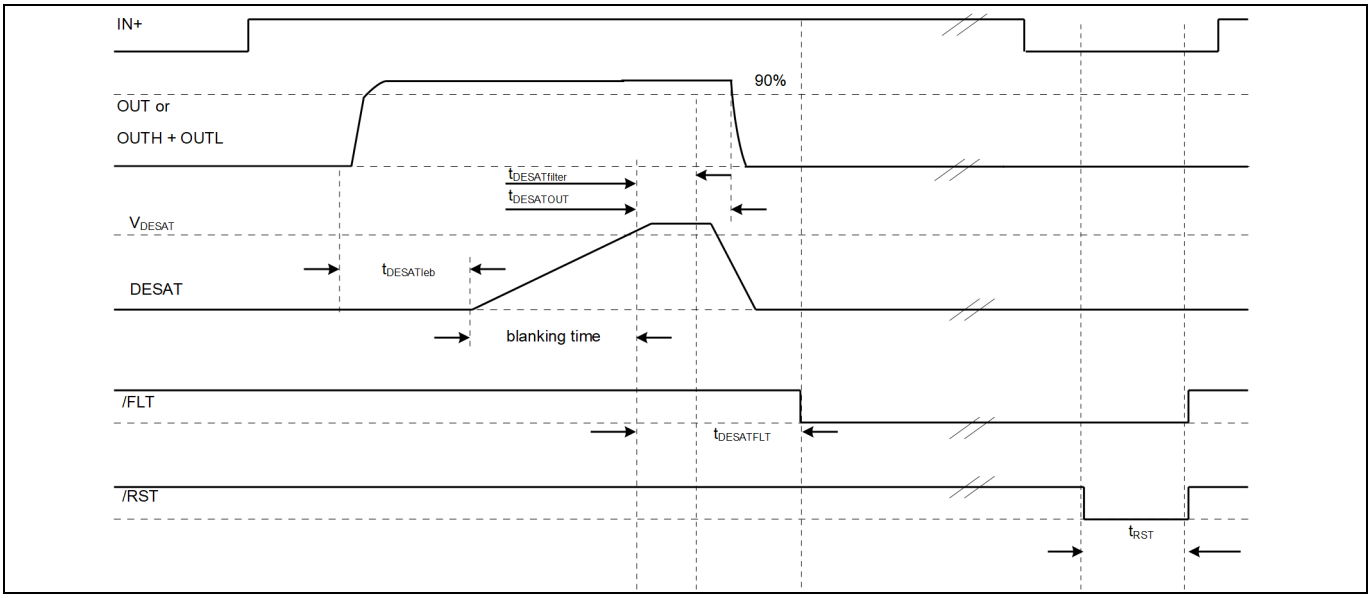

Figure 11 DESAT timing diagram with a hard-off turn-off

In the case of a soft-off variant, as shown in Figure 12, an internal current source is used to turn-off the gate in a controlled way. This minimizes the power transistor turn-off overshoot generated by circuit inductance and high short-circuit currents.

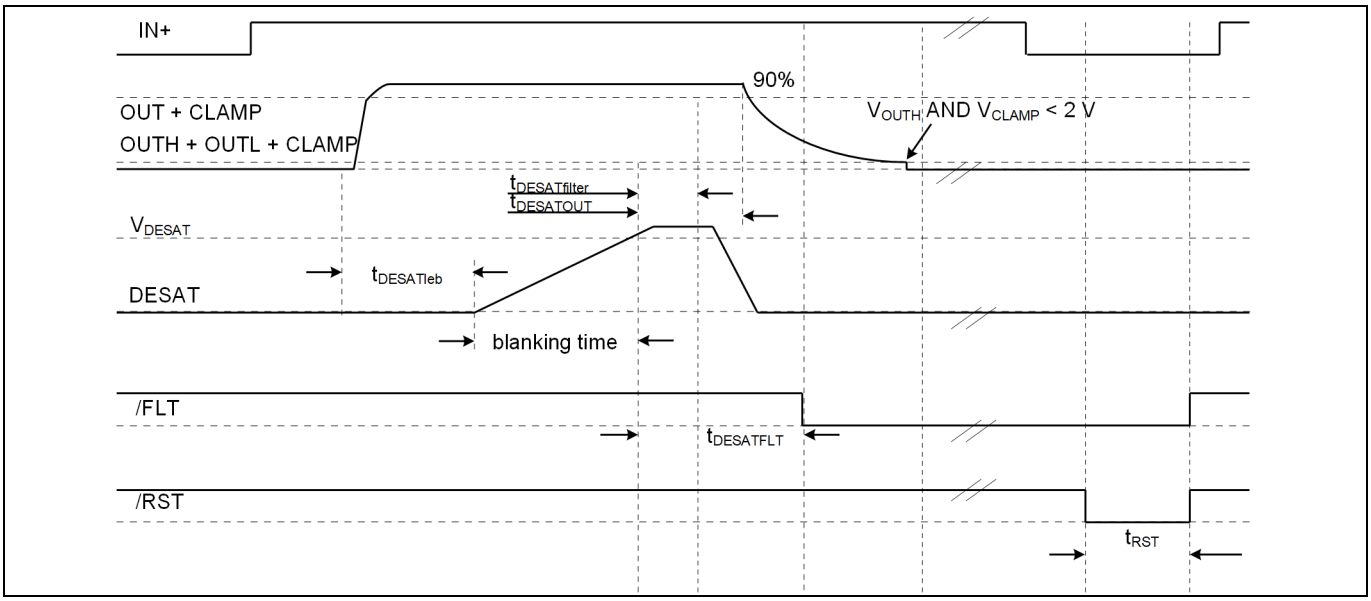

Figure 12 DESAT timing diagram with a soft-off turn-off

The external capacitor, C_{DESAT} defines the DESAT blanking time, $t_{DESATBLANK}$. It can be expressed as per the following equation:

$$C_{\mathrm{DESAT}} = \frac{I_{\mathrm{DESATC}} \cdot t_{\mathrm{DESATBLANK}}}{V_{\mathrm{DESATth}}} \quad (1)$$

If the C_{DESAT} value is too big, it will slow down the charging procedure and result in slow sensing of desaturation current. This can be dangerous considering the short-circuit withstand time, t_{SC} of IGBTs (typically <10 µs). The choice of C_{DESAT} must fulfill the following condition:

$$t_{\mathrm{DESATBLANK}} + t_{\mathrm{DESATOUT}} < t_{\mathrm{SC}} \quad (2)$$

here the $t_{DESATOUT}$ is the desaturation sensing delay to out low that is defined in the product datasheet. It is recommended to choose a DESAT capacitance of C_{DESAT} = 56 pF that corresponds to a blanking interval of $t_{DESATBLANK}$ = 2 µs.

In series with the desaturation diode, D_{DESAT}, an external decoupling resistor, R_{DESAT} is required to limit the current flowing in and out of the *DESAT* pin which can occur due to noise coupled through the desaturation diode, D_{DESAT} during the DESAT sensing time. R_{DESAT} can be calculated using the following formula:

$$V_{R_{\mathrm{DESAT}}} + V_{R_{\mathrm{DESAT}}} + V_{\mathrm{CE(sat)}} < V_{\mathrm{DESATth}} \quad (3)$$

$$R_{\mathrm{DESAT}} = \frac{V_{R_{\mathrm{DESAT}}}}{I_{\mathrm{DESATC}}} \quad (4)$$

The recommended value for a decoupling resistor R_{DESAT} is 1 kΩ for a half-bridge topology. A higher R_{DESAT} value results in a higher sensitivity of this function with respect to collector current, but this increased sensitivity can also lead to wrong triggering.

This function should, therefore, be used only for the detection of full desaturation instead of overcurrents. The desaturation capacitor C_{DESAT} and decoupling resistor R_{DESAT} should be placed as close as possible to *DESAT* pin.

4 Design consideration

The design aspects describe the gate resistor and output supply capacitor selection as well as the power dissipation estimation for a selected design.

4.1 Output supply capacitor selection

A general design rule for the location of the driver output supply capacitor is that it be placed as close to the IC's supply pins *VCC2* and *VEE2* as possible.

Additionally, the value of the capacitor needs to be big enough to limit the voltage drop during the power switch turn-on. A first approximation for this capacitor can be calculated using the following equation:

$$C = \frac{I_{Q2}/f_{sw} + Q_G}{\Delta V_{VCC}} \cdot 1.2 \quad (5)$$

Here, I_{Q2} is the gate driver supply current, f_{sw} is the switching frequency, Q_G is the total gate charge of the selected power transistor for the selected operating conditions, and ΔV_{VCC} is the maximum allowable voltage variation for the gate supply voltage. An additional margin of 20% is added to cover the typical tolerance variations in the capacitor and gate charge parameters.

For example, if an Infineon TRENCHSTOP™ IGBT4 IKW40N120H3 with a gate charge, Q_G = 160 nC is being driven with a frequency of 15 kHz, and we accept a gate supply voltage variation of 200 mV, the minimum capacitance needed would be:

$$C = \frac{3\ \text{mA}/15\ \text{kHz} + 160\ \text{nC}}{200\ \text{mV}} \cdot 1.2 = 2.16\ \mu\text{F} \quad (6)$$

In this case, the next larger capacitor size should be chosen. This capacitor is needed to decouple the gate supply voltage and should be placed as close as possible to the *VCC2* and *VEE2* pins. To provide proper decoupling, a 100 nF capacitor should be placed between pins *VCC2* and *GND2,* and *GND2* and *VEE2*.

4.2 Gate resistor selection

The gate resistor selection is an important step in designing the gate driving circuit. The gate of the power transistor (e.g. IGBT) is charged to V_{VCC2} and discharged to V_{VEE2} using the gate driver IC internal source and sink transistors via gate resistors. This is shown in a simplified way in Figure 13.

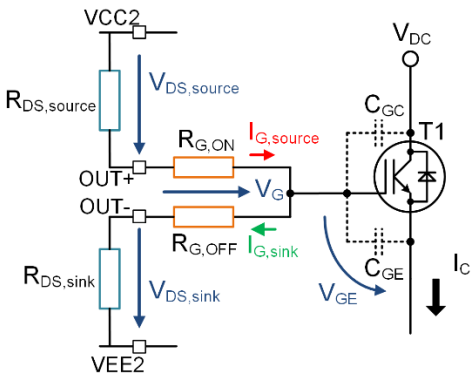

Figure 13 Simplified gate charging circuit

The MOSFET-based gate driver outputs can be simplified as dynamic resistors ($R_{DS,source}$, $R_{DS,sink}$) with a voltage drop ($V_{DS,source}$, $V_{DS,sink}$) during switching. Figure 14 shows the typical switching waveforms of an IGBT.

In the initial state, at time t_0, the gate is discharged and it has the same potential as the *VEE2* pin. At this point the supply voltage, *VCC2-VEE2*, is split between the inner gate resistance, $R_{DS,source}$, the turn-on resistance, $R_{G,ON}$, and the IGBT internal gate resistance, $R_{G,int}$. This is the highest current that needs to be supplied by the gate driver IC and can be used to select the appropriate pulse current class for the external gate resistor.

Between time intervals t_0 and t_2 the gate-emitter capacitance, C_{GE} gets charged. As the gate voltage, V_{GE} increases, the gate current, I_{GE}, decreases.

At t_2, the gate voltage reaches the Miller plateau level voltage, V_{pl}. This is where the IGBT collector current reaches its nominal application current, $I_{C,nom}$. This current also determines the amplitude of the Miller plateau voltage. So, the higher the application current, the higher the plateau voltage will be.

Between t_2 and t_3, the gate voltage and gate current are constant while the gate-collector capacitance, C_{GC} gets charged. This is an important step in the turn-on of the power transistors. The duration of this interval is decided by the gate current amplitude. Thus, a gate driver that can deliver higher average current would make the turn-on faster. During this time interval, the collector-emitter voltage, V_{CE} decreases to its on-state value and the dV/dt across the device is defined. The shorter the Miller plateau interval, the higher the dV/dt.

At t_3, after the gate-collector capacitance is charged and the V_{CE} reaches its approximate on-state value, the gate voltage starts increasing again to reach the *VCC2* level. During this time, the V_{CE} continues decreasing until it reaches its saturation voltage, associated with the *VCC2* voltage selected. Here, the capability of the gate driver to reach the rail voltage and the time it takes is important because it reduces the IGBT losses.

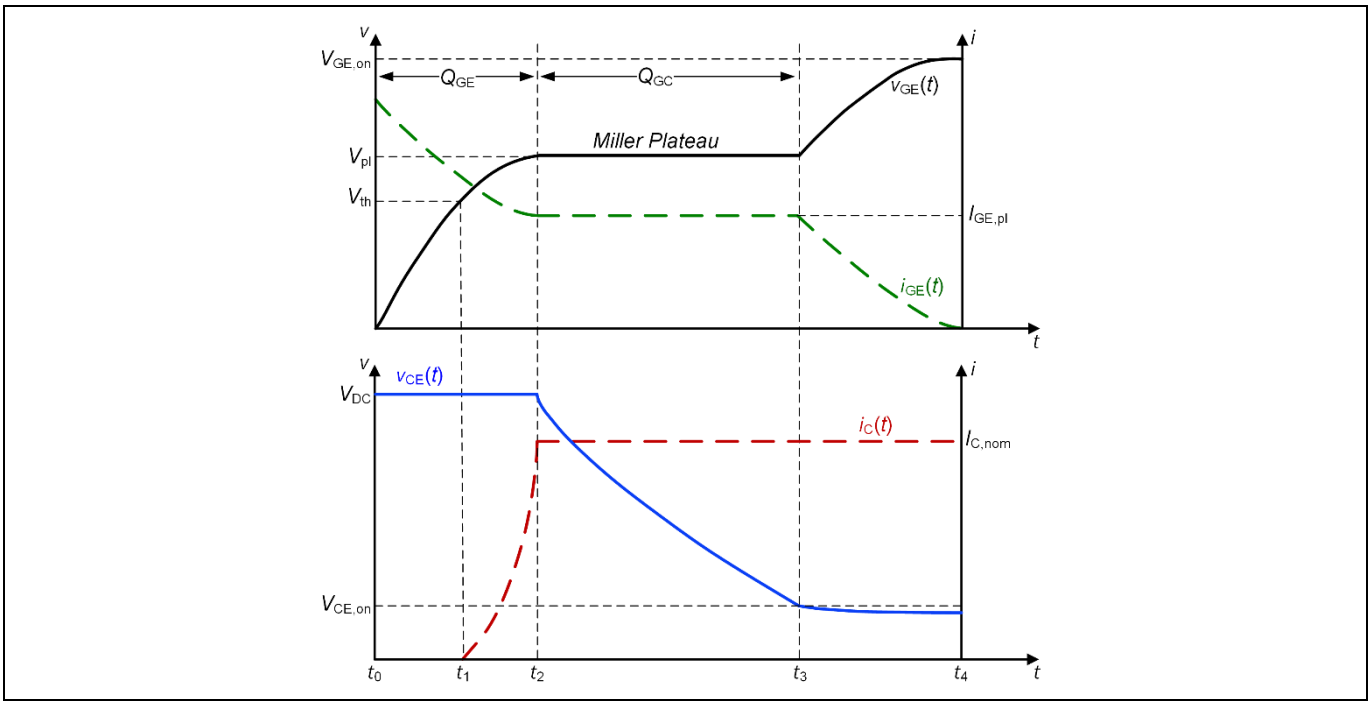

Figure 14 IGBT turn-on waveforms

From the above explanation it can be shown that one of the most important part in IGBT switching is between t_2 and t_3 during the Miller plateau, when the gate-collector capacitance is charged and the collector-emitter voltage decreases. As the collector-emitter voltage for the application is known, the collector-emitter voltage transition time, t_{ON} can be calculated using the following equation:

$$t_{\mathrm{ON}} = \frac{R_{\mathrm{G,on}} + R_{\mathrm{DS,source}} + R_{\mathrm{G,int}}}{V_{\mathrm{VCC2}} - V_{pl}} \cdot Q_{\mathrm{GC}} \quad (7)$$

As the desired collector-emitter voltage transition time t_{ON} is known, $R_{G,on}$ can be derived using the following equation:

$$R_{\mathrm{G,on}} = \frac{t_{\mathrm{ON}}}{Q_{\mathrm{GC}}} \cdot \left(V_{\mathrm{VCC2}} - V_{pl}\right) - R_{\mathrm{DS,source}} - R_{\mathrm{G,int}} \quad (8)$$

4.3 Power dissipation estimation

Apart from the power losses in the gate resistor during switching of any power switch, there is also considerable power loss inside the driver IC.

Every package can achieve a maximum power dissipation at a certain operating condition without exceeding the maximum junction temperature. The internal power loss of the output section (POUT) of the gate driver IC can be estimated as follows:

$$P_{\mathrm{OUT}} = P_{\mathrm{Q}} \cdot P_{\mathrm{Source}} \cdot P_{\mathrm{Sink}} \quad (9)$$

P_{OUT} is the operating power loss of the output side of the gate driver. It can be calculated by multiplying the operating supply current, I_{Q2} and the supply voltage of the output stage V_{VCC2} – V_{VEE2}:

$$P_{\mathrm{Q}} = I_{\mathrm{Q2}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \quad (10)$$

The turn-on (P_{source}) and turn-off (P_{sink}) losses can be estimated using the resistive voltage divider between inner gate driver resistance, R_{DS} and outer gate resistor, R_G with the total gate charge, Q_G and switching frequency, f_{sw}:

$$P_{\mathrm{Source}} = \frac{1}{2} \cdot Q_{\mathrm{G}} \cdot f_{\mathrm{sw}} \cdot \frac{R_{\mathrm{DS,source}}}{R_{\mathrm{DS,source}} - R_{\mathrm{G,on}}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \quad (11)$$

$$P_{\mathrm{Sink}} = \frac{1}{2} \cdot Q_{\mathrm{G}} \cdot f_{\mathrm{sw}} \cdot \frac{R_{\mathrm{DS,sink}}}{R_{\mathrm{DS,sink}} - R_{\mathrm{G,off}}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \quad (12)$$

5 Application examples

In this chapter, a few examples of the 1ED3321MC12N operation are shown using the Eval-1ED3321MC12N evaluation board. For easy evaluation and better understanding of the Infineon EiceDRIVER™ 1ED332xMC12N gate driver IC family, the Eval-1ED3321MC12N evaluation board can be used.

The Infineon EiceDRIVER™ 1ED332xMC12N gate driver IC family can deliver currents up to 8.5 A. This makes them suitable for both high gate charge switches such as IGBT modules, and applications where fast switching frequencies are needed.

5.1 IGBT short-circuit turn-off

The DESAT function is designed to protect the application against short-circuit events. When a power transistor, in this case an IGBT, is turned on into a short circuit, the gate driver with added DESAT circuit components can protect it from a catastrophic failure. Figure 15 shows such an event.

In this example, an Infineon TRENCHSTOP™ IGBT4 IKW40N120H3 is used.

At time t = 0 ns, the IGBT is turned on. As the gate voltage rises, the IGBT starts switching on, as it can be observed in collector-emitter voltage, V_{CE}, and current, I_C. The current increases rapidly to its saturation value of approximately 150 A.

The *DESAT* pin voltage is kept low by the internal DESAT-clamp until the leading-edge blanking time elapses, after approximately 400 ns. After this, the clamp releases the pin and the internal DESAT current source starts charging the DESAT capacitor, C_{DESAT} with a controlled current, i_{DESATC} (500 µA.)

After the *DESAT* pin voltage, V_{DESAT}, reaches the DESAT threshold voltage, $V_{DESATth}$, the internal filter is activated, and after the desaturation sense to out low delay elapses, $t_{DESATOUT}$, the output is turned low.

The short circuit is turned off in approximately 1.3 µs.

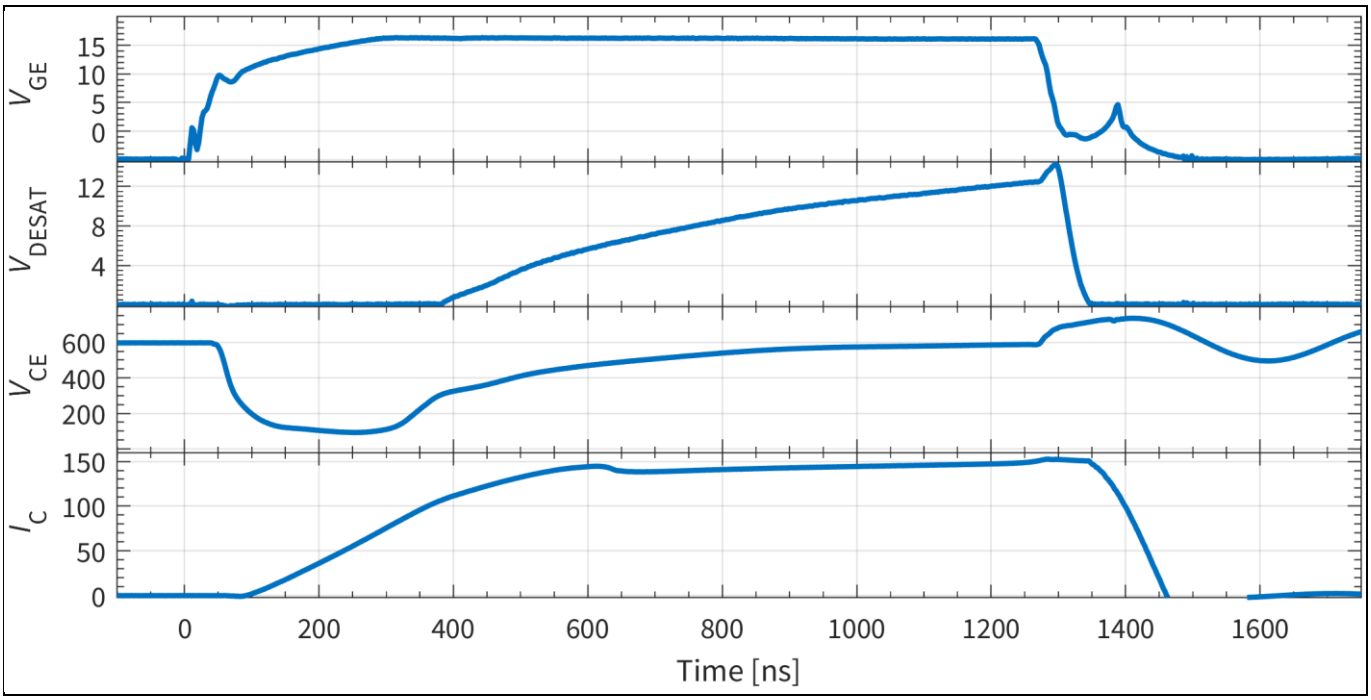

Figure 15 Turn-off of Type I short circuit

5.2 Short circuit turn-off with CoolSiC™ MOSFETs and C_{DESAT} = 51 pF

The DESAT function can also be used to protect SiC MOSFETs. In this example, an Infineon CoolSiC™ IMW120R045M1 MOSFET is used.

To correctly drive the gate of the SiC MOSFET, the output side power supply is adjusted so that the secondary sides of the gate driver IC can be supplied with +15 V/-2 V. The SiC MOSFET is connected directly to a 400 V DC-link capacitor.

Similar to the example in Section 5.1, the SiC MOSFET is turned on into a Type I short circuit as shown in Figure 16. The SiC MOSFET goes into saturation with the current rising up to 250 A. After the leading-edge blanking time elapses, the DESAT pin voltage starts increasing. Once it surpasses the desaturation reference level, $V_{DESATth}$, desaturation is detected and the internal circuitry initiates a turn-off.

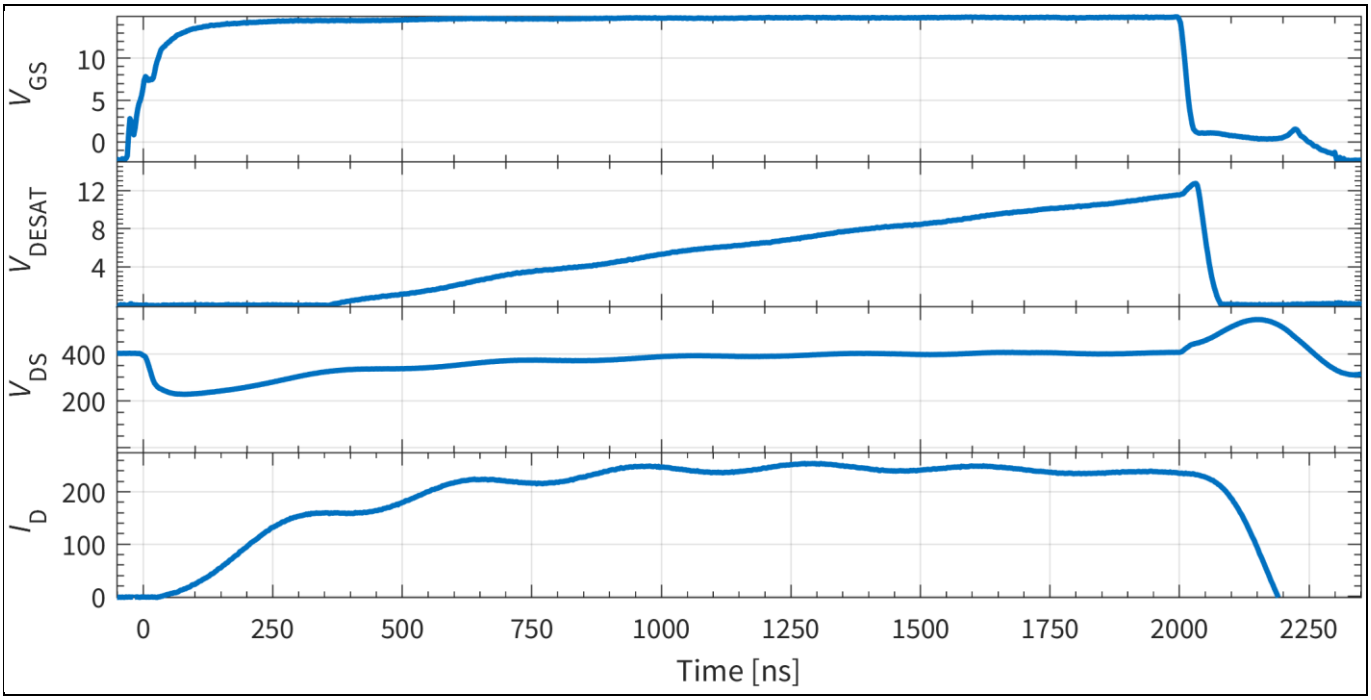

Figure 16 Turn-off of Type I short circuit with CoolSiC™ and C_{DESAT} = 51 pF

The CoolSiC™ turns off in approximately 2 µs. This protection is adequate for the CoolSiC™ IMW120R045M1 MOSFET, which has a short-circuit withstand time capability of 3 µs.

5.3 Short circuit turn-off with CoolSiC™ MOSFETs without desaturation capacitor

In the example provided in Section 5.2, an approximately 2 µs short-circuit protection time was achieved. If a faster desaturation protection time is needed, the desaturation capacitor can be reduced or completely removed. However, note that there will always be a parasitic capacitance component due to the layout and the parasitics of the other components connected to the DESAT pin of the gate driver. By removing the DESAT capacitor, the DESAT protection times can be reduced to a minimum allowed by the circuit.

Figure 17 shows the SiC transistor turning on directly into a type I short circuit. The transistor goes into saturation with the current rising up to 250 A. As described in Sections 5.1 and 5.2, after the leading-edge blanking time elapses, the *DESAT* pin voltage starts increasing. As there is no desaturation capacitor to be charged, the voltage rises much faster. After the desaturation reference level, $V_{DESATth}$ is reached, the protection mechanism is activated.

In this case, the short circuit is detected and turned off in approximately 1.2 µs

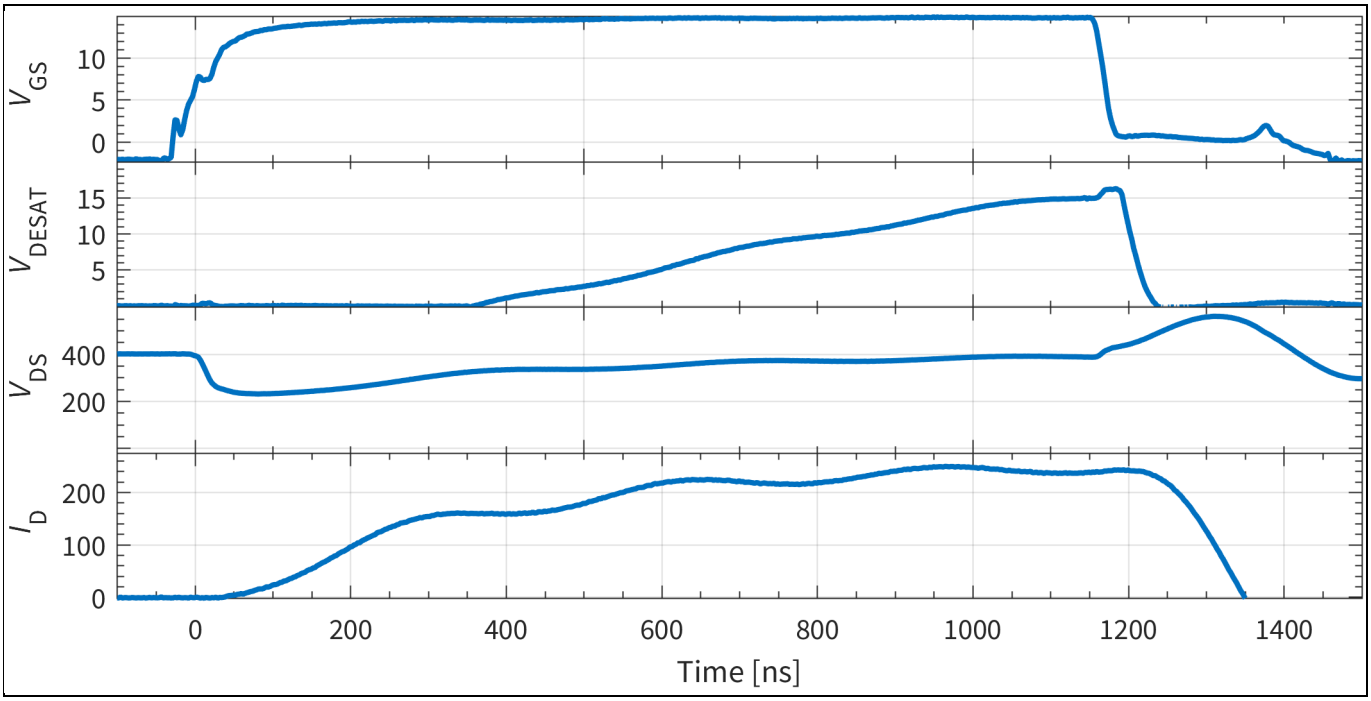

Figure 17 Turn-off of Type I short circuit with CoolSiC™ without desaturation capacitor

5.4 Short circuit turn-off with CoolSiC™ MOSFETs with overdrive circuit for DESAT charge circuit

In the rare cases when even reducing the desaturation capacitance is not sufficient, the desaturation detection circuit can be overdriven by external circuitry. The DESAT circuit current source can be supplemented by connecting the *DESAT* pin to the transistor gate via a resistor (R9) and a diode (D5). The resistor limits the charge current and the current going into the *DESAT* pin while the leading-edge blanking time is active. Without the resistor, the power dissipation inside the DESAT-clamp transistor will unnecessarily increase. The diode is required to prevent the *DESAT* pin from being pulled below ground when the gate of the transistor is driven negatively. The increased current decreases the DESAT reaction time.

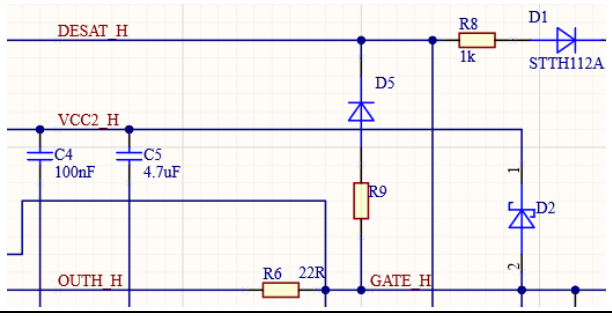

Figure 18 DESAT pin overdrive circuit

Revision history

Document version	Date	Description of changes
V1.0	2022-01-28	Initial release

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