AN2930

Implementing IEEE 1588-2008 with LAN7430

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INTRODUCTION

This application note describes an implementation of IEEE 1588 Precision Time Protocol (PTP) using LAN7430 PCIe to Ethernet bridge. The LAN7430 device has an integrated 10/100/1000 Mbps Ethernet PHY, PCIe PHY and MAC that supports IEEE 1588-2008. The Ethernet PHY supports timestamping of outgoing and incoming Ethernet frames using hardware that provides precise timings. For this application note, PTP was tested on the EVB-LAN7430 Rev B evaluation board and Linux PTP software stack. This application note provides only a basic overview of the IEEE1588-2008 standard. The user is encouraged to review the official IEEE 1588-2008 documentation from the IEEE organization.

Sections

This document includes the following topics:

References

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- *LAN7430 Data Sheet*
- *IEEE-1588-2008 Official Standard*
- *ptp4l (Precision Time Protocol for Linux) Manual*

IEEE 1588-2008 OVERVIEW

The IEEE 1588 protocol is used for synchronization within a distributed network. The standard provides accuracy of nanoseconds. The protocol autocorrects the latency in the network. Due to the high accuracy requirement, it is advised to perform all the necessary tasks of this standard in the hardware domain rather than in software.

The standard is highly suitable for industrial, telecommunication, smart power grid, and financial applications. For example, in an industrial environment when one task is required to start within finite time of another task, the use of IEEE1588-2008 PTP ensures determinism.

This is a master-slave protocol where a main clock (grandmaster clock) acts as the master and another clock in a node acts as the slave. To synchronize timing, the standard uses following messages between the master and the slave:

- Announce
- Timestamped messages
  - Sync
  - Delay_Req
  - Pdelay_Req
  - Pdelay_Resp
- General Messages
  - Follow_Up
  - Delay_Resp
  - Pdelay_Resp_Follow_Up
- Management
- Signaling

The time difference between the master clock and the slave clock is a combination of the clock offset and message transmission delay. Hence, correcting the clock skew is done in two phases: offset correction and delay correction.

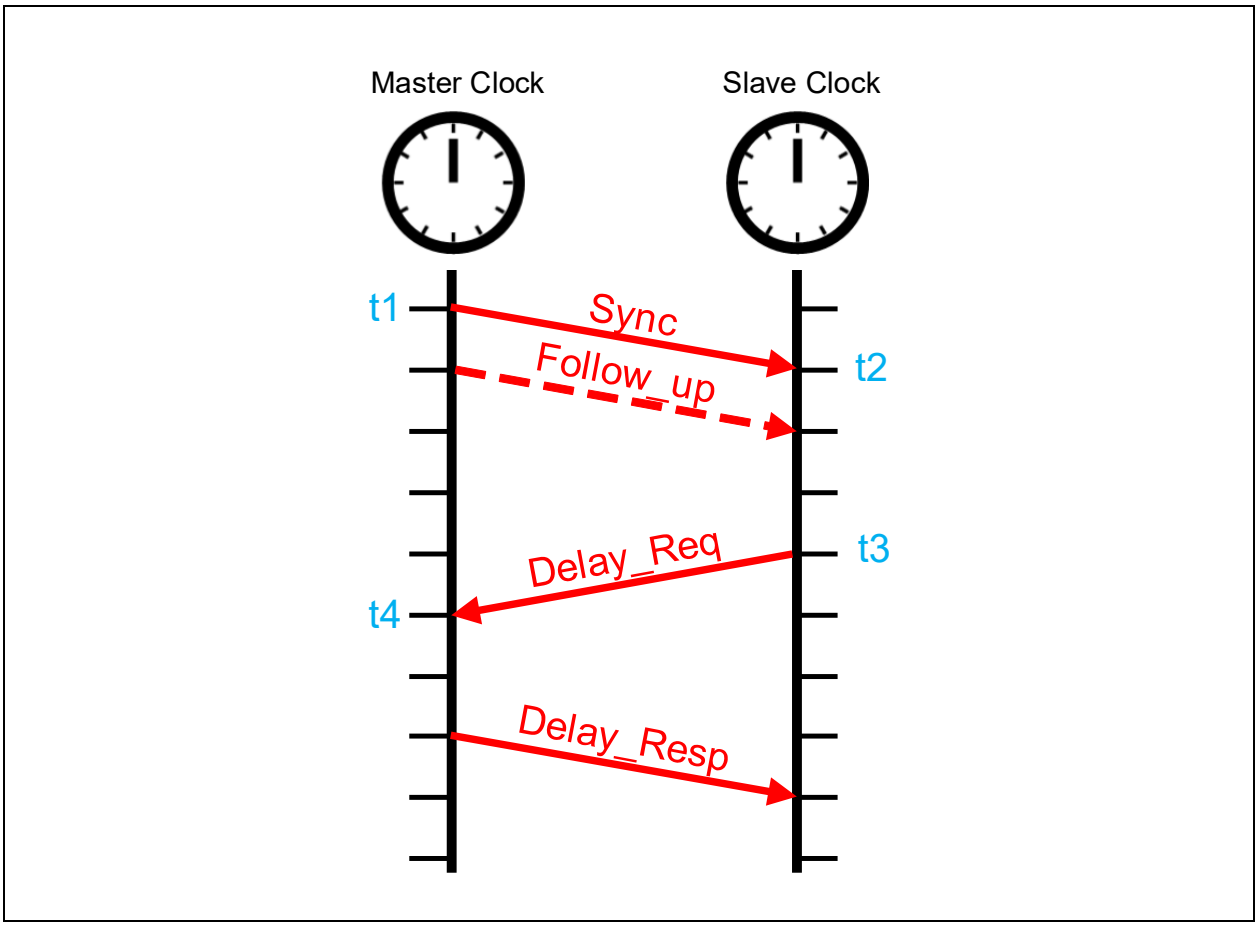
The master clock initiates offset correction using sync and follow-up messages. When the master sends a sync message, the slave uses its local clock to timestamp the arrival of the sync message and compares it to the actual sync transmission timestamp in the follow-up message of the master clock. The difference between the two timestamps represents the offset of the slave plus the message transmission delay. The slave clock then adjusts the local clock by this difference at point A.

To correct for the message transmission delay, the slave uses a second set of sync and follow-up messages with its corrected clock to calculate the master-to-slave delay at point B. The second set of messages is necessary to account for variations in network delays.

The slave then timestamps the sending of a delay request message. The master clock timestamps the arrival of the delay request message. It then sends a delay response message with the delay request arrival timestamp at point C. The difference between the timestamps is the slave-to-master delay. The slave averages the two directional delays and then adjusts the clock by the delay to synchronize the two clocks. Because the master and slave clocks drift independently, periodically repeating offset correction and delay correction keeps the clocks synchronized.

Figure 1 shows the PTP clock synchronization steps. The offset and the path delay can be calculated using Equation 1 and Equation 2, respectively.

FIGURE 1: PTP CLOCK SYNCHRONIZATION



EQUATION 1: MEAN PATH DELAY

$$PathDelay = \frac{(t2 - t1) + (t4 - t3)}{2}$$

EQUATION 2: OFFSET

$$Offset = \frac{(t2 - t1) - (t4 - t3)}{2}$$

IEEE 1588-2008 WITH LAN7430

The device provides hardware support for the IEEE 1588-2008 (v2) Precision Time Protocol (PTP), allowing clock synchronization with remote Ethernet devices, packet timestamping, and time driven event generation.

The device may function as a master or a slave clock per the IEEE 1588-2008 Specification. End-to-end and peer-to-peer link delay mechanisms are supported in the same way as one-step and two-step operations.

The 1588 Clock of the LAN7430 device consists of a 32-bit wide seconds portion, a 30-bit wide nanoseconds counter, and a 32-bit subnanosecond counter. Running at a nominal reference frequency of 125 MHz, the nanoseconds portion is normally incremented by a value of 8 every reference clock period. Upon reaching or exceeding its maximum value of 10^9, the nanoseconds portion rolls over to or past zero and the seconds portion is incremented.

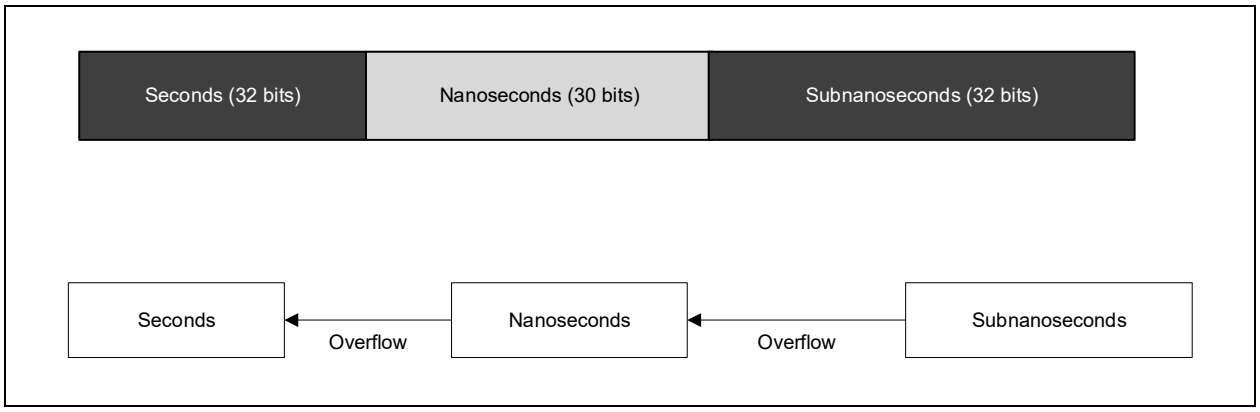
The System Time Clock (STC) of the device is a readable and writable high-precision counter that is used to keep the PTP time. The counter resolution is 2-32 ns.

STC either works as master clock or is synchronized to a master clock to provide the time for PTP-related functions.

This clock can be read or written through the CPU interface, and it is constructed with three counters: 32-bit counter for the second units, 30-bit counter for the nanosecond units, and 32-bit counter for the subnanosecond units.

Figure 2 shows a block diagram of the internal 1588 clock.

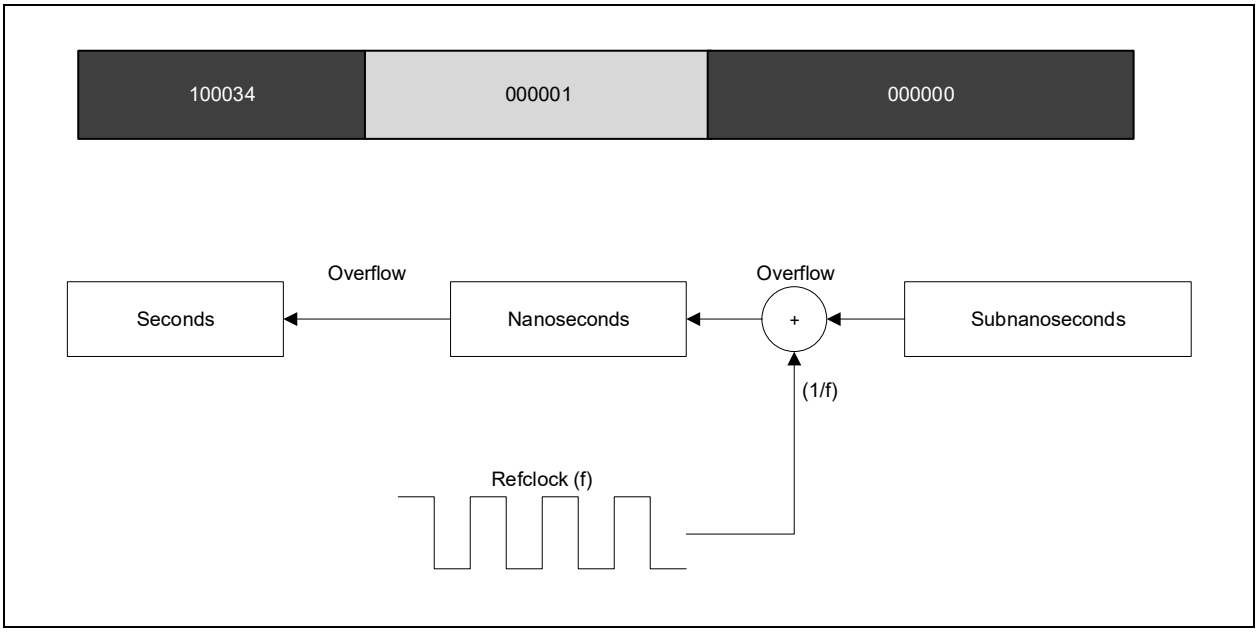
FIGURE 2: LAN7430 1588 CLOCK



For the LAN7430 device, the system clock can be set by writing directly to the clock registers. This can be used to correct for any gross errors in the slave clock or when the system is first powering up.

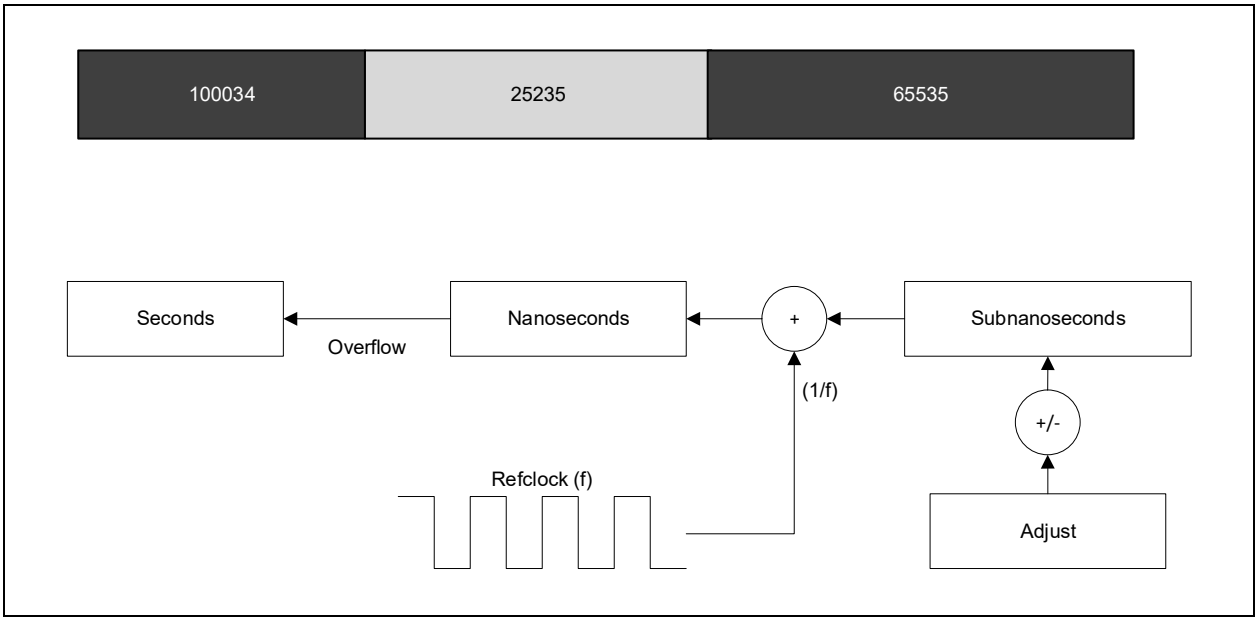
As shown in Figure 3, the system clock is maintained by the Refclock of the target device. Every time a clock edge is detected, it increments the nanosecond counter by the value of the period of the clock. A more accurate Refclock yields a more accurate system clock.

FIGURE 3: LAN7430 1588 CLOCK SETUP



The system clock can also be adjusted to fine tune the clock based on the offset and delay calculated by the messages. Figure 4 shows the block diagram.

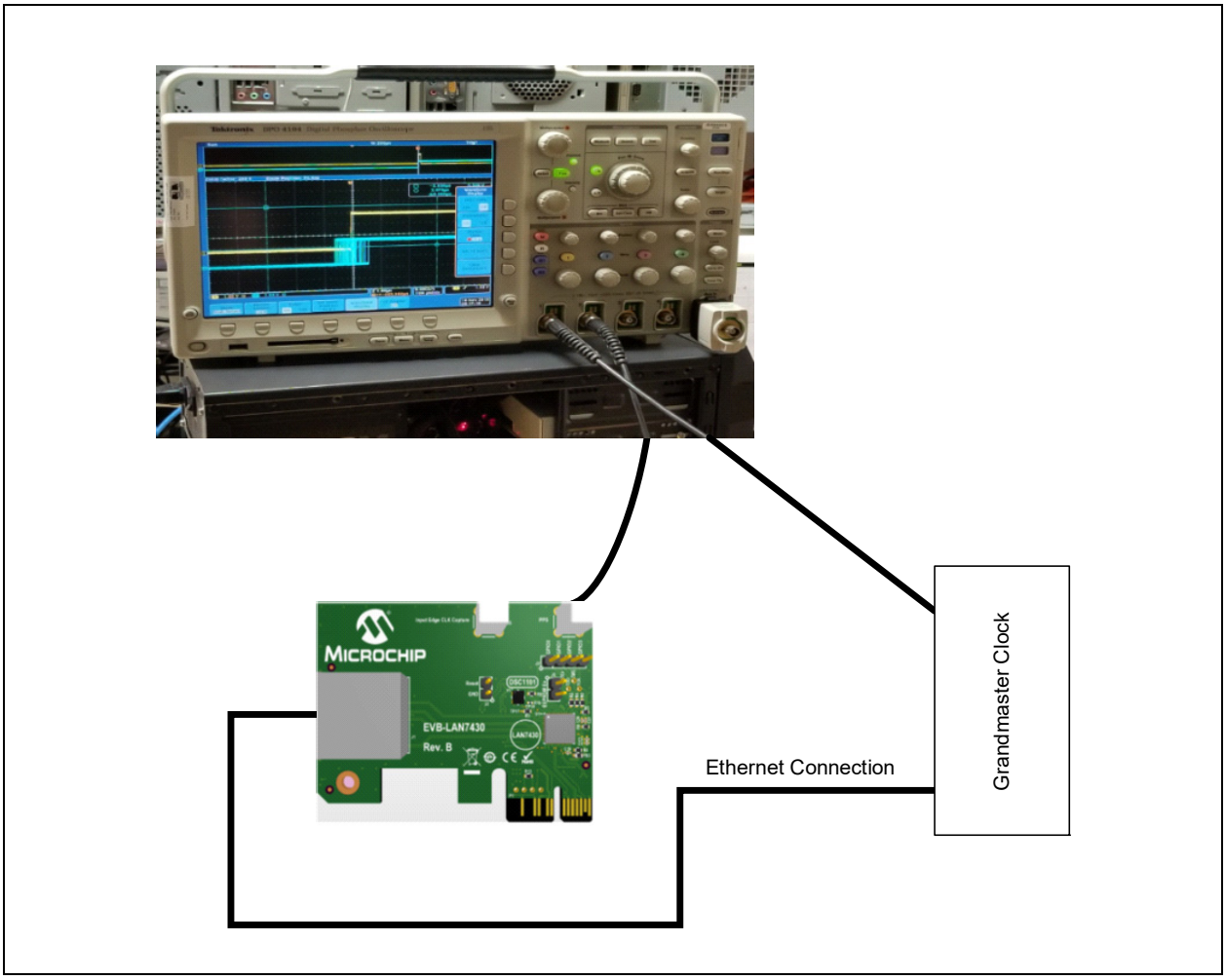
FIGURE 4: LAN7430 1588 CLOCK ADJUSTMENT



DEMONSTRATION SETUP

Figure 5 illustrates the setup using a GPS disciplined grandmaster clock. The grandmaster clock is connected to the EVB-LAN7430 board using an Ethernet cable. One connection of the grandmaster clock is connected to the oscilloscope, and one connection to the oscilloscope is from the EVB-LAN7430 EVB Pulse Per Second (PPS) connection.

FIGURE 5: DEMONSTRATION SETUP



STEPS TO DEMONSTRATE PTP

The demonstration is performed on Linux operating system using PTP4L utility. The following steps are followed:

1. Open the PTP4L utility on Linux.
2. Confirm the setup as per Demonstration Setup on page 6.
3. Set up a PTP configuration file, `ptp4l.conf`. A configuration file includes a few sections that configure several options for PTP. A section is labeled inside a bracket. For example, the following configuration file defines two sections (they are shown in brackets), `global` and `enp0s31f6`. The `global` section defines program options, clock options, and default port options, and the `enp0s31f6` section defines the PTP port.

   ```
   [global]
   verbose 1
   time_stamping hardware
   slaveOnly 0
   priority1 128
   priority2 128
   logging_level 6
   boundary_clock_jbod 0
   twoStepFlag 0


   [enp0s31f6]
   delay_mechanism E2E
   network_transport UDPv4
   ```

   The `ptp4l.conf` file is saved in the etc directory (`/etc/ptp4l.conf`).
4. Run the configuration file as follows:

   ```
   sudo ptp4l -f /etc/ptp4l.conf
   ```

RESULTS

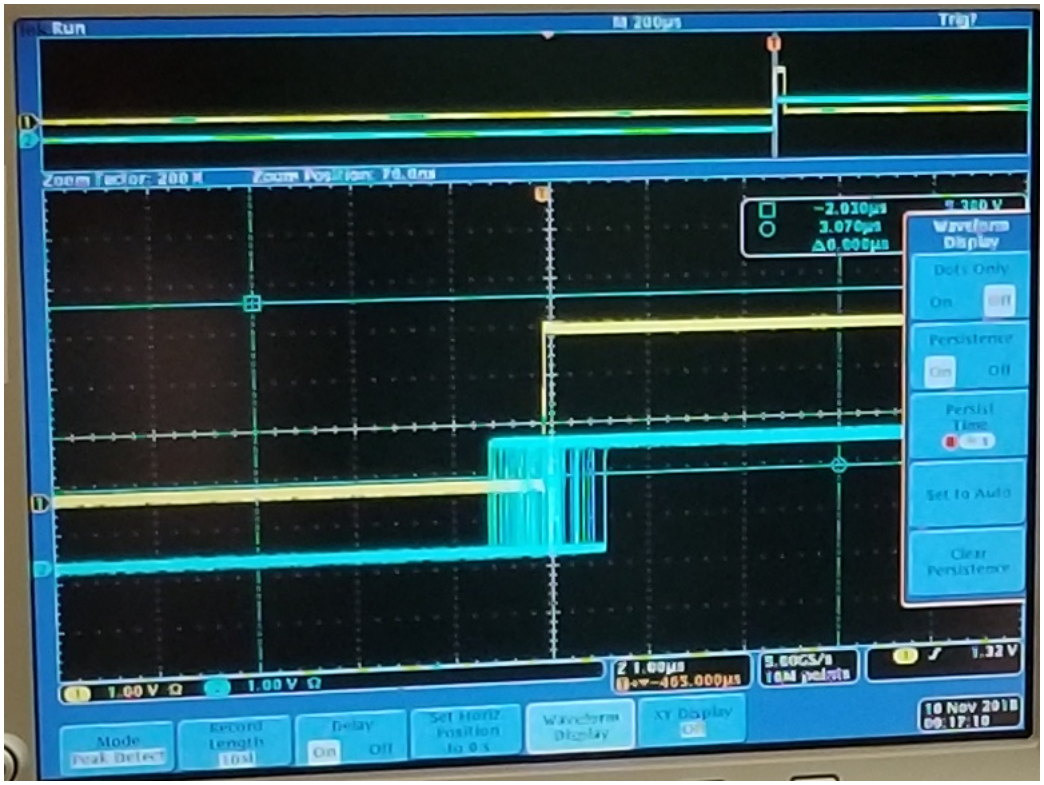
Figure 6 shows the output of the PTP demonstration. Results shows the offset and the path delay. It can be observed that after few seconds the LAN7430 tightly follows the GPS 1588 clock where the offset and the path delay are in single digit.

FIGURE 6: LAN7430 PTP RESULTS

```
validation1@validation1-Z170X-UD5-TH:~/Documents/LAN7430_Driver/lan743x.0.7.1.180501/lan743x.0.7.1.180501/src$ sudo ptp4l -f /etc/ptp4l.conf
ptp4l[151.820]: selected /dev/ptp2 as PTP clock
ptp4l[151.845]: port 1: INITIALIZING to LISTENING on INITIALIZE
ptp4l[151.845]: port 0: INITIALIZING to LISTENING on INITIALIZE
ptp4l[151.845]: port 1: link up
ptp4l[152.433]: port 1: new foreign master 00b0ae.fffe.04e28f-3
ptp4l[156.433]: selected best master clock 00b0ae.fffe.04e28f
ptp4l[156.433]: port 1: LISTENING to UNCALIBRATED on RS_SLAVE
ptp4l[158.370]: master offset 2894399134462 s0 freq      +0 path delay      6007
ptp4l[159.370]: master offset 2894399117758 s1 freq  -16704 path delay      5519
ptp4l[161.370]: master offset      -6325 s2 freq  -23029 path delay      4485
ptp4l[161.379]: port 1: UNCALIBRATED to SLAVE on MASTER_CLOCK_SELECTED
ptp4l[162.370]: master offset        533 s2 freq  -18069 path delay      3451
ptp4l[163.370]: master offset       1396 s2 freq  -17046 path delay      3451
ptp4l[164.370]: master offset       2893 s2 freq  -15130 path delay      1792
ptp4l[165.370]: master offset        816 s2 freq  -16339 path delay      1792
ptp4l[166.370]: master offset       1605 s2 freq  -15305 path delay       133
ptp4l[167.370]: master offset       -677 s2 freq  -17106 path delay       512
ptp4l[168.370]: master offset       -403 s2 freq  -17035 path delay       133
ptp4l[169.370]: master offset       -564 s2 freq  -17317 path delay       112
ptp4l[170.370]: master offset       -441 s2 freq  -17363 path delay        89
ptp4l[171.370]: master offset       -217 s2 freq  -17271 path delay         3
ptp4l[172.370]: master offset       -164 s2 freq  -17283 path delay         5
ptp4l[173.370]: master offset       -105 s2 freq  -17274 path delay         5
ptp4l[174.370]: master offset        -42 s2 freq  -17242 path delay       -10
ptp4l[175.370]: master offset        -24 s2 freq  -17237 path delay       -10
ptp4l[176.370]: master offset        -12 s2 freq  -17232 path delay       -10
ptp4l[177.370]: master offset        -14 s2 freq  -17238 path delay       -10
ptp4l[178.370]: master offset         -9 s2 freq  -17237 path delay       -10
ptp4l[179.370]: master offset        -15 s2 freq  -17245 path delay         0
ptp4l[180.370]: master offset         -8 s2 freq  -17243 path delay         5
ptp4l[181.370]: master offset          2 s2 freq  -17235 path delay         5
ptp4l[182.370]: master offset         -4 s2 freq  -17241 path delay         6
ptp4l[183.370]: master offset         -4 s2 freq  -17242 path delay         6
ptp4l[184.370]: master offset        -12 s2 freq  -17251 path delay         6
ptp4l[185.370]: master offset         -1 s2 freq  -17244 path delay         6
ptp4l[186.370]: master offset         -6 s2 freq  -17249 path delay         6
ptp4l[187.370]: master offset         -7 s2 freq  -17252 path delay         7
ptp4l[188.370]: master offset        -12 s2 freq  -17259 path delay         7
ptp4l[189.370]: master offset         -3 s2 freq  -17254 path delay         8
ptp4l[190.370]: master offset         -8 s2 freq  -17259 path delay         9
ptp4l[191.370]: master offset        -13 s2 freq  -17267 path delay         9
ptp4l[192.370]: master offset         -3 s2 freq  -17261 path delay         9
ptp4l[193.370]: master offset         -8 s2 freq  -17267 path delay         9
ptp4l[194.370]: master offset        -14 s2 freq  -17275 path delay         9
ptp4l[195.370]: master offset         -3 s2 freq  -17268 path delay         9
ptp4l[196.370]: master offset         -8 s2 freq  -17274 path delay         9
ptp4l[197.370]: master offset         -6 s2 freq  -17275 path delay         9
ptp4l[198.370]: master offset        -12 s2 freq  -17282 path delay         9
ptp4l[199.370]: master offset         -2 s2 freq  -17276 path delay         9
ptp4l[200.370]: master offset         -7 s2 freq  -17282 path delay         9
ptp4l[201.370]: master offset         -6 s2 freq  -17283 path delay         9
ptp4l[202.370]: master offset         -4 s2 freq  -17282 path delay         9
ptp4l[203.370]: master offset         -3 s2 freq  -17283 path delay         9
ptp4l[204.370]: master offset         -9 s2 freq  -17290 path delay         9
ptp4l[205.370]: master offset         -7 s2 freq  -17290 path delay         8
```

Figure 7 shows the oscilloscope captures of the offset and jitters of the PPS signal between master and the LAN7430 slave clock.

FIGURE 7: JITTER COMPARISON OF LAN7430 SLAVE AND MASTER PPS OUTPUTS



CONCLUSION

The results show that the integrated IEEE 1588-2008 of the LAN7430 device is very precise, which is extremely useful in industrial and automotive applications.

APPENDIX A: PTP4L COMMAND DESCRIPTION

TABLE A-1: PTP4L COMMAND DESCRIPTION

Command	Description
`[global]`	Sets the program options, clock options, and default port options.
`-f config`	Reads configuration from the specified file. No configuration file is read by default.
`verbose`	Prints messages to the standard output if enabled. The default is 0 (disabled).
`time_stamping`	The time stamping method. The allowed values are hardware, software, and legacy. The default is hardware.
`slaveOnly`	The local clock is a slave-only clock if enabled. This option is only for use with 1588 clocks and should not be enabled for 802.1AS clocks. The default is 0 (disabled).
`priority1`	The priority1 attribute of the local clock. It is used in the best master selection algorithm, lower values take precedence. Must be in the range 0 to 255. The default is 128.
`priority2`	The priority2 attribute of the local clock. It is used in the best master selection algorithm, lower values take precedence. Must be in the range 0 to 255. The default is 128.
`logging_level`	The maximum logging level of messages that should be printed. The default is 6 (LOG_INFO).
`boundary_clock_jbod`	When running as a boundary clock (that is, when more than one network interface is configured), ptp4l performs a sanity check to make sure that all of the ports share the same hardware clock device. This option allows ptp4l to work as a boundary clock using “just a bunch of devices” that are not synchronized to each other. For this mode, the collection of clocks must be synchronized by an external program, for example phc2sys(8) in an automatic mode. The default is 0 (disabled).
`twoStepFlag`	Enables two-step mode for sync messages. One-step mode can be used only with hardware time stamping. The default is 1 (enabled).
`delay_mechanism`	Selects the delay mechanism. Possible values are E2E, P2P, and Auto. The default is E2E.
`network_transport`	Selects the network transport. Possible values are UDPv4, UDPv6, and L2. The default is UDPv4.

APPENDIX B: APPLICATION NOTE REVISION HISTORY

TABLE B-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002930A (01-24-19)	Initial release	

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