

## GRF5617

### HIGH LINEARITY POWER AMPLIFIER 1710 to 1785 MHz

#### FEATURES

- Excellent OP1dB, OIP3, ACLR and IM3 Performance
- Native Linearity Provides up to +26.5 dBm  $P_{OUT}$  with 45 dBc ACLR – Without the Need for Digital Predistortion Correction
- +26 dBm Linear Output Power Maintained at 85 °C
- Flexible Biasing Provides Latitude for Linearity Optimization
- 345 mA Native Mode Quiescent Current Consumption
- 5 V Supply Voltage
- 50  $\Omega$  Single-ended Input and Output Impedances
- Digital Shutdown
- Rugged Design is Extremely Resilient to Mismatched Loads
- -40 to 85 °C Operating Temperature Range
- Compact 3 x 3 mm QFN-16 Package
- RoHS Compliant

**Reference: 5 V / 345 mA  $I_{CCQ}$  / 1747 MHz**

- Gain: 25.1 dB
- OIP3: 49.3 dBm @ 25 dBm  $P_{OUT}$ /tone
- OP1dB: 35.4 dBm
- Evaluation Board Noise Figure: 4.2 dB

#### APPLICATIONS

- Cellular Boosters
- Automotive Compensators
- Picocells/Femtocells
- Customer Premise Equipment

#### DESCRIPTION

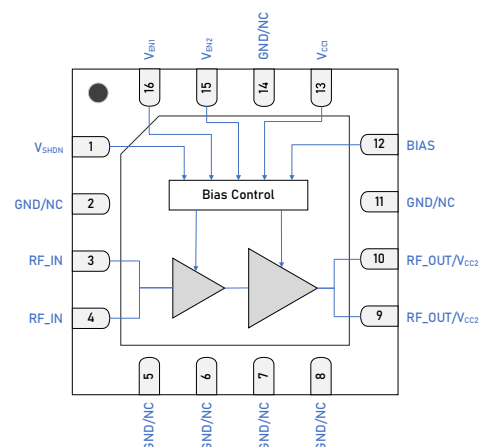
The GRF5617 is a high gain, two-stage InGaP HBT power amplifier designed to deliver excellent P1dB, ACLR and IM3 performance over the 1710 to 1785 MHz band. Its exceptional native linearity makes it an ideal choice for transmitter applications that typically do not employ digital predistortion correction schemes.

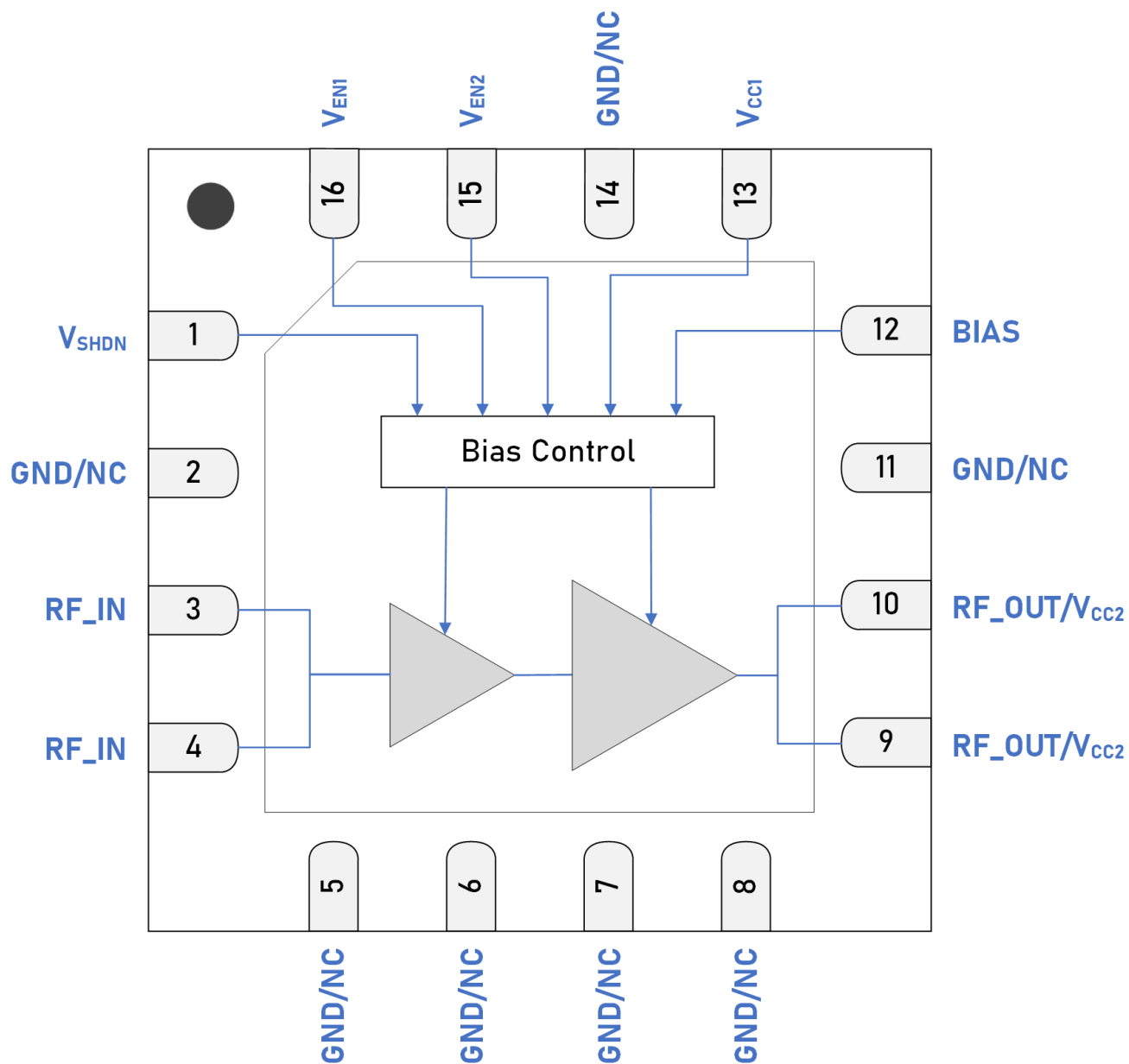
This device is part of a complete family of externally matched linear amplifiers that cover the following frequency ranges:

|                        |                          |
|------------------------|--------------------------|
| GRF5605: 617 - 652 MHz | GRF5610: 865 - 928 MHz   |
| GRF5606: 663 - 716 MHz | GRF5611: 902 - 960 MHz   |
| GRF5607: 703 - 748 MHz | GRF5617: 1710 - 1785 MHz |
| GRF5608: 746 - 830 MHz | GRF5618: 1800 - 1900 MHz |
| GRF5609: 814 - 862 MHz | GRF5626: 2500 - 2700 MHz |
|                        | GRF5636: 3400 - 3800 MHz |

Please consult with the GRF applications engineering team for custom tuning/evaluation board data.

#### BLOCK DIAGRAM





3 x 3 mm QFN-16 Pin Out (Top View)

## Pin Assignments

| Pin                   | Name                    | Description            | Note  |
|-----------------------|-------------------------|------------------------|---|
| 1                     | V <sub>SHDN</sub>       | Digital Shutdown Pin   | V <sub>SHDN</sub> ≥ 1.8 V (Logic HIGH) disables device. V <sub>SHDN</sub> ≤ 0.8 V (Logic LOW) enables device.   |
| 2, 5, 6, 7, 8, 11, 14 | GND/NC                  | Ground or No Connect   | No internal connection to die. These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.  |
| 3, 4                  | RF_IN                   | RF Input               | Pins 3 & 4 tied together on system board. An external DC blocking capacitor must be used.   |
| 9, 10                 | RF_OUT/V <sub>CC2</sub> | PA Output/Bias Voltage | Pins 9 & 10 tied together on system board. V <sub>CC2</sub> must be applied to this pin via an RF choke.  |
| 12                    | Bias                    | Bias Circuit Supply    | Connect to V <sub>CC2</sub> through external resistor.  |
| 13                    | V <sub>CC1</sub>        | Bias Voltage           | Connect to V <sub>CC1</sub> through external inductor (or 0 Ω resistor) with capacitive termination above (see application schematic).  |
| 15                    | V <sub>EN2</sub>        | Enable2 Voltage Input  | V <sub>EN2</sub> and series resistor set I <sub>CCQ</sub> for the output stage. V <sub>EN2</sub> ≤ 0.2 volts disables stage 2.  |
| 16                    | V <sub>EN1</sub>        | Enable1 Voltage Input  | V <sub>EN1</sub> and series resistor set I <sub>CCQ</sub> for the input stage. V <sub>EN1</sub> ≤ 0.2 volts disables stage 1.   |
| PKG BASE              | GND                     | Ground                 | Provides DC and RF ground for the amplifier, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page. |

## Absolute Ratings

| Parameter  |  | Symbol                      | Min. | Max.    | Unit |
|--|--|-----------------------------|------|---------|------|
| Supply Voltage   |  | $V_{CC}$                    | 3    | 5.25    | V    |
| RF Input Power   | 50 $\Omega$ , $V_{CC} = 5$ V, CW Tone, 100% Duty Cycle, $T_{PKG \text{ HEAT SINK}} = 25$ °C.                                     | $P_{IN \text{ MAX} - 1:1}$  |      | 20      | dBm  |
|  | Load VSWR $\leq 8:1$ , all phase angles, $V_{CC} = 5$ V, CW Tone, 100% Duty Cycle, $T_{PKG \text{ HEAT SINK}} = -40$ to $85$ °C. | $P_{IN \text{ MAX} - 8:1}$  |      | 10      |      |
| Operating Temperature (Package Heat Sink).                 |  | $T_{PKG \text{ HEAT SINK}}$ | -40  | 85      | °C   |
| Maximum Junction Temperature (MTTF > $10^6$ Hours).        |  | $T_{J \text{ MAX}}$         |      | 190     | °C   |
| Maximum Dissipated Power Stage 1 (DC only, no RF applied). |  | $P_{DISS \text{ MAX}}$      |      | * 750   | mW   |
| Maximum Dissipated Power Stage 2 (DC only, no RF applied). |  | $P_{DISS \text{ MAX}}$      |      | * 2250  | mW   |
| Shutdown Voltage   |  | $V_{SHDN}$                  |      | ** 5.25 | V    |

## Electrostatic Discharge

|                      |     |     |  |   |
|----------------------|-----|-----|--|---|
| Charged Device Model | CDM | TBD |  | V |
| Human Body Model     | HBM | TBD |  | V |

## Storage

|                            |           |     |     |    |
|----------------------------|-----------|-----|-----|----|
| Storage Temperature        | $T_{STG}$ | -65 | 150 | °C |
| Moisture Sensitivity Level | MSL       |     | 1   | —  |

## NOTES:

\* Bias resistance at M5/M9 has been empirically optimized for linearity. Thus, there will be no benefit in decreasing (increasing) resistance ( $I_{CCQ}$ ).

\*\* M4 = 0  $\Omega$ .  $I_{SHDN}$  with  $V_{SHDN} = 5.25$  V = 540  $\mu$ A., decreasing linearly to 65  $\mu$ A with nominal (and also minimum)  $V_{SHDN} = 1.8$  V.



**Caution! ESD Sensitive Device.**

**Exceeding Absolute Maximum Rating conditions may cause permanent damage.**

Note: For additional information, please refer to [Manufacturing Note MN-001 — Package and Manufacturing Information](#).



All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging requiring no exemptions. Additional information for this topic can be found at this link - [Environmental and Restricted Substance Statement Library](#)

## Recommended Operating Conditions

| Parameter                                 | Symbol                      | Specification |      |      | Unit     | Condition                          |
|---|-----------------------------|---------------|------|------|----------|------------------------------------|
|   |                             | Min.          | Typ. | Max. |          |                                    |
| Supply Voltage                            | $V_{CC}$                    | 3             | 5    | 5.25 | V        |                                    |
| Operating Temperature (Package Heat Sink) | $T_{PKG \text{ HEAT SINK}}$ | -40           |      | 85   | °C       |                                    |
| RF Frequency Range                        | $F_{RF}$                    | 1710          | 1747 | 1785 | MHz      | <b>Note 1.</b>                     |
| RFIN Port Impedance                       | $Z_{RFIN}$                  |               | 50   |      | $\Omega$ | Single Ended with 3-element Match. |
| RFOUT Port Impedance                      | $Z_{RFOUT}$                 |               | 50   |      | $\Omega$ | Single Ended with 3-element Match. |

**Note 1:** Operation outside this range is possible, but with degraded performance of some parameters.

## Nominal Operating Parameters – General

The following conditions apply unless noted otherwise: Typical Application Schematic using the 1710 to 1785 MHz tuning set, M5 = 9.76 k $\Omega$ , M9 = 5.6 k $\Omega$ , V<sub>SHDN</sub> = LOW, V<sub>CC</sub> = 5 V, I<sub>CCQ</sub> = 345 mA, 50  $\Omega$  system impedance, P<sub>OUT</sub> = 26.5 dBm, F<sub>TEST</sub> = 1747 MHz, T<sub>PKG HEAT SINK</sub> = 25 °C. Evaluation board losses are included within the specifications.

| Parameter                      | Symbol                     | Specification |      |                 | Unit    | Condition  |
|--------------------------------|----------------------------|---------------|------|-----------------|---------|--|
|                                |                            | Min.          | Typ. | Max.            |         |  |
| Supply Quiescent Current       | I <sub>CCQ</sub>           |               | 345  |                 | mA      | I <sub>CCQ1</sub> + I <sub>CCQ2</sub> . No RF Applied.                             |
| Supply Current with RF Applied | I <sub>CC</sub>            |               | 650  |                 | mA      | I <sub>CC1</sub> + I <sub>CC2</sub> . RF Applied with P <sub>OUT</sub> = 26.5 dBm. |
| Enable Current 1               | I <sub>ENABLE1</sub>       |               | 0.3  |                 | mA      | V <sub>CC</sub> = 5 V, T <sub>PKG HEAT SINK</sub> = 25 °C.                         |
| Enable Current 2               | I <sub>ENABLE2</sub>       |               | 0.5  |                 | mA      | V <sub>CC</sub> = 5 V, T <sub>PKG HEAT SINK</sub> = 25 °C.                         |
| Operating Temperature Range    | T <sub>PKG HEAT SINK</sub> | -40           |      | +85             | °C      | Measured on Package Heat Sink.   |
| Logic Input Low                | V <sub>IL</sub>            | 0             |      | 0.8             | V       | Applies to V <sub>SHDN</sub> Input.  |
| Logic Input High               | V <sub>IH</sub>            | 1.8           |      | V <sub>CC</sub> | V       | Applies to V <sub>SHDN</sub> Input.  |
| Logic Current Low              | I <sub>IL</sub>            |               | 1.3  |                 | nA      | Applies to V <sub>SHDN</sub> Input, V <sub>IL</sub> = 0.8 V.                       |
| Logic Current High             | I <sub>IH</sub>            |               | 65   |                 | $\mu$ A | Applies to V <sub>SHDN</sub> Input, V <sub>IH</sub> = 1.8 V.                       |
|                                |                            |               | 285  |                 |         | Applies to V <sub>SHDN</sub> Input, V <sub>IH</sub> = 3.3 V.                       |
| Switching Rise Time            | T <sub>RISE</sub>          |               | 50   |                 | ns      | Applies to V <sub>SHDN</sub> Input.  |
| Switching Fall Time            | T <sub>FALL</sub>          |               | 50   |                 | ns      | Applies to V <sub>SHDN</sub> Input.  |

### Disabled Mode

|                          |                           |  |      |  |         |  |
|--------------------------|---------------------------|--|------|--|---------|--|
| Supply Quiescent Current | I <sub>CCQ-SHDN</sub>     |  | 10   |  | $\mu$ A | V <sub>CC</sub> = 5 V, V <sub>SHDN</sub> /V <sub>EN1</sub> /V <sub>EN2</sub> = HIGH. |
| Enable Current 1         | I <sub>ENABLE1-SHDN</sub> |  | 0.6  |  | mA      | V <sub>CC</sub> = 5 V, V <sub>SHDN</sub> /V <sub>EN1</sub> /V <sub>EN2</sub> = HIGH. |
| Enable Current 2         | I <sub>ENABLE2-SHDN</sub> |  | 0.85 |  | mA      | V <sub>CC</sub> = 5 V, V <sub>SHDN</sub> /V <sub>EN1</sub> /V <sub>EN2</sub> = HIGH. |

### Thermal Data (Stage 1 and Stage 2)

|   |                |  |     |  |      |  |
|---|----------------|--|-----|--|------|--|
| Stage 1: Thermal Resistance (Infrared Scan). DC only (no RF applied). | $\Theta_{JC}$  |  | 60  |  | °C/W | On Standard Evaluation Board.  |
| Stage 2: Thermal Resistance (Infrared Scan). DC only (no RF applied). | $\Theta_{JC}$  |  | 30  |  | °C/W | On Standard Evaluation Board.  |
| Thermal Data Stage 1 & 2: See plot of junction Temp vs. Output Power. | T <sub>J</sub> |  | TBD |  | °C   | V <sub>CC</sub> = V <sub>EN1</sub> = V <sub>EN2</sub> = 5 V. On Standard Evaluation Board ( <b>note 2</b> ). |

**Note 2:** MTTF > 10<sup>6</sup> hours for T<sub>CHANNEL</sub>  $\leq$  190 °C.

## Nominal Operating Parameters – RF: 1.71 to 1.785 GHz, 5 V Operation

The following conditions apply unless noted otherwise: Typical Application Schematic using the 1710 to 1785 MHz tuning set,  $M5 = 9.76 \text{ k}\Omega$ ,  $M9 = 5.6 \text{ k}\Omega$ ,  $V_{\text{SHDN}} = \text{LOW}$ ,  $V_{\text{CC}} = 5 \text{ V}$ ,  $I_{\text{CCQ}} = 345 \text{ mA}$ ,  $50 \text{ }\Omega$  system impedance,  $P_{\text{OUT}} = 26.5 \text{ dBm}$ ,  $F_{\text{TEST}} = 1747 \text{ MHz}$ ,  $T_{\text{PKG HEAT SINK}} = 25 \text{ }^\circ\text{C}$ . Evaluation board losses are included within the specifications.

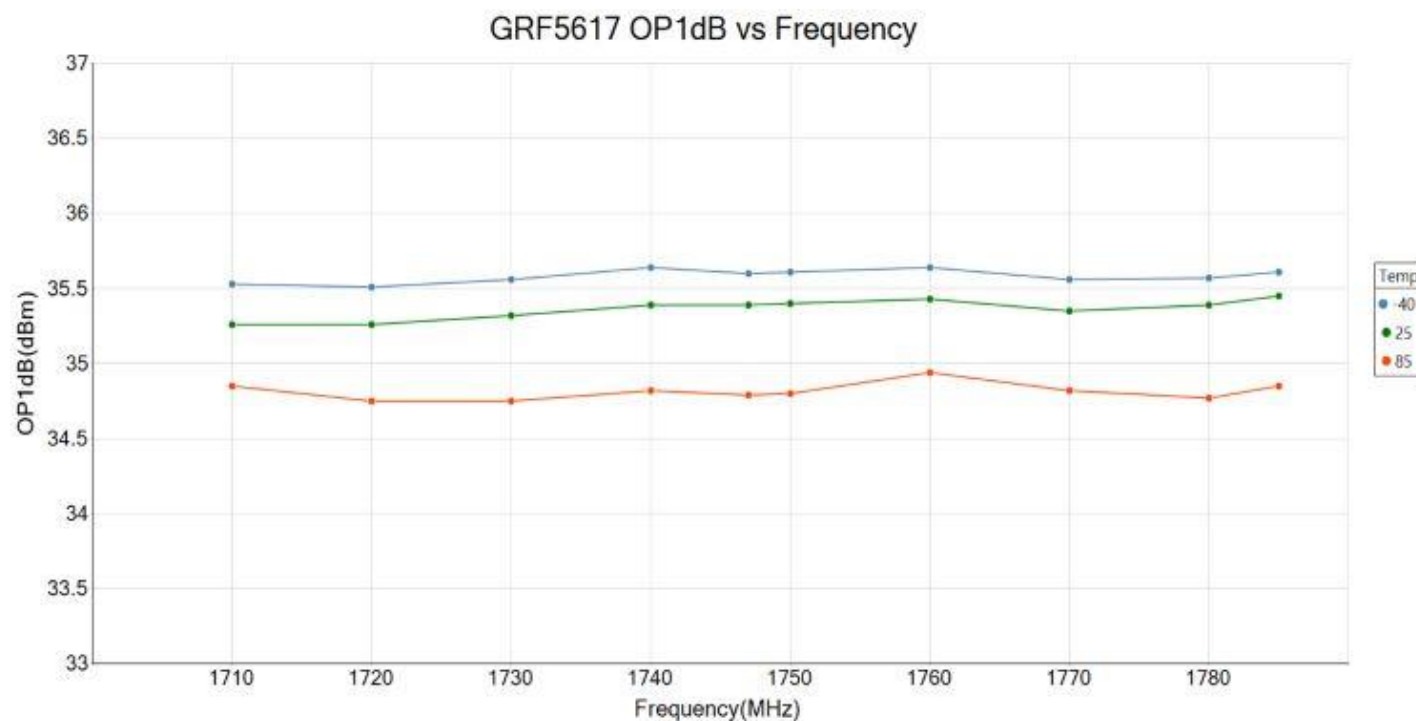
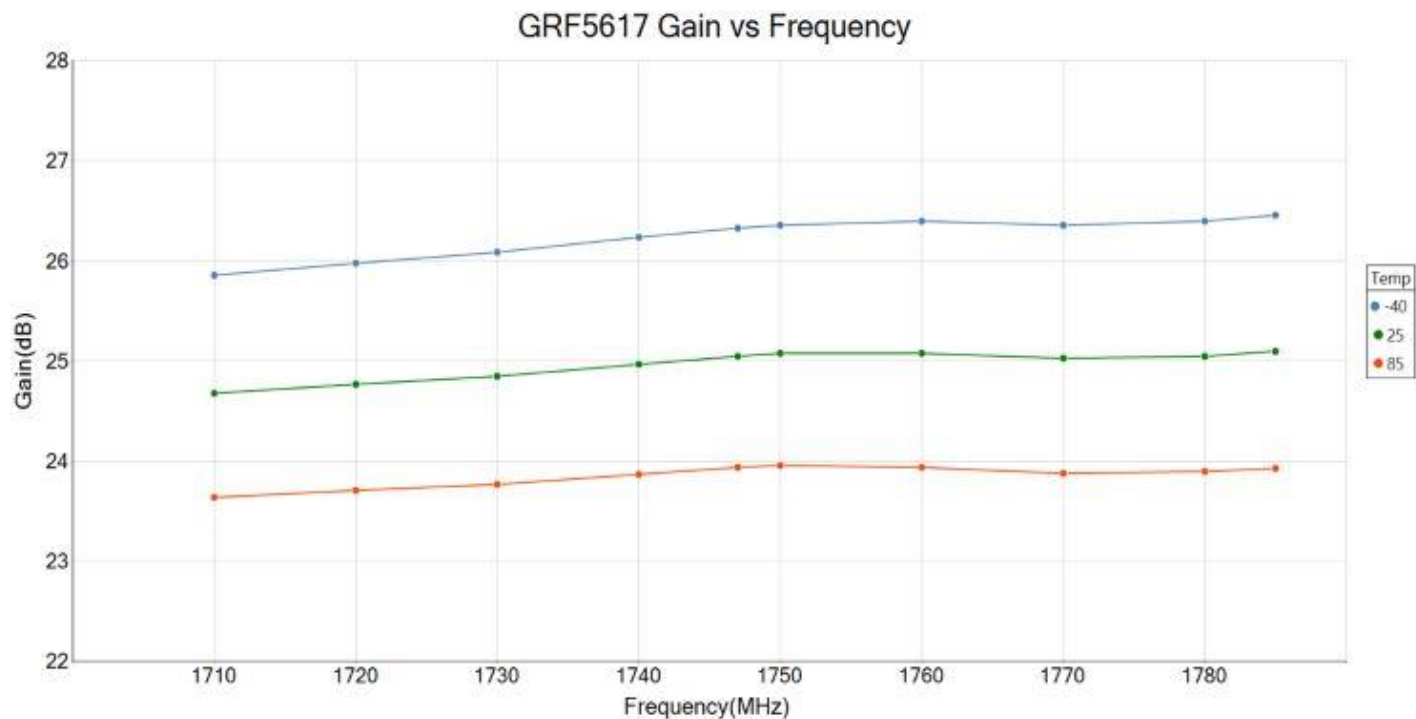
| Parameter                        | Symbol              | Specification |       |      | Unit | Condition  |
|----------------------------------|---------------------|---------------|-------|------|------|--|
|                                  |                     | Min.          | Typ.  | Max. |      |  |
| Small Signal Gain                | S21                 |               | 25.1  |      | dB   | $F_{\text{TEST}} = 1747 \text{ MHz}$ , $T_{\text{PKG HEAT SINK}} = 25 \text{ }^\circ\text{C}$ , $V_{\text{CC}} = 5 \text{ V}$ , $P_{\text{IN}} = -25 \text{ dBm}$ .  |
| Standby Mode Gain                | S21 <sub>STBY</sub> |               | -27   |      | dB   | Disabled Mode, $V_{\text{SHDN}}/V_{\text{EN1}}/V_{\text{EN2}} = \text{HIGH}$ , $P_{\text{IN}} = 0 \text{ dBm}$ .   |
| Input Return Loss                | S11                 |               | < -9  |      | dB   | $F_{\text{RF}} = 1710 \text{ to } 1785 \text{ MHz}$ .  |
| Output Return Loss               | S22                 |               | < -6  |      | dB   | $F_{\text{RF}} = 1710 \text{ to } 1785 \text{ MHz}$ .  |
| Reverse Isolation                | S12                 |               | < -42 |      | dB   | $F_{\text{RF}} = 1710 \text{ to } 1785 \text{ MHz}$ .  |
| Evaluation Board Noise Figure    | NF                  |               | 4.2   |      | dB   |  |
| Output 3rd Order Intercept Point | OIP3                |               | 49.3  |      | dBm  | 25 dBm $P_{\text{OUT}}$ per tone at 600 kHz Spacing.   |
| Output 1 dB Compression Power    | OP1dB               |               | 35.4  |      | dBm  | Sine wave input, $V_{\text{CC}} = 5 \text{ V}$ , $T_{\text{PKG HEAT SINK}} = 25 \text{ }^\circ\text{C}$ .  |
| Adjacent Channel Leakage Ratio   | ACLR                |               | -45   |      | dBc  | $P_{\text{OUT}} = +26.5 \text{ dBm}$ , LTE 20MHz 100RB TM1.1 Downlink Waveform with 9.6dB PAR, $F_{\text{TEST}} = 1747 \text{ MHz}$ , $T_{\text{PKG HEAT SINK}} = 25 \text{ }^\circ\text{C}$ , $V_{\text{CC}} = 5 \text{ V}$ . |

**Note 3:** MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. As additional production lots are fabricated, accumulated test data will be used to refine the MIN/MAX limits.

## Typical Operating Curve Conditions

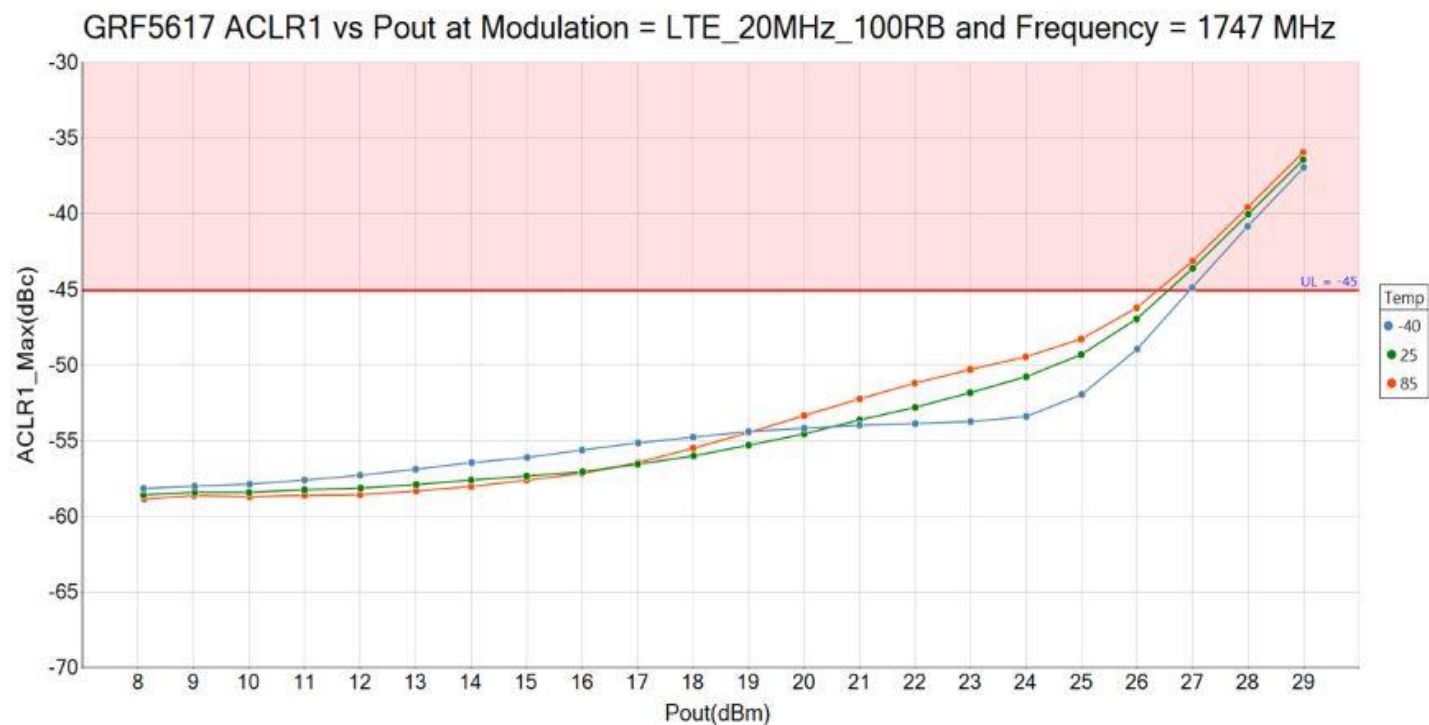
The following conditions apply unless noted otherwise: Typical Application Schematic using the 1710 to 1785 MHz tuning set,  $M5 = 9.76 \text{ k}\Omega$ ,  $M9 = 5.6 \text{ k}\Omega$ ,  $V_{\text{SHDN}} = \text{LOW}$ ,  $V_{\text{CC}} = 5 \text{ V}$ ,  $I_{\text{CCQ}} = 345 \text{ mA}$ ,  $50 \text{ }\Omega$  system impedance,  $F_{\text{TEST}} = 1747 \text{ MHz}$ ,  $T_{\text{PKG HEAT SINK}} = 25 \text{ }^\circ\text{C}$ . Evaluation board losses are included within the plots.

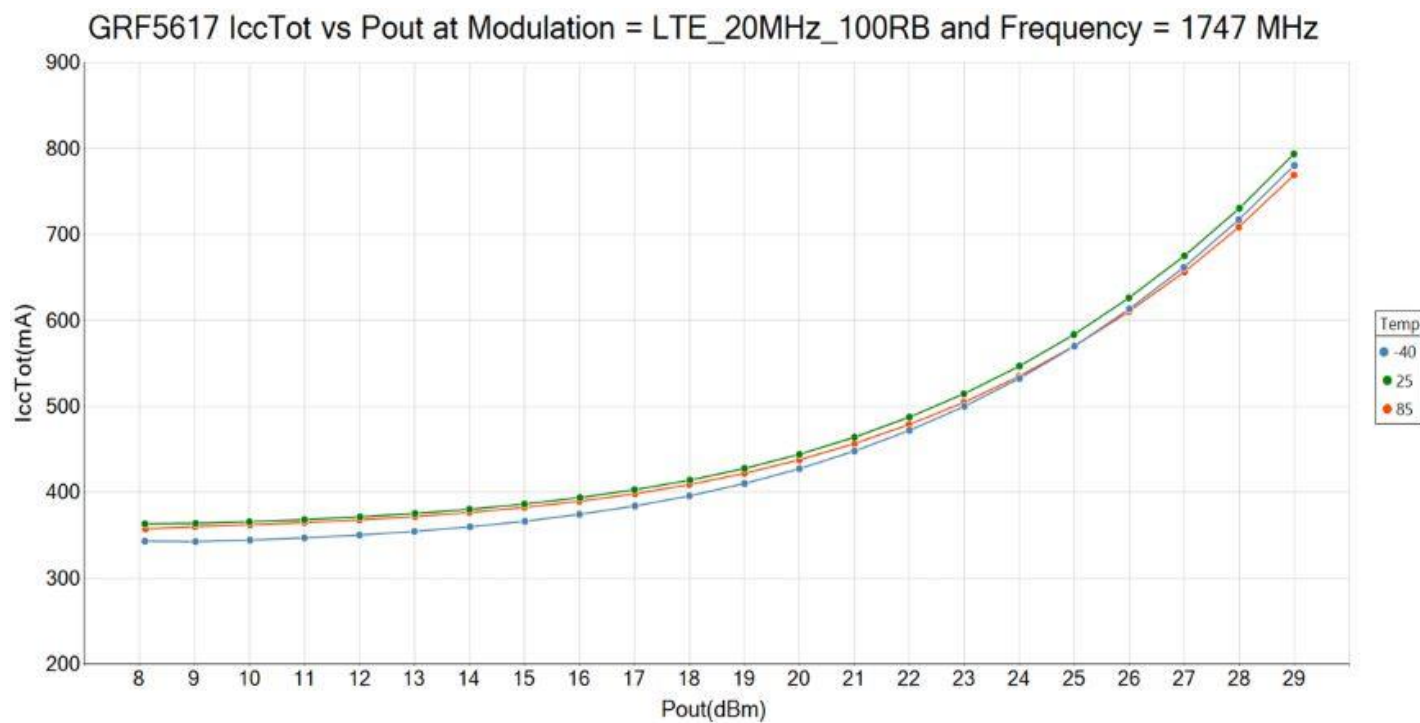
## GRF5617 Typical Operating Curves: 1710 to 1785 MHz Tune



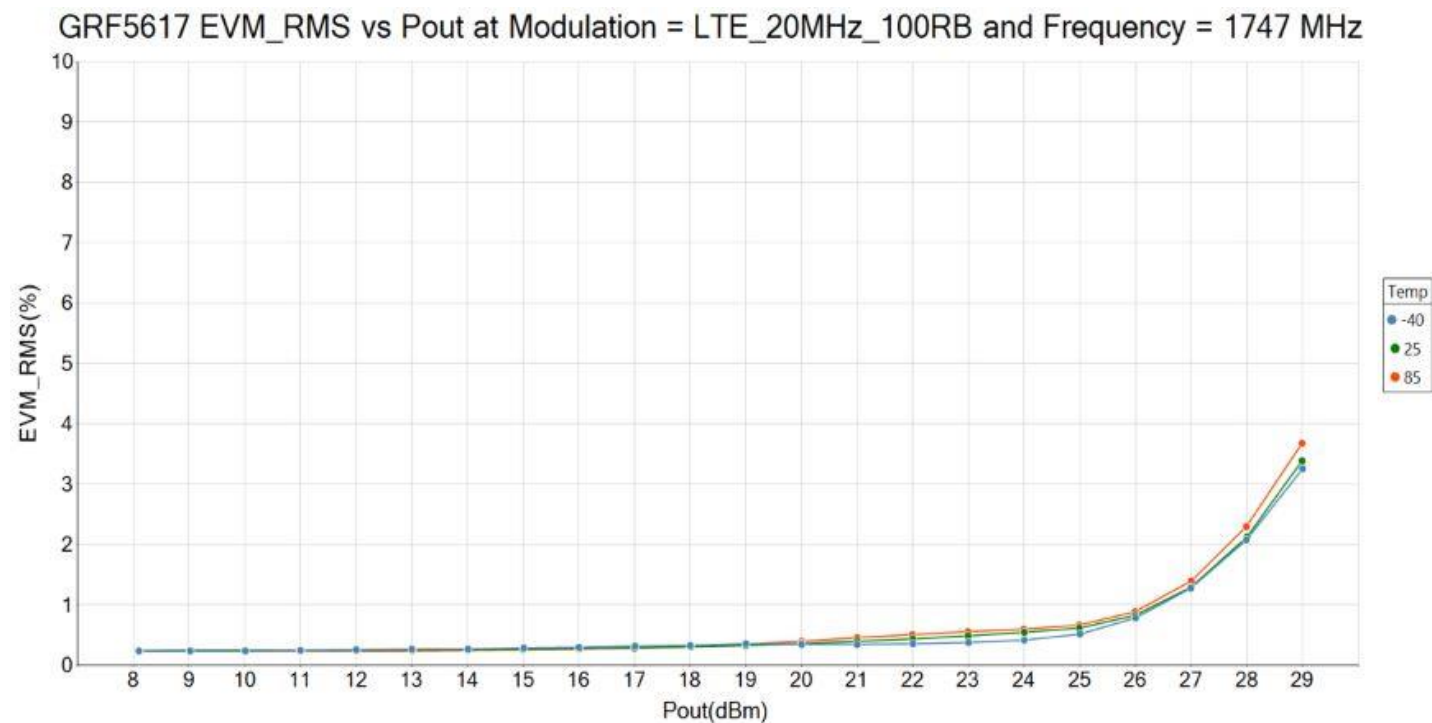


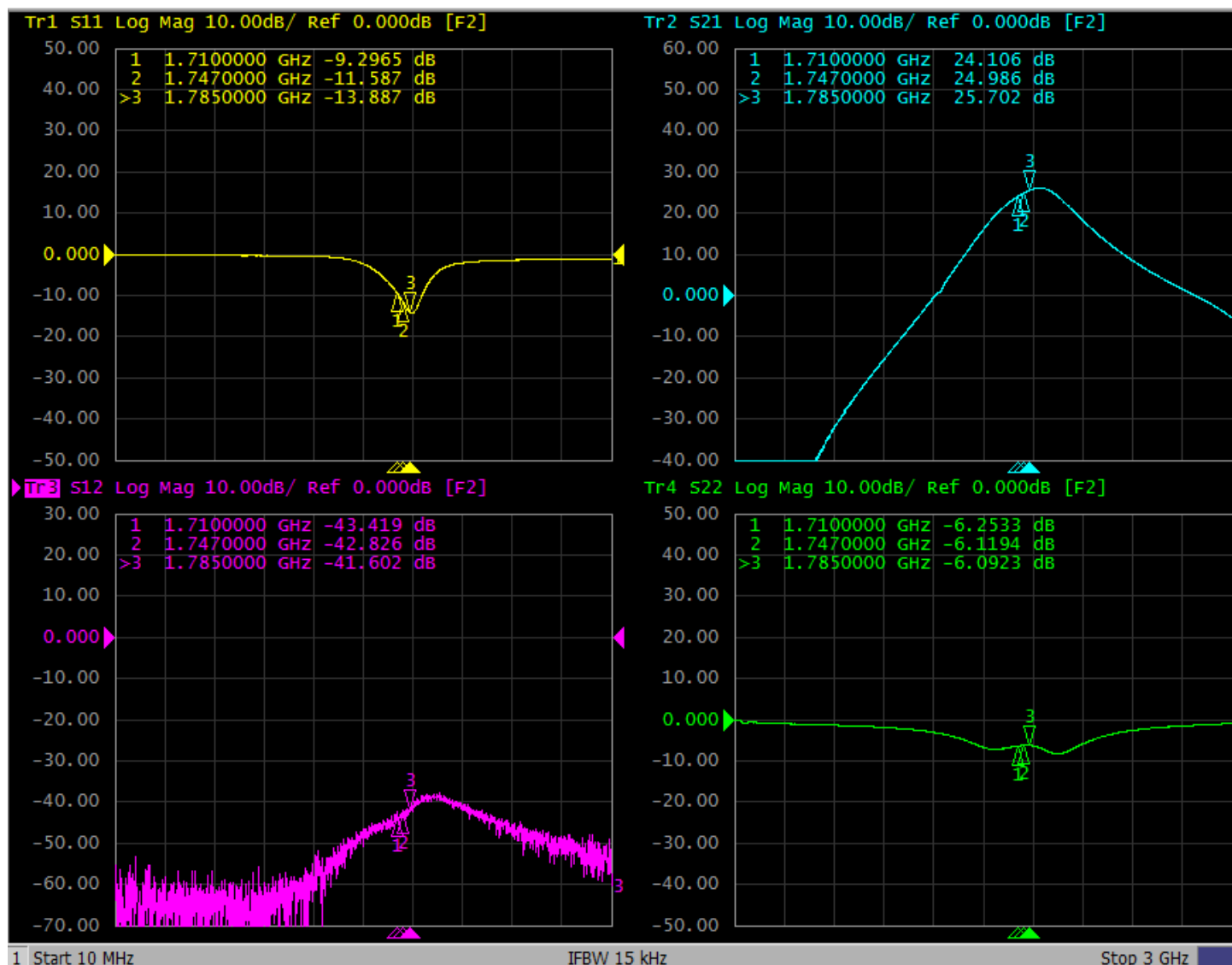
## GRF5617 Typical Operating Curves: ACLR vs. Pout (LTE 20Q100RB TM1.1 9.6 dB PAR)



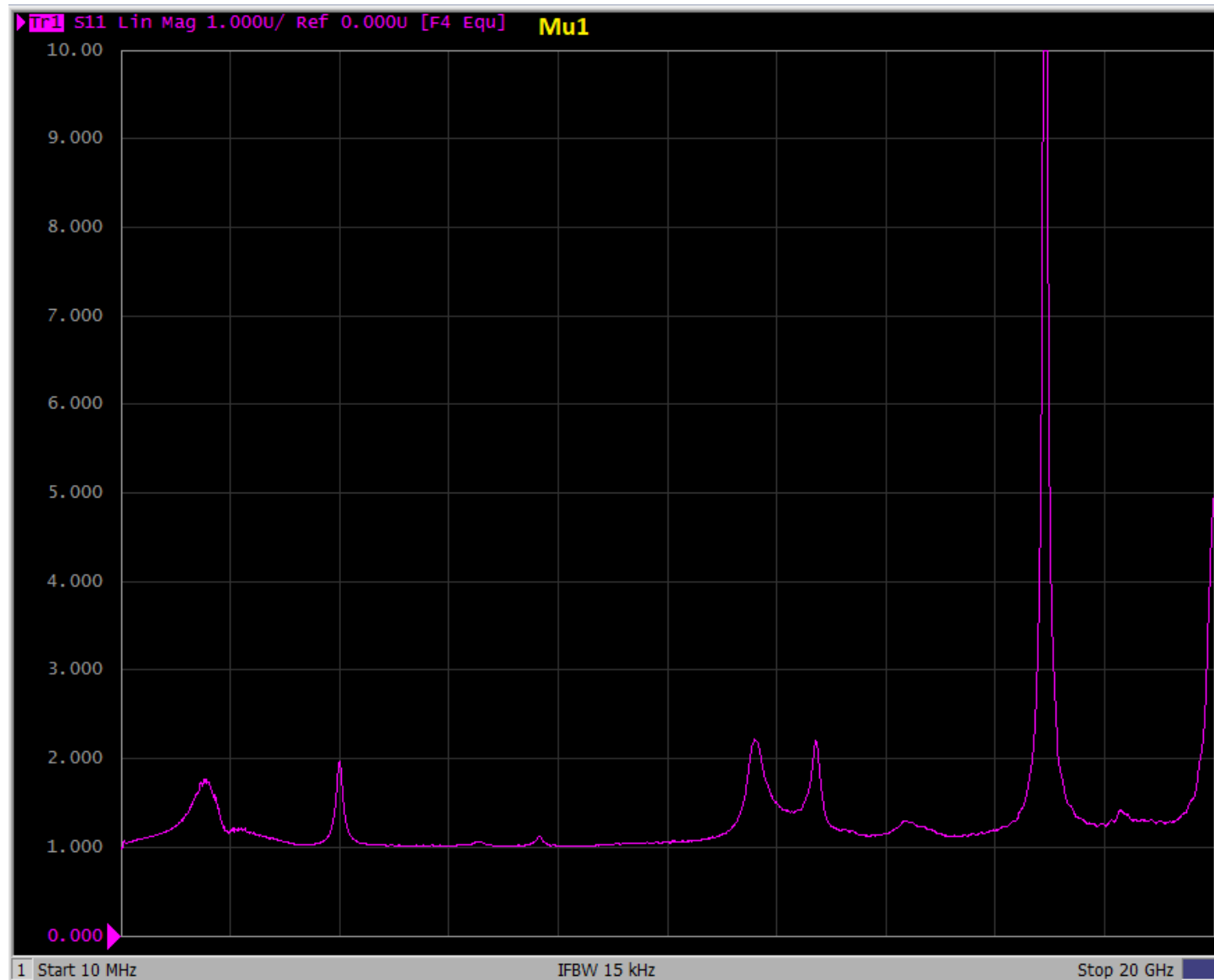
**GRF5617 Typical Operating Curves: Stage1 + Stage2 Icc vs. Pout (LTE 20Q100RB TM1.1 9.6 dB PAR)**


## GRF5617 Typical Operating Curves: EVM vs. Pout (LTE 20Q100RB TM1.1 9.6 dB PAR)



**GRF5617 Typical Operating Curves: S-Parameters (1710 to 1785 MHz Tune)**


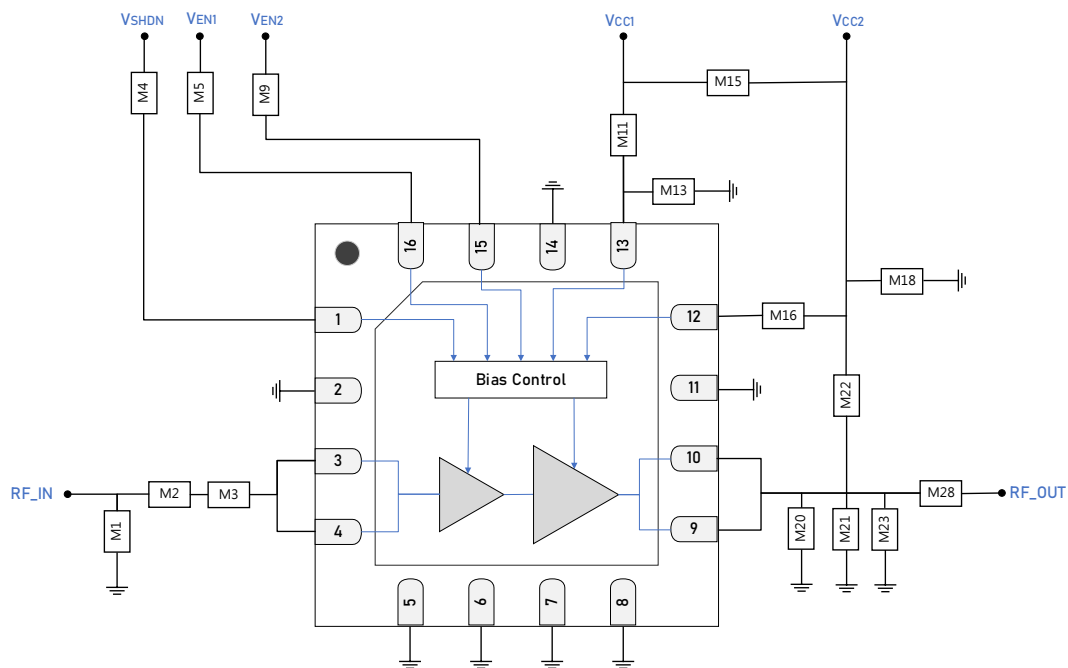
### GRF5617 Typical Operating Curves: Stability Mu (10 MHz to 20 GHz Tune)



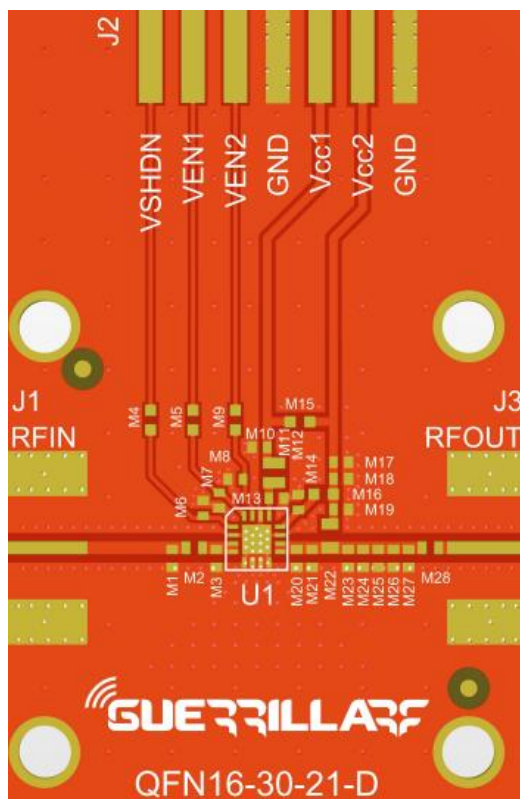
**Note:** Mu Factor  $\geq 1.0$  implies unconditional stability.

**Truth Table**

| Pin               | Logic | Condition             |
|-------------------|-------|-----------------------|
| $V_{\text{SHDN}}$ | LOW   | Full Operation        |
|                   | HIGH  | All Amplifiers Off    |
| $V_{\text{EN1}}$  | LOW   | Stage 1 Amplifier Off |
|                   | HIGH  | Stage 1 Amplifier On  |
| $V_{\text{EN2}}$  | LOW   | Stage 2 Amplifier Off |
|                   | HIGH  | Stage 2 Amplifier On  |



**GRF5617 Standard Test Schematic**



**GRF5617 Evaluation Board Assembly Diagram**

## GRF5617 Evaluation Board Assembly Diagram Reference

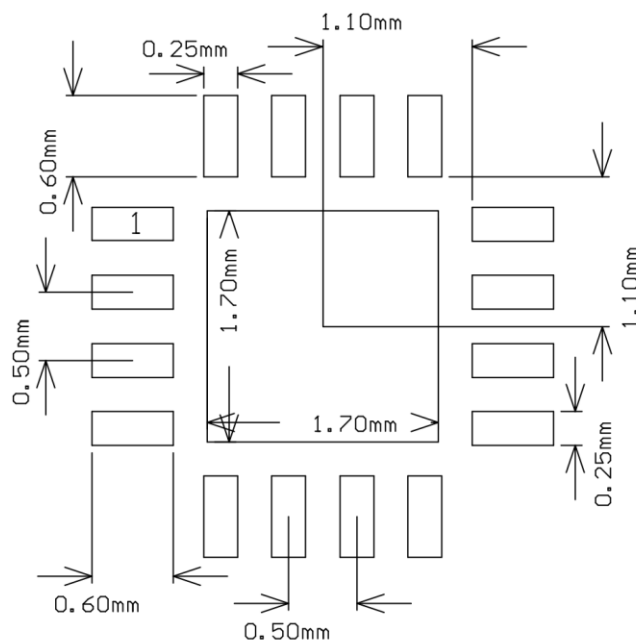
| Component        | Type              | Manufacturer | Family | Value         | Package Size | Substitution |
|------------------|-------------------|--------------|--------|---------------|--------------|--------------|
| M1               | Inductor          | Murata       | LQG    | 2.0 nH        | 0402         | ok           |
| M2               | Capacitor         | Murata       | GJM    | 2.7 pF        | 0402         | ok           |
| M3               | Resistor          | Various      | --     | 2.0 $\Omega$  | 0402         | ok           |
| M4               | Resistor          | Various      | --     | 0 $\Omega$    | 0402         | ok           |
| M5               | Resistor          | Various      | 1%     | 9760 $\Omega$ | 0402         | ok           |
| M9               | Resistor          | Various      | 1%     | 5600 $\Omega$ | 0402         | ok           |
| M11              | Resistor          | Various      | --     | 0 $\Omega$    | 0402         | ok           |
| M13              | Capacitor         | Murata       | GRM    | 0.1 $\mu$ F   | 0402         | ok           |
| M15              | Resistor (jumper) | Various      | --     | 0 $\Omega$    | 0402         | ok           |
| M16              | Resistor (jumper) | Various      | --     | 0 $\Omega$    | 0402         | ok           |
| M18              | Capacitor         | Murata       | GRM    | ** 10 $\mu$ F | 0402         | ok           |
| M20              | Capacitor         | Murata       | GJM    | 0.8 pF        | 0402         | ok           |
| M21              | Capacitor         | Murata       | GJM    | 2.7 pF        | 0402         | ok           |
| M22              | Inductor          | Coilcraft    | 0807SQ | 14 nH         | 0807         | ok           |
| MXX              | Capacitor         | Murata       | GJM    | 2.2 pF        | 0402         | ok           |
| M28              | Capacitor         | Murata       | GJM    | 22 pF         | 0402         | ok           |
| Evaluation Board | QFN16-30-21-D     |              |        |               |              |              |

**Notes:**

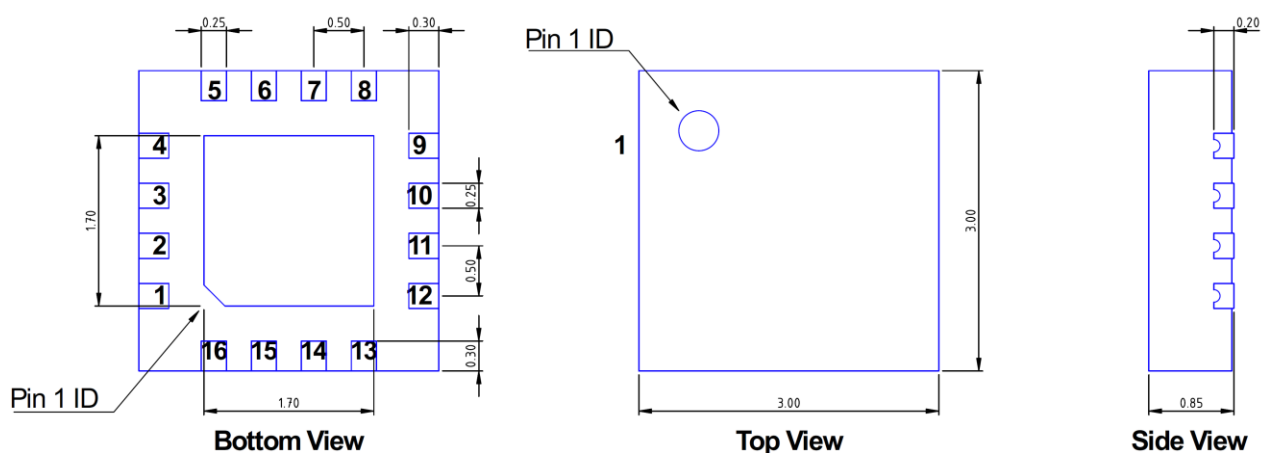
 Standard evaluation board bias:  $V_{CC} = 5\text{ V}$ ,  $V_{ENABLE} = 5\text{ V}$ .

 \*\* 10  $\mu$ F must be rated for > 5 V maximum ambient temperature. Manufacturer Part Number in this case = GRM155C80J106ME11D.





**3 x 3 mm QFN-16 Suggested PCB Footprint (Top View)**



**QFN16 3x3mm**  
Dimensions in millimeters

### 3 x 3 mm QFN-16 Package Dimensions

## Package Marking Diagram



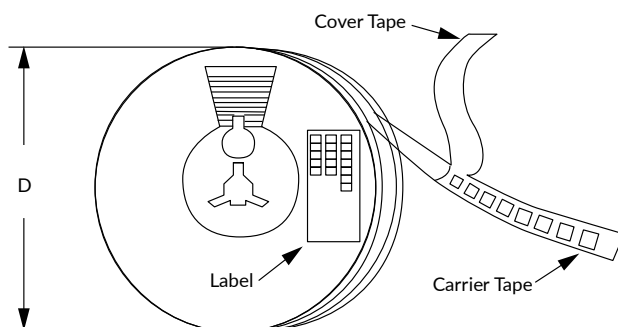
- Line 1: "XXXX" = PART NUMBER.
- Line 2: "YY" = YEAR and "WW" = WORK WEEK the device was assembled.

## Tape and Reel Information

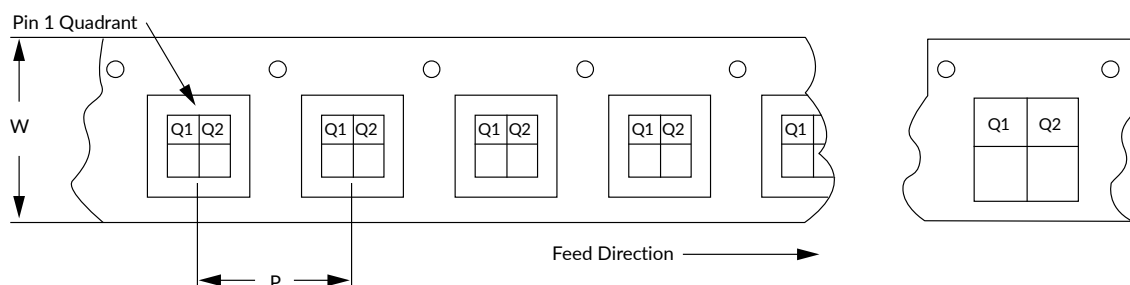
Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). See the following page for the Tape and Reel Specification and Device Package Information table, which includes units per reel.

Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag and the outside surface of the box.

For the Tape and Reel Reference Table, please refer to: <https://www.guerrilla-rf.com/prodFiles/Manufacturing/MN001.pdf>



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

## Revision History

| Revision Date    | Description of Change   |
|------------------|-------------------------|
| October 11, 2023 | Advance Data Sheet.     |
| December 6, 2023 | Preliminary Data Sheet. |



## Data Sheet Classifications

| Data Sheet Status | Notes  |
|-------------------|--|
| Advance           | S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.  |
| Preliminary       | All data based on limited evaluation board measurements taken within the Guerrilla RF Applications Lab. All parametric values are subject to change pending the collection of additional data.   |
| Release Ø         | All data based on measurements taken with <i>production-released</i> material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using <i>modelled estimates</i> that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory. |
| Release A-Z       | All data based on measurements taken with production-released material <i>derived from multiple lots which have been fabricated over an extended period of time</i> . MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.   |

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