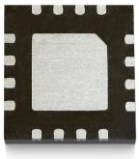
Data Sheet

PRELIMINARY DATA SHEET

GRF5617

HIGH LINEARITY POWER AMPLIFIER 1710 to 1785 MHz

FEATURES

- Excellent OP1dB, OIP3, ACLR and IM3 Performance
- Native Linearity Provides up to +26.5 dBm P_{OUT} with 45 dBc ACLR – Without the Need for Digital Predistortion Correction
- +26 dBm Linear Output Power Maintained at 85 °C
- Flexible Biasing Provides Latitude for Linearity Optimization
- 345 mA Native Mode Quiescent Current Consumption
- 5 V Supply Voltage
- 50 Ω Single-ended Input and Output Impedances
- Digital Shutdown
- Rugged Design is Extremely Resilient to Mismatched Loads
- -40 to 85 °C Operating Temperature Range
- Compact 3 x 3 mm QFN-16 Package
- RoHS Compliant

Reference: 5 V / 345 mA I_{CCQ} / 1747 MHz

- Gain: 25.1 dB
- OIP3: 49.3 dBm @ 25 dBm P_{OUT}/tone
- OP1dB: 35.4 dBm
- Evaluation Board Noise Figure: 4.2 dB

APPLICATIONS

- Cellular Boosters
- Automotive Compensators
- Picocells/Femtocells
- Customer Premise Equipment

DESCRIPTION

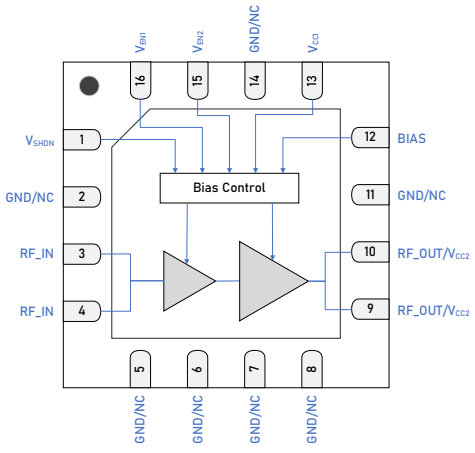
The GRF5617 is a high gain, two-stage InGaP HBT power amplifier designed to deliver excellent P1dB, ACLR and IM3 performance over the 1710 to 1785 MHz band. Its exceptional native linearity makes it an ideal choice for transmitter applications that typically do not employ digital predistortion correction schemes.

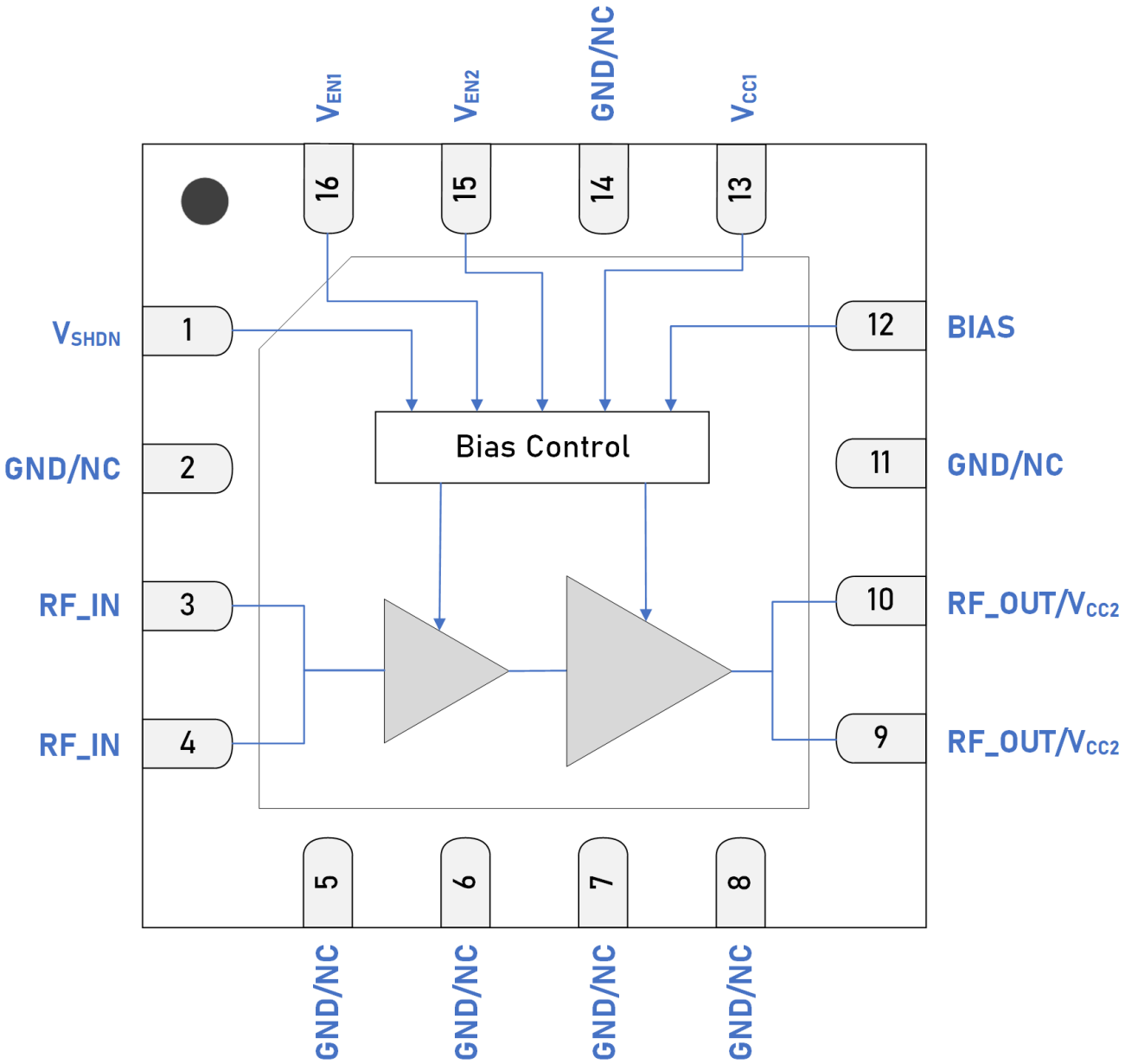
This device is part of a complete family of externally matched linear amplifiers that cover the following frequency ranges:

GRF5605: 617 - 652 MHz
GRF5606: 663 - 716 MHz
GRF5607: 703 - 748 MHz
GRF5608: 746 - 830 MHz
GRF5609: 814 - 862 MHz
GRF5610: 865 - 928 MHz
GRF5611: 902 - 960 MHz
GRF5617: 1710 - 1785 MHz
GRF5618: 1800 - 1900 MHz
GRF5626: 2500 – 2700 MHz
GRF5636: 3400 – 3800 MHz

Please consult with the GRF applications engineering team for custom tuning/evaluation board data.

BLOCK DIAGRAM





3 x 3 mm QFN-16 Pin Out (Top View)

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Pin Assignments

Pin	Name	Description	Note
1	V_{SHDN}	Digital Shutdown Pin	$V_{SHDN} \geq 1.8$ V (Logic HIGH) disables device. $V_{SHDN} \leq 0.8$ V (Logic LOW) enables device.
2, 5, 6, 7, 8, 11, 14	GND/NC	Ground or No Connect	No internal connection to die. These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
3, 4	RF_IN	RF Input	Pins 3 & 4 tied together on system board. An external DC blocking capacitor must be used.
9, 10	RF_OUT/V_{CC2}	PA Output/Bias Voltage	Pins 9 & 10 tied together on system board. V_{CC2} must be applied to this pin via an RF choke.
12	Bias	Bias Circuit Supply	Connect to V_{CC2} through external resistor.
13	V_{CC1}	Bias Voltage	Connect to V_{CC1} through external inductor (or 0 Ω resistor) with capacitive termination above (see application schematic).
15	V_{EN2}	Enable2 Voltage Input	V_{EN2} and series resistor set I_{CCQ} for the output stage. $V_{EN2} \leq 0.2$ volts disables stage 2.
16	V_{EN1}	Enable1 Voltage Input	V_{EN1} and series resistor set I_{CCQ} for the input stage. $V_{EN1} \leq 0.2$ volts disables stage 1.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

Absolute Ratings

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{CC}	3	5.25	V
RF Input Power	50 Ω, V_{CC} = 5 V, CW Tone, 100% Duty Cycle, $T_{PKG\ HEAT\ SINK}$ = 25 °C.	$P_{IN\ MAX-1:1}$		20	dBm
	Load VSWR ≤ 8:1, all phase angles, V_{CC} = 5 V, CW Tone, 100% Duty Cycle, $T_{PKG\ HEAT\ SINK}$ = -40 to 85 °C.	$P_{IN\ MAX-8:1}$		10	
Operating Temperature (Package Heat Sink).		$T_{PKG\ HEAT\ SINK}$	-40	85	°C
Maximum Junction Temperature (MTTF >10^6 Hours).		$T_{J\ MAX}$		190	°C
Maximum Dissipated Power Stage 1 (DC only, no RF applied).		$P_{DISS\ MAX}$		* 750	mW
Maximum Dissipated Power Stage 2 (DC only, no RF applied).		$P_{DISS\ MAX}$		* 2250	mW
Shutdown Voltage		V_{SHDN}		** 5.25	V
Electrostatic Discharge					
Charged Device Model		CDM	TBD		V
Human Body Model		HBM	TBD		V
Storage					
Storage Temperature		T_{STG}	-65	150	°C
Moisture Sensitivity Level		MSL		1	–

NOTES:

* Bias resistance at M5/M9 has been empirically optimized for linearity. Thus, there will be no benefit in decreasing (increasing) resistance (I_{CCQ}).

** M4 = 0 Ω. I_{SHDN} with V_{SHDN} = 5.25 V = 540 µA., decreasing linearly to 65 µA with nominal (and also minimum) V_{SHDN} = 1.8 V.

Caution! ESD Sensitive Device.
Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to *Manufacturing Note MN-001 — Package and Manufacturing Information.*

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging requiring no exemptions. Additional information for this topic can be found at this link - *Environmental and Restricted Substance Statement Library*

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Recommended Operating Conditions

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	3	5	5.25	V	
Operating Temperature (Package Heat Sink)	$T_{PKG\ HEAT\ SINK}$	-40		85	°C	
RF Frequency Range	F_{RF}	1710	1747	1785	MHz	**Note 1.**
RFIN Port Impedance	Z_{RFIN}		50		Ω	Single Ended with 3-element Match.
RFOUT Port Impedance	Z_{RFOUT}		50		Ω	Single Ended with 3-element Match.

Note 1: Operation outside this range is possible, but with degraded performance of some parameters.

Nominal Operating Parameters – General

The following conditions apply unless noted otherwise: Typical Application Schematic using the 1710 to 1785 MHz tuning set, M5 = 9.76 kΩ, M9 = 5.6 kΩ, V_{SHDN} = LOW, V_{CC} = 5 V, I_{CCQ} = 345 mA, 50 Ω system impedance, P_{OUT} = 26.5 dBm, F_{TEST} = 1747 MHz, $T_{PKG\ HEAT\ SINK}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Quiescent Current	I_{CCQ}		345		mA	I_{CCQ1} + I_{CCQ2}. No RF Applied.
Supply Current with RF Applied	I_{CC}		650		mA	I_{CC1} + I_{CC2}. RF Applied with P_{OUT} = 26.5 dBm.
Enable Current 1	$I_{ENABLE1}$		0.3		mA	V_{CC} = 5 V, $T_{PKG\ HEAT\ SINK}$ = 25 °C.
Enable Current 2	$I_{ENABLE2}$		0.5		mA	V_{CC} = 5 V, $T_{PKG\ HEAT\ SINK}$ = 25 °C.
Operating Temperature Range	$T_{PKG\ HEAT\ SINK}$	-40		+85	°C	Measured on Package Heat Sink.
Logic Input Low	V_{IL}	0		0.8	V	Applies to V_{SHDN} Input.
Logic Input High	V_{IH}	1.8		V_{CC}	V	Applies to V_{SHDN} Input.
Logic Current Low	I_{IL}		1.3		nA	Applies to V_{SHDN} Input, V_{IL} = 0.8 V.
Logic Current High	I_{IH}		65		µA	Applies to V_{SHDN} Input, V_{IH} = 1.8 V.
			285			Applies to V_{SHDN} Input, V_{IH} = 3.3 V.
Switching Rise Time	T_{RISE}		50		ns	Applies to V_{SHDN} Input.
Switching Fall Time	T_{FALL}		50		ns	Applies to V_{SHDN} Input.

Disabled Mode

Supply Quiescent Current	$I_{CCQ-SHDN}$		10		µA	V_{CC} = 5 V, V_{SHDN}/V_{EN1}/V_{EN2} = HIGH.
Enable Current 1	$I_{ENABLE1-SHDN}$		0.6		mA	V_{CC} = 5 V, V_{SHDN}/V_{EN1}/V_{EN2} = HIGH.
Enable Current 2	$I_{ENABLE2-SHDN}$		0.85		mA	V_{CC} = 5 V, V_{SHDN}/V_{EN1}/V_{EN2} = HIGH.

Thermal Data (Stage 1 and Stage 2)

Stage 1: Thermal Resistance (Infrared Scan). DC only (no RF applied).	Θ_{JC}		60		°C/W	On Standard Evaluation Board.
Stage 2: Thermal Resistance (Infrared Scan). DC only (no RF applied).	Θ_{JC}		30		°C/W	On Standard Evaluation Board.
Thermal Data Stage 1 & 2: See plot of junction Temp vs. Output Power.	T_J		TBD		°C	V_{CC} = V_{EN1} = V_{EN2} = 5 V. On Standard Evaluation Board **(note 2)**.

Note 2: MTTF >10^6 hours for $T_{CHANNEL}$ ≤190 °C.

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Nominal Operating Parameters – RF: 1.71 to 1.785 GHz, 5 V Operation

The following conditions apply unless noted otherwise: Typical Application Schematic using the 1710 to 1785 MHz tuning set, M5 = 9.76 kΩ, M9 = 5.6 kΩ, V_{SHDN} = LOW, V_{CC} = 5 V, I_{CCQ} = 345 mA, 50 Ω system impedance, P_{OUT} = 26.5 dBm, F_{TEST} = 1747 MHz, $T_{PKG\ HEAT\ SINK}$ = 25 °C. Evaluation board losses are included within the specifications.

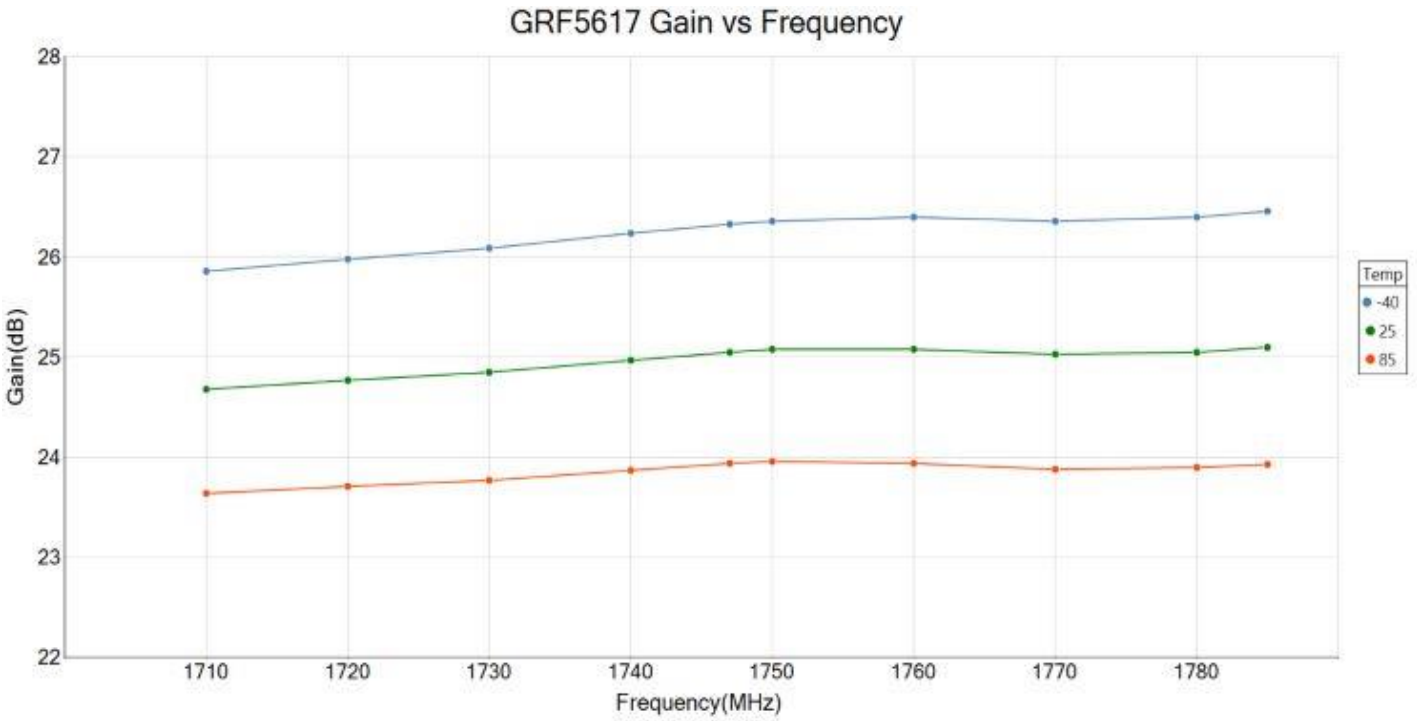
Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Small Signal Gain	S21		25.1		dB	F_{TEST} = 1747 MHz, $T_{PKG\ HEAT\ SINK}$ = 25 °C, V_{CC} = 5 V, P_{IN} = -25 dBm.
Standby Mode Gain	$S21_{STBY}$		-27		dB	Disabled Mode, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH, P_{IN} = 0 dBm.
Input Return Loss	S11		< -9		dB	F_{RF} = 1710 to 1785 MHz.
Output Return Loss	S22		< -6		dB	F_{RF} = 1710 to 1785 MHz.
Reverse Isolation	S12		< -42		dB	F_{RF} = 1710 to 1785 MHz.
Evaluation Board Noise Figure	NF		4.2		dB	
Output 3rd Order Intercept Point	OIP3		49.3		dBm	25 dBm P_{OUT} per tone at 600 kHz Spacing.
Output 1 dB Compression Power	OP1dB		35.4		dBm	Sine wave input, V_{CC} = 5 V, $T_{PKG\ HEAT\ SINK}$ = 25 °C.
Adjacent Channel Leakage Ratio	ACLR		-45		dBc	P_{OUT} = +26.5 dBm, LTE 20MHz 100RB TM1.1 Downlink Waveform with 9.6dB PAR, F_{TEST} = 1747 MHz, $T_{PKG\ HEAT\ SINK}$ = 25 °C, V_{CC} = 5 V.

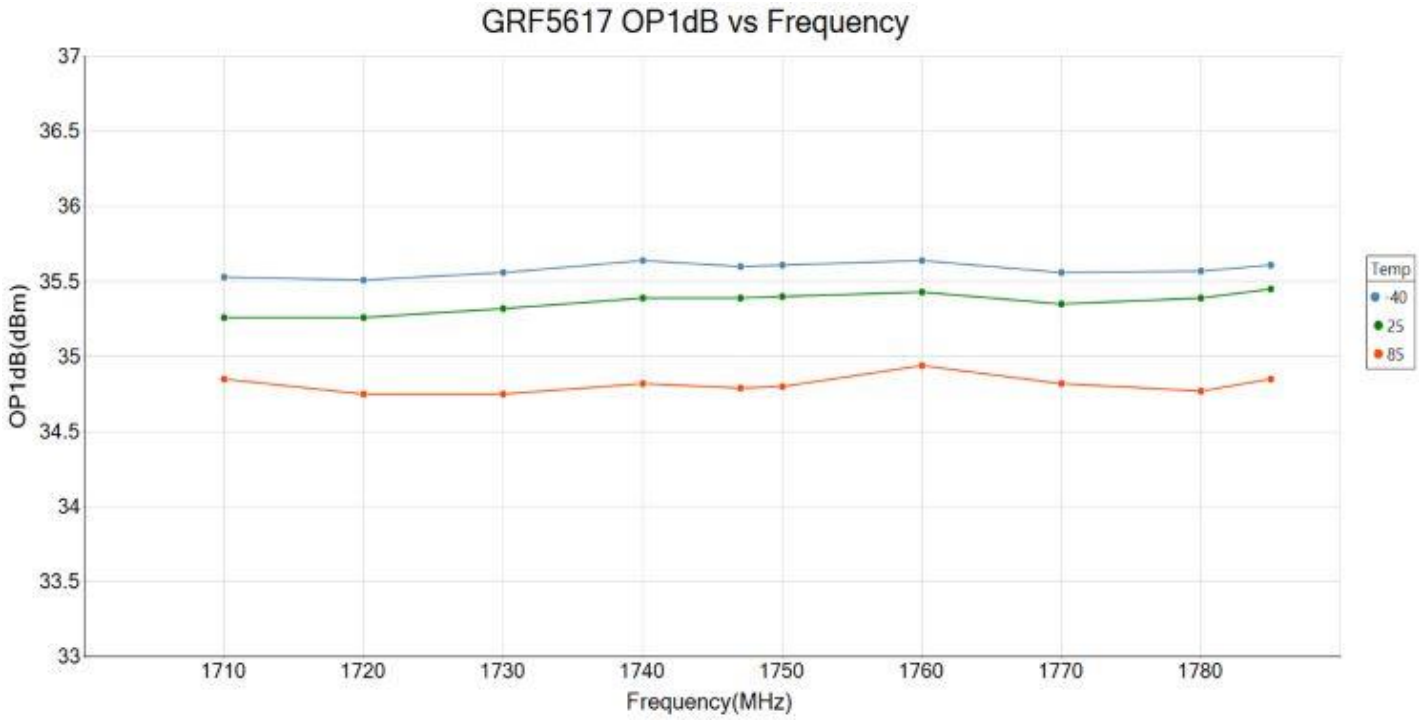
Note 3: MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. As additional production lots are fabricated, accumulated test data will be used to refine the MIN/MAX limits.

Typical Operating Curve Conditions

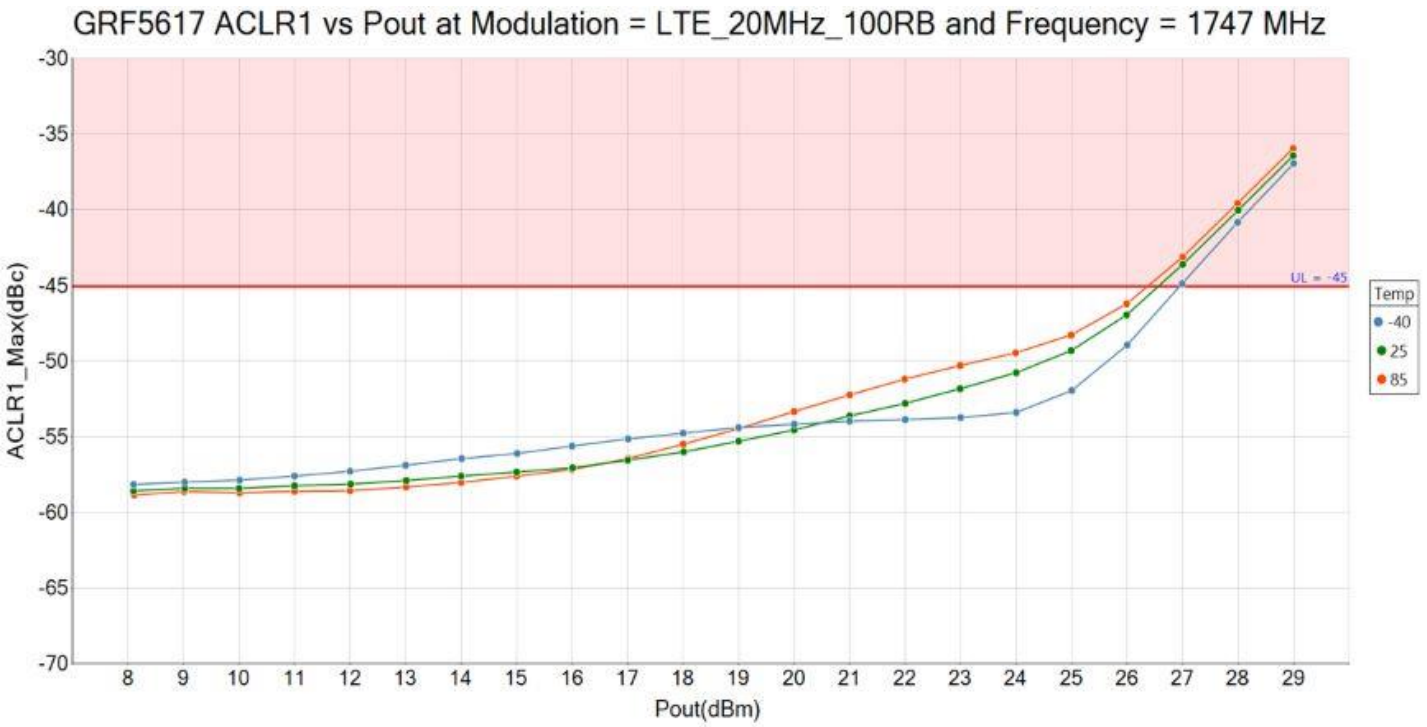
The following conditions apply unless noted otherwise: Typical Application Schematic using the 1710 to 1785 MHz tuning set, M5 = 9.76 kΩ, M9 = 5.6 kΩ, V_{SHDN} = LOW, V_{CC} = 5 V, I_{CCQ} = 345 mA, 50 Ω system impedance, F_{TEST} = 1747 MHz, $T_{PKG\ HEAT\ SINK}$ = 25 °C. Evaluation board losses are included within the plots.

GRF5617 Typical Operating Curves: 1710 to 1785 MHz Tune

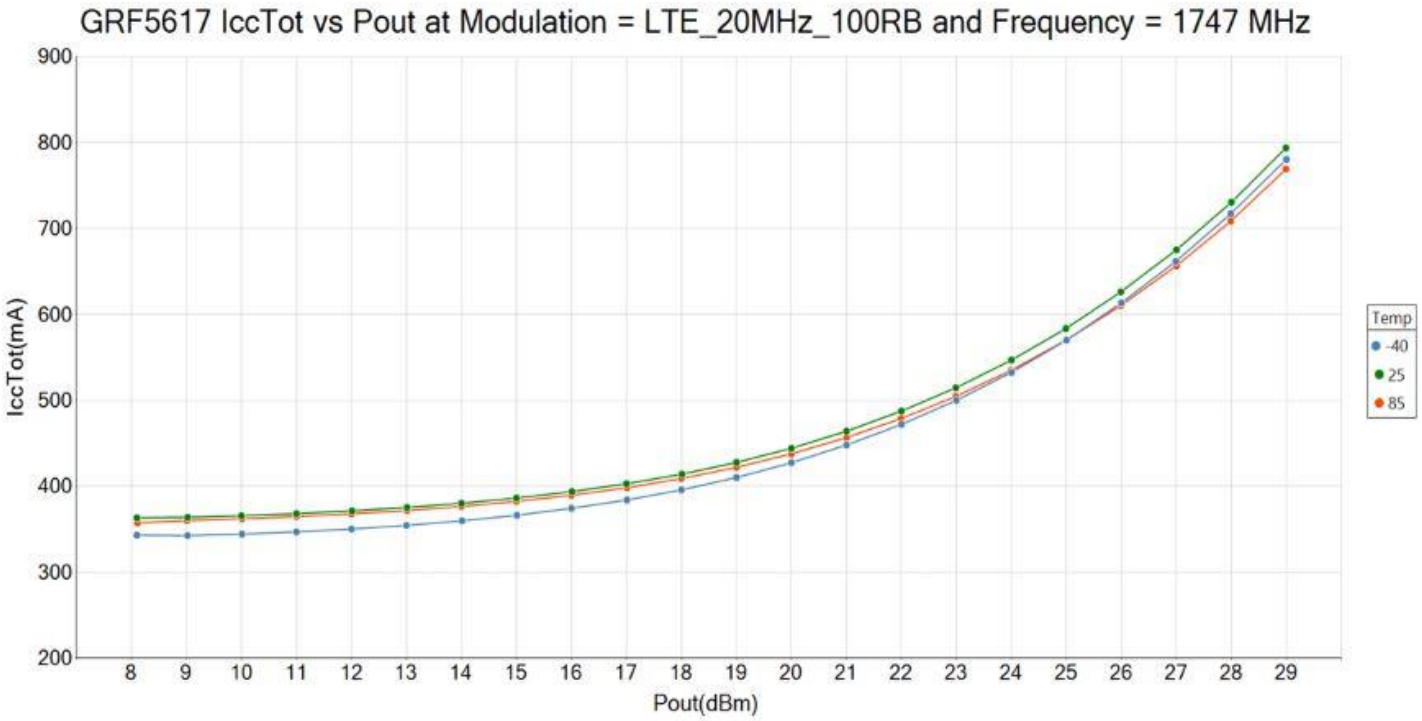




GRF5617 Typical Operating Curves: ACLR vs. Pout (LTE 20Q100RB TM1.1 9.6 dB PAR)



GRF5617 Typical Operating Curves: Stage1 + Stage2 Icc vs. Pout (LTE 20Q100RB TM1.1 9.6 dB PAR)



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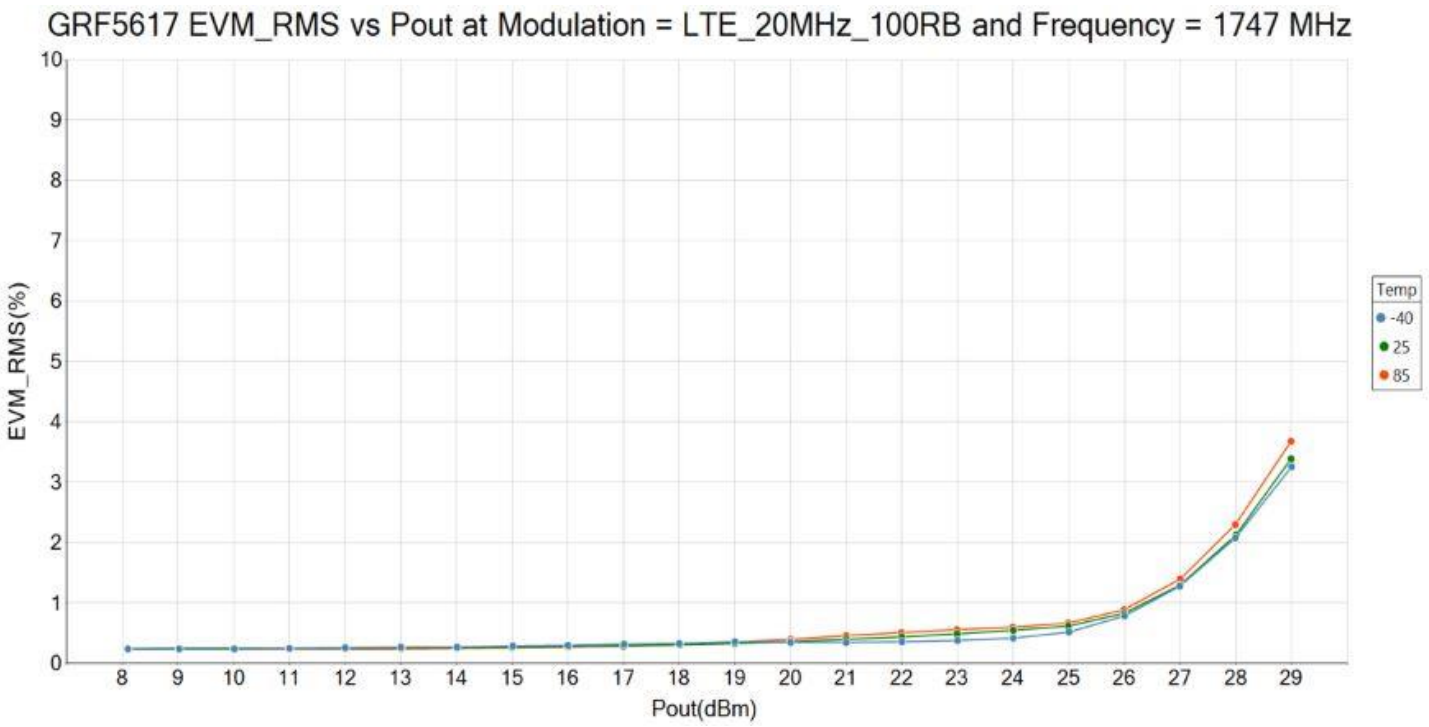
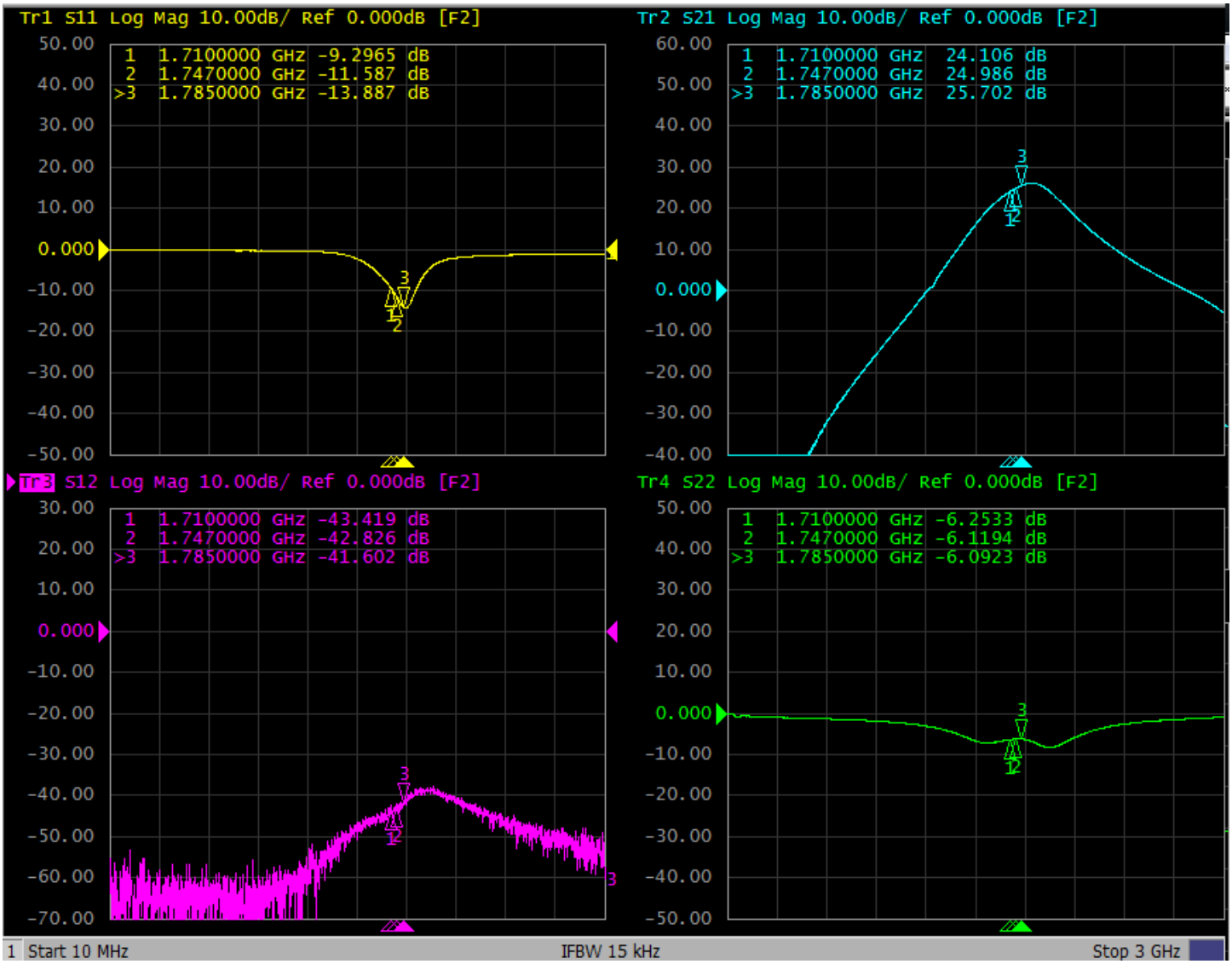
GRF5617 Typical Operating Curves: EVM vs. Pout (LTE 20Q100RB TM1.1 9.6 dB PAR)



GRF5617 Typical Operating Curves: S-Parameters (1710 to 1785 MHz Tune)



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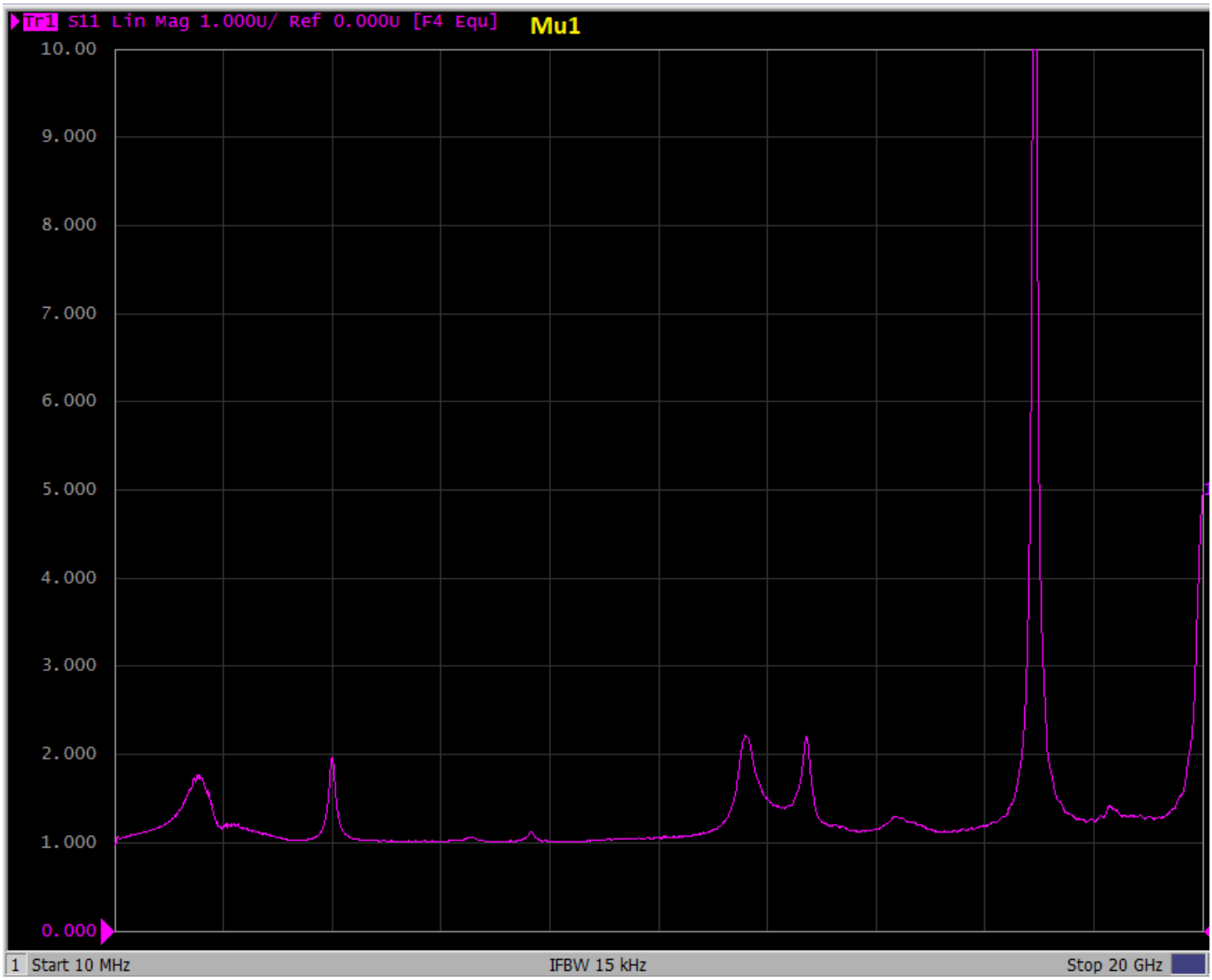
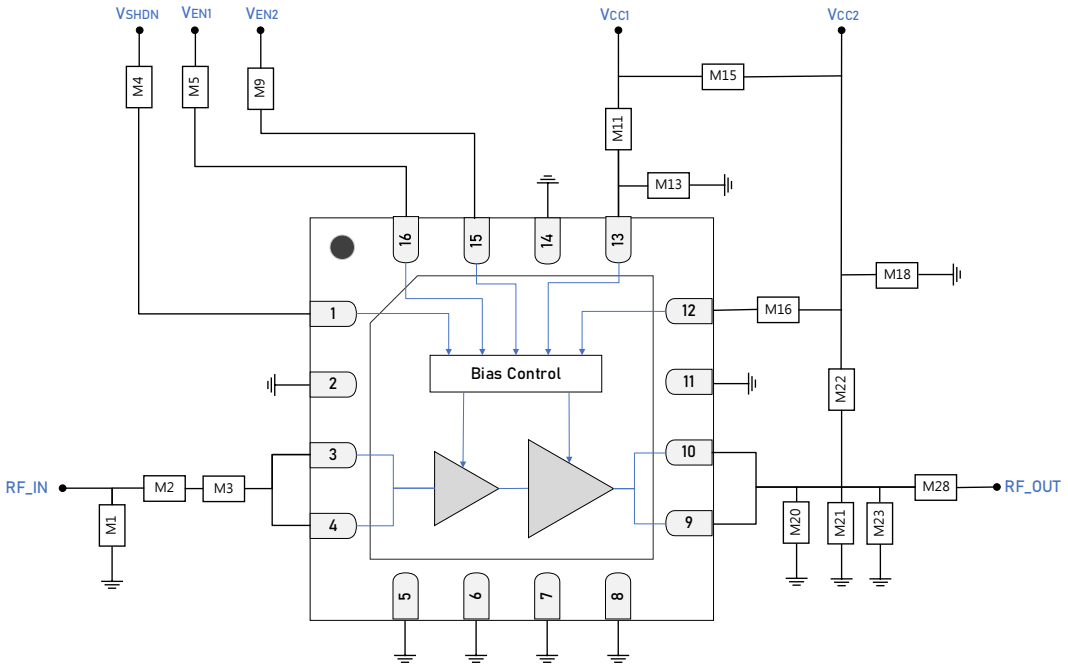
GRF5617 Typical Operating Curves: Stability Mu (10 MHz to 20 GHz Tune)



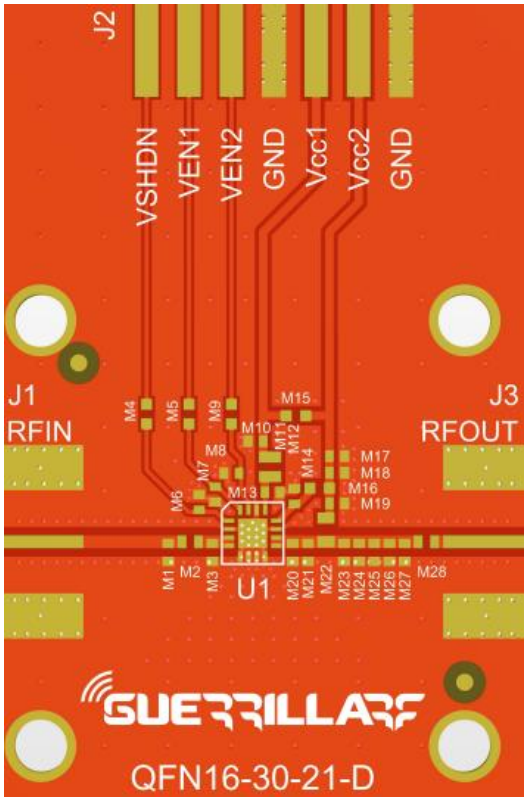
Note: Mu Factor ≥ 1.0 implies unconditional stability.

Truth Table

Pin	Logic	Condition
V_{SHDN}	LOW	Full Operation
	HIGH	All Amplifiers Off
V_{EN1}	LOW	Stage 1 Amplifier Off
	HIGH	Stage 1 Amplifier On
V_{EN2}	LOW	Stage 2 Amplifier Off
	HIGH	Stage 2 Amplifier On



GRF5617 Standard Test Schematic



GRF5617 Evaluation Board Assembly Diagram

GRF5617 Evaluation Board Assembly Diagram Reference

Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M1	Inductor	Murata	LQG	2.0 nH	0402	ok
M2	Capacitor	Murata	GJM	2.7 pF	0402	ok
M3	Resistor	Various	--	2.0 Ω	0402	ok
M4	Resistor	Various	--	0 Ω	0402	ok
M5	Resistor	Various	1%	9760 Ω	0402	ok
M9	Resistor	Various	1%	5600 Ω	0402	ok
M11	Resistor	Various	--	0 Ω	0402	ok
M13	Capacitor	Murata	GRM	0.1 µF	0402	ok
M15	Resistor (jumper)	Various	--	0 Ω	0402	ok
M16	Resistor (jumper)	Various	--	0 Ω	0402	ok
M18	Capacitor	Murata	GRM	** 10 µF	0402	ok
M20	Capacitor	Murata	GJM	0.8 pF	0402	ok
M21	Capacitor	Murata	GJM	2.7 pF	0402	ok
M22	Inductor	Coilcraft	0807SQ	14 nH	0807	ok
MXX	Capacitor	Murata	GJM	2.2 pF	0402	ok
M28	Capacitor	Murata	GJM	22 pF	0402	ok
Evaluation Board	QFN16-30-21-D					

Notes:
Standard evaluation board bias: V_{CC} = 5 V, V_{ENABLE} = 5 V.
** 10 uF must be rated for > 5 V maximum ambient temperature. Manufacturer Part Number in this case = GRM155C80J106ME11D.

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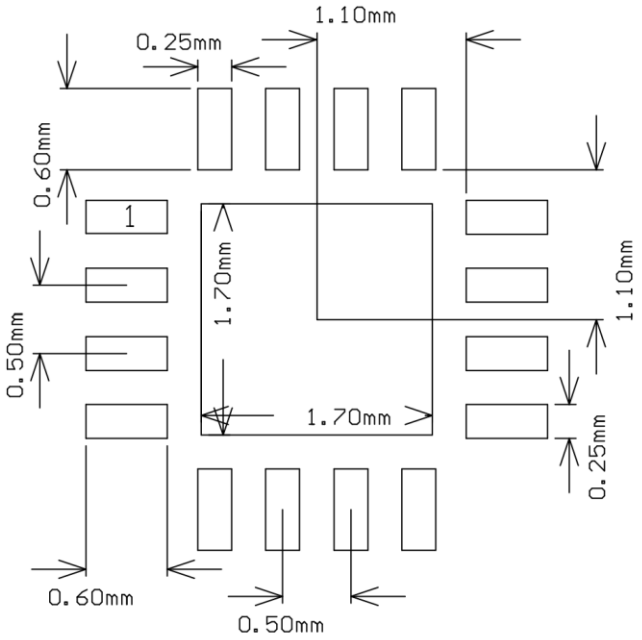
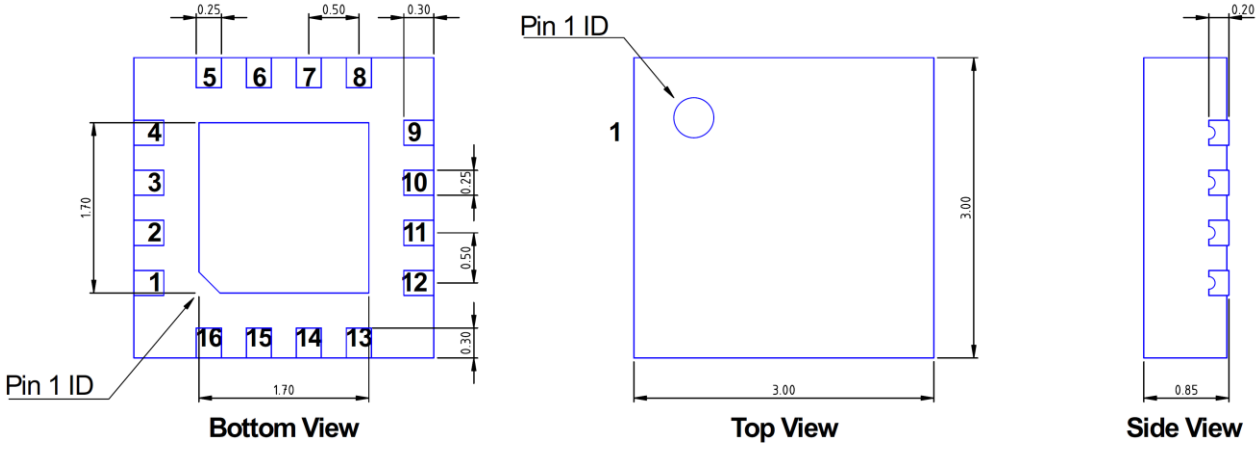


3 x 3 mm QFN-16 Suggested PCB Footprint (Top View)



3 x 3 mm QFN-16 Package Dimensions

Package Marking Diagram

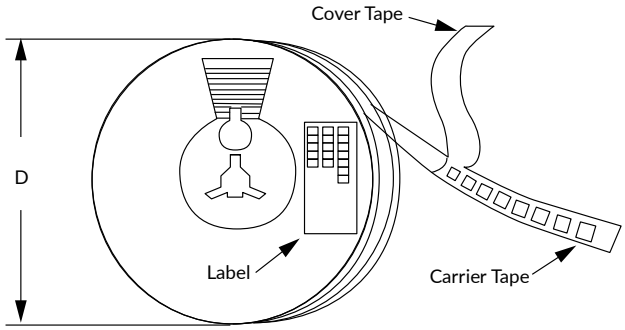
- Line 1: "XXXX" = PART NUMBER.
- Line 2: "YY" = YEAR and "WW" = WORK WEEK the device was assembled.

Tape and Reel Information

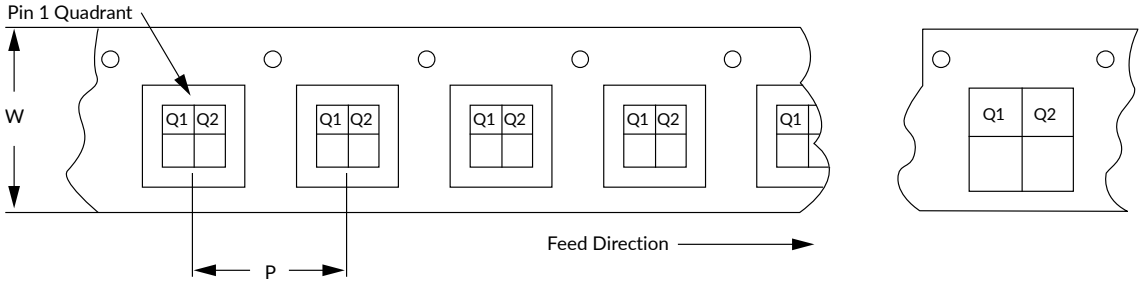
Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). See the following page for the Tape and Reel Specification and Device Package Information table, which includes units per reel.

Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag and the outside surface of the box.

For the Tape and Reel Reference Table, please refer to: *https://www.guerrilla-rf.com/prodFiles/Manufacturing/MN001.pdf*



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

Revision History

Revision Date	Description of Change
October 11, 2023	Advance Data Sheet.
December 6, 2023	Preliminary Data Sheet.

Data Sheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on limited evaluation board measurements taken within the Guerrilla RF Applications Lab. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time.* MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.