Sub-LVDS Signaling Using Lattice Devices

Technical Note

FPGA-TN-02028-2.3

November 2022

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
PCB	Printed Circuit Board

1. Introduction

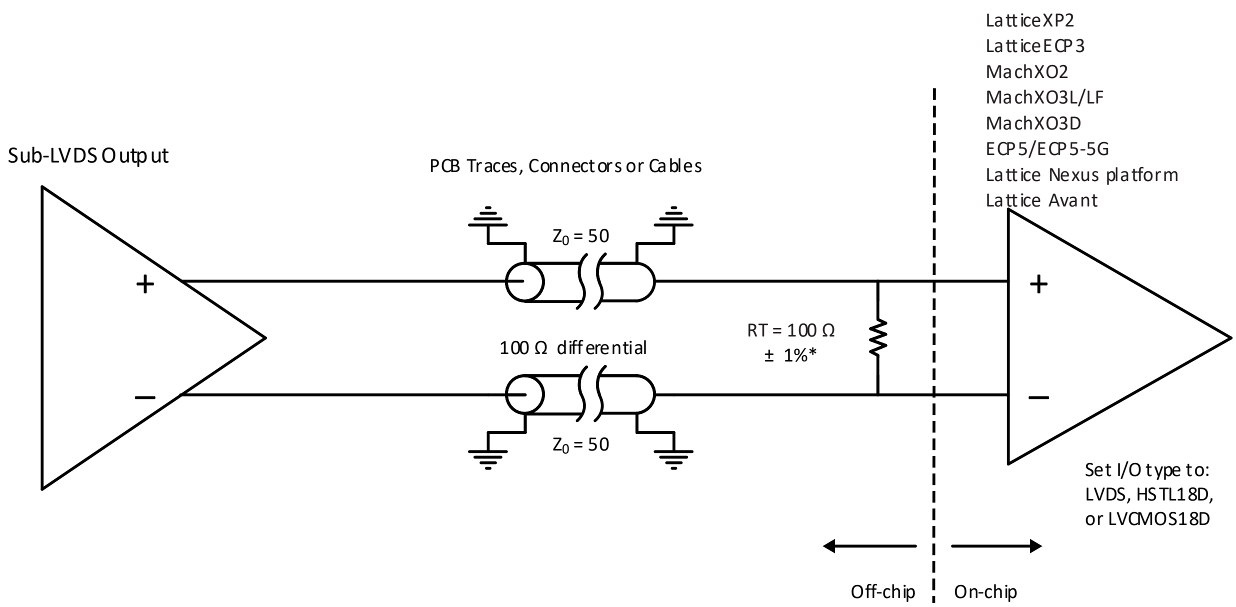
Sub-LVDS is a reduced-voltage form of LVDS signaling. This technical note summarizes the main differences between sub-LVDS and LVDS, to show how Lattice FPGA devices can support the sub-LVDS I/O standard. This knowledge can be applied to the Lattice data sheets to confirm compatibility when selecting I/O types to implement sub-LVDS solutions with Lattice devices.

2. Differences between LVDS and Sub-LVDS Signals

The following Lattice devices include the LVDS I/O types:

- ECP5™/ECP5-5G™
- LatticeECP3™
- LatticeXP2™
- MachXO2™
- MachXO3L/LF™
- MachXO3L/LF™
- Lattice Nexus platform
    - CrossLink™-NX
    - CrossLink™-NX-33
    - Certus™-NX
    - CertusPro™-NX
    - MachXO5™-NX/MachXO5D™-NX
- Avant™

Sub-LVDS is different from LVDS in which the differential and common mode signal levels are reduced. As such, a sub-LVDS output can directly drive an LVDS input, as shown in Figure 2.1.



* The LatticeXP2, LatticeECP3, MachXO2, MachXO3L/LF, MachXO3D, ECP5/ECP5-5G, Lattice Nexus platform, and Lattice Avant devices can be configured to do the 100 Ω termination on-chip.

Figure 2.1. Sub-LVDS Output Driving a Lattice Device Input

Table 2.1 shows sub-LVDS output signal voltages, and the Lattice device LVDS input specifications. When comparing the values in the table, it is clear that the Lattice device LVDS inputs are compatible to receive sub-LVDS output signals.

Table 2.1. Sub-LVDS Output Signal Voltages and LVDS Input Specifications

Sub-LVDS Output Characteristic		ECP5/ ECP5-5G LVDS Input	LatticeECP3 LVDS Input	LatticeXP2 LVDS Input	MachXO2, MachXO3L/ LF and MachXO3D LVDS Input	MachXO2 HSTL18D_I Input	MachXO3L/LF and MachXO3D LVCMOS18D Input	Lattice Nexus Platform LVDS Input	Avant LVDS Input	Unit
Common Mode Voltage Min (Vcm)	0.75	0.05	0.05	0.05	0.05	0.05	0.05	0.05	—	V
Common Mode Voltage Max (Vcm)	1.05	2.35	2.35	2.35	2.0	1.1	1.1	1.55	—	V
Differential Voltage Min (Vod)	100	100	100	100	100	100	100	100	—	mV
Differential Voltage Max (Vod)	200	2400	2400	2400	2050	1105	1105	1600	—	mV

In some instances, a sub-LVDS receiver is expected to detect signals below the sub-LVDS minimum differential output level of 100 mV. Based on simulation and characterization tests, the LVDS inputs for LatticeXP2, LatticeECP3, and ECP5/ECP5-5G family devices can detect differential signal levels down to 70 mV. Figure 2.2 shows a typical simulation waveform of an ECP5/ECP5-5G device, a LatticeECP3, and a LatticeXP2 differential input buffer that is able to properly detect the input differential at 70 mV. Figure 2.3 and Figure 2.4 show a similar hardware test condition that shows the input and output signals associated with the differential input voltage at 70 mV.

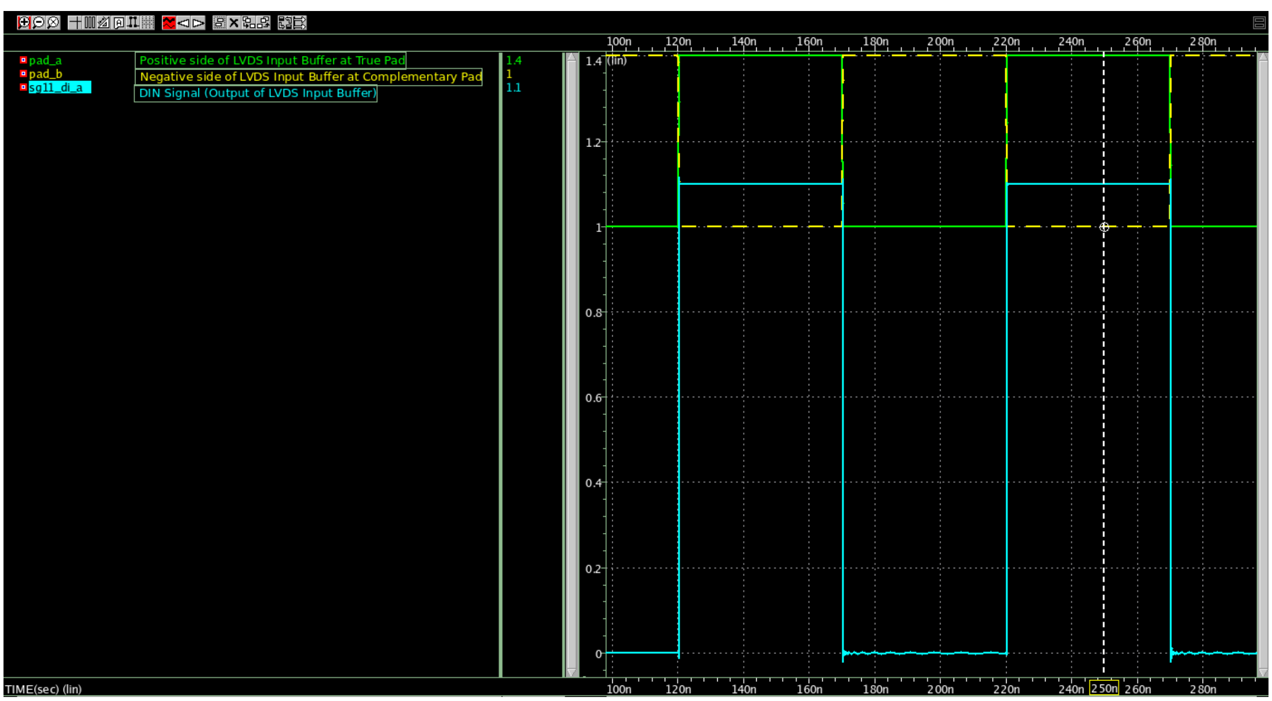


Figure 2.2. Typical Differential Input Simulation Waveform

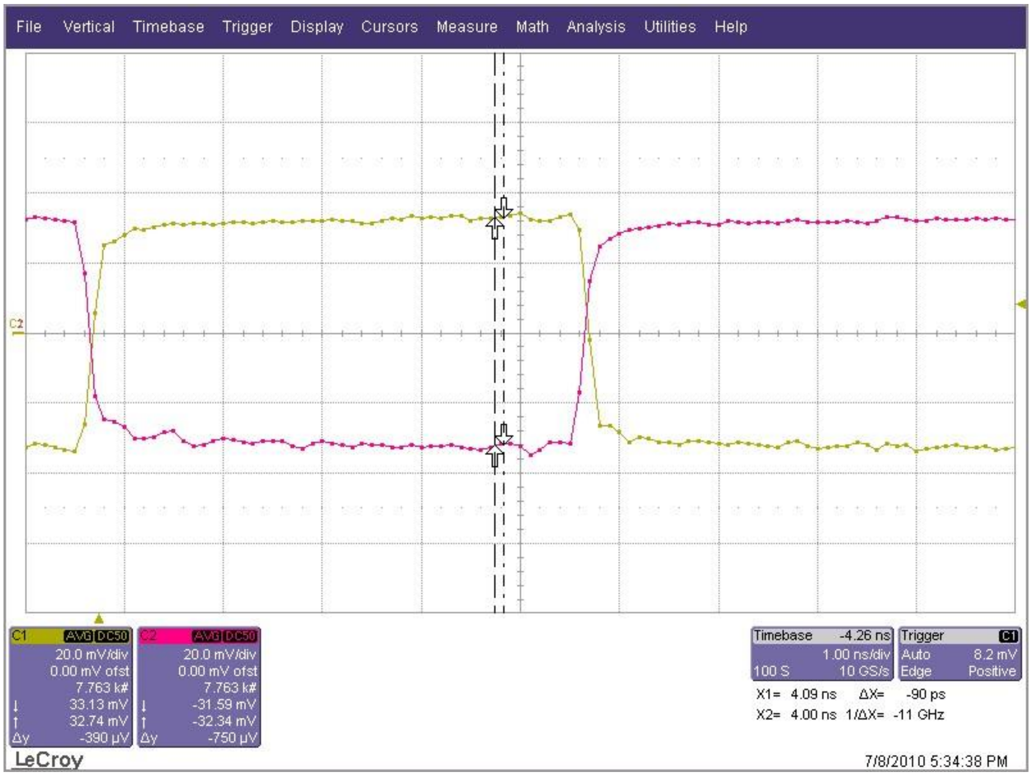


Figure 2.3. <70 mV Differential Input Waveform for Hardware Test

Figure 2.4. Typical Differential Output Waveform > 200 mV from Hardware Test

The LatticeECP3 and LatticeXP2 devices, when configured as an HSTL18D input, have the same input differential and common mode performance as the LVDS input type. As a result, HSTL18D can be set in the Lattice design software to represent a sub-LVDS input. On the MachXO2, the HSTL18D inputs have a different specification compared to the LVDS inputs. For the MachXO3L and MachXO3D devices, it would be the LVCMOS18D inputs that supports the sub-LVDS specifications. See Table 2.1 for values and IO_TYPES to be used for each of the devices.

Sub-LVDS, like LVDS, requires 100 Ω termination at the receiver but does not specify that the termination is internal or external to the receiver. Avant, the Nexus platform, and ECP5/ECP5-5G devices have internal 100 Ω differential termination that the user can select. The LatticeECP3 device has built-in differential termination with selectable values of 80, 100, 120, or off. The internal differential 100 Ω terminations are only available for inputs on the left and right sides of the device. See LatticeECP3 Family Data Sheet (DS1021) for additional information about on-die termination. The MachXO2, MachXO3L/LF, and MachXO3D devices support on-chip 100 Ω (nominal) input differential termination on the bottom edge. The LatticeXP2 device has no internal input termination, so it requires external 100 Ω differential input terminations. When external termination is used, the resistor should be either 0402 body size or surface mount resistor packs, placed as close as possible to the input BGA balls on the device.

If you would like to generate sub-LVDS output signals using LatticeECP3 and LatticeXP2 devices, it is recommended to set the I/O type to SSTL18D_II, and add the resistor network shown in Figure 2.5 to emulate a sub-LVDS output type.

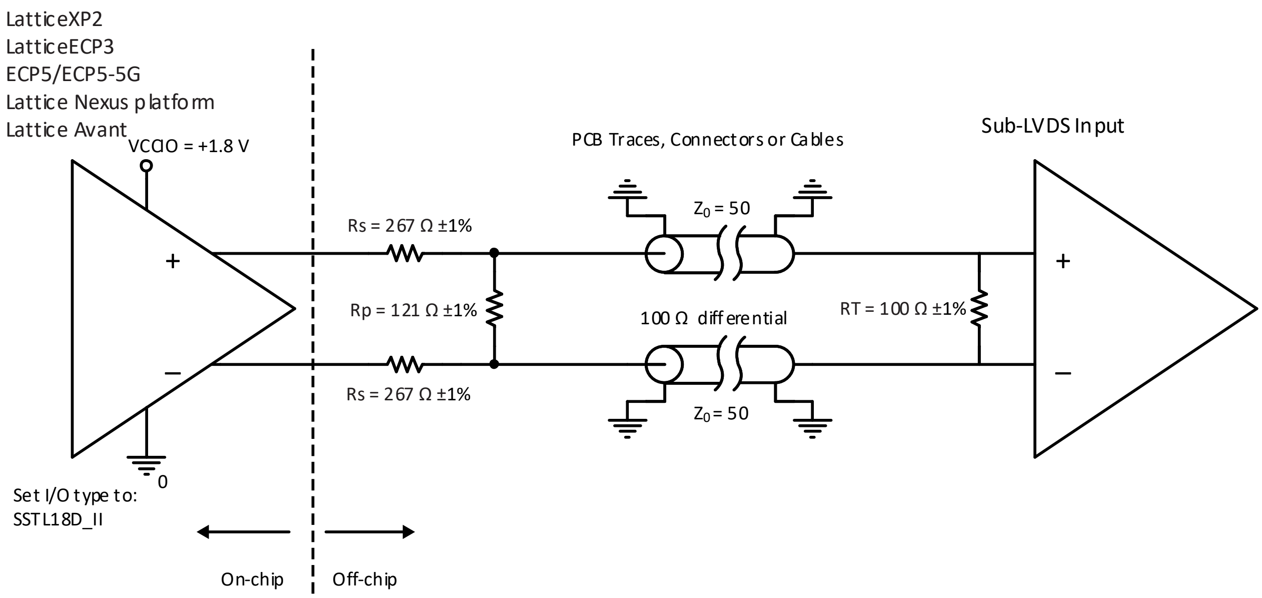


Figure 2.5. Lattice Device Generating a Sub-LVDS Signal Level – LatticeXP2, LatticeECP3, ECP5/ECP5-5G, Lattice Nexus Platform, and Lattice Avant

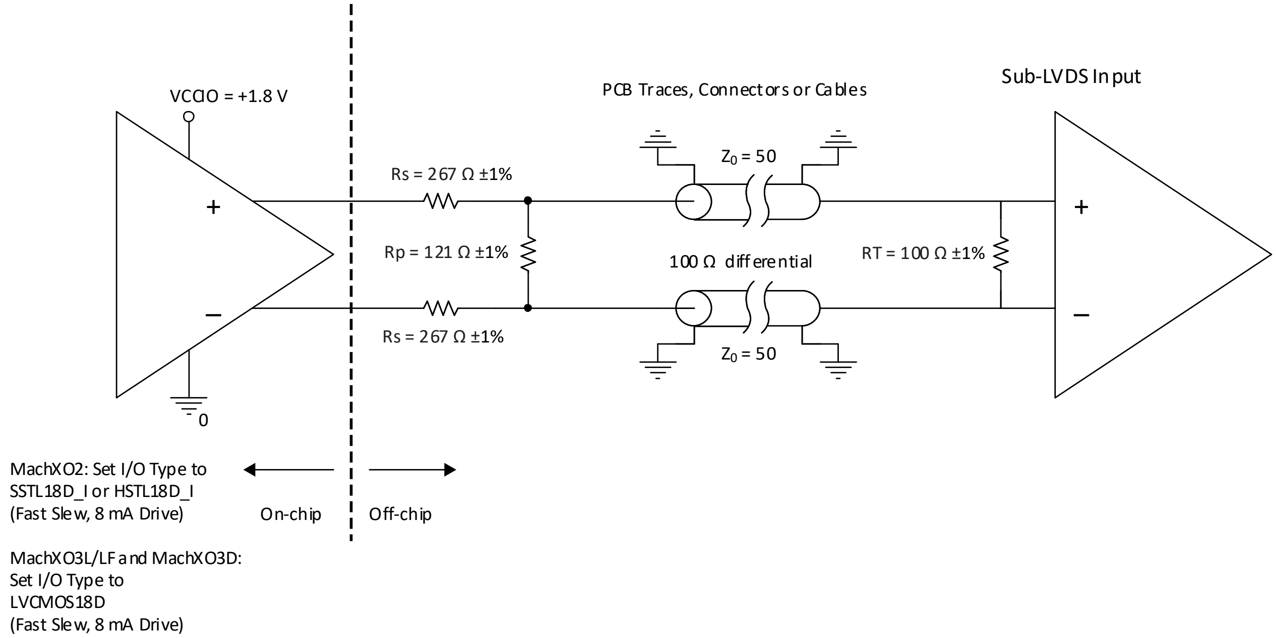


Figure 2.6. Lattice Device Generating a Sub-LVDS Signal Level – MachXO2, MachXO3L/LF, and MachXO3D

The resistor network shown in Figure 2.5 and Figure 2.6 can produce Vod = 156 mV at the RT termination. Table 2.2 lists various resistor values that can be used to produce other output voltage levels smaller or larger than 156 mV, while maintaining a 100 Ω differential source termination.

Table 2.2. Sub-LVDS Output Voltages for Rs and Rp 1% Resistor Values

Vod (mV)	Rs (Ω)	Rp (Ω)
104	412	113
136	309	118
156	267	121
174	237	124
207	196	130

The Vcm value for the network shown in Figure 2.5 and Figure 2.6 is half the VCCIO voltage by default. The Rp and Rs resistors should be placed as close as possible to the Lattice device output pins and should be either 0402 body size or surface mount resistor packs with minimal stub length traces to the resistors.

If you need the lowest common mode output noise, you can get the best performance with the output resistor network shown in Figure 2.7 and Figure 2.8. The main difference being that the original Rp resistor has been split into two resistors of value one-half Rp each with their center connection to a floating, or a 0.9 V VTT, plane island that is itself bypassed to the GND plane. The GND plane should cover the entire extent of the PCB with no major line or area breaks in the plane.

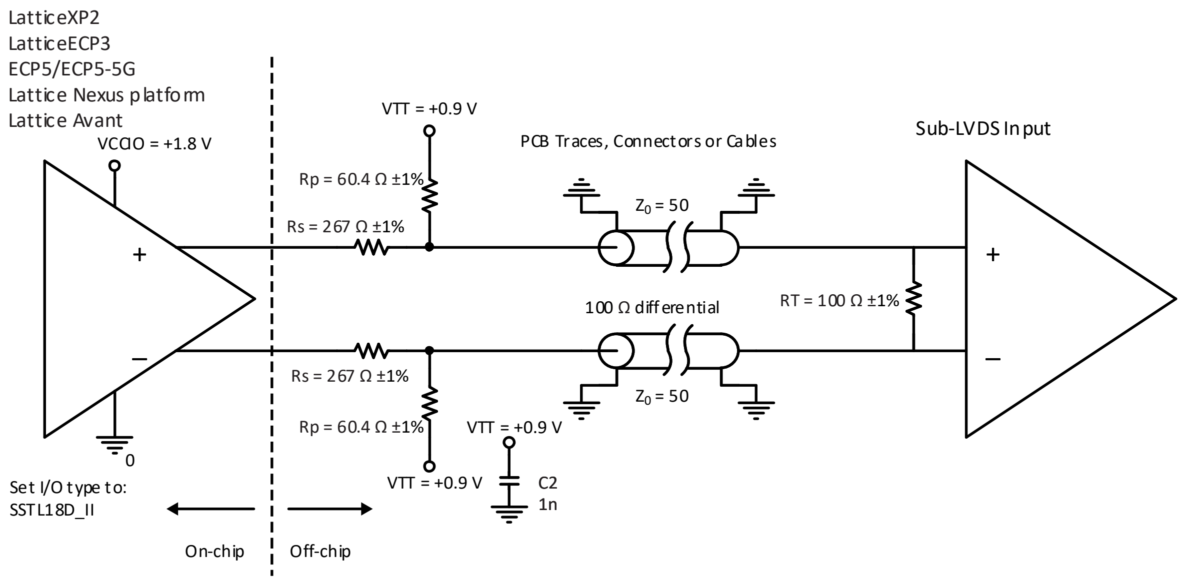


Figure 2.7. Lattice Device Generating a Low Noise Sub-LVDS Signal – LatticeXP2, LatticeECP3, ECP5/ECP5-5G, Lattice Nexus Platform, and Lattice Avant

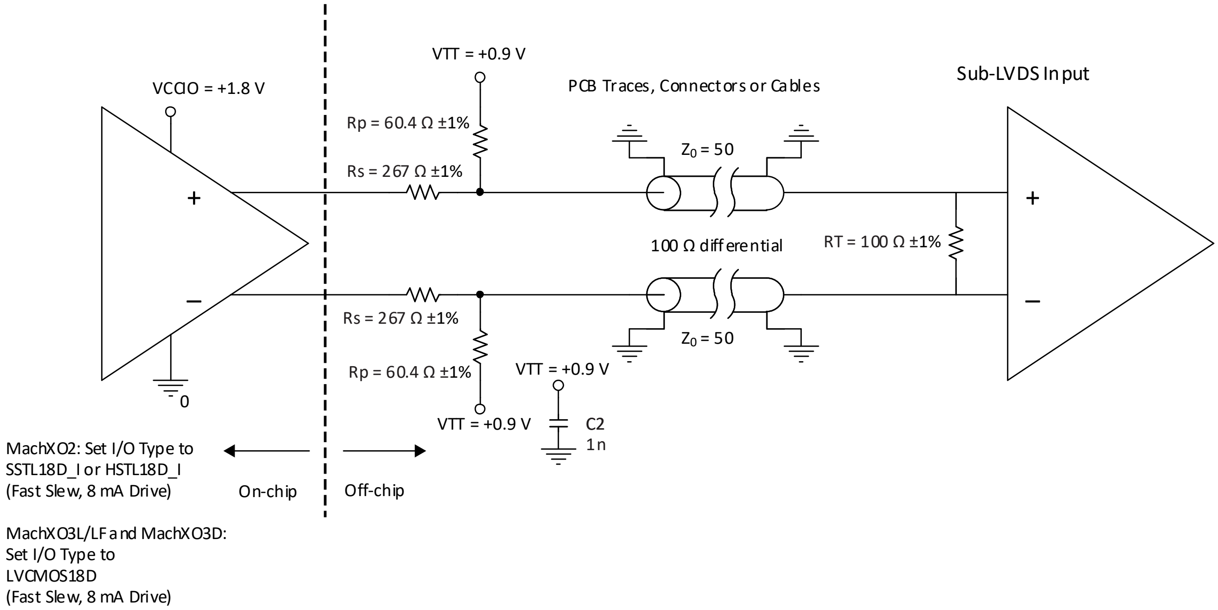


Figure 2.8. Lattice Device Generating a Low Noise Sub-LVDS Signal – MachXO2, MachXO3L/LF, and MachXO3D

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.
For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 2.3, November 2022

Section	Change Summary
Differences between LVDS and Sub-LVDS Signals	Added Avant devices support.

Revision 2.2, October 2022

Section	Change Summary
Introduction	General update.
Differences between LVDS and Sub-LVDS Signals	• Added MachXO5-NX devices support. • General update.

Revision 2.1, June 2022

Section	Change Summary
Differences between LVDS and Sub-LVDS Signals	Added CrossLink-NX-33 support.

Revision 2.0, July 2021

Section	Change Summary
Differences between LVDS and Sub-LVDS Signals	In Table 2.1: Merged the table header for the first two columns to *Sub-LVDS Output Characteristic*. Added the LVDS Input Spec column.

Revision 1.9, June 2021

Section	Change Summary
All	Changed Certus-NX/CrossLink-NX to Lattice Nexus platform.
Differences between LVDS and Sub-LVDS Signals	• Added MachXO3D support to the description, Figure 2.1, Figure 2.6, Figure 2.8, and Table 2.1. • Revised statement to The MachXO2, MachXO3L/LF, and MachXO3D devices support on-chip 100 Ω (nominal) input differential termination on the bottom edge.

Revision 1.8, June 2020

Section	Change Summary
All	Added support for Certus-NX device family.
Differences between LVDS and Sub-LVDS Signals	• Updated the screenshot of waveform for Figure 2.2 removing ECP5/ECP5-5G, LatticeECP3 and LatticeXP2 from the figure caption. • Changed the figure caption of Figure 2.3 adding < 70 mV. • Changed the figure caption of Figure 2.4 adding > 200 mV.

Revision 1.7, December 2019

Section	Change Summary
All	• Changed document number from TN1210 to FPGA-TN-02028. • Added support off CrossLink-NX device family. • Updated document template. • Updated document links.
Technical Support Assistance	Updated this section.

Revision 1.6, October 2015

Section	Change Summary
All	Product name adjustment. Included MachXO3LF device.

Revision 1.5, November 2015

Section	Change Summary
All	Added support for ECP5-5G device family.

Revision 1.4, June 2015

Section	Change Summary
All	Updated Differences Between LVDS and Sub-LVDS Signals section.
Differences between LVDS and Sub-LVDS Signals	Added MachXO3L/LF in Table 2.1. Sub-LVDS Output Signal Voltages and LVDS Input Specifications.

Revision 1.3, January 2015

Section	Change Summary
All	Added support for MachXO3L device family.

Revision 1.2, March 2014

Section	Change Summary
All	Added support for ECP5 device family.

Revision 1.1, April 2013

Section	Change Summary
All	Added sub-LVDS implementation for MachXO2.

Revision 1.0, July 2010

Section	Change Summary
All	Initial release.