Enhancing Heat Sink Performance

Using Thermoelectric Coolers

With the increase in the power dissipation of components and the parallel reduction of their size, engineers and researchers across the globe have been predicting that the era of air cooling might come to an end. Even though in some applications, with very high power dissipations such as IGBTs, air cooling may not be adequate and liquid cooling is a must; air cooling will continue to be the first choice for most electronic cooling applications for many years to come. Advances in air cooling continue to extend its use and the implementation of thermoelectric coolers (TECs) in heat sink applications is one such effort.

Figure 1 shows a heat sink assembly with a TEC. In this figure, the TEC is placed between the CPU and the heat sink. The goal is to reduce the junction temperature of the CPU by adding the TEC module to the CPU heat sink assembly.

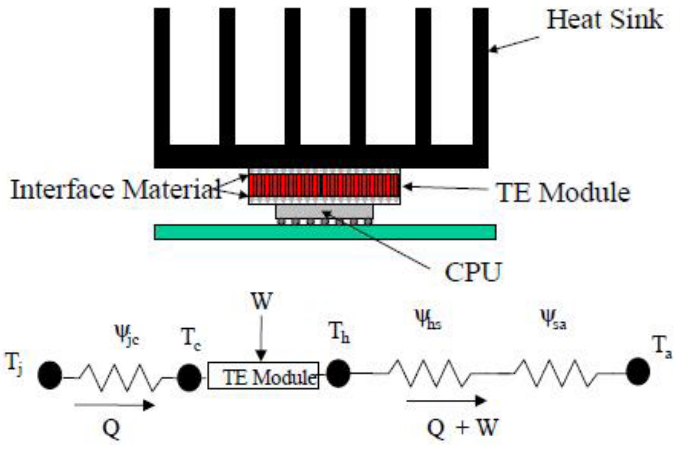

Figure 1. Thermal Resistance Network for a Heat Sink TEC assembly [1]

In general, the heat load of a TEC can be expressed as:

$$Q_c = 2N\alpha IT_c - 1/2I^2R_{TE} - \Delta T/\psi_{TE} \quad (1)$$

Where,

N = number of couples in the TEC
α = seebeck coefficient (V/K)
T_C = Cold temperature of the TEC (°C)
I = current input to the TEC (Amp)
R_{TE} = electrical resistance of the TEC (Ohm)
ΔT = temperature difference across TEC (°C)
ψ_{TE} = thermal resistance of the TEC (°C/W)

The first term is the heat pumped by the motion of electrons, the second term is the joule heating due to electrical input to the TEC and the third term is the conduction heat transfer.

The input work into the TE module is the product of voltage and current and the electron heat pumping.

$$W = I^2R_{TE} + 2NI\alpha\Delta T \quad (2)$$

The hot side temperature of the TEC can be calculated as:

$$T_h = T_a + (Q + W)\,\psi_{sa} = T_c + \Delta T \quad (3)$$

Where,

Q = heat load (W)
Ta = ambient temperature (°C)
Ψ_{sa} = Thermal resistance of the heat sink plus TIM resistance

The junction temperature can easily be calculated as:

$$T_j = T_a + (Q + W)\,\psi_{ha} - \Delta T + Q\,\psi_{jc} \quad (4)$$

Where,

Ψ_{ha} = Thermal resistance of heat sink plus TIM (°C/W)
Ψ_{jc} = Thermal resistance of TIM between heat source and TEC plus junction to case thermal resistance (°C/W)

There are two approaches in implementing a TEC. One approach is to maximize the heat load Q_c and the second approach is to minimize the junction temperature. In electronics cooling applications, the goal is mostly to minimize the junction temperature. The only independent variable in a TEC is the current. To minimize the junction temperature, its derivative with respect to current must be zero:

$$\frac{dT_j}{dI} = 0 \quad (5)$$

Given a TEC with specific geometry and a given heat load Q_c, equation 1, 3 and 5 can be solved simultaneously to find the values of T_c, ΔT and I.

Solbereken et al [1] used a Commercial TE module with its characteristics shown in table 1:

Where,

ρ = electrical resistivity (Ohm-m)
γ = TE element geometry (m)

Element Materials	Bi_2Te_3
γ	1.196 cm
N	31
Module Size	5.5 cm x 5.5 cm
α	2×10^{-4} V/K
ρ	1×10^{-5} Ω-m
k	1.5 W/mK

Table 1. Characteristic of a TEC Module [1]

Figure 2 shows the junction temperature as a function of CPU heat dissipation. This figure shows that for CPU powers less than 75 W, the junction temperature is less than the junction temperature achieved by the heat sink only (solid line). In this figure, I_min is referred to as the current that minimizes the junction temperature. The I_max refers to the current that maximizes the COP, which we will not discuss in this article. It is also shown that, by assuming constant properties of the TEC, the error in the junction temperature calculation is minimal up to the 75 W power dissipation, compared to a TEC with a temperature dependent properties.

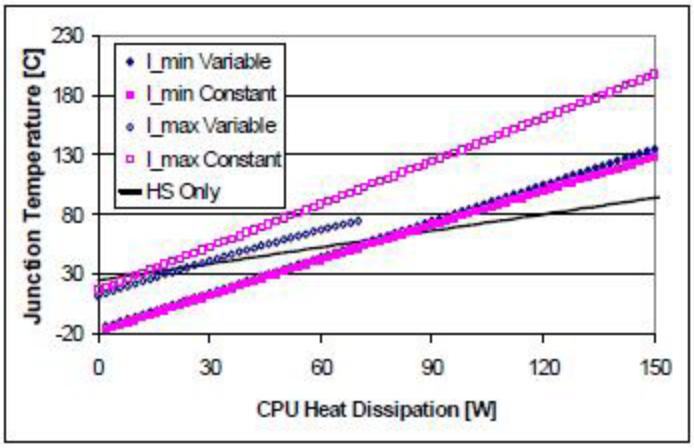

Figure 2. Minimum Junction Temperature as a Function of Heat Load [1]

The authors[1] simulated the above TEC on a die with dimensions of 1.5x1.5 cm, with heat dissipation of 50 W. The interface material resistance was assumed at 0.2 °C/W. The heat sink and the associated TIM resistance were assumed at 0.3 °C/W.

Figure 3 shows the junction temperature as a function of TEC current. The graph shows a parabolic shape with temperature first decreasing up to about 40 Amps and then increasing. This clearly shows that there is an optimum point for the current to minimize the junction temperature.

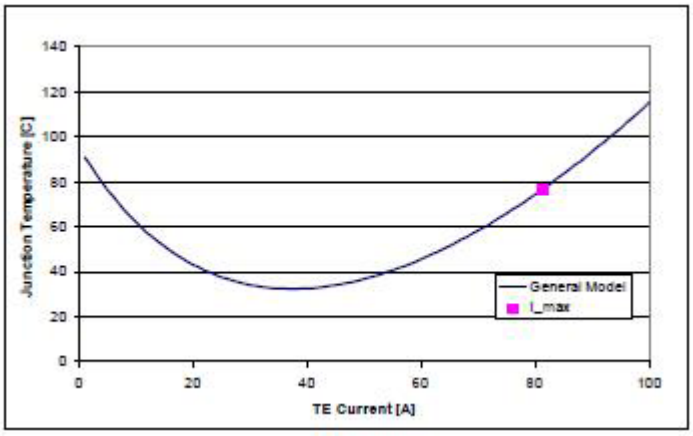

Figure 3. Junction Temperature as a Function of TEC Current [1]

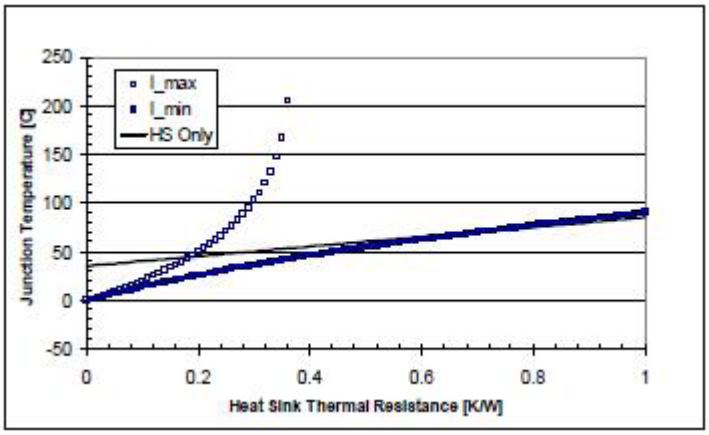

Figure 4. Junction Temperature as a Function of Heat Sink Thermal Resistance [1]

Figure 4 shows the junction temperature as a function of the heat sink thermal resistance. The graph indicates that, for heat sink thermal resistances below 0.6 °C/W, the junction temperature of the TEC assembly is less than the case of heat sink only for a 50 W device. The junction temperatures reported in this graph are for optimized current.

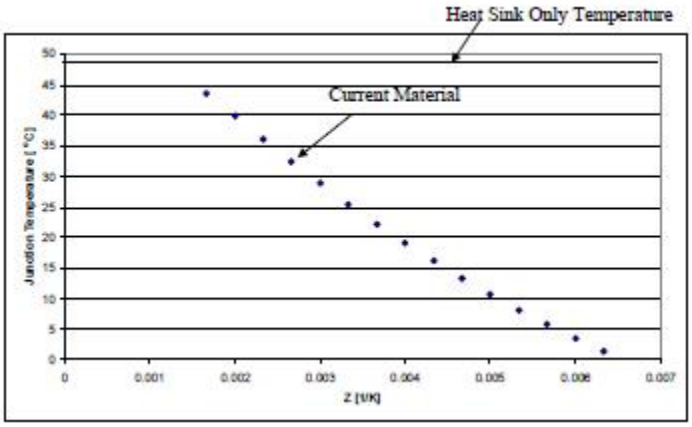

Figure 5. Junction Temperature as a Function of TEC Figure of Merit Z [2]

Solbrekken et al. [2] extended their simulation of the effect of the figure of merit Z ($Z=\alpha/\rho\kappa$). Figure 5 shows that junction temperature can be drastically reduced for higher values of Z. One way to increase the value of Z would be to reduce the thermal conductivity of the P/N junctions. Material science researchers are actively in pursuit of such materials.

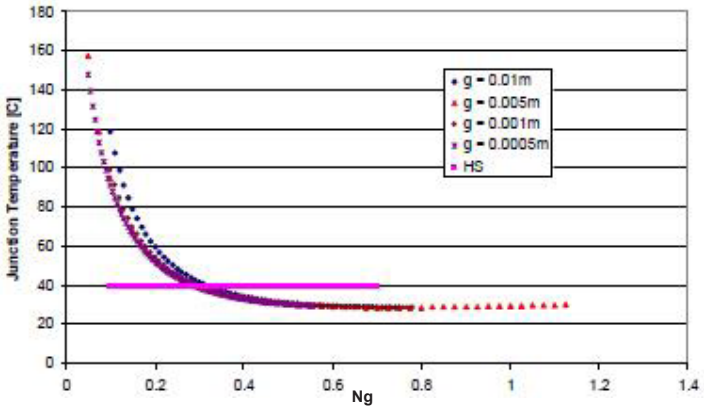

Figure 6. Junction Temperature As a Function Of TEC Geometry for 50W Load [2]

Solbreken et al. [2] also did a simulation on the effect of TEC geometry on the junction temperature. Figure 6 shows junction temperature as a function of Ng, where N is the number of couples and g is the aspect ratio of the TEC:

Where,

g = A_e/L, A_e is the area of the element and L is the thickness of the element (m)

The graph shows that a single parameter, Ng, can represent the geometry of a TEC to optimize the junction temperature. It can be seen that for values of g larger than 0.3, the junction temperature is always lower than the base line with just the heat sink.

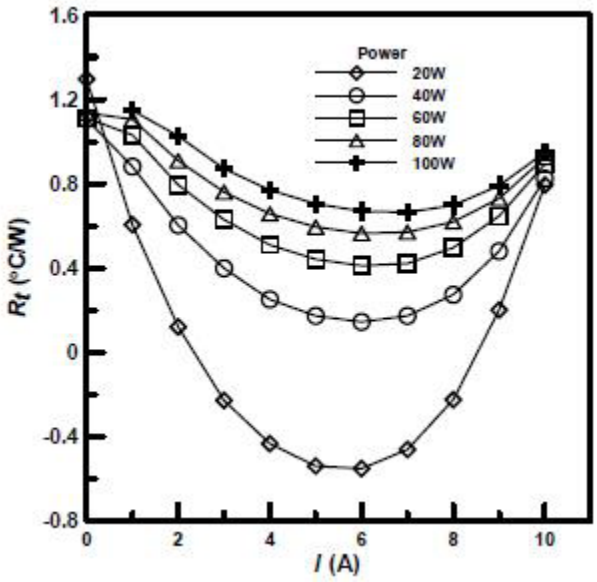

Figure 7. Total Thermal Resistance as a Function of Current for Different Heat Loads [2]

Yu-Wei Chang et al. [3] performed an experiment with a heat sink TEC assembly and reported the total thermal resistance from junction to ambient as a function of applied current to the TEC. Figure 7 shows that the overall thermal resistance is lower than just the heat sink assembly up to 57 W. The thermal resistance of the heat sink in this experiment was 0.385 °C/W. After 57 W, the heat sink only design performed better than the TEC assembly.

The work done so far clearly shows that application of a TEC in air cooling can improve the overall thermal resistance from junction to ambient. Its application requires careful selection and implementation; otherwise, it will have negative consequences. The parameters of importance to consider in the design are the heat sink thermal resistance and the temperature difference across the TEC for a given heat load. Advances in material science to improve the figure of merit value (Z), will enhance the application of a TEC in electronics cooling applications. However, until such time, the heat sink/TEC assembly needs to be carefully designed. It should be apparent to the reader that the addition of power dissipation, because of the deployment of a TEC, must be addressed and considered at the device and system level.

References:

1. **Solbreken, G., Yazawa, K., Bar-Cohen, A., "Chip level refrigeration of portable electronic equipment using thermoelectric devices", Proceedings of InterPack, 2003**

2. **Taylor, R., Solbrekken, G., "An improved optimization approach for thermoelectric refrigeration applied to portable electronic equipment", Proceedings of InterPack, 2005**

3. **Chang, Y., Cheng, C., Wu, W., Chen, S., "An experimental investigation of thermoelectric air-cooling module", International Journal of Engineering and Applied Sciences, 2008**