
Abstract

Space applications are inherently mission-critical and often real-time in nature. Traditional methods for connecting compute with I/O in space, suffer from significant drawbacks both economically and technically. Ethernet, complemented by Time-Sensitive Networking (TSN) addresses these drawbacks while enabling the higher speed connectivity next-generation space systems demand. This white paper explores the requirements for networking in space, discusses how the TSN Ethernet addresses the requirements, and concludes with how Microchip's PIC64-HPSC's unique combination of high-performance 64-bit computing and TSN Ethernet unleashes a new era of innovation to power the global space economy.

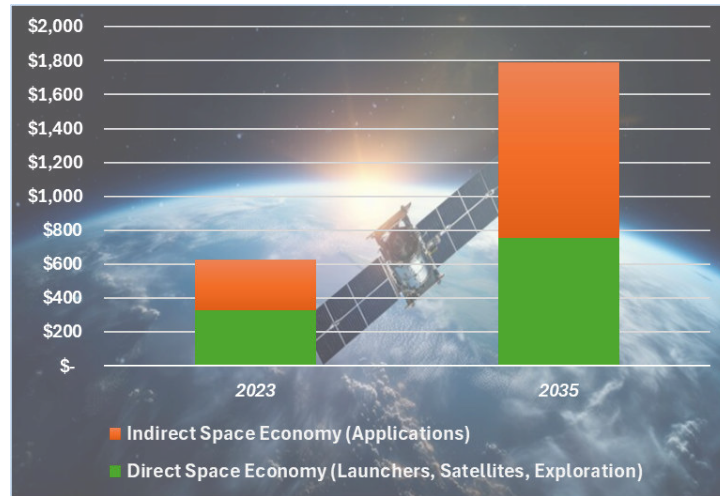
Table of Contents

Abstract.....	1
1. Introduction.....	3
2. Space Applications.....	4
3. Space Application Requirements.....	6
3.1. Networking.....	6
3.2. Fault-Tolerance.....	7
3.3. Determinism.....	7
3.4. Synchronization.....	8
4. Ethernet and TSN for Space Applications.....	9
4.1. Introduction to IEEE P802.1DP: TSN Aerospace Profile.....	9
5. PIC64-HPSC Delivers TSN for Space.....	11
5.1. TSN Feature Set.....	11
5.2. PIC64-HPSC Software Features for TSN.....	13
5.3. PIC64-HPSC Application Enablement.....	13
6. Conclusion.....	15
7. Appendix: TSN Technical Details.....	16
7.1. TSN Standards.....	16
7.2. Credit-Based Shaper Algorithm (CBSA).....	16
7.3. Time-Aware Shaper (TAS).....	17
7.4. Per-Stream Filtering and Policing (PSFP).....	17
7.5. Frame Replication and Elimination for Reliability (FRER).....	18
7.6. Fault-Tolerant Time Synchronization and Time Integrity (gPTP and FTTM).....	19
7.7. Cyclic Queuing and Forwarding (CQF).....	21
7.8. Frame Preemption.....	23
8. References.....	24
9. Revision History.....	25
Microchip Information.....	26
The Microchip Website.....	26
Product Change Notification Service.....	26
Customer Support.....	26
Microchip Devices Code Protection Feature.....	26
Legal Notice.....	26
Trademarks.....	27
Quality Management System.....	28
Worldwide Sales and Service.....	29

1. Introduction

Driven by a wide range of new applications and opportunities, the global space economy is entering a period of tremendous growth. The World Economic Forum forecasts direct investment in launchers, satellites, and space exploration will grow from \$330B in 2023 to \$755B in 2035.

Figure 1-1. Investment in Launchers, Satellites, and Space Exploration (\$Billions)



Source: Space: The \$1.8 Trillion Opportunity for Global Economic Growth, World Economic Forum

Whether it be satellites, launchers, landers, or rovers, there is an ever-present need within space applications for both more compute and more bandwidth. Subsequently, the networks used to connect the compute with the I/O (sensors, actuators, instruments, camera, and motors) must also scale. However, not all networks are created equal. Typical networking and connectivity methods used in space applications such as SpaceWire and SpaceFibre struggle to keep up with the need to move increasing volumes of data, faster, more reliably, and with determinism. Further, since these methods are only used in space applications, they are often exceptionally costly. Relying on older, slower, and proprietary technologies is a factor that could slow the growth rate of space applications.

The solution to these challenges is Ethernet complemented by Time-Sensitive Networking (TSN). Ethernet has dominated our networks since its inception and as a result enjoys unmatched economies of scale. Similarly, for the same reasons that TSN is growing in importance in the Industrial, Automotive, and Communications markets, TSN will be a key technology in aerospace applications such as Low-earth Orbit (LEO) satellites, launch systems, landers, and rovers. TSN and Ethernet provide the reliability and determinism that mission critical applications require, while providing the necessary bandwidth required in space applications. Furthermore, Ethernet is a true-unifying layer allowing the simultaneous support of real-time and non-real time traffic flows. Lastly, the ubiquitous nature of Ethernet coupled with robust ecosystem ensures that Ethernet is the most cost-effective networking solution on Earth or in space.

This white paper discusses the following:

- The architecture of a representative space application—the satellite
- The requirements for a networking solution in space
- Why the TSN and Ethernet are ideal for space applications
- How Microchip's PIC64-HPSC provides TSN with Ethernet to catalyze and enable the future of spaceflights

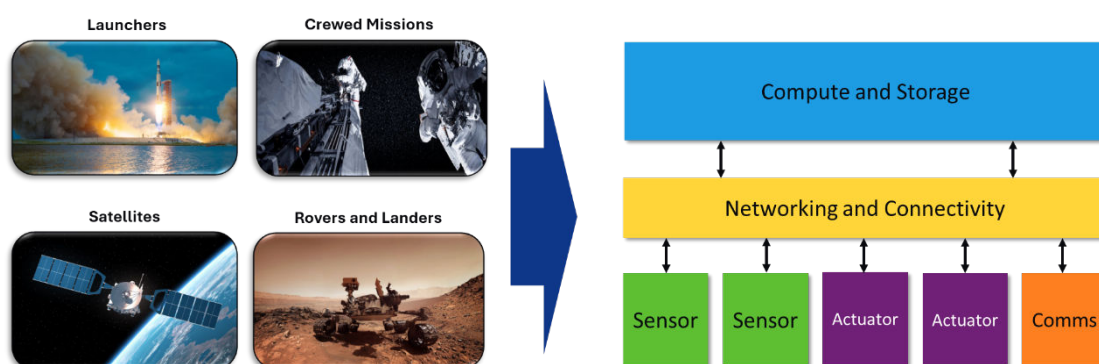
2. Space Applications

Figure 2-1 shows that much like Earth-based applications, space applications and systems are built out of three basic layers or components:

- Compute and Storage
- Sensors and Actuators
- Networking and Connectivity

In the simplest case, the compute layer takes sensor data as input and outputs control information to actuators. Meanwhile, the compute layer interfaces with the outside world through the communication links for command-and-control information. All these system elements are interconnected through the networking and connectivity layer.

Figure 2-1. Basic Building Blocks of Space Applications

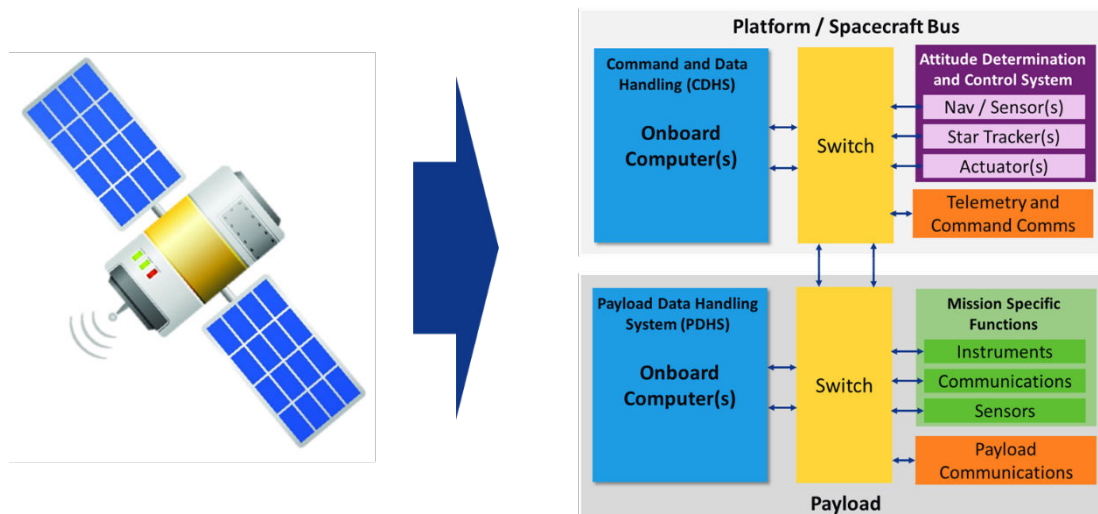


Let's take a satellite for example.

Figure 2-2 shows that a typical satellite is composed of a Platform or Spacecraft Bus as well as a Payload section. The Platform section is responsible for the flight and navigation of the satellite itself. Onboard computers in the Command and Data Handling System (CDHS) perform mission-critical and real-time processing on sensor and navigational data received from the Attitude Determination and Control System (ADCS). Meanwhile, Telemetry and Command information is sent to and received from ground stations through the Telemetry and Command Communications system. The mission-critical, real-time nature of the Platform section requires an interconnect that is Fault-tolerant, resilient, deterministic, and synchronized.

Meanwhile, the Payload section is responsible for conducting the specific mission of the satellite itself. Example missions include Earth Observation, Science, Broadband Communications, and Positioning Navigation and Timing (for example, GPS). As the Platform section, the Payload section features a set of onboard computers in the Payload Data Handling System (PDHS) which interfaces with mission specific functions such as instruments, communications, and sensors. Earth-based ground stations communicate with the Payload section through the Payload Communications system. Generally, the payload section handles significantly higher data bandwidths than the platform section, in some cases up to 10 Gbps or more. Requirements such as Fault-tolerance, resiliency, and determinism are generally mission-specific.

Figure 2-2. Example Architecture for a Satellite



The following table summarizes the key technical characteristics of the Platform and Payload sections of a satellite.

Table 2-1. Platform and Payload Technical Characteristics

	Platform	Payload
Mission Critical	Mandatory	Mission-Specific
Real-Time	Mandatory	Mission-Specific
Bandwidth	Mbps	Gbps or 10s of Gbps
Fault-Tolerance/Resiliency	Mandatory	Mission-Specific
Determinism	Mandatory	Mission-Specific
Synchronization	Mandatory	Mission-Specific

These differences traditionally have led to different technology choices in the Platform and Payload sections. MIL-STD-1553 is a common Platform level interconnect, while SpaceWire has traditionally been used in the Payload section.

The next section of this white paper takes a closer look at the requirements of a typical space application.

3. Space Application Requirements

In general, space applications, whether they are launchers, satellites, landers, rovers, or crewed systems are considered as mission-critical and requires real-time processing. Figure 3-1 shows mission-critical and real-time systems are built on four fundamental characteristics:

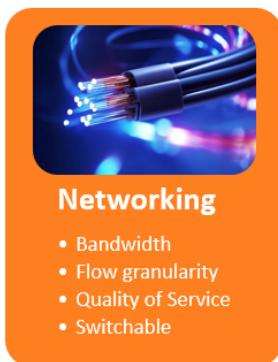
- Networking, efficient, scalable, and quality-of-service aware
- Fault-tolerance, inclusive of all components in the system
- Determinism, enabling events to happen at predictable times
- Synchronization, enabling all components to have a common view of time

Figure 3-1. Mission-Critical and Real-Time Characteristics



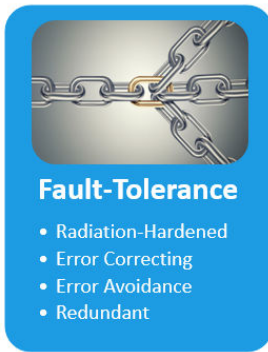
Let's explore each of these characteristics.

3.1 Networking



Mission-critical and real-time systems such as space applications can have a wide variation in their data transfer capacity requirements, ranging from very low (for example, 10 Mbps) to very large (> 10 Gbps). Networking protocols need to be defined for these extremes, for rates between these extremes, and for even higher capacities in the future. In addition, individual data transfer flows within an aggregated link must also have high probability guarantees for the quality of service. For instance, some flows within a system are critical, while the others are less. It is imperative to ensure priority is given to the most critical flows. Likewise, the network must be switchable to enable flexibility and scalability.

3.2 Fault-Tolerance

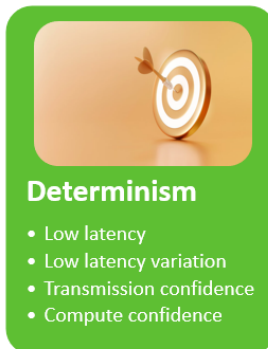


All mission-critical systems need to be Fault-tolerant and resilient. Space adds the additional complexity of a harsh radiation environment, which increases Fault rates. By performing radiation-hardening strategies, the Fault rate of a device can be reduced significantly, making it more resistant to damage or malfunction due to high levels of ionizing radiation (particle radiation and high-energy electromagnetic radiation). Hardening can be implemented in many ways, including the use of Error Correction Codes (ECC) to fix Faults, the use of redundant instances of logic or of functions to detect a Fault or to enable majority voting to overcome a Fault, and the use of radiation-hardened standard cells to reduce the probability that a logic instance can become faulty.

Beyond hardening against radiation effects, a Fault-tolerant and resilient space application must also endeavor to ensure that the data transfers reach their intended target. The probability of success can be improved significantly by sending redundant copies over diverse transmission paths.

Lastly, a resilient system must also endeavor to ensure that unintended data transmissions are not sent or received, and when they are, the consequences are contained. Thus, a mechanism to filter and police must be in place to improve Fault-isolation.

3.3 Determinism



Determinism refers to the confidence that a data transmission will be sent and received within an expected time slot.

Key characteristics of a deterministic system are its latency and latency variation. In a mission-critical application, the late arrival of a time-critical packet could have devastating effects on the mission.

Traditionally, latency performance has been achieved using network protocols and topologies developed specifically for the given application.

Beyond the network, the compute layer must also provide determinism. Determinism at the compute layer can be achieved using real-time or time and space partitioning operating systems, tightly coupled memory structures, and high-precision timers.

3.4 Synchronization



Finally, all nodes within a mission-critical and real-time system must have a common and accurate view of both time and phase.

For critical time sensitive functions, this synchronized time must be continuously available and trustworthy. These features have not been generally available or possible with Ethernet until recently, with newly defined TSN functions.

While it is expected that most modern use cases will require synchronization, there might still be some that do not (for example, segregated sub-networks supporting legacy non-mission-critical and non-real-time applications). For these use cases, *IEEE® P802.1DP* provides an asynchronous option, in which all the benefits of TSN except those associated with synchronization are still available.

4. Ethernet and TSN for Space Applications

As noted previously, space applications have traditionally relied on legacy protocols such as MIL-STD-1553 or SpaceWire for interconnect. However, these legacy protocols suffer from various challenges, not the least of which includes limited bandwidth and high cost. For the space economy and the innovation unlocked by it to truly flourish, a new solution is required.

That solution is Ethernet. Ethernet offers the bandwidth, flow granularity, quality-of-service, and prioritization that space applications demand. Furthermore, the widespread nature of the Ethernet ecosystem provides the opportunity to lower the cost of space applications.

To address mission-critical and real-time applications, Ethernet is complemented by Time-Sensitive Networking (TSN). TSN is a set of standards developed by the Time-Sensitive Networking Task Group (TG) of the IEEE 802.1 Working Group (WG). TSN provides Fault-tolerance, resiliency, determinism, and synchronization for Ethernet based networks.

The TSN TG is developing a set of profiles to assist the aerospace, industrial, communications, and automotive industries to adopt TSN in their applications, see the following figure. The IEEE P802.1DP project covers aerospace, including space applications. Microchip has been a leading contributor to this industry effort.

Figure 4-1. TSN Profiles by End-Market Application



Let's explore IEEE P802.1DP in further detail and see why it enables mission-critical applications in space.

4.1 Introduction to IEEE P802.1DP: TSN Aerospace Profile

IEEE P802.1DP, TSN for Aerospace Onboard Ethernet Communications, is a profile intended for use in aerospace applications spanning military and commercial aviation as well as space. The profile provides a selection of the TSN functions needed to deliver Fault-tolerance, determinism, and synchronization to an Ethernet-based network. The following table summarizes the TSN functions included in IEEE P802.1DP and the key capabilities they bring to service mission-critical and real-time aerospace applications.

Table 4-1. Key Functions of the IEEE P802.1DP TSN Profile for Aerospace

Function Group	Specification Name	Features to Enable Mission Critical Applications
Fault-Tolerance and Resiliency	IEEE [®] 802.1CB, 802.1CBdb Frame Replication and Elimination for Reliability (FRER)	<ul style="list-style-type: none"> Protects against loss of a packet Protects against loss of a link Protects against equipment failure
	IEEE 802.1Qci Per-Stream Filtering and Policing (PSFP)	<ul style="list-style-type: none"> Detects and drop packets that exceed the configured maximum size configured for the stream Detects and drop packets that arrive outside of the associated transmission window for the stream Detects and drop packets from a stream that has exceeded its allocated bandwidth Optionally drops the entire stream when any of its packets violate a PSFP rule
Determinism	IEEE 802.1Qbv Time-Aware Shaper (TAS)	Transmits packets of a given stream at deterministic times, enabling reduced latency and latency variation
	IEEE 802.1Qav Credit Based Shaper Algorithm (CBSA)	Creates a smoothly paced stream with a fixed upper bandwidth limit
Synchronization	802.1AS Generalized Precision Timing Protocol (gPTP)	Synchronizes each node within a network
	IEEE P802.1ASed	Fault-Tolerant Timing Module (FTTM) enables constant availability of time and time integrity
Management	802.1Qcc Time-Sensitive Networking Configuration	Describes fully-centralized network configuration and user configuration models

Aside from the functions listed in the preceding table, TSN also includes other functions that may prove valuable in space applications:

- Cyclic Queuing and Forwarding (CQF), as defined in *subclause 5.13.1.2 of IEEE 802.1Q-2022 and IEEE 802.1Qch-2017*
- Frame Preemption, as defined in *subclause 6.7 of IEEE 802.1Q-2022 and IEEE 802.1Qbu-2016*, and the associated MAC Merge sublayer, as defined in *clause 99 of IEEE 802.3-2022 and IEEE 802.3br-2016*

The appendix of this white paper includes a detailed description of each of these TSN functions.

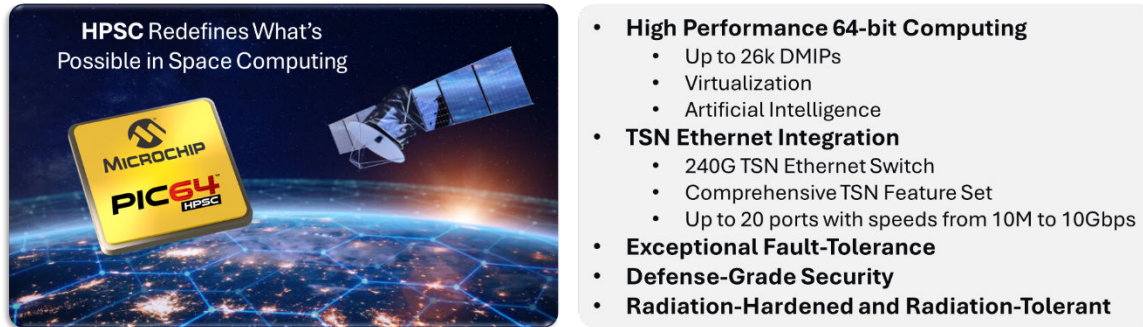
Now, let's explore how Microchip's PIC64-HPSC delivers high-performance compute along with integrated TSN for mission-critical applications.

5. PIC64-HPSC Delivers TSN for Space

Microchip's PIC64-HPSC represents a revolutionary breakthrough in the capabilities available in a 64-bit microprocessor – on Earth let alone for space applications. The device blends the best features of Commercial Off The Shelf (COTS) processors such as high-performance computing, virtualization, and AI, with the Fault-tolerance and radiation hardening required to survive in the demanding environment of space. Crucially, the PIC64-HPSC also features an extensive array of Ethernet features complemented by TSN to enable mission-critical and real-time applications.

The following figure shows the key features of the PIC64-HPSC.

Figure 5-1. Key Features of the PIC64-HPSC



Traditionally, compute and switching are implemented in separate, discrete devices. In space applications, this can add significant cost and power. By integrating these features in the same device, Microchip's PIC64-HPSC not only helps reducing the cost and power consumption of space systems but also unlocks the important technical advantages for mission-critical and real-time applications.

PIC64-HPSC provides the ability to synchronize or align compute timers (Elapsed Timers (ET) and high-precision timers) with PTP timers, allowing the Operating System (OS) and associated workloads running to be synchronized to the network time (for instance, in the case of TAS).

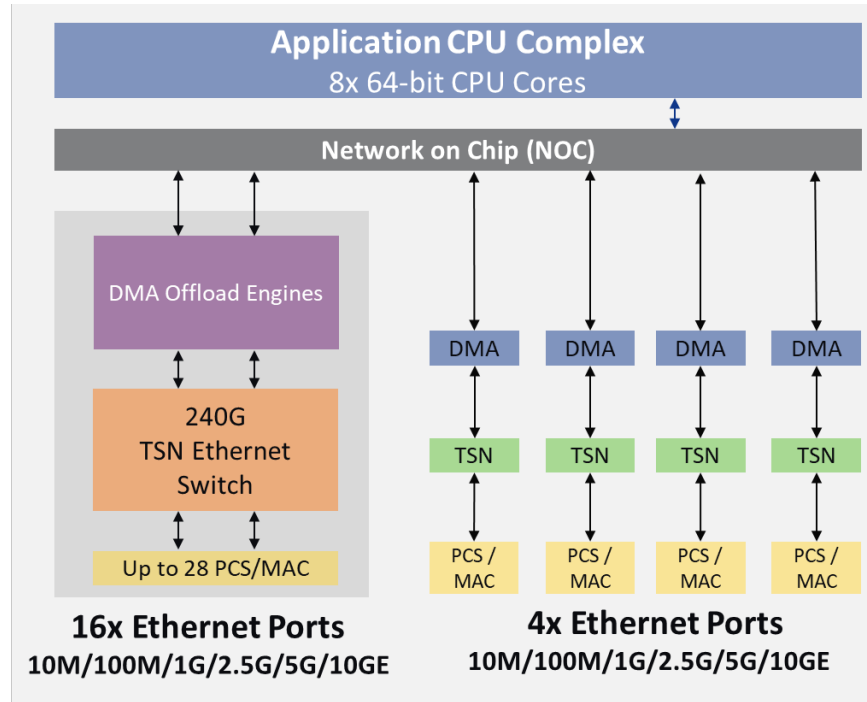
This is important because within a node responsible for real-time or mission-critical workloads, there is often a need to quantify the potential interference channels to bound a given application's real-time performance. Without the coordination of OS and the PTP/ET/TAS views, the node's interference due to inter-node communication is hard to control, especially when involving shared resources like DDR and on-chip interconnect bandwidth. By combining a time partitioned OS with TAS scheduling (and linking external transmission windows to specific I/O partition windows), PIC64-HPSC enables increased determinism and performance bounding of the compute within a given node.

5.1 TSN Feature Set

The following figure shows that PIC64-HPSC integrates two distinct subsystems for supporting TSN:

- A 240G TSN Ethernet Switch
 - The Ethernet switch supports L2 switching as well as static L3 forwarding
 - DMA offload engines enable connectivity between the Application CPUs and the switch
- Four TSN-capable Ethernet Endpoints are provided for connectivity between the Application Complex and external ports while bypassing the TSN switch entirely

Figure 5-2. PIC64-HPSC Block Diagram Highlighting TSN Features



PIC64-HPSC provides one of, if not, the most complete sets of TSN functions available. Based on Microchip's field-proven and best-in-class VSC75xx and LAN96xx families, the PIC64-HPSC supports the following TSN functions, see the following figure. Importantly, PIC64-HPSC is fully aligned to the IEEE P802.1DP aerospace profile. As noted previously, Microchip is a leading contributor to this industry initiative.

Figure 5-3. TSN Functions Supported by PIC64-HPSC

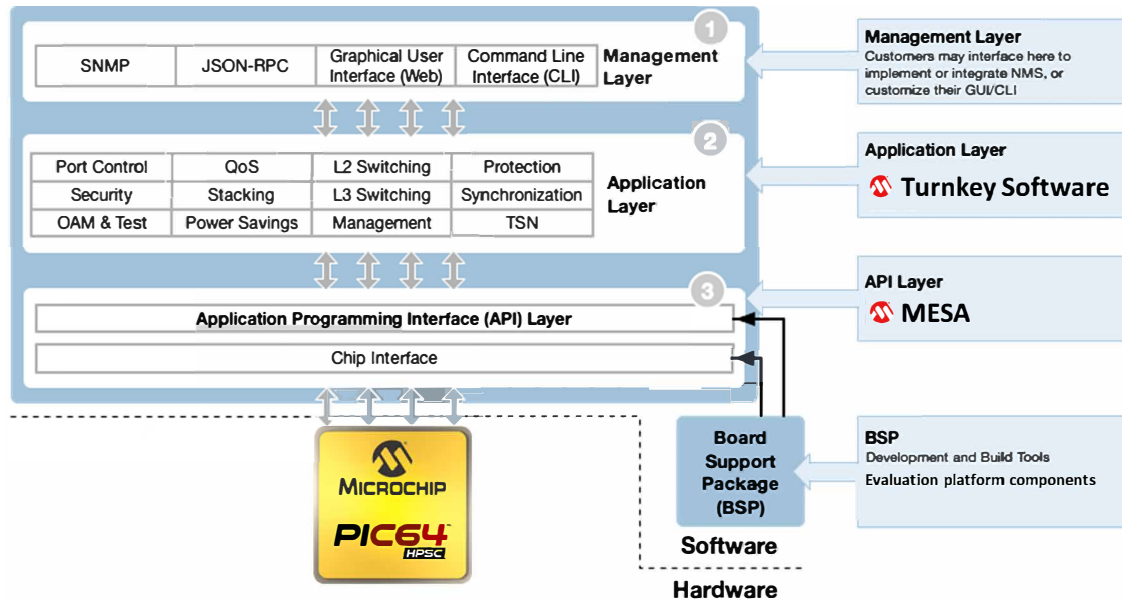
Feature Group	Standard	Standard Name	Aerospace Profile (P802.1DP)	HPSC Switch Ports	HPSC Endpoint Ports
Timing	802.1AS	Timing and Synchronization for Time-Sensitive Applications	Proposed	✓	✓
	IEEE1588	Precision Clock Synchronization Protocol for Networked Measurement and Control Systems		✓	✓
	802.1ASed FTTM	Fault Tolerant Timing with Time Integrity (Fault-Tolerant Timing Module)	Proposed	✓	✓
Forwarding and queuing	802.1Qav	Forwarding and Queuing Enhancements for Time Sensitive Streams (Credit Based Shaper)	Proposed	✓	✓
	802.1Qbv	Enhancements to Traffic Scheduling (Time Aware Shaper)	Proposed	✓	✓
	802.1Qch	Cyclic Queuing and Forwarding		✓	Not applicable
Policing	802.1Qci	Per Stream Filtering and Policing	Proposed	✓	✓
Redundancy	802.1CB	Frame replication and elimination for redundancy	Proposed	✓	✓
Configuration	802.1Qcc	Stream Reservation Protocol (SRP) Enhancements and Performance Improvements	Proposed	✓	✓
Delay Reduction	802.1Qbu	Frame Preemption		✓	✓
	802.3br	Interspersing Express Traffic		✓	✓

5.2 PIC64-HPSC Software Features for TSN

Software is a critical component of any TSN application. The TSN feature set of the PIC64-HPSC is enabled by a complete software package of Drivers/APIs, and Turnkey Application Software. The following figure shows the high-level software architecture from the perspective of the Ethernet switch. Here, system developers may choose to interface with the switch at three different layers:

- Management Layer
- Application Layer
- API Layer

Figure 5-4. Ethernet Switch Software Architecture



At the API layer, PIC64-HPSC leverages Microchip's field proven MESA SDK for switch configuration.

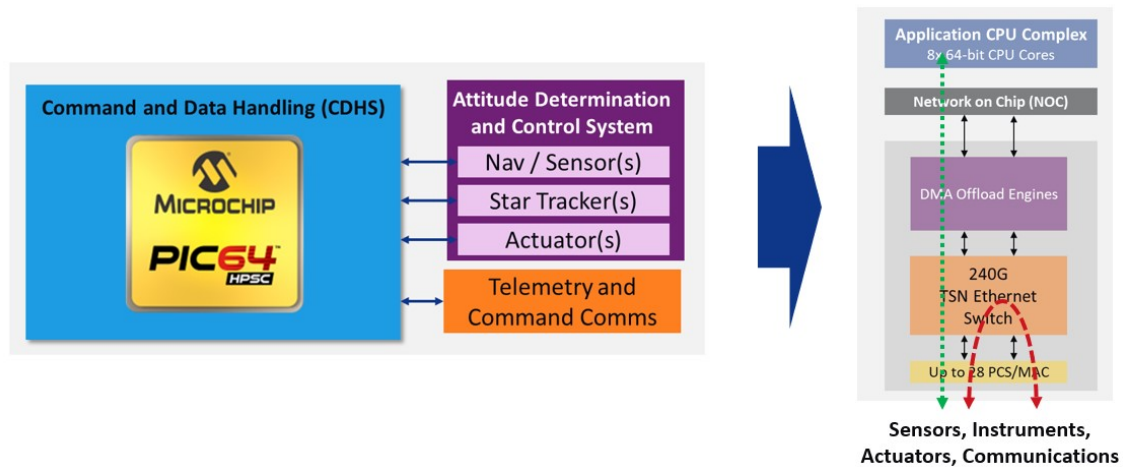
At the Application layer, Microchip provides turnkey application software, with the following benefits:

- Standards-based
- Reduced development time
- Reduced development cost
- Alignment to IEEE P802.1DP TSN profile for aerospace
- Seamless integration with MESA SDK

5.3 PIC64-HPSC Application Enablement

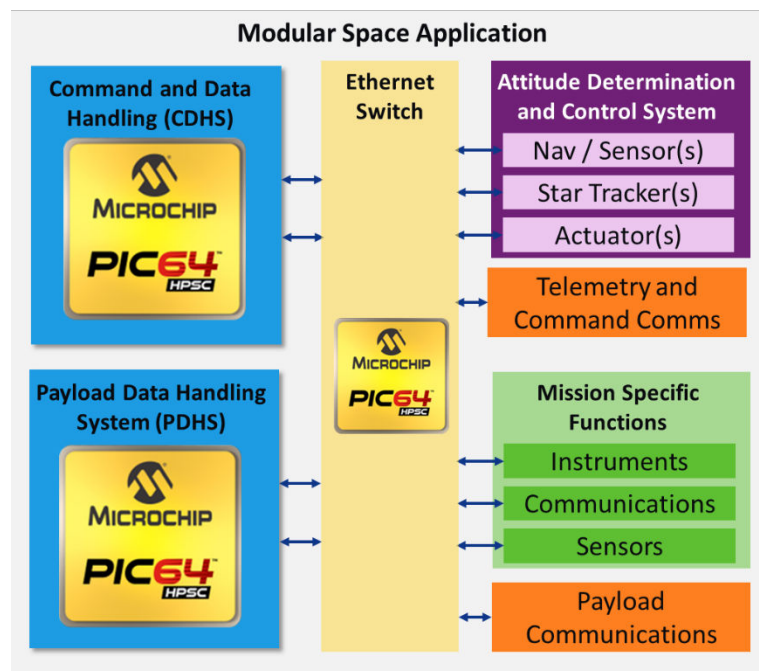
In space, the variables Space, Weight, and Power (SWaP) has critical importance. By integrating TSN switching alongside compute, PIC64-HPSC provides system developers new opportunities to reduce SWaP as well as Cost (SWaP-C) by reducing the number of discrete components. In Figure 5-5, the PIC64-HPSC acts as the main on-board computer and switch for the Platform section of the satellite. As shown in the **red** data path, various platform or payload components can communicate with each other through the switch. The **green** data path demonstrates the case where the Application CPU Complex of the PIC64-HPSC is used to process the data, for instance to make decisions regarding the flight of the spacecraft.

Figure 5-5. PIC64-HPSC Enables Convergence of Compute and Switching



The following figure shows how the PIC64-HPSC may be used on separate compute and switch modules in larger or modular systems.

Figure 5-6. PIC64-HPSC Enables Modular Space Systems



PIC64-HPSC provides space application system designers with architectural and feature flexibility to optimize SWaP-C and to meet their mission goals.

6. Conclusion

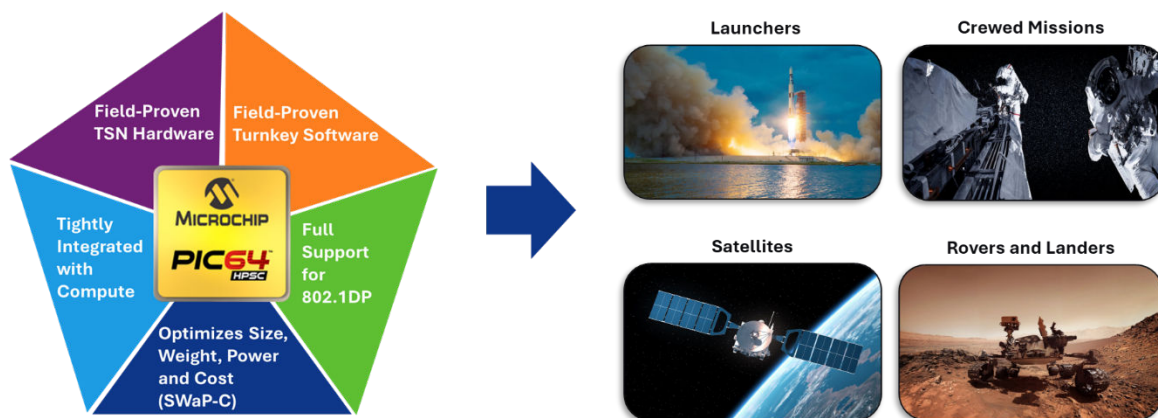
The global space economy is poised for tremendous growth over the next decade. New satellites, new missions to the Moon and beyond, and new applications will drive ever-increasing needs for bandwidth on these mission-critical systems. Ethernet and TSN deliver the best combination of technical features, ecosystem, and economic value to help enable this growth.

Microchip's PIC64-HPSC provides space system developers with high-performance 64-bit computing and TSN Ethernet in a radiation-hardened/radiation-tolerant silicon platform enabled by an ever-growing software ecosystem. With PIC64-HPSC, space system developers can take advantage of the following key value for space applications ranging from launchers to rovers and landers:

- Optimized SWaP-C
- Field-proven TSN hardware
- Field-proven turnkey software
- Full support for IEEE P802.1DP
- TSN Ethernet switching and connectivity tightly coupled with high-performance computing

The following figure shows the PIC-64-HPSC's TSN Ethernet value proposition.

Figure 6-1. PIC-64-HPSC's TSN Ethernet Value Proposition



7. Appendix: TSN Technical Details

This section discusses the TSN technical details.

7.1 TSN Standards

Following are the pointers to the standards that define the TSN functions discussed in this whitepaper:

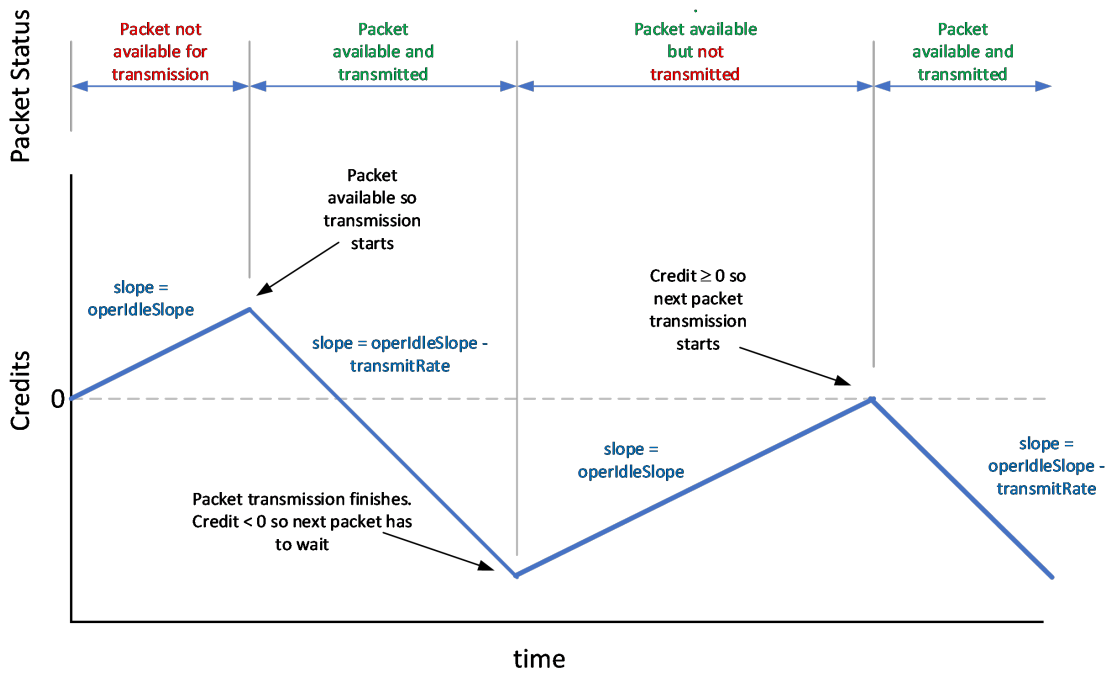
- Credit Based Shaper Algorithm (CBSA) is defined in *subclause 8.6.8.2 of IEEE 802.1Q-2022 and IEEE 802.1Qav-2009*
- Enhancements for Scheduled Traffic (commonly known as the Time-Aware Shaper (TAS)) is defined in *subclause 8.6.8.4 of IEEE 802.1Q-2022 and IEEE 802.1Qbv-2015*
- Per-Stream Filtering and Policing (PSFP) is defined in *subclause 8.6.5.2 of IEEE 802.1Q-2022 and IEEE 802.1Qci-2017*
- Frame Replication and Elimination for Reliability (FRER) is defined in *IEEE 802.1CB-2017 and IEEE 802.1CBdb-2021*
- Timing and Synchronization for Time-Sensitive Applications (commonly known as the generalized Precision Timing Protocol, gPTP) is defined in *IEEE 802.1AS-2020 and draft standards IEEE P802.1ASdm and IEEE P802.1ASed*
- Time-Sensitive Networking (TSN) configuration is defined in *clause 46 of IEEE 802.1Q-2022 and IEEE 802.1Qcc-2018*
- Cyclic Queuing and Forwarding (CQF) is defined in *subclause 5.13.1.2 of IEEE 802.1Q-2022 and IEEE 802.1Qch-2017*
- Frame Preemption is defined in *subclause 6.7 of IEEE 802.1Q-2022 and IEEE 802.1Qbu-2016*, and the associated MAC Merge sublayer is defined in *clause 99 of IEEE 802.3-2022 and IEEE 802.3br-2016*

7.2 Credit-Based Shaper Algorithm (CBSA)

The TSN Credit-Based Shaper Algorithm (CBSA) creates Ethernet streams that have a defined upper bandwidth limit and that are steadily paced. The following figure shows an example of credit-based pacing. Credits are incremented at a configured rate with a positive slope = `operIdleSlope`, when no frame from the stream is being transmitted. Credits are decremented with a negative slope = `(operIdleSlope - transmitRate)`, when the stream is being transmitted, where `transmitRate` is the transmit rate of the Ethernet MAC. The start of transmission of a frame is only performed when the credit value is zero or greater.

Streams that use the CBSA are assigned to traffic classes with higher priority than those that do not use CBSA. When the TSN network is configured accordingly, the combination of these pacing and priority characteristics allows CBSA streams to pass through the TSN network with little congestion, hence achieving deterministic latency with little latency variation for these streams.

Figure 7-1. Pacing Example for TSN Credit-Based Shaper Algorithm



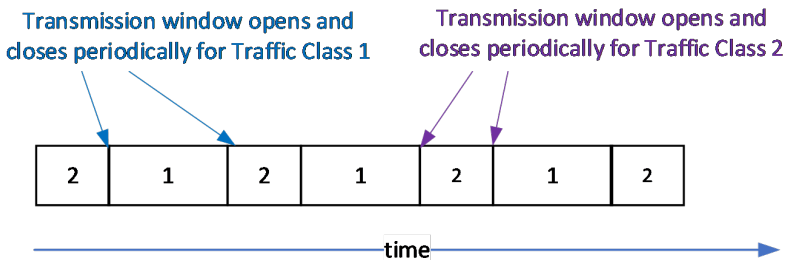
7.3 Time-Aware Shaper (TAS)

The TSN enhancements for scheduled traffic function, also known as the Time-Aware Shaper (TAS), uses transmission gates to create time-division multiplexed windows on the Ethernet link. Example windows for traffic classes 1 and 2 are shown in Figure 7-2. Each TSN stream is assigned to a gate and can only be transmitted while its assigned gate is open. Each TAS gate scheduler must ensure that no transmission starts before the gate is open and that all transmission must end before the gate is closed.

The TAS function isolates the transmission of a TSN stream of one traffic class from the transmission of other TSN streams of other traffic classes. This isolation protects the transmission of a traffic class from the transmissions of a misbehaving traffic class.

The TAS function also gives better determinism of the arrival time of the frames from a TSN stream at its destination.

Figure 7-2. TSN Time-Aware Shaper Transmission Windows



7.4 Per-Stream Filtering and Policing (PSFP)

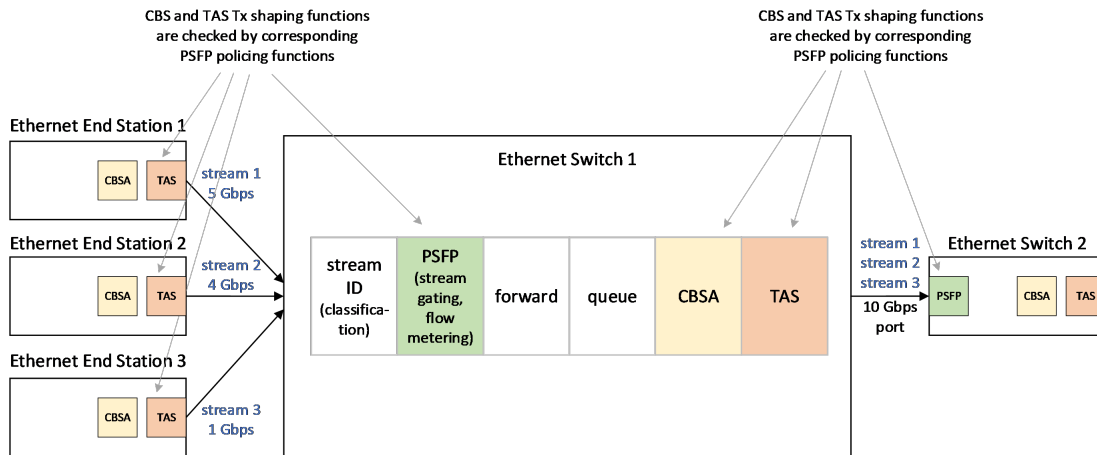
The TSN Per-Stream Filtering and Policing (PSFP) function performs frame-size filtering, flow metering, and stream gate filtering on individual TSN streams. For frame-size filtering, any Ethernet frame from the TSN stream that exceeds its maximum size is dropped. For flow metering, Ethernet

frames from the TSN stream that cause it to exceed its bandwidth limit are dropped. For stream gate filtering, any Ethernet frame from the TSN stream that is not completely contained within its assigned transmission window is dropped. Options are available to permanently, until changed by network management, drop all frames from the TSN stream if any of the TSN stream's frames violates at least one of the PSFP functions.

Fault isolation is enhanced when PSFP is combined with CBSA and/or TAS. Figure 7-3 shows that the PSFP functions located downstream of a transmit port, at its peer receive port, detects misbehavior on the transmit port and prevent this misbehavior from propagating through the network.

For example, if the CBSA function for stream 1 erroneously transmitted at 6 Gbps and was not policed, the 10 Gbps egress port of Ethernet Switch 1 will be overwhelmed with 11 Gbps of traffic. The resulting congestion on this egress port affects streams 2 and 3. However, the PSFP flow metering function in Ethernet Switch 1 polices stream 1 and limits it to 5 Gbps.

Figure 7-3. Enhanced Fault Isolation with CBSA, TAS, and PSFP

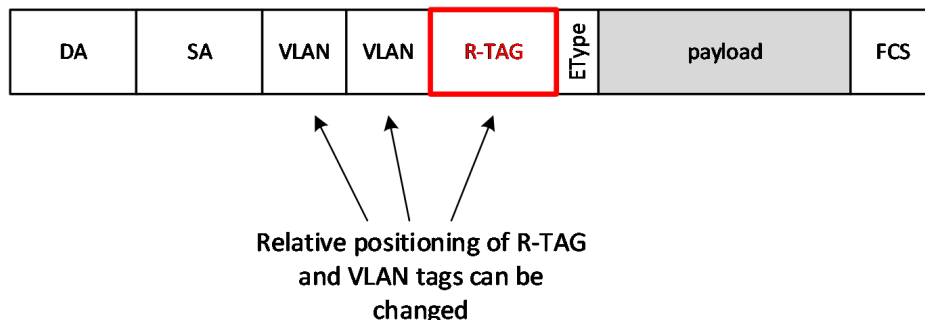


7.5 Frame Replication and Elimination for Reliability (FRER)

The TSN FRER function provides frame redundancy to Ethernet solutions. It performs frame replication on a TSN stream at the talker side and frame elimination at the listener side.

The following figure shows that an additional field called an R-TAG is added to every frame of the TSN stream that undergoes FRER replication.

Figure 7-4. Typical Ethernet Frame with FRER R-TAG



The following figure shows that the R-TAG is 6-bytes in size and consists of a 2-byte EtherType field with value 0xF1C1, followed by a 2-byte RESERVED field, and then a 2-byte Sequence Number field. The Sequence Number increments for each subsequent frame of the TSN stream.

Figure 7-5. Format of FRER R-TAG

EtherType = 0xF1C1 (2 bytes)	RESERVED (2 bytes)	Sequence Number (2 bytes)
---------------------------------	-----------------------	------------------------------

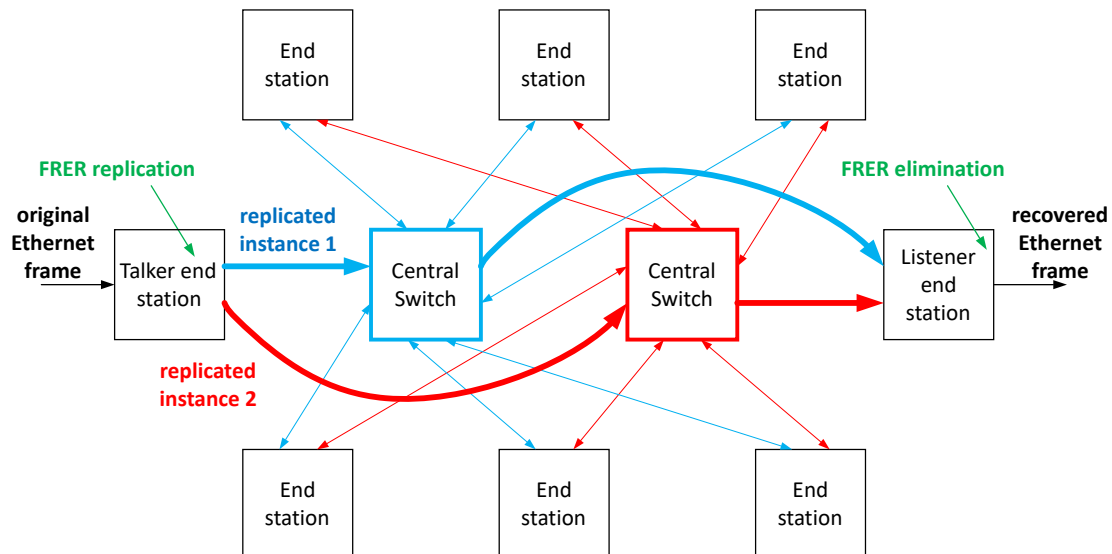
While there is no fundamental limit to the number of replications that can be produced by FRER, it is typically limited in practice to one replicated frame per original frame (that is, 1+1) or two replicated frames per original frame (that is, 1+2).

With 1+1 FRER, two versions of the same frame travel two different paths from the talker to the listener and the probability of the listener not receiving any non-faulty instance of the frame is reduced from P to P^2 , where P is the probability of a frame suffering an error when passing from the talker to the listener on a single path.

With 1+2 FRER, three versions of the same frame travel three different paths from the talker to the listener and the probability of the listener not receiving any non-faulty instance of the frame is reduced from P to P^3 , where P is the probability of a frame suffering an error when passing from the talker to the listener on a single path.

The following figure shows an example of 1+1 FRER operating over a VITA 78.0 dual-star topology Ethernet network, where frame replication is performed at a talker end station and the frame elimination is performed at a listener end station.

Figure 7-6. FRER over a Dual-Star Ethernet Network



7.6 Fault-Tolerant Time Synchronization and Time Integrity (gPTP and FTTM)

The TSN gPTP function distributes time across an Ethernet network using event (timestamped) frames and general (non-timestamped) frames. The basic mechanisms used by gPTP to distribute time are already well described by many papers and tutorials (for example, [Tutorial on Synchronization: A Key Function in Time-Sensitive Networking and Beyond](#)) and are not further discussed in this paper.

For space applications, the most stringent time alignment requirement between all nodes in a network is $1\ \mu\text{s}$, with the network expected to be of a size that has 5 to 15 timing hops.

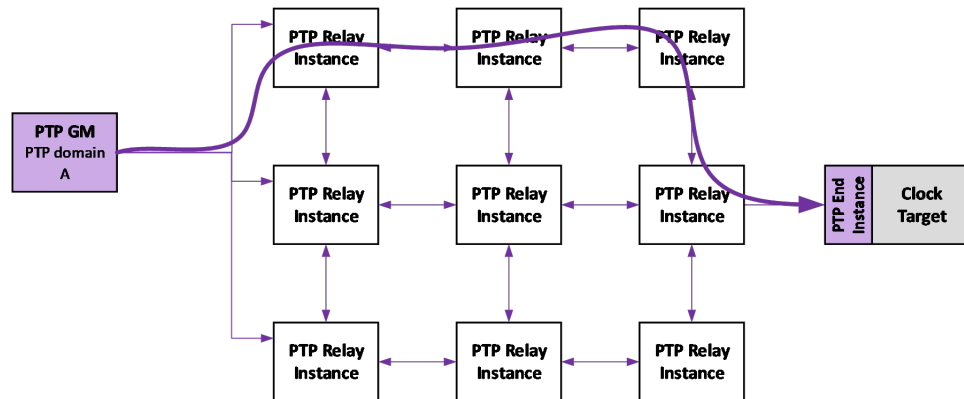
Space applications also use the external port configuration mode for gPTP. That is, the gPTP time distribution paths are manually configured rather than dynamically determined by a gPTP Best

Transmitter Clock Algorithm (BTCA). This is done by manually configuring the timeTransmitter and timeReceiver attributes of each port of each PTP Instance (that is, each end station and each switch).

However, space applications require something new such as, continuous availability of the time and timing integrity, even during Fault scenarios. No existing gPTP mechanism satisfies both requirements.

The following figure shows a typical connection from a gPTP Grandmaster Clock (GM) to a clock target. The availability of the time to the clock target could be temporarily lost if a PTP Relay Instance or a link fails, resulting in a change to the distribution path to the clock target. Also, the integrity of the time cannot inherently be trusted because the basic gPTP mechanisms cannot detect if the time has been corrupted by any of the PTP Instances in the distribution path or by the GM itself.

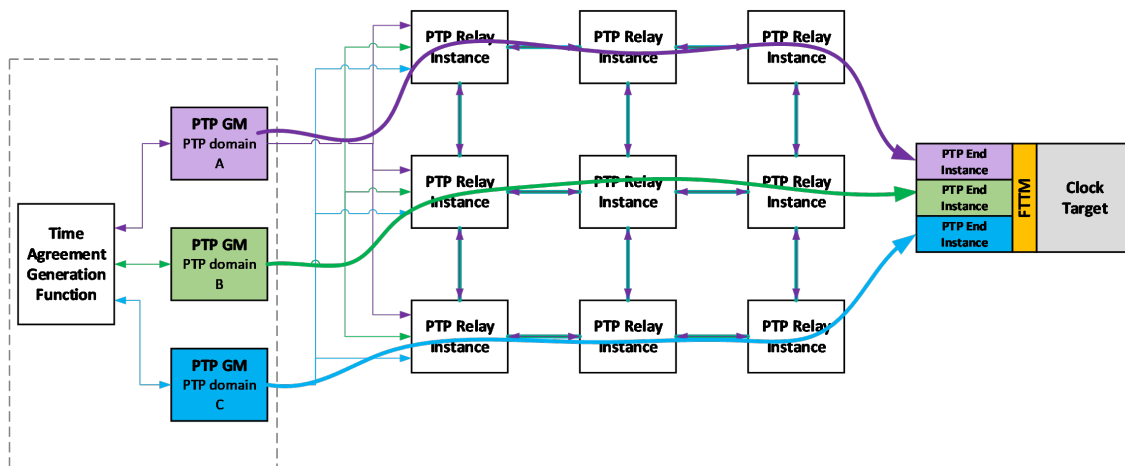
Figure 7-7. Typical Connection From GM to Clock Target



Solutions to achieve constant availability and timing integrity were initially developed in the IEEE P802.1DP project but were subsequently moved to, and will ultimately be defined in, the IEEE P802.1ASed project. At the time of this paper, the definitions of the solutions are still unfinished. However, the concepts behind the potential solutions are discussed here.

To achieve continuous availability and timing integrity, even during Fault scenarios, a new function called the Fault-Tolerant Timing Module (FTTM) is defined. The FTTM is used in a network that has access to multiple independent instances of time, see the following figure. It is placed between PTP instances and the clock target.

Figure 7-8. Independent Connections from Three GMs to a FTTM and Clock Target



In the preceding figure, a time agreement generation function is used to align the multiple GMs. To provide true independence between the aligned (when not-faulty) GMs, this function must be resilient to Byzantine faults. This function is worthy of having its own paper and is not further discussed here. However, some references for it are provided in [8. References](#) section.

The FTTM receives and monitors the time from the multiple gPTP instances and, using an appropriate algorithm, finds and selects a time that is both available and has integrity to deliver to the clock target.

To achieve constant availability of time, the FTTM receives multiple sources of time. If one source is lost or corrupted, another is still available.

To achieve time integrity, the FTTM compares the times from the multiple PTP instances. An error in one can be detected by its deviation from the others. If multiple times are matched with a sufficiently small difference, then they can be deemed to be trustworthy and, thus, have integrity. The FTTM can then select any of the trustworthy times to give to the clock target. This selection is based on which trusted PTP instance has the median time.

7.7 Cyclic Queuing and Forwarding (CQF)

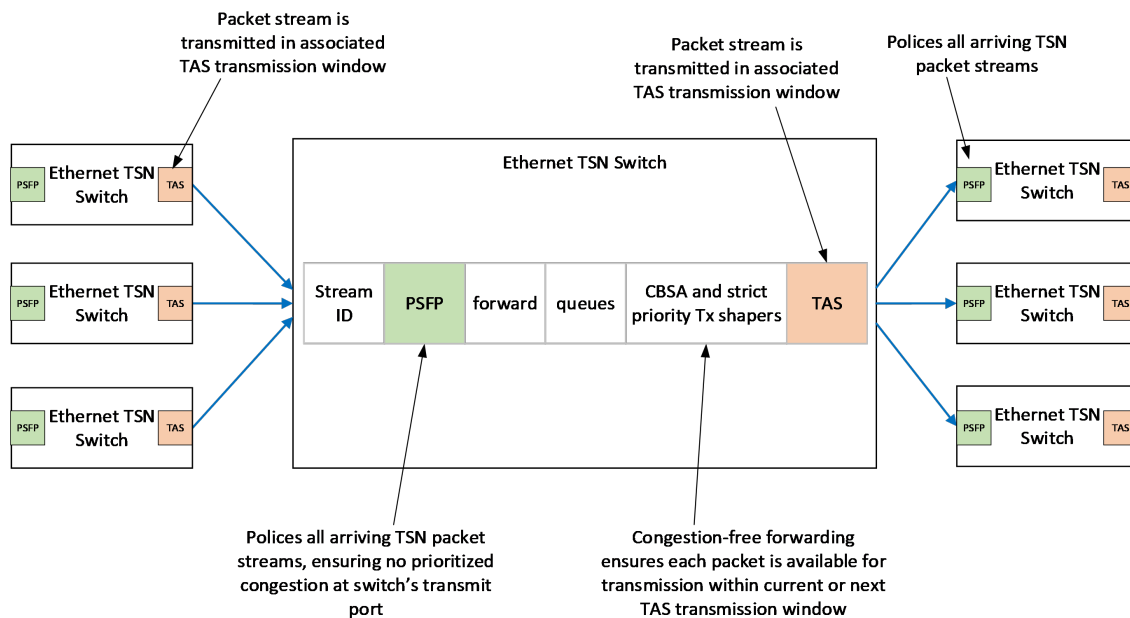
The TSN CQF function is the result of combining PSFP and TAS in a communication system and concluding what is the maximum delay through each switch.

CQF assumes that all well-behaving time-sensitive traffic is setup over the TSN network in a manner that does not cause congestion. When this behavior is combined with TAS, for which all transmission windows of all switches and end stations are aligned, then if that well-behaving time-sensitive traffic arrives within its transmission window on a switch's ingress port, its minimum and maximum latency through the switch to the transmission window of an egress port of the switch can be determined.

PSFP is used to ensure that no unexpected congestion occurs for the TSN streams. It does this by dropping all frames received by the switch that cause a TSN stream to violate its maximum frame size limit, its allowed capacity, or its stream gating.

The following figure shows the operations and expectations discussed in this section.

Figure 7-9. Latency Control with CQF



When the preceding expectations are met:

- The minimum latency of a frame in the switch is equal to the intrinsic delay of the switch, see [Figure 7-10](#).
- The maximum latency of a frame in the switch is represented by the difference between the time at the end of the next transmission window and the time at the start of the current transmission window, see [Figure 7-11](#).

Figure 7-10. Minimum CQF delay

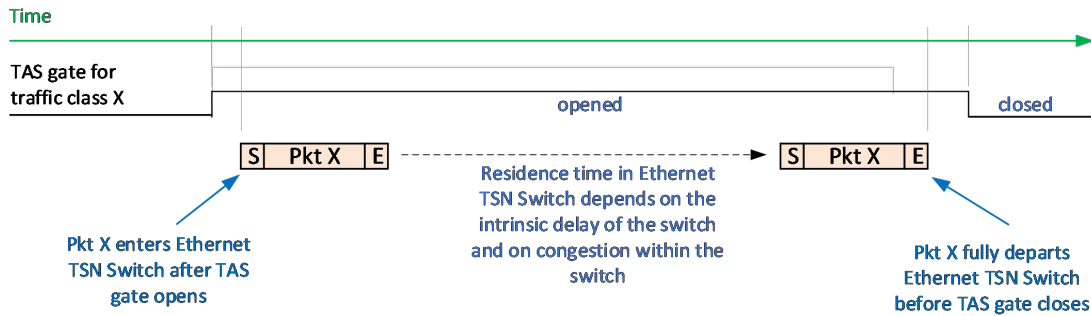
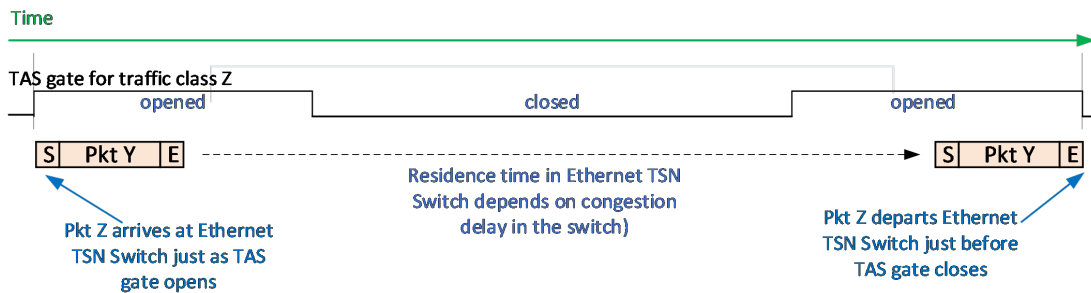


Figure 7-11. Maximum CQF delay

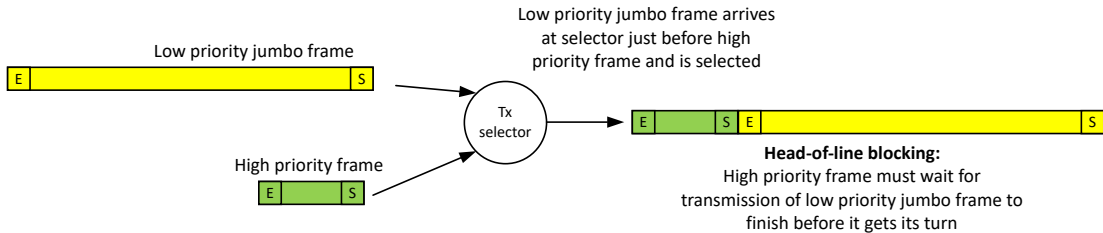


7.8 Frame Preemption

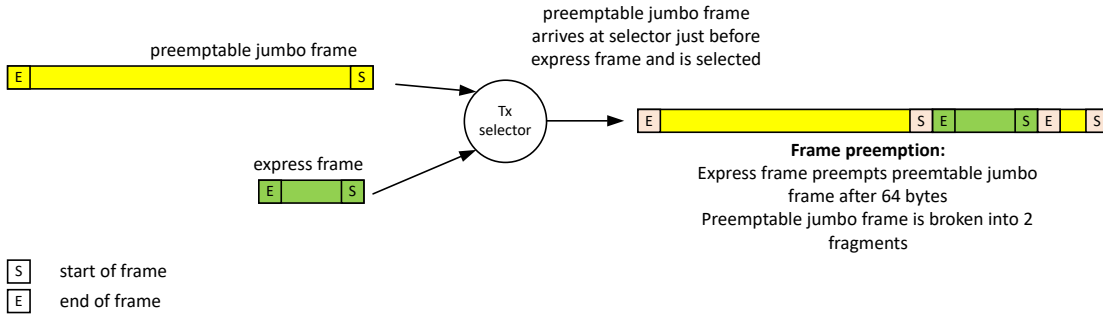
The TSN frame preemption function segregates traffic into two classes, express and preemptable, and pauses the in-progress transmission of frames from the preemptable class to allow frames from the express class to be transmitted sooner. The potential head-of-line blocking delay experienced by express frames is reduced. These concepts are illustrated in the following figure.

Figure 7-12. Frame Preemption Concepts

Without Frame Preemption:



With Frame Preemption:



As listed in the following table, the head-of-line blocking delay has a significant impact on the end-to-end transfer latency of a frame, especially in a system that uses slow Ethernet link rates and that permits large frames.

Table 7-1. Example—Head-of-Line Blocking Delays with And without Frame Preemption

Mode	Head-of-Line Blocking Delay (ms)		
	Without Frame Preemption		With Frame Preemption
Blocking frame Size (bytes)	1522	9622	127
Ethernet Rate			
10M	1217.6	7697.6	101.6
100M	121.8	769.8	10.2
1G	12.2	77.0	1.0
10G	1.2	7.7	0.1

8. References

The following reference documents are applicable for this white paper:

- *ANSI/VITA 78.0-2022, SpaceVPX System Standard, Aug 2022*
- *IEEE 802.1AS-2020, IEEE Standard for Local and Metropolitan Area Networks—Timing and Synchronization for Time-Sensitive Applications, Jan 2020*
- *IEEE P802.1ASdm/D2.3, Draft Standard for Local and metropolitan area networks—Timing and Synchronization for Time-Sensitive Applications, Amendment: Hot Standby and Clock Drift Error Reduction, May 2024*
- [Draft for Local and Metropolitan Area Networks-Timing and Synchronization for Time-Sensitive Applications, Amendment: Fault-Tolerant Timing with Time Integrity, Jun 2024](#)
- *IEEE 802.1CB-2017, IEEE Standard for Local and metropolitan area networks—Frame Replication and Elimination for Reliability, Sept 2017*
- *IEEE 802.1CBdb-2021, IEEE Standard for Local and metropolitan area networks—Frame Replication and Elimination for Reliability, Amendment 2: Extend Stream Identification Functions, Dec 2021*
- *IEEE P802.1DP/D1.1, Draft Standard for Local and metropolitan area networks—Time-Sensitive Networking for Aerospace Onboard Ethernet Communications, Dec 2023*
- *IEEE P802.1DP/D2.0, Draft Standard for Local and metropolitan area networks—Time-Sensitive Networking for Aerospace Onboard Ethernet Communications, May 2024*
- *IEEE 802.1Q-2022, IEEE Standard for Local and metropolitan area networks—Bridges and Bridged Networks, Sept 2022*
- *IEEE 802.1Qav-2009, IEEE Standard for Local and metropolitan area networks—Virtual Bridged Local Area Networks, Amendment 12: Forwarding and Queuing Enhancements for Time-Sensitive Streams, Dec 2009*
- *IEEE 802.1Qbu-2016, IEEE Standard for Local and metropolitan area networks—Bridges and Bridged Networks, Amendment 26: Frame Preemption, Jun 2016*
- *IEEE 802.1Qbv-2015, IEEE Standard for Local and metropolitan area networks—Bridges and Bridged Networks, Amendment 25: Enhancements for Scheduled Traffic, Dec 2015*
- *IEEE 802.1Qcc-2018, IEEE Standard for Local and Metropolitan Area Networks—Bridges and Bridged Networks, Amendment 31: Stream Reservation Protocol (SRP) Enhancements and Performance Improvements, Jun 2018*
- *IEEE 802.1Qch-2017, IEEE Standard for Local and metropolitan area networks—Bridges and Bridged Networks, Amendment 29: Cyclic Queuing and Forwarding, May 2017*
- *IEEE 802.1Qci-2017, IEEE Standard for Local and metropolitan area networks—Bridges and Bridged Networks, Amendment 28: Per-Stream Filtering and Policing, Feb 2017*
- *IEEE 802.3br-2016, IEEE Standard for Ethernet Amendment 5: Specification and Management Parameters for Interspersing Express Traffic, Jun 2016*
- L Lamport, PM Melliar-Smith, [Synchronizing clocks in the presence of Faults](#), 1982
- D Dolev, J Halpern, [On the Possibility and Impossibility of Achieving Clock Synchronization](#), 1984
- P Miner, A Geser, L Pike, Jeffery Maddalon, [A Unified Fault-Tolerance Protocol](#), 2004
- P Ramanathan, KG Shin, RW Butler, [Fault-Tolerant Clock Synchronization in Distributed Systems](#), 1990M Pease, R Shostak, L Lamport, [Reaching Agreement in the Presence of Faults](#), 1980

9. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description
B	07/2024	Updated the application layer software details in 5.2. PIC64-HPSC Software Features for TSN section
A	07/2024	Initial Revision

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure

that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGaT, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2024, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.

ISBN: 978-1-6683-4876-5

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	Australia - Sydney Tel: 61-2-9868-6733 China - Beijing Tel: 86-10-8569-7000 China - Chengdu Tel: 86-28-8665-5511 China - Chongqing Tel: 86-23-8980-9588 China - Dongguan Tel: 86-769-8702-9880 China - Guangzhou Tel: 86-20-8755-8029 China - Hangzhou Tel: 86-571-8792-8115 China - Hong Kong SAR Tel: 852-2943-5100 China - Nanjing Tel: 86-25-8473-2460 China - Qingdao Tel: 86-532-8502-7355 China - Shanghai Tel: 86-21-3326-8000 China - Shenyang Tel: 86-24-2334-2829 China - Shenzhen Tel: 86-755-8864-2200 China - Suzhou Tel: 86-186-6233-1526 China - Wuhan Tel: 86-27-5980-5300 China - Xian Tel: 86-29-8833-7252 China - Xiamen Tel: 86-592-2388138 China - Zhuhai Tel: 86-756-3210040	India - Bangalore Tel: 91-80-3090-4444 India - New Delhi Tel: 91-11-4160-8631 India - Pune Tel: 91-20-4121-0141 Japan - Osaka Tel: 81-6-6152-7160 Japan - Tokyo Tel: 81-3-6880-3770 Korea - Daegu Tel: 82-53-744-4301 Korea - Seoul Tel: 82-2-554-7200 Malaysia - Kuala Lumpur Tel: 60-3-7651-7906 Malaysia - Penang Tel: 60-4-227-8870 Philippines - Manila Tel: 63-2-634-9065 Singapore Tel: 65-6334-8870 Taiwan - Hsin Chu Tel: 886-3-577-8366 Taiwan - Kaohsiung Tel: 886-7-213-7830 Taiwan - Taipei Tel: 886-2-2508-8600 Thailand - Bangkok Tel: 66-2-694-1351 Vietnam - Ho Chi Minh Tel: 84-28-5448-2100	Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen Tel: 45-4485-5910 Fax: 45-4485-2829 Finland - Espoo Tel: 358-9-4520-820 France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 Germany - Garching Tel: 49-8931-9700 Germany - Haan Tel: 49-2129-3766400 Germany - Heilbronn Tel: 49-7131-72400 Germany - Karlsruhe Tel: 49-721-625370 Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 Germany - Rosenheim Tel: 49-8031-354-560 Israel - Hod Hasharon Tel: 972-9-775-5100 Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781 Italy - Padova Tel: 39-049-7625286 Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340 Norway - Trondheim Tel: 47-72884388 Poland - Warsaw Tel: 48-22-3325737 Romania - Bucharest Tel: 40-21-407-87-50 Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 Sweden - Gothenberg Tel: 46-31-704-60-40 Sweden - Stockholm Tel: 46-8-5090-4654 UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820