# EmCORE-i2305

## 3.5” Compact Board

# User’s Manual

**Version 1.1**

2017.05

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## Revision History

| Version | Release Time | Description |
|---|---|---|
| 1.0 | July 2014 | Initial release |
| 1.1 | May 2017 | Added supported SDXC information in 1.3. Specifications and 2.3.3. Connectors SD1 section |

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## Copyright Notice



The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.



## Declaration of Conformity

### CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

**Warning**

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

**FCC Class A**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

**RoHS**

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

**SVHC / REACH**

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

## Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

## Replacing Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

## Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor-technology.com

E-mail:info@arbor.com.tw

## Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

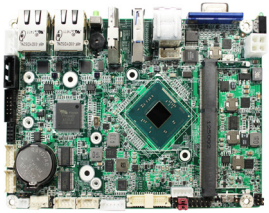
Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

# Chapter 1

# Introduction

## 1.1. The Product

- Support Intel® Atom™ Processor E3800 family
- Integrated Gigabit Ethernet
- LVDS, Analog RGB Port, HDMI port
- Support Dual Independent Displays
- Soldered Onboard 16GB eMMC (optional)
- **Extended Operating Temp.: -20 ~ 70°C**
- **Wide Range Operating Temp.: -40 ~ 85°C (WT series)**



## 1.2. About this Manual

This manual is intended for experienced users and integrators with hardware knowledge of computers. If you are not sure about the description in this manual, consult your vendor before further handling.

We recommend that you keep one copy of this manual for the quick reference for any necessary maintenance in the future. Thank you for choosing ARBOR products.

## 1.3. Specifications

| | | |
|---|---|---|
| **Form Factor** | 3.5" Compact Board | |
| **CPU** | Soldered onboard Intel® Atom™ Processor E3825 dual-core 1.33GHz or E3845 quad-core 1.91GHz | |
| **System Memory** | 1 x DDR3L SO-DIMM socket, supporting SDRAM up to 8GB | |
| **Graphics Chipset** | Integrated Intel® HD Graphics | |
| **Graphics Interface** | HDMI | Vertical HDMI connector |
| | LCD | Dual-channel 24-bit LVDS |
| | Analog RGB that supports resolution up to 2048 x 1536 | |
| **Ethernet** | 2 x Realtek® RTL8111 PCIe GbE controllers | |
| **BIOS** | Insyde BIOS | |
| **Audio** | Realtek ALC662 HD Audio CODEC, MIC-in/ Line-out/Line-in | |
| **Storage** | 1 x Serial ATA port with 300MB/s HDD transfer rate | |
| | 1 x mSATA socket | |
| | Soldered onboard 16GB eMMC(optional) | |
| **Serial Port** | 2 x COM ports (1 x RS-232 port, 1 x RS-232/485 port selectable) | |
| **Universal Serial Bus** | 4 x USB 2.0 ports | |
| | 1 x USB 3.0 port | |
| **Digital I/O** | 8-bit programmable Digital Input/Ouput | |
| **Expansion Bus** | 1 x Mini-card socket | |
| | 1 x Micro-SDXC socket (E3800 family only, supports SDXC card SD 3.0 only) | |
| | 2 x I2C ports (optional) | |
| **Power Requirement** | +12V DC | |
| **Power Consumption** | 0.56A@+12V (typical) (E3825)<br>0.65A@+12V (typical) (E3845) | |
| **Operating Temp.** | -20°C ~ 70°C (-4°F ~ 158°F)<br>-40°C ~ 85ºC (-40°F ~ 185ºF, WT series) | |
| **Operating Humidity** | 10% ~ 95% @ 70°C (non-condensing)<br>10% ~ 95% @ 85ºC (non-condensing, WT series) | |
| **Watchdog Timer** | 1~255 levels reset | |
| **Dimension (L x W)** | 146 x 102 mm (5.7” x 4.0”) | |

## 1.4. Inside the Package

Before starting to install the single board, make sure the following items are shipped:

| | |
|---|---|
|  | 1 x EmCORE-i2305 3.5" Compact Board with heatsink |
|  | 1 x Driver CD |
|  | 1 x Quick Installation Guide |

If any of the aforelisted items is damaged or missing, contact your vendor immediately.

## 1.5. Ordering Information

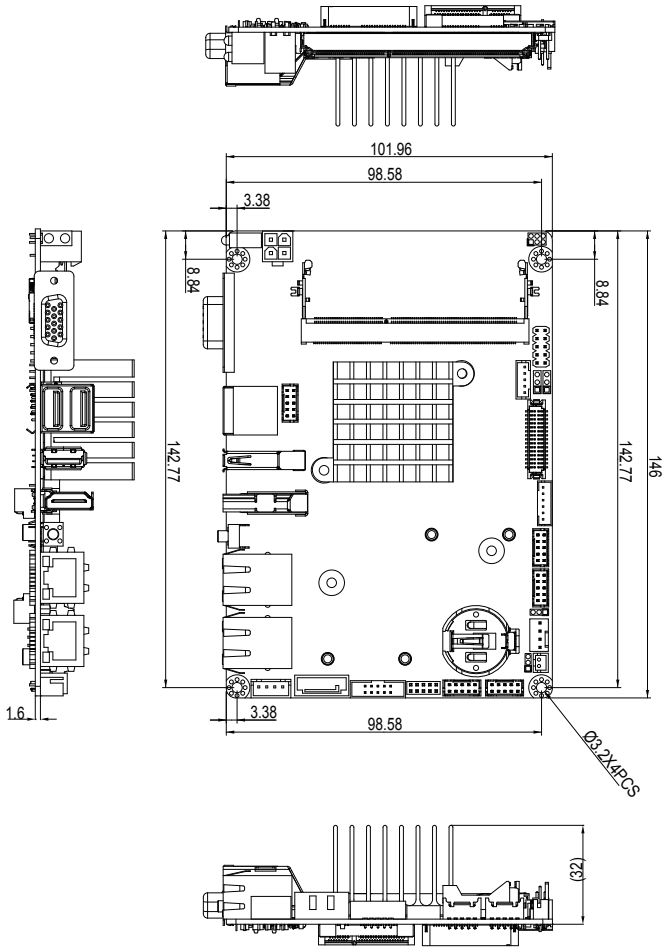
| | |
|---|---|
| **EmCORE-i2305-E3825** | Intel® Atom™ Processor E3825 3.5" Compact Board |
| **EmCORE-i2305-WT-E3825** | Wide range temperature Intel® Atom™ Processor E3825 3.5" Compact Board |
| **EmCORE-i2305-E3845** | Intel® Atom™ Processor E3845 3.5" Compact Board |
| **EmCORE-i2305-WT-E3845** | Wide range temperature Intel® Atom™ Processor E3845 3.5" Compact Board |
| **EmCORE-i2305-N2807 (BTO)** | Intel® Celeron® Processor N2807 3.5" Compact Board |
| **EmCORE-i2305-N2930 (BTO)** | Intel® Celeron® Processor N2930 3.5" Compact Board |
| **CBK-07-2305-00** | Cable kit<br>1 x AUDIO cable<br>2 x COM port latching cables<br>1 x Keyboard & mouse latching y-cable<br>1 x SATA cable<br>1 x SATA power cable<br>1 x USB cable |

# Chapter 2

# Getting Started

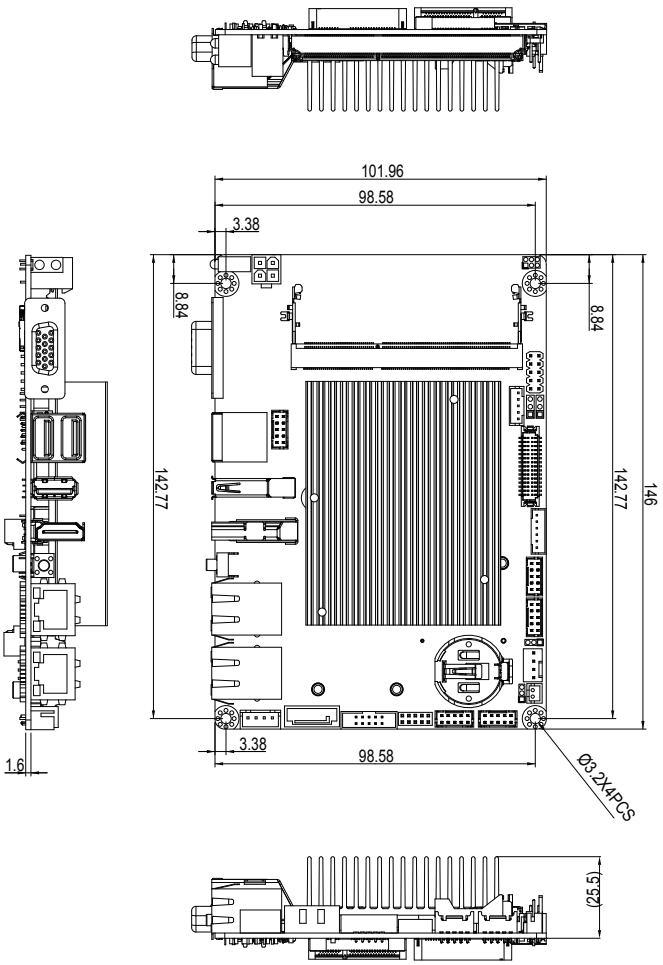
## 2.1. Board Dimensions

### 2.1.1. SKU-E3825



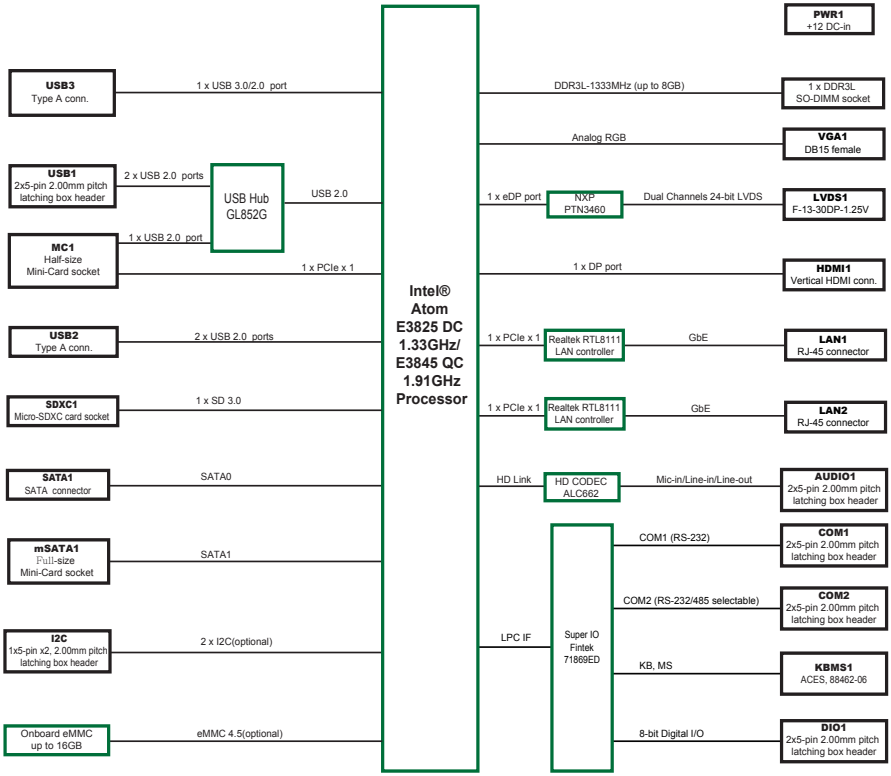

Unit: mm

### 2.1.2. SKU-E3845




Unit: mm

## 2.2. Block Diagram



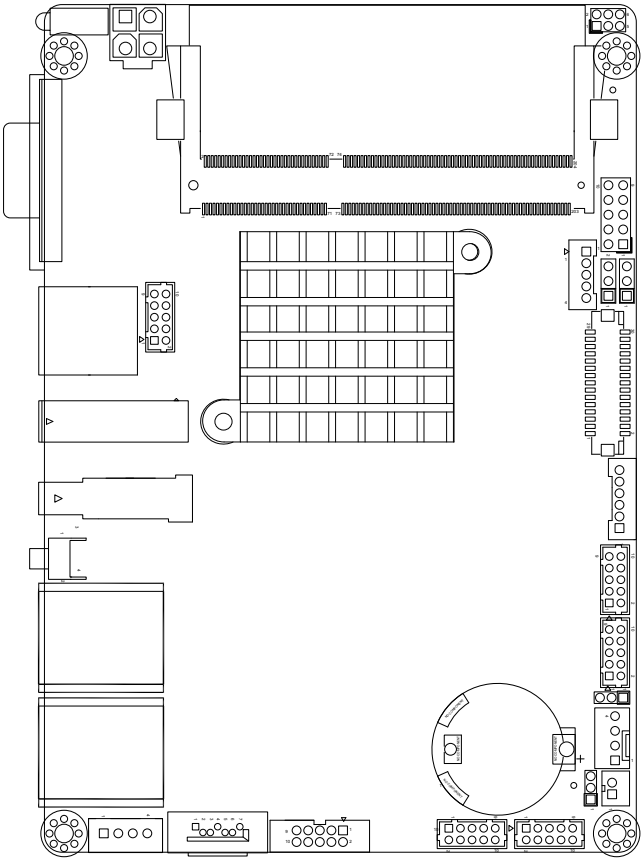
## 2.3. Jumpers & Connectors

The board comes with some connectors to join some devices and also some jumpers to alter the hardware configuration. The following in this chapter will explicate each of these components one-by-one.

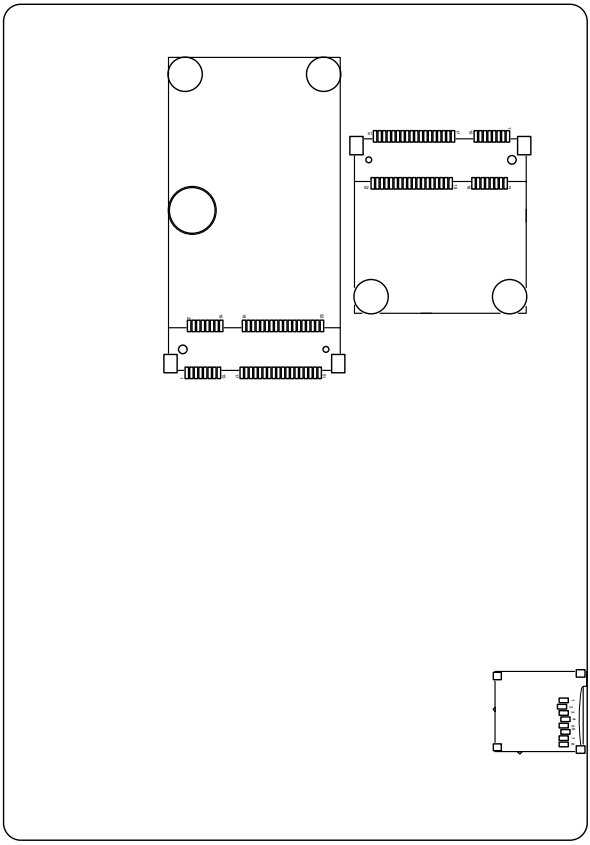
### 2.3.1. Layout

This section will provide an overview of this board, both the top and bottom sides.

**Board Top**



## Board Bottom



## 2.3.2. Jumpers

### JPIC1

**Function:** Sets the AT/ATX mode

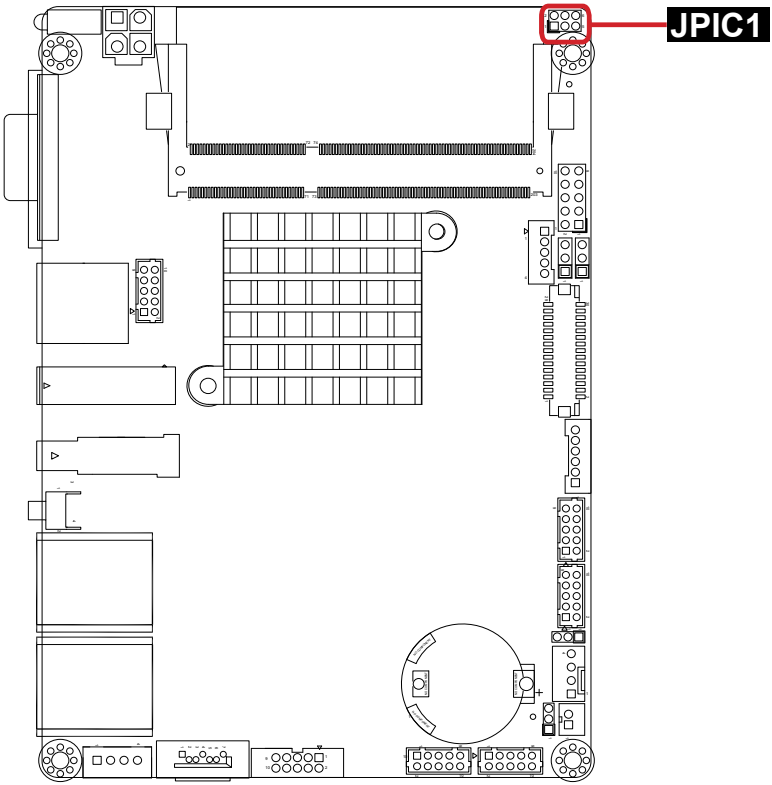
**Jumper Type:** 2.00mm pitch 2x3-pin header

**Setting:**

| Pin | Description | |
|---|---|---|
| **2-4** | AT |  |
| **4-6** | ATX mode (default) |  |

Note to make consistent setting in **BIOS** | **Advanced** menu | **ACPI Settings** | **Power-Supply Type** to avoid possible conflict. See 3.2.1. Boot Configuration on page 45.

### Board Top



## JINV1

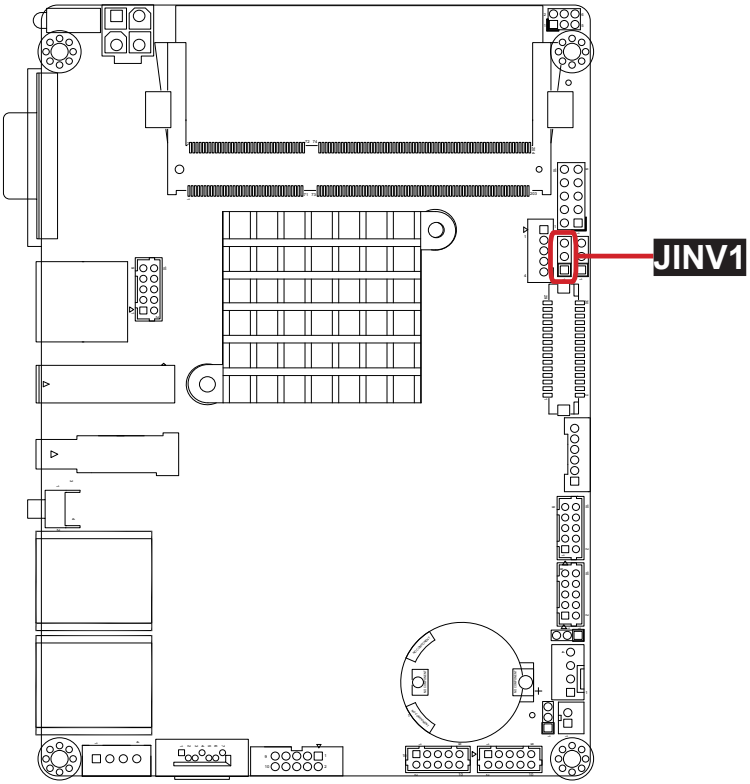
**Function:** Sets the LCD inverter voltage

**Jumper Type:** 2.54mm pitch 1x3-pin header

**Setting:**

| Pin | Description | |
|---|---|---|
| **1-2** | +12V |   |
| **2-3** | +5V (default) |   |

## Board Top



## JVLCD1

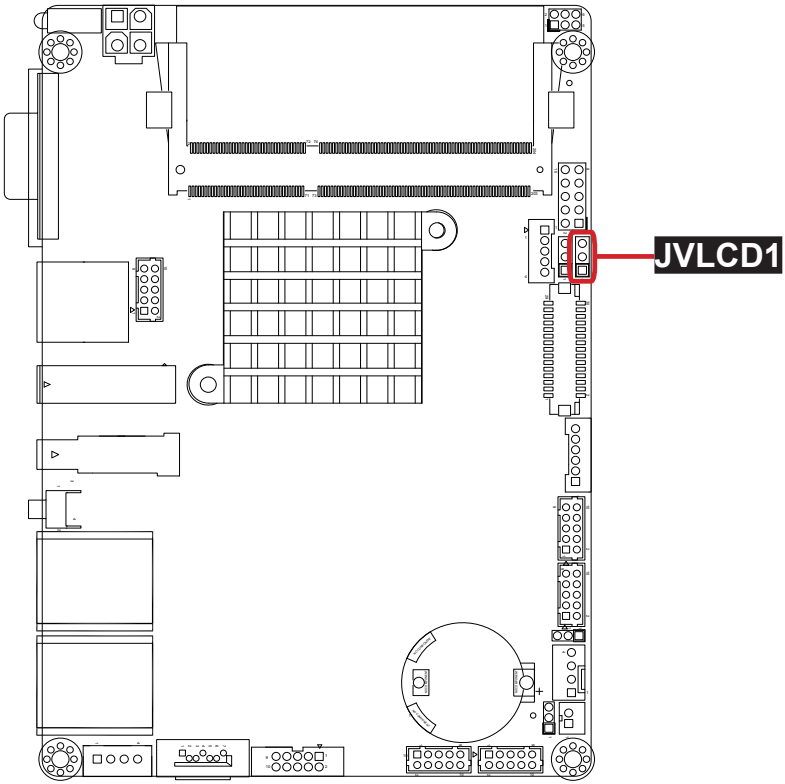
**Function:** Sets the power voltage fro LVDS1 LCD

**Jumper Type:** 2.54mm pitch 1x3-pin header

**Setting:**

| Pin | Description | |
|---|---|---|
| **1-2** | +5V |   |
| **2-3** | +3.3V (default) |   |

## Board Top



## JBAT1

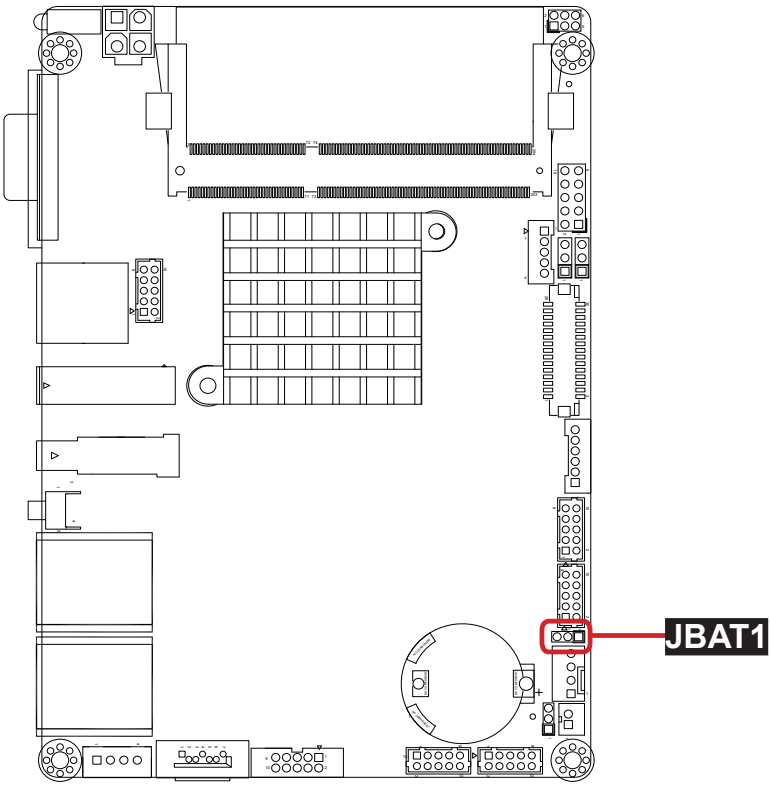
**Function:** Clears/keeps CMOS

**Jumper Type:** 2.00 mm pitch 1x3-pin header

**Setting:**

| Pin | Description | |
|---|---|---|
| **1-2** | Keeps CMOS (default) |   |
| **2-3** | Clears CMOS |   |

## Board Top



## JRS1

**Function:** COM2 RS-232/485 selection

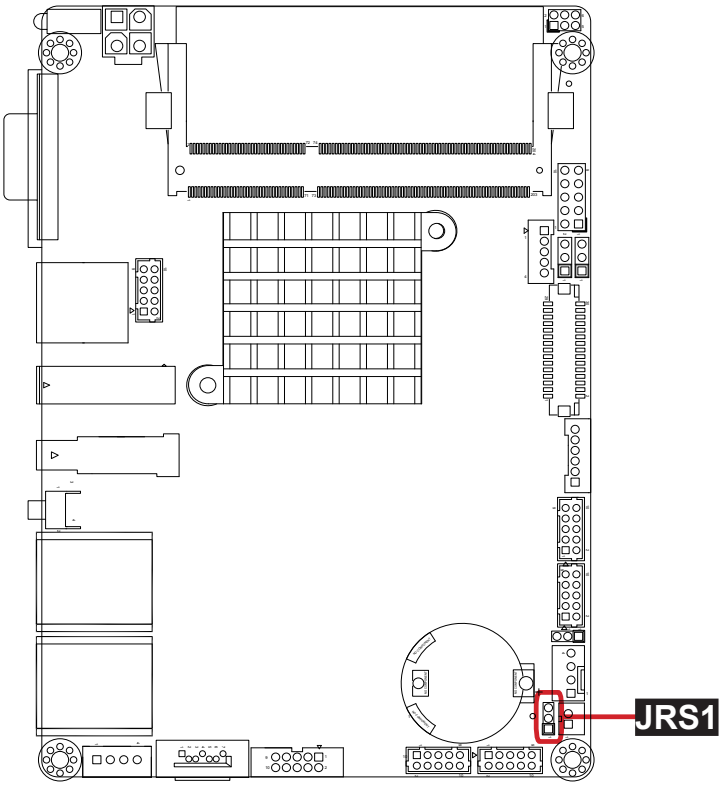
**Jumper Type:** 2.00 mm pitch 1x3-pin header

**Setting:**

| Pin | Description | |
|---|---|---|
| **1-2** | RS-232 (default) |   |
| **2-3** | RS-485 |   |

**Note:** To enable RS-485 Port (CN1) , beside jumper setting, please go to BIOS Setting Menu to Enable RS-485 mode of COM2. Option is under **Advanced/ SIO FINTEK71869E/ RS-232/485 Setting/ RS-485**. After enabled RS-485 Mode, CN1 will be activated as RS-485 port

## Board Top



### 2.3.3. Connectors

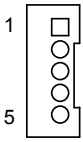
#### INV1

**Function:** LCD inverter connector

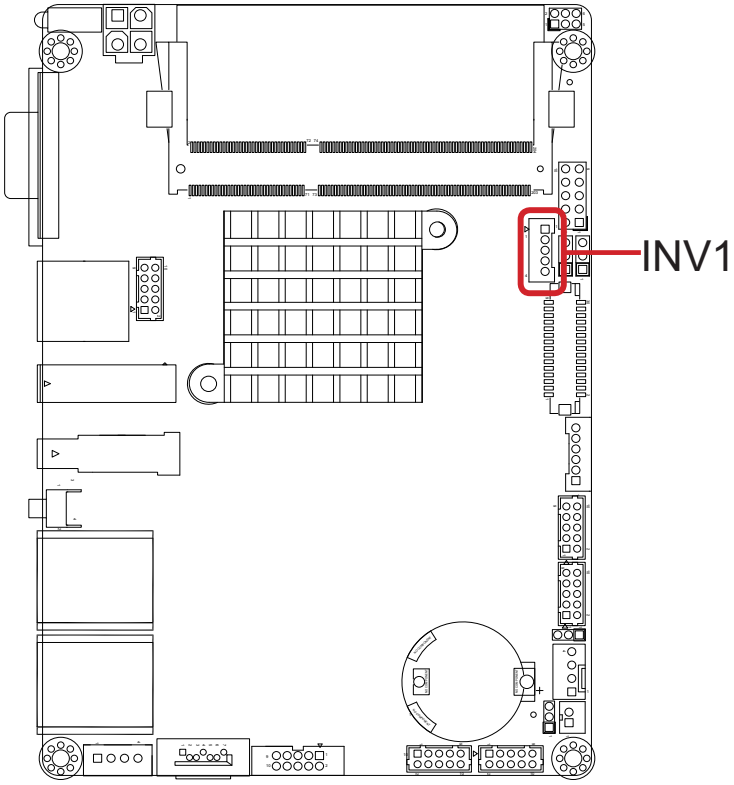
**Connector Type:** 2.00mm pitch 1x5-pin box wafer

**Pin Assignment:**

| Pin | Description |
|---|---|
| 1 | Vin |
| 2 | GND |
| 3 | on/off |
| 4 | Brightness control |
| 5 | GND |




#### Board Top



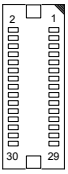
## LVDS1

**Function:** LVDS LCD panel connector

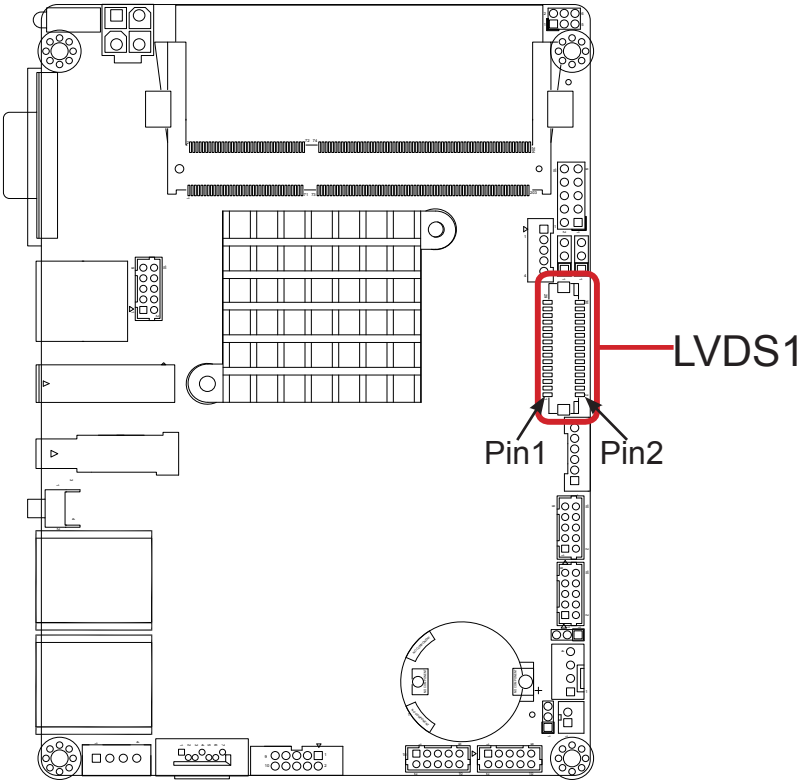
**Connector Type:** ACES 1.25mm 87209-3040-06 connector that supports 24-bit dual channels.

**Pin Assignment:**

| Pin | Description | Pin | Description | Pin | Description |
|---|---|---|---|---|---|
| **2** | VDD | **22** | TX2_D2+ | **11** | TX1_D0- |
| **4** | TX2_CLK+ | **24** | TX2_D2- | **13** | GND |
| **6** | TX2_CLK- | **26** | GND | **15** | TX1_D1+ |
| **8** | GND | **28** | TX2_D3+ | **17** | TX1_D1- |
| **10** | TX2_D0+ | **30** | TX2_D3- | **19** | GND |
| **12** | TX2_D0- | **1** | VDD | **21** | TX1_D2+ |
| **14** | GND | **3** | TX1_CLK+ | **23** | TX1_D2- |
| **16** | TX2_D1+ | **5** | TX1_CLK- | **25** | GND |
| **18** | TX2_D1- | **7** | GND | **27** | TX1_D3+ |
| **20** | GND | **9** | TX1_D0+ | **29** | TX1_D3- |




## Board Top



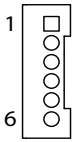
## KBMS1

**Function:** Keyboard & Mouse connector

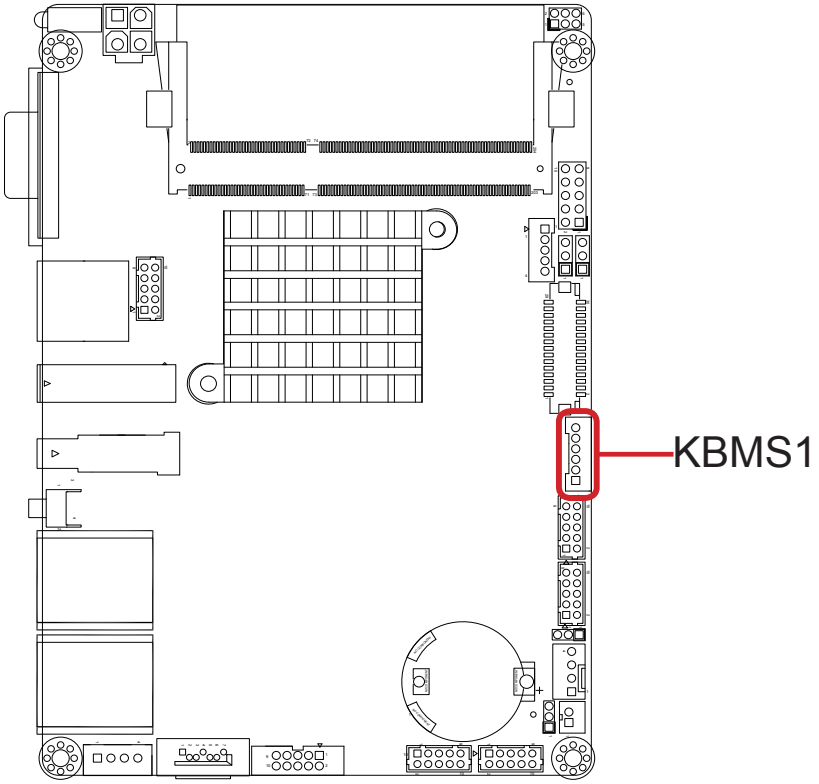
**Connector Type:** 2.0mm pitch 1x6-pin header

**Pin Assignment:**

| Pin | Description |
|---|---|
| 1 | KB_DATA |
| 2 | GND |
| 3 | MS_DATA |
| 4 | KB_CLK |
| 5 | PS2_VCC |
| 6 | MS_CLK |




## Board Top



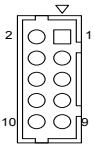
## COM1&2

**Function:** Serial port connector

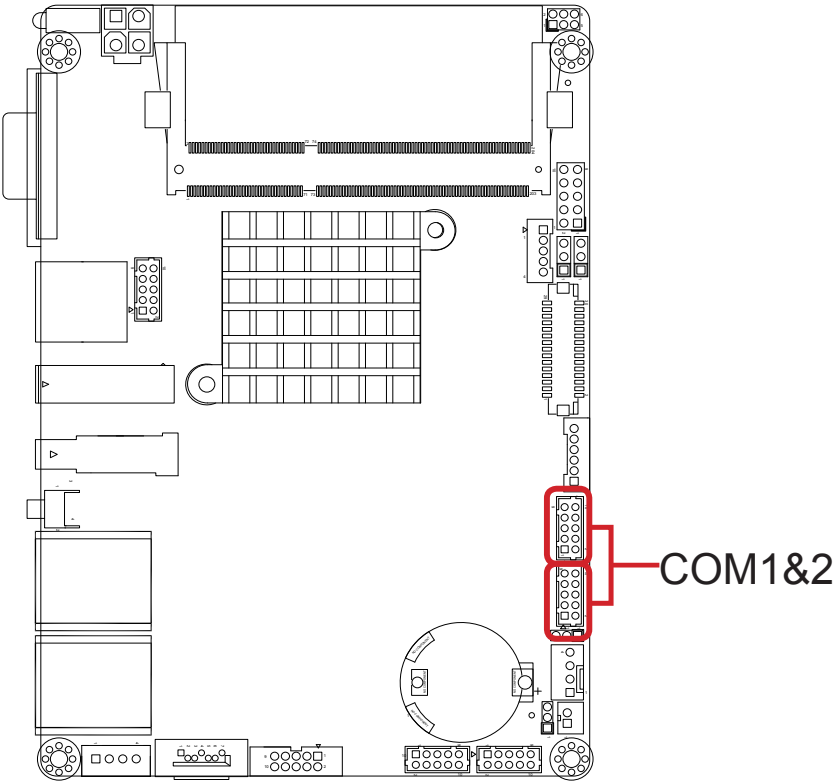
**Connector Type:** 2.00mm pitch 2x5-pin wafer connector

**Pin Assignment:**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 2 | RX | 1 | DCD# |
| 4 | DTR# | 3 | TXD |
| 6 | DSR# | 5 | GND |
| 8 | CTS# | 7 | RTS# |
| 10 | N/C | 9 | RI# |




## Board Top



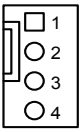
## FAN1

**Function:** Fan connector

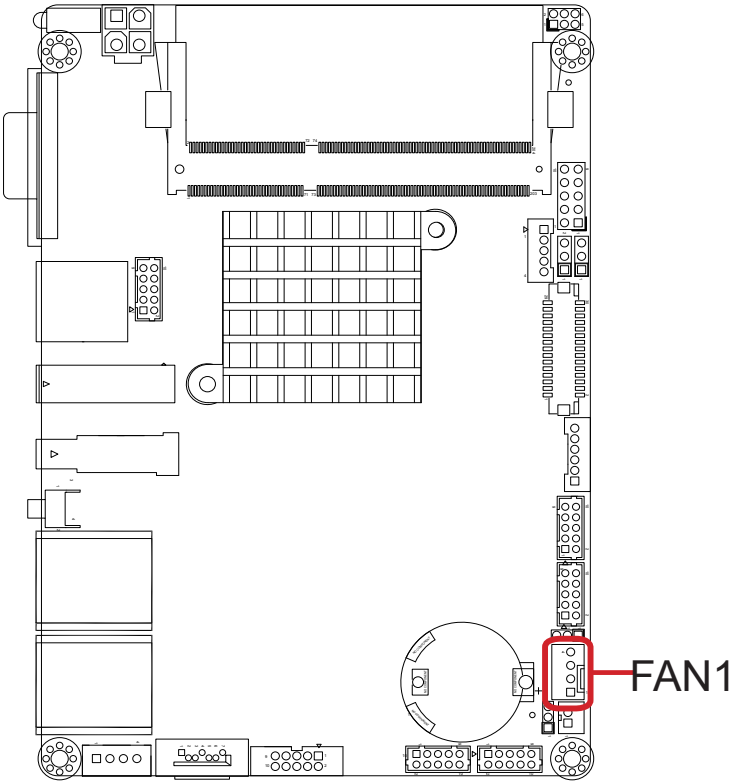
**Connector Type:** 2.54mm pitch 1x4-pin wafer connector.

**Pin Assignment:**

| Pin | Description |
|---|---|
| 1 | GND |
| 2 | +12V |
| 3 | Fan_Detect |
| 4 | Control |




## Board Top



## CN1

**Function:** RS-485 connector

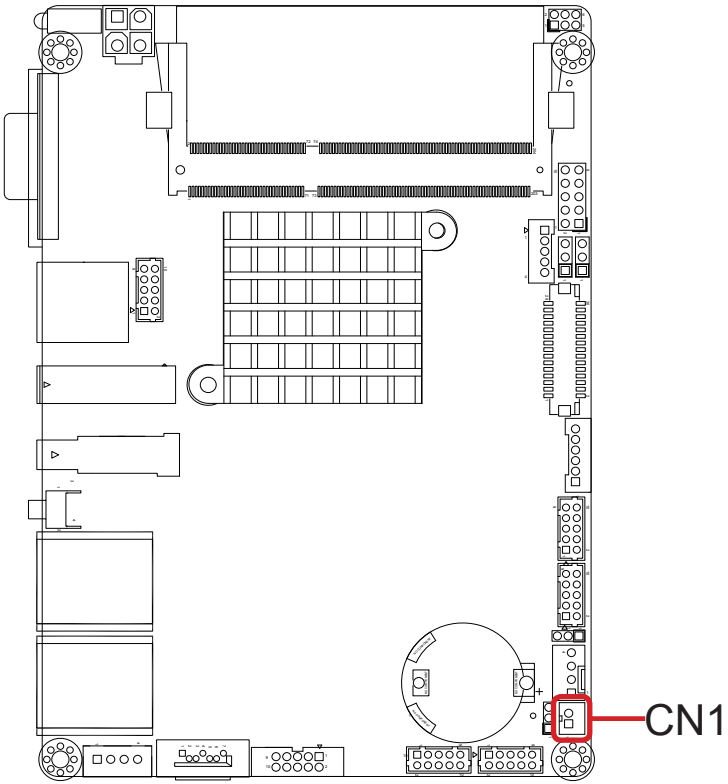
**Connector Type:** 2.00mm pitch 1x2-pin Box Wafer Connector

**Pin Assignment:**

| Pin | Description |
|---|---|
| 1 | DATA- |
| 2 | DATA+ |


Note: To enable this port, please refer to JRS1 on page 15 .

## Board Top



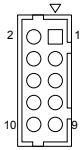
## DIO1

**Function:** Digital I/O connector

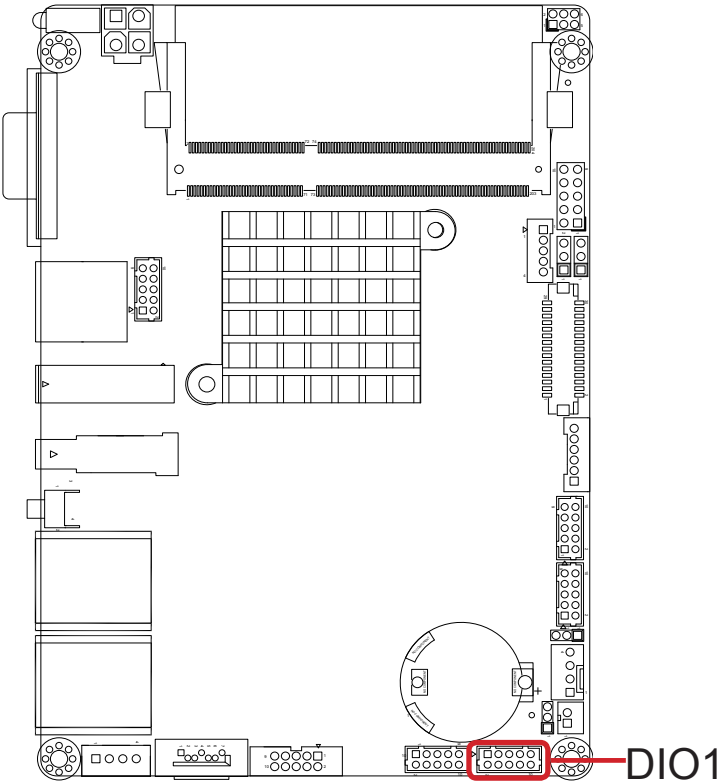
**Connector Type:** 2.00mm pitch 2x5-pin wafer connector

**Pin Assignment:**

| Pin | Description | Pin | Description |
|---|---|---|---|
| **2** | GPIO1 | **1** | GPIO0 |
| **4** | GPIO3 | **3** | GPIO2 |
| **6** | GPIO5 | **5** | GPIO4 |
| **8** | GPIO7 | **7** | GPIO6 |
| **10** | GND | **9** | +5V |




## Board Top



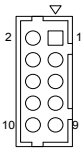
## I2C1

**Function:** I2C connector

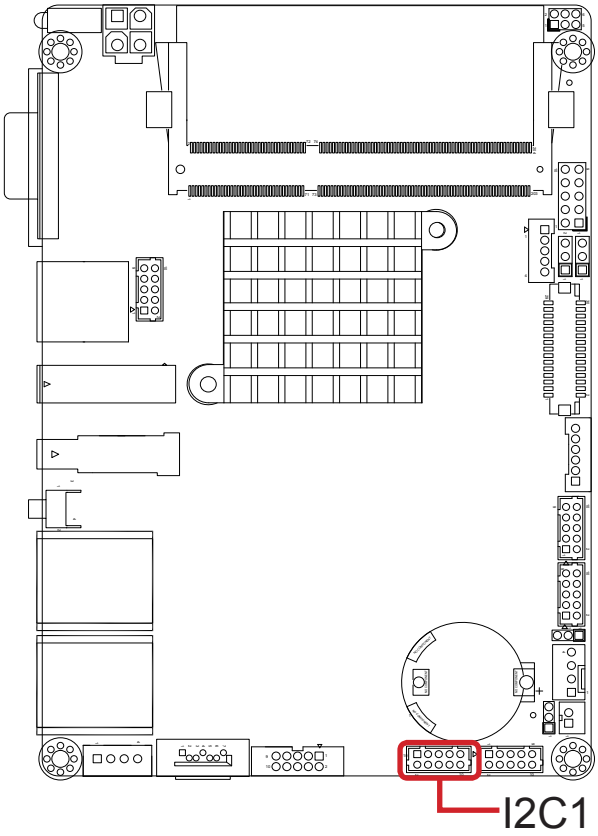
**Connector Type:** 2.00mm pitch 2x5-pin wafer connector

**Pin Assignment:**

| Pin | Description | Pin | Description |
|---|---|---|---|
| **2** | +3.3V | **1** | +3.3V |
| **4** | I2C_CLK1(3.3V) | **3** | I2C_CLK0(3.3V) |
| **6** | I2C_DATA1(3.3V) | **5** | I2C_DATA0(3.3V) |
| **8** | GND | **7** | GND |
| **10** | GND | **9** | GND |




## Board Top



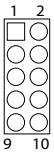
## AUDIO1

**Function:** Audio connector

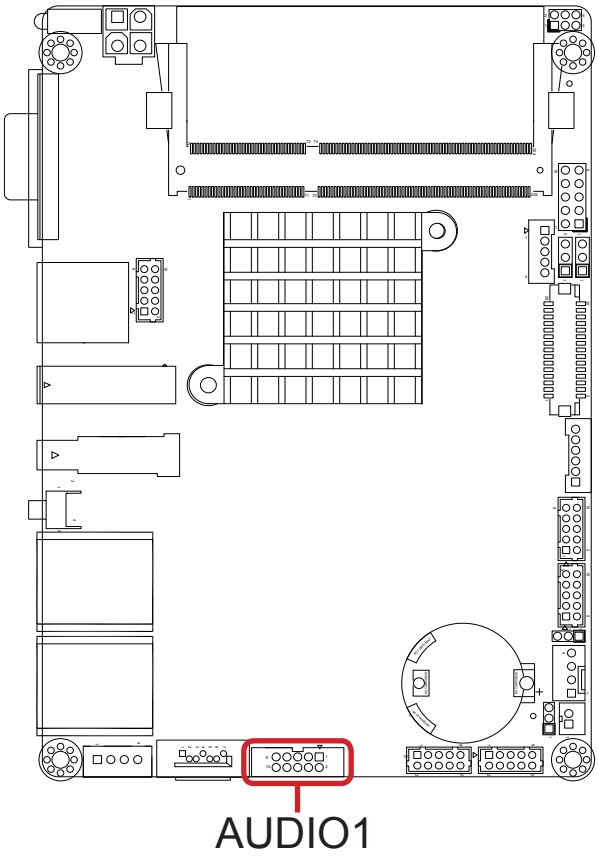
**Connector Type:** 2.00mm pitch 2x5-pin header

**Pin Assignment:**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | Line Left In | 2 | Line Right In |
| 3 | GND | 4 | GND |
| 5 | MIC1 | 6 | MIC2 |
| 7 | GND | 8 | GND |
| 9 | Line-out Left | 10 | Line-out Right |




## Board Top

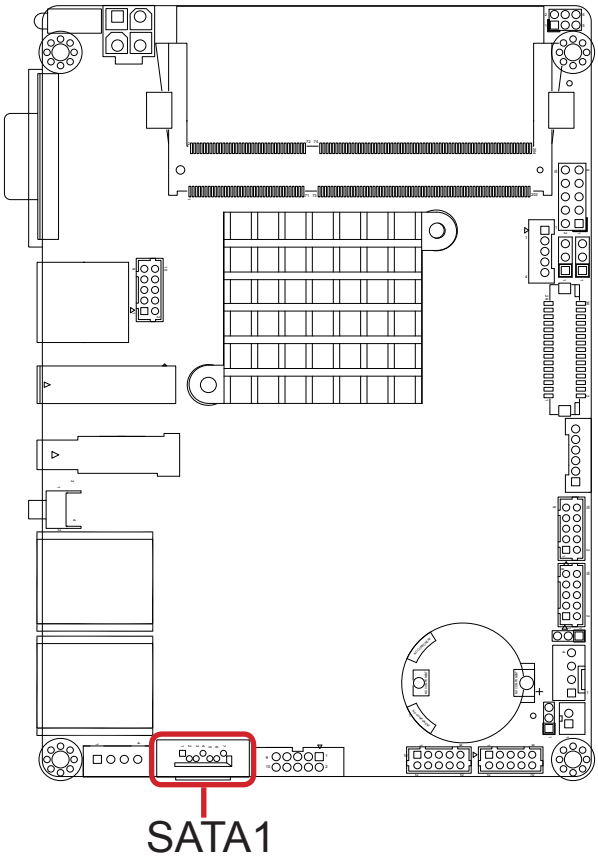


## SATA1

**Function:** Serial ATA connector

**Pin Assignment:** The pin assignments conform to the industry standard.

## Board Top



## PWROUT1

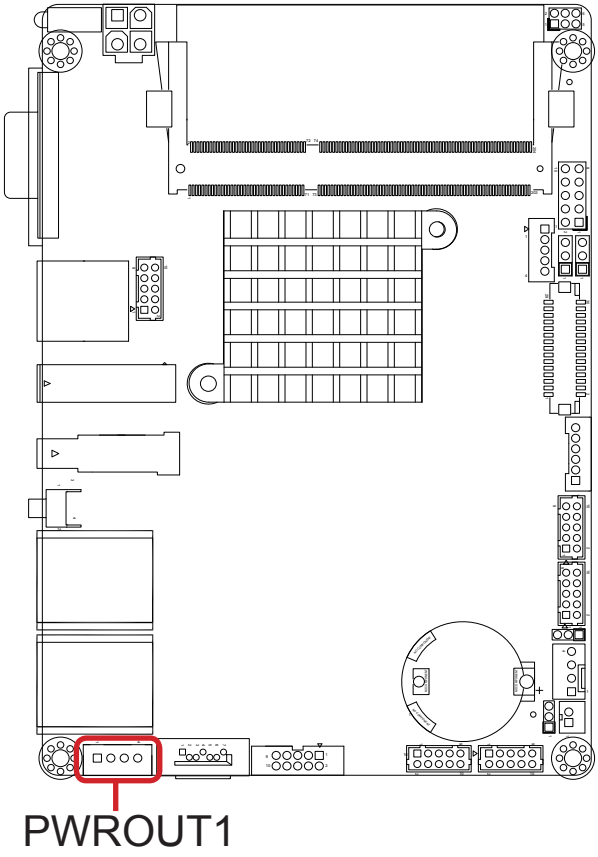
**Function:** SATA power connector

**Connector Type:** 2.54mm pitch 1x4-pin wafer connector

**Pin Assignment:**

| Pin | Description |
|---|---|
| 1 | VCC 5V |
| 2 | GND |
| 3 | GND |
| 4 | VCC 12V |


## Board Top



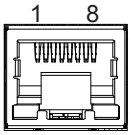
## LAN1, 2

**Function:** Ethernet connectors

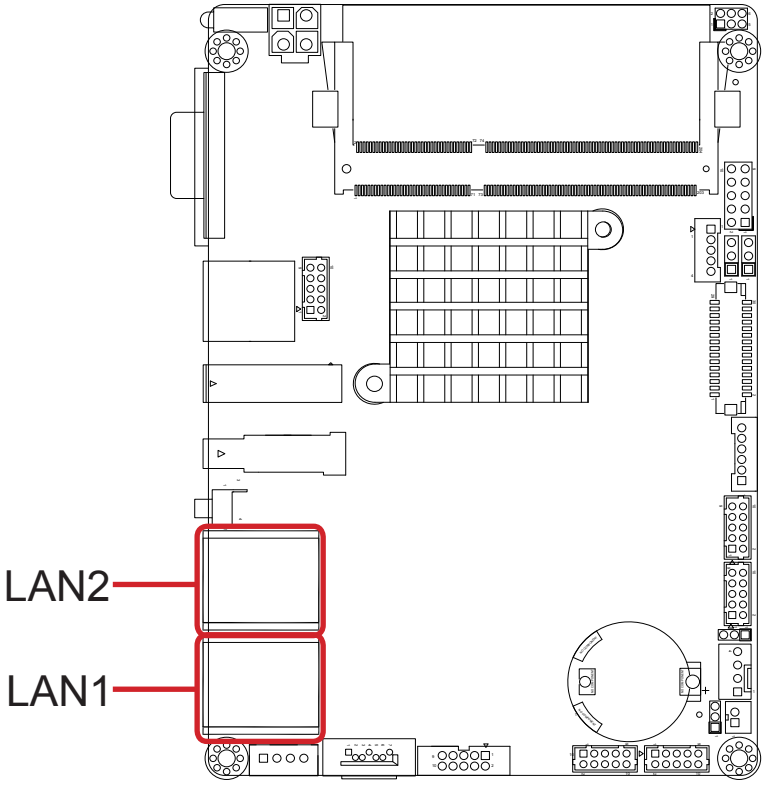
**Connector Type:** RJ-45 connector that supports 10/100/1000Mbps fast Ethernet

**Pin Assignment:**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | MDI0+ | 2 | MDI0- |
| 3 | MDI1+ | 4 | MDI1- |
| 5 | MDI2+ | 6 | MDI2- |
| 7 | MDI3+ | 8 | MDI3- |



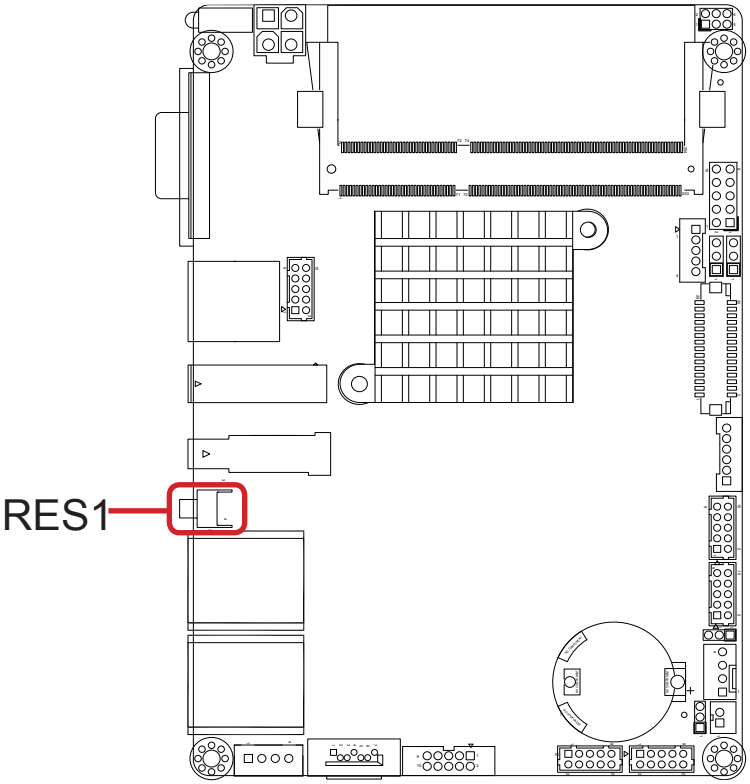

## Board Top



## RES1

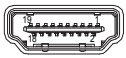
**Function:** Reset button

## Board Top

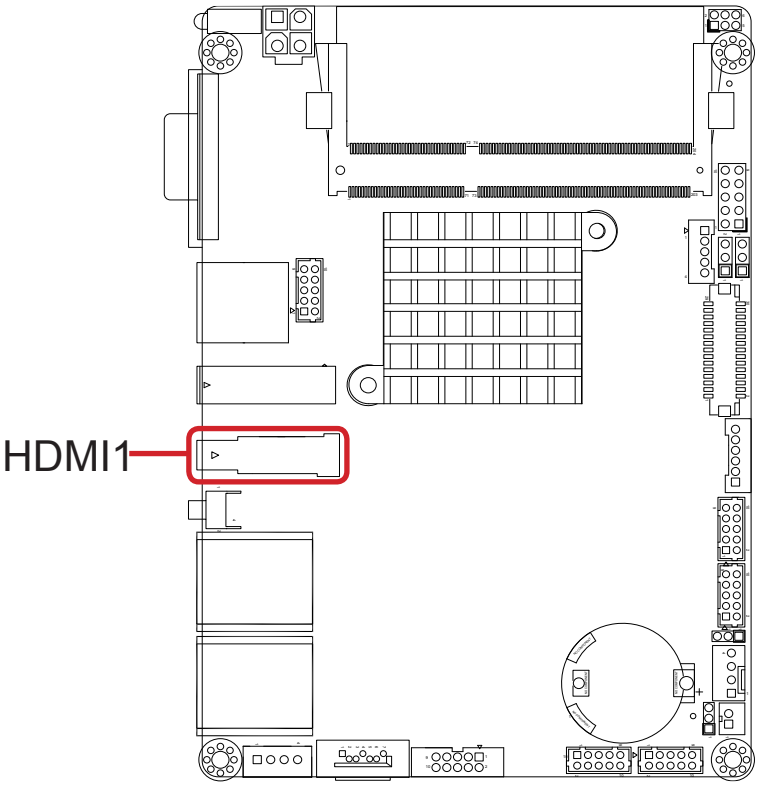


## HDMI1

| | |
|---|---|
| **Function:** | HDMI connector |
| **Connector Type:** | 19-pin HDMI connector with flange |
| **Pin Assignment:** | The pin assignments conform to the industry standard. |



## Board Top

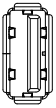


## USB2

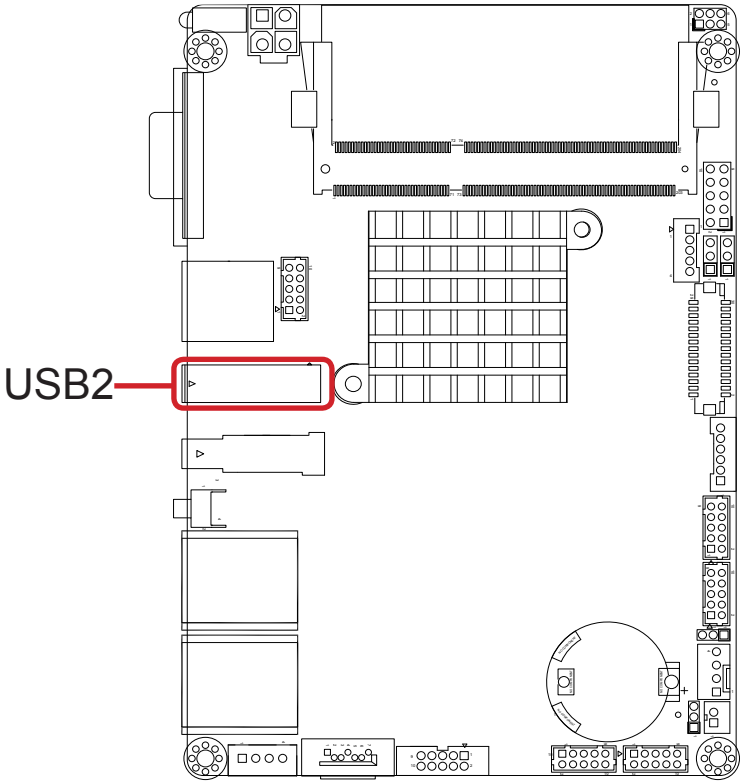
**Function:** USB 3.0 connector

**Connector Type:** USB 3.0/2.0 type-A connectors

**Pin Assignment:** The pin assignments conform to the industry standard.



## Board Top

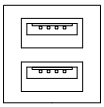


## USB3

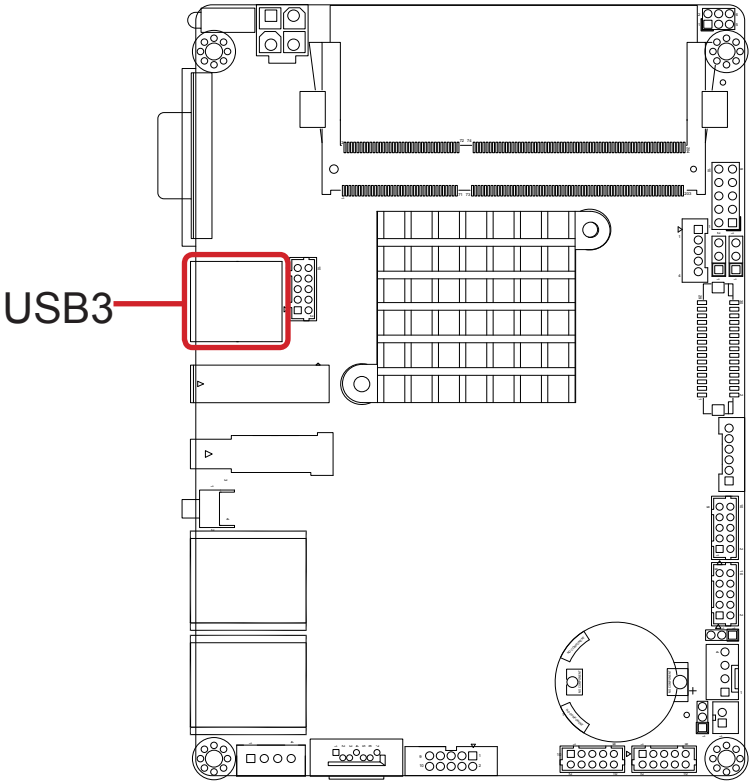
**Function:** Double-stacked USB connectors

**Connector Type:** Two USB 2.0/1.0 type-A connectors

**Pin Assignment:** The pin assignments conform to the industry standard.



## Board Top



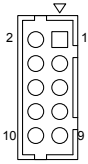
## USB1

**Function:** USB 2.0 connector

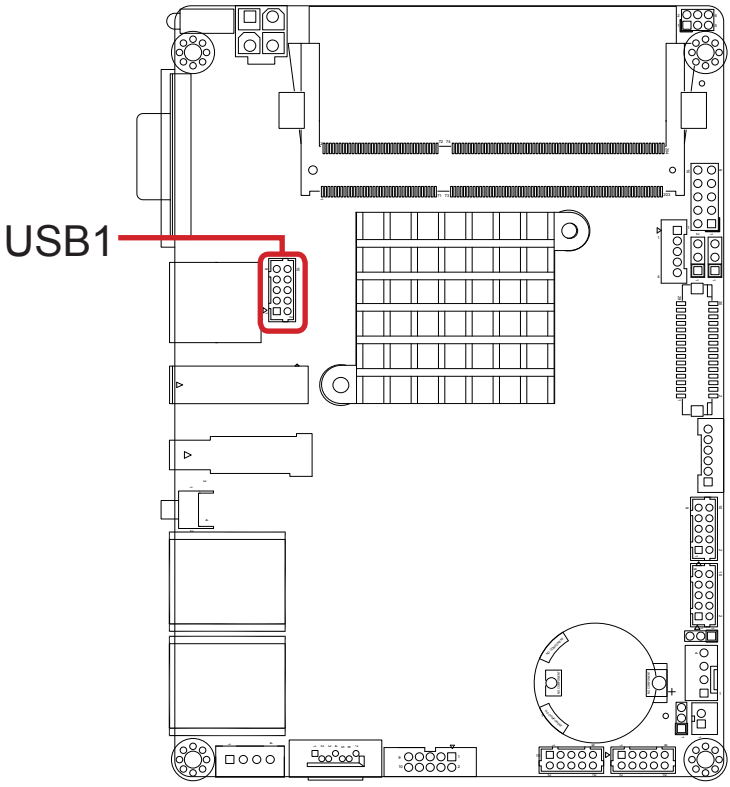
**Connector Type:** 2.00mm pitch 2x5-pin wafer connector

**Pin Assignment:**

| Pin | Description | Pin | Description |
|---|---|---|---|
| **2** | +5V- | **1** | +5V |
| **4** | USBP1- | **3** | USBP0- |
| **6** | USBP1+ | **5** | USBP0+ |
| **8** | GND | **7** | GND |
| **10** | GND | **9** | GND |




## Board Top



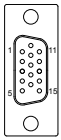
## VGA1

**Function:** Analog RGB connector

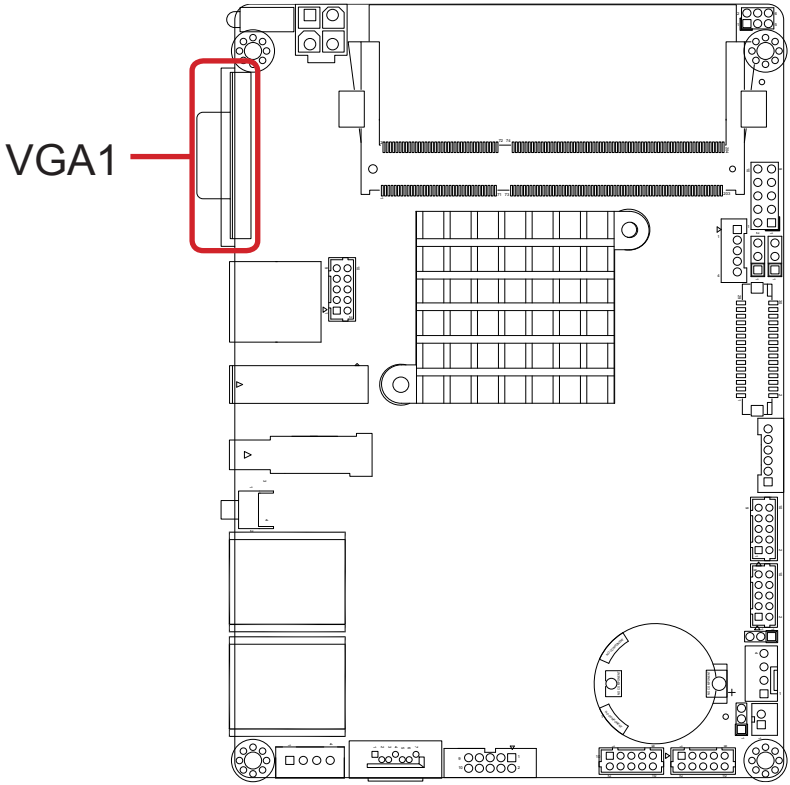
**Connector Type:** D-Sub 15-pin female connector

**Pin Assignment:**

| Pin | Description. | Pin | Description |
|---|---|---|---|
| **1** | RED | **9** | 5V |
| **2** | GREEN | **10** | GND |
| **3** | BLUE | **11** | N/C |
| **4** | N/C | **12** | D-DATA |
| **5** | GND | **13** | H-SYNC |
| **6** | GND | **14** | V-SYNC |
| **7** | GND | **15** | D-DCLK |
| **8** | GND | | |



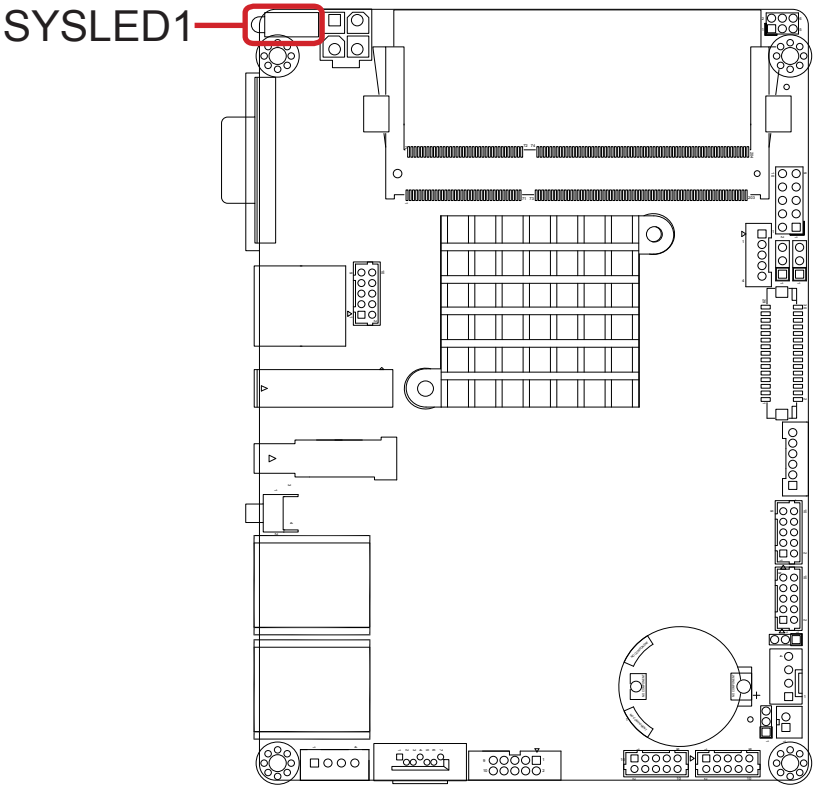
## Board Top



**SYSLED1:**

**Function:** Power ON & HDD LED Indicator

**Board Top**



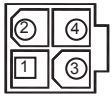
## 12VIN1

**Function:** Supplies ATX +12V

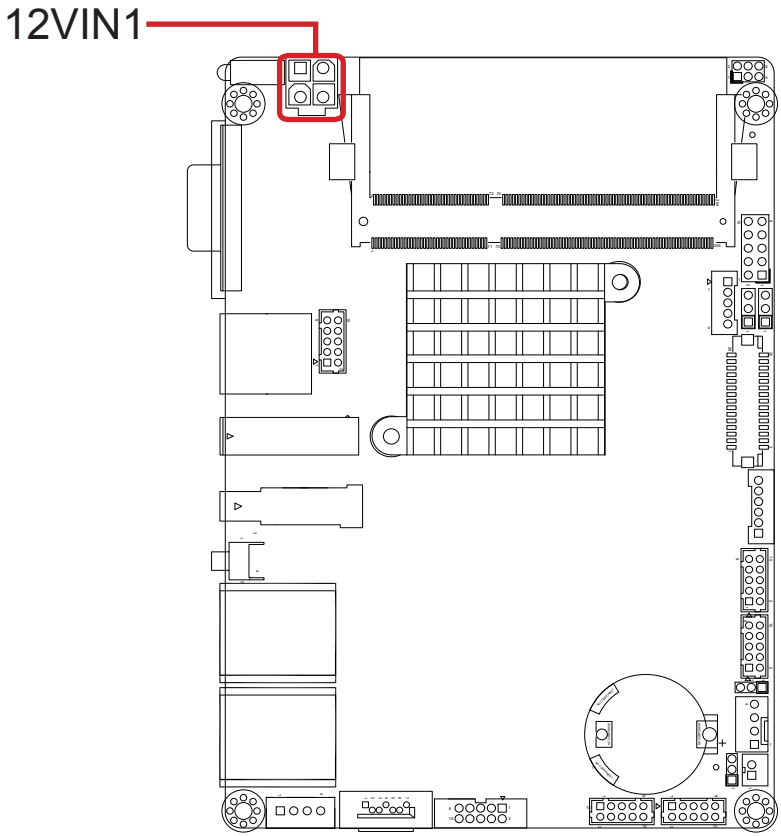
**Connector Type:** 4-pin power connector

**Pin Assignment:**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 2 | GND | 4 | +12V |
| 1 | GND | 3 | +12V |




## Board Top



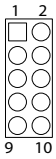
## JFRT1

**Function:** Provides connectors to front-panel status LED and toggles

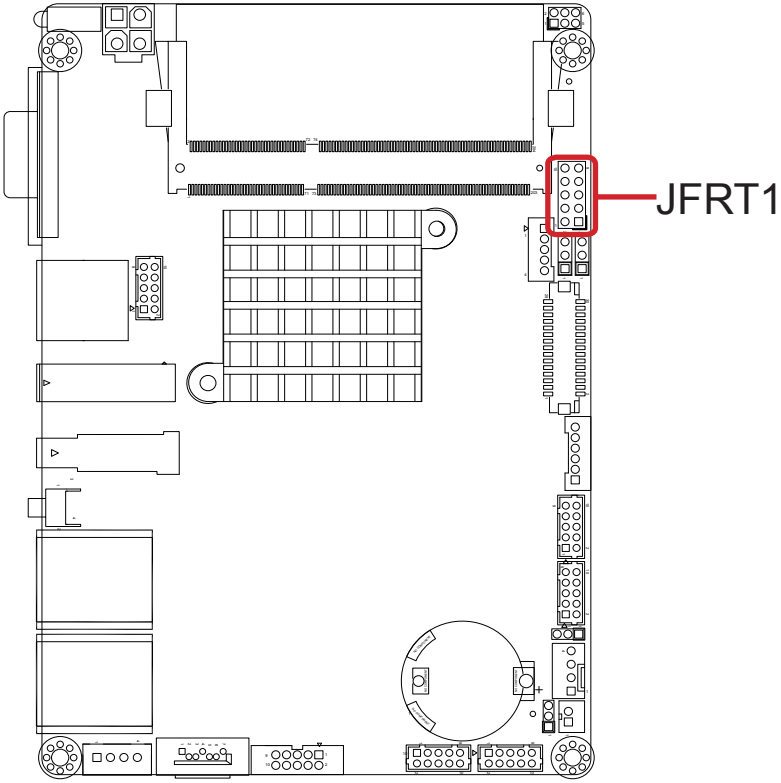
**Connector Type:** 2.54mm pitch 2x5-pin header

**Pin Assignment:**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | RESET+ | 2 | RESET- |
| 3 | PLED+ | 4 | PLED- |
| 5 | HLED+ | 6 | HLED- |
| 7 | SPEAK+ | 8 | SPEAK- |
| 9 | PSON+ | 10 | PSON- |



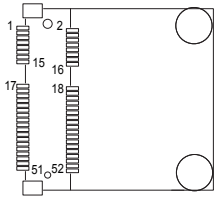

## Board Top



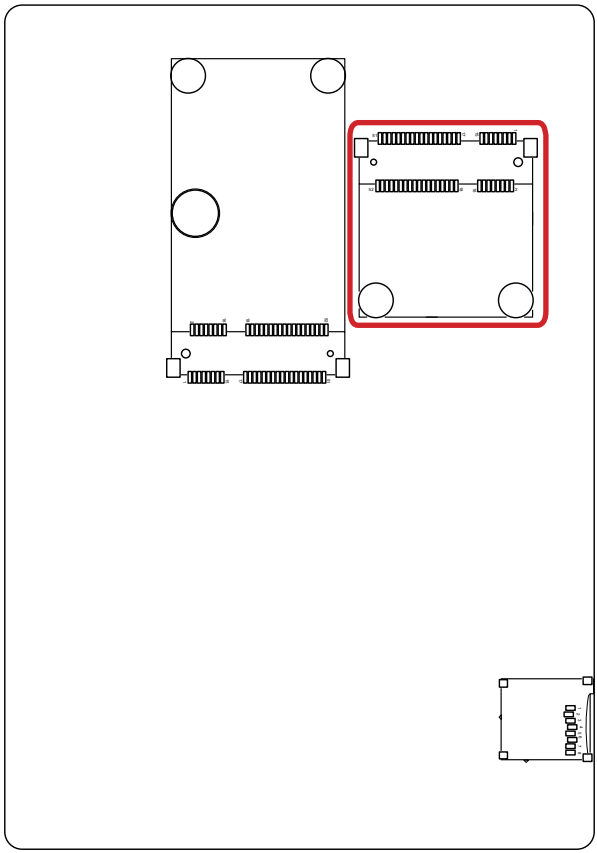
## MC1

**Function:** Mini-card socket

**Connector Type:** Onboard 0.8mm-pitch 52-pin edge card connector interconnected with SIM card socket.




## Board Bottom

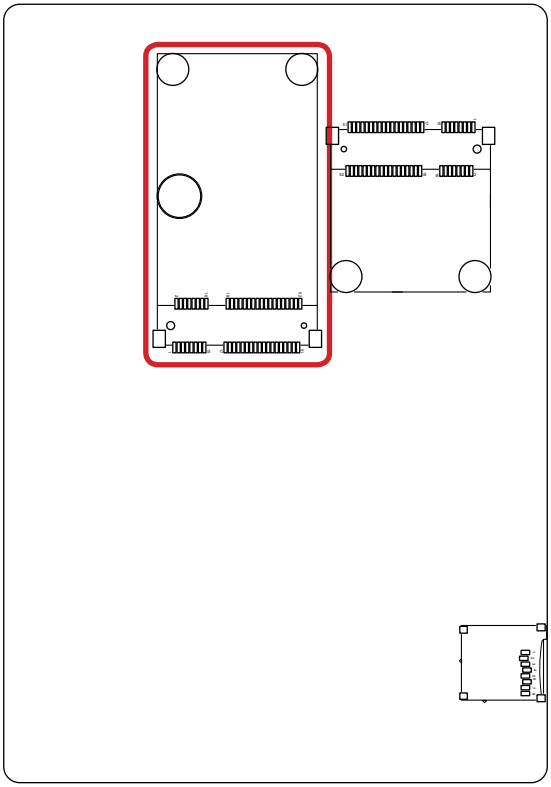


## mSATA1

**Function:** mSATA socket

**Connector Type:** Onboard 0.8mm pitch 52-pin edge card connector
The pin assignments conform to the industry standard.

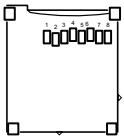

## Board Bottom



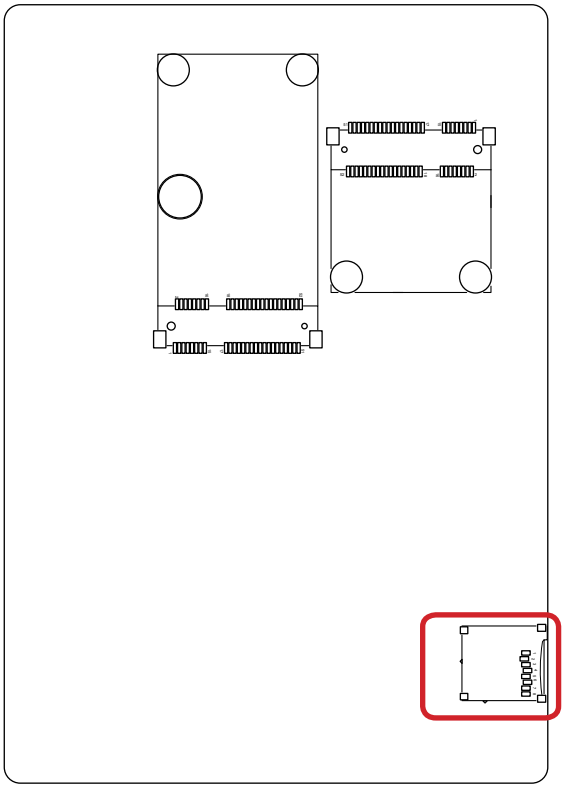
## SD1

**Function:** Micro SDXC card socket
(E3800 family only, supports SDXC card SD 3.0 only)

The pin assignments conform to the industry standard.



## Board Bottom



## 2.4. Driver Installation Notes

The board supports Windows 7 and Windows 8.1. Find the necessary drivers on the CD that comes with your purchase. For different OS, the driver/utility installation may vary slightly, but generally they are similar. **DO** follow the sequence below to install all drivers to prevent errors:

**Chipset→.NET Framework→Graphics→Audio→LAN→USB3.0**

Find the drivers on CD by the following paths:

### Windows 7

| Device | Driver Path |
|---|---|
| **Audio** | \Audio\32bit_Win7_Win8_Win81_R275 |
| | \Audio\64bit_Win7_Win8_Win81_R275 |
| **Chipset** | \Chipset\SetupChipset_10.0.13_PC |
| **Ethernet** | \Ethernet\Realtek\Win7\Install_Win7_7085_05222014 |
| **GPIO** | \GPIO\windows 7 32_64\Intel Atom E3800 Win7 IO Drivers_Gold_v1.0 package 501232_ 20140211 |
| **Graphic** | \Graphics\WIN7_32\Intel_EMGD.WIN7_PC_Version_36_15_0_1073 |
| | \Graphics\WIN7_64\Intel_EMGD.WIN7_PC_Version_37_15_0_1073 |
| **TXE** | \TXE\Installers (Only for 64-bit) |
| **USB3.0** | \USB3.0\Intel(R) USB 3.0 eXtensible Host Controller_Win7_32bit_64bit_R3.0.0.33 |
| **Serial IO** | \Serial IO\Intel Processor IO Drivers_Win7_32bit_64bit_Gold_v2.0 |

### Windows 8.1

| Device | Driver Path |
|---|---|
| **Audio** | \Audio\32bit_Win7_Win8_Win81_R275 |
| | \Audio\64bit_Win7_Win8_Win81_R275 |
| **Chipset** | \Chipset\SetupChipset_10.0.13_PC |
| **Ethernet** | \Ethernet\Realtek\Win8_8.1\Install_Win8_8.1_8031_05222014 |
| **GPIO** | \GPIO\Kit 100882 20140211 windows 8.1 64\GPIO(Only for 64-bit) |
| **Graphic** | \Graphics\WIN8_32\15.33.22.3621 |
| | \Graphics\WIN8_64\15.33.22.64.3621 |
| **TXE** | \TXE\Installers |
| **Serial IO** | \Serial IO\SerialIO_Installer_Win8.1_64bit_WW23 |

# Chapter 3

# BIOS

The BIOS Setup utility is featured by AMI BIOS to configure the system settings stored in the system's BIOS ROM. AMI BIOS is activated once the computer powers on.

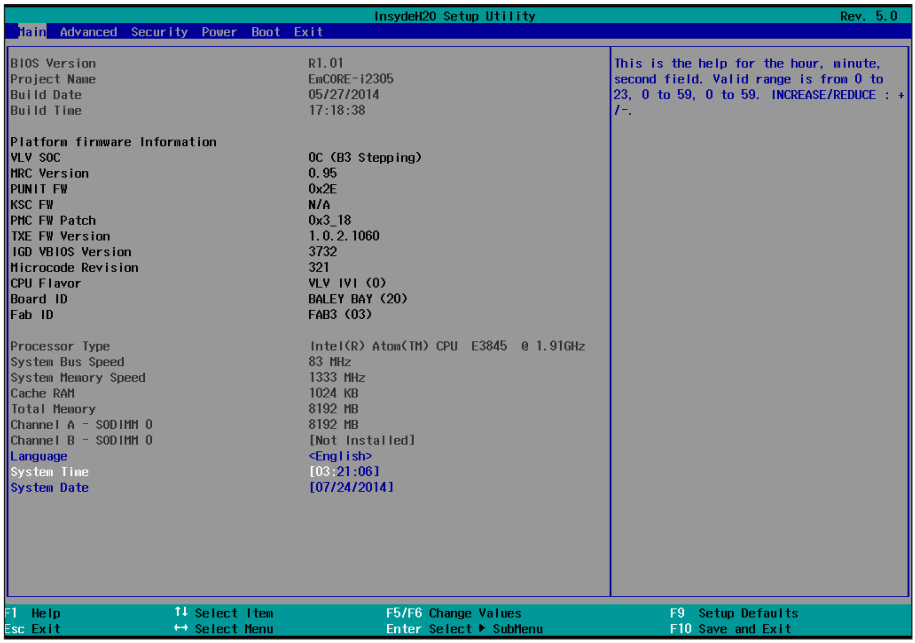
After entering the utility, use the left/right arrow keys to navigate between the top menus and use the down arrow key to access one.

| Menu | Description |
|---|---|
| **Main** | See 3.1. Main on page 43. |
| **Advanced** | See 3.2. Advanced on page 44. |
| **Security** | See 3.3. Security on page 49. |
| **Power** | See 3.4. Power on page 53. |
| **Boot** | See 3.5. Boot on page 53. |
| **Exit** | See 3.6. Exit on page 55. |

NOTE: For system stability and performance, this BIOS utility is constantly improved. The screenshots demonstrated and descriptions hereinafter are for reference only and may not exactly meet what is presented onscreen.

## 3.1. Main

The **Main** menu displays some BIOS info and features the settings of **System Date** and **System Time**.




The BIOS info displayed is:

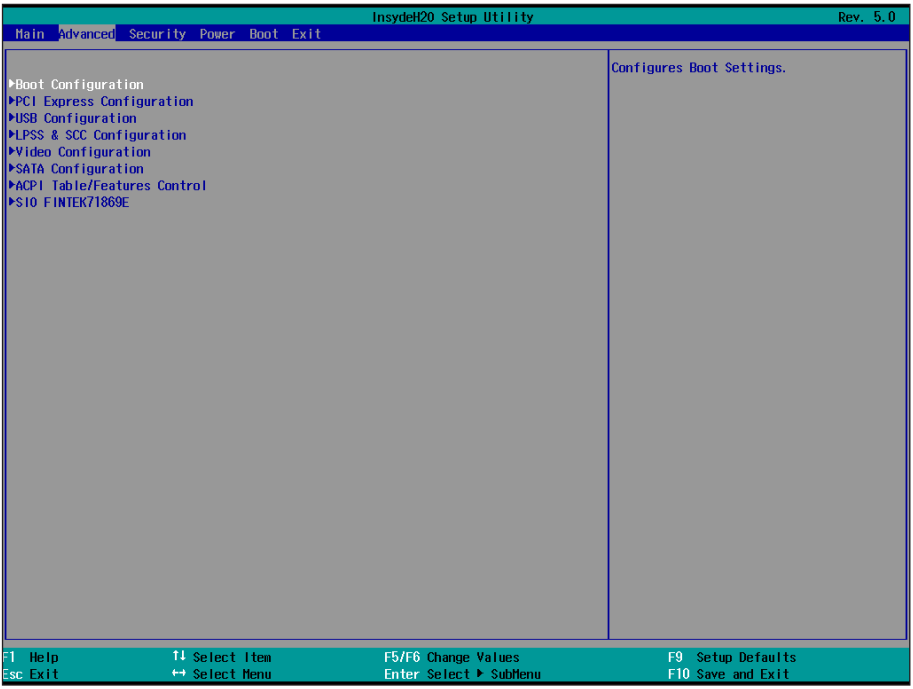
| Info Item | Description |
|---|---|
| **BIOS Version** | Delivers the computer's BIOS version. |
| **Project name** | Delivers the name of the project |
| **Build Date and Time** | Delivers the date and time when the BIOS Setup utility was created/ updated. |
| **Platform firmware Information** | Delivers the Platform firmware Information |

The featured settings are:

| Setting | Description |
|---|---|
| **Language** | Select the current default language used by the InsydeH20 |
| **System Time** | Sets system time. |
| **System Date** | Sets system date. |

## 3.2. Advanced

The **Advanced** menu controls the system's CPU, IDE, Super IO, AHCI and USB. It also helps users monitor hardware health.




The featured submenus are:

| Submenu | Description |
|---|---|
| **Boot Configuration** | See 3.2.1. Boot Configuration on page 45. |
| **PCI Express Configuration** | See 3.2.2. PCI Express Configuration on page 45. |
| **USB Configuration** | See 3.2.3. USB Configuration on page 45. |
| **LPSS & SCC Configuration** | See 3.2.4. LPSS & SCC Configuration on page 46. |
| **Video Configuration** | See 3.2.5. Video Configuration on page 46. |
| **SATA Configuration** | See 3.2.6. SATA Configuration on page 46. |
| **ACPI Table/Feature Control** | See 3.2.7 ACPI Table/Feature Control on page 47. |
| **SIO FINTEK71869E** | See 3.2.8. SIO FINTEK71869E on page 48. |

### 3.2.1. Boot Configuration

| Setting | Description |
|---|---|
| Numlock | Select Power-on state for Num lock |

### 3.2.2. PCI Express Configuration

Configures PCI Express by the following settings:

| Setting | Description |
|---|---|
| PCI Express Root Port 1/2/3/4 | ▸ PCI Express Root Port<br>Enables/disables this PCIe port.<br>▸ PCIe Speed<br>Options are: Auto, Gen 1, Gen 2<br>Auto is the default.<br>▸ ASPM Support<br>Options are:<br>Disable : disables ASPM<br>L0s : force all links to L0s state<br>L1 : force all links to L1 state<br>L0sL1 : force all links to L0s+L1 state<br>Auto : BIOS auto configure |

### 3.2.3. USB Configuration

Select this submenu to view the status of the USB ports and configure USB features.

The featured settings are:

| Setting | Description |
|---|---|
| XHCI Pre-Boot Mode Support | Enables/Disables XHCI Pre-Boot mode support |
| xHCI Mode | Set the mode of operation of xHCI controller<br>Options are Disabled/Enabled/Auto/Smart Auto(default) |
| XCHI Controller | Enables/Disables XHCI controller |
| USB2 Link Power Management | Enables/Disables USB2 Link Power Management. |
| XCHI Streams | Enables/disables XHCI Stream |
| USB OTG Support | Enables/disables USB OTG Support |
| USB VBUS | Turn ON/OFF USB VBUS. Turn ON in HOST mode, and turn OFF in OTG device mode. |
| USB RMH Mode | Enables/disables USB RMH Mode |
| USB ECHI debug | Enables/disables USB ECHI debug |
| USB Per-Port Control | Enables/Disables USB Per-port control |

### 3.2.4. LPSS & SCC Configuration

The featured settings are:

| Setting | Description |
|---|---|
| **OS Selection** | Set the mode of OS Selection<br>Options are Windows(default)/Android |
| **SCC eMMC Boot Controller** | Set the mode of eMMC Boot mode<br>Options are Disable/ Auto Detect(Default)/ eMMC 4.41/ eMMC 4.5 |

**Warning:** Windows 7 does not include any driver support for eMMC devices. If you select Windows 7 as your OS selection in BIOS, the eMMC device is disabled and grayed out.

### 3.2.5. Video Configuration

Configure video settings

The featured setting is:

3.2.5.1 PTN3460 (eDP to LVDS) Configuration

| Setting | Description |
|---|---|
| **PTN3460 Output Format** | Set the Output Format of PTN3460.<br>Options are (00) VESA (24bpp) / (01) VESA or JEIDA (18bpp) / (10) JEIDA (24bpp) / (11) JEIDA (24bpp) |
| **PTN3460 Channel Control** | Set the Channel of PTN3460.<br>Options are Single(default), Dual. |
| **PTN3460 EDID Table** | Set the EDID Table of PTN3460. |

3.2.5.2 IGD- LCD Control

| Setting | Description |
|---|---|
| **GMCH BLC Control** | Set the mode of GMCH BLC Control<br>Options are Auto(default) / PWM-Inverted |

### 3.2.6. SATA Configuration

Select this submenu to configure the SATA controller and HD.

| Setting | Description |
|---|---|
| **SATA Controller(s)** | Enables/disables the present SATA controller.<br>▸ **Enabled** is the default. |
| **SATA Test Mode** | Enables/disables the SATA test mode. |
| **Configures SATA Mode** | Configures how to sun the SATA drives.<br>▸ Options available are **AHCI** (default) and **IDE**. |
| **SATA Port 0 Hot Plug Capability** | Enables/disables hot-pluggable feature for the SATA port.<br>▸ **Enabled** is the default. |
| **SATA Port 1 Hot Plug Capability** | |
| **SATA Port 0 Connect to an ODD** | Enables/disables the SATA port connect to an ODD<br>If enabled, when you connect an ODD to a SATA port. The software auto detection for media insert and tray will be enabled.<br>▸ **Disabled** is the default. |
| **SATA Port 1 Connect to an ODD** | |
| **Serial ATA Port 0** | Delivers the SATA port Media information and Security Mode. |
| **Serial ATA Port 1** | |

### 3.2.7 ACPI Table/Feature Control

| Setting | Description |
|---|---|
| **FACP - RTC S4 Wakeup** | This function will be avalible only when ACPI is enabled.<br>Enables/disables S4 Wakup from RTC. |
| **APIC - IO APIC Mode** | This item is valid only for WIN2K and WINXP. Also, a frech install of the OS must occur when APIC mode is desired.<br>Enables/disables the APIC mode |
| **DSDT - ACPI S3** | Enables/disables ACPI S3 state |
| **DSDT - ACPI S4** | Enables/disables ACPI S4 state |
| **BGRT - ACPI BGRT** | Enables/disables ACPI BGRT Table |

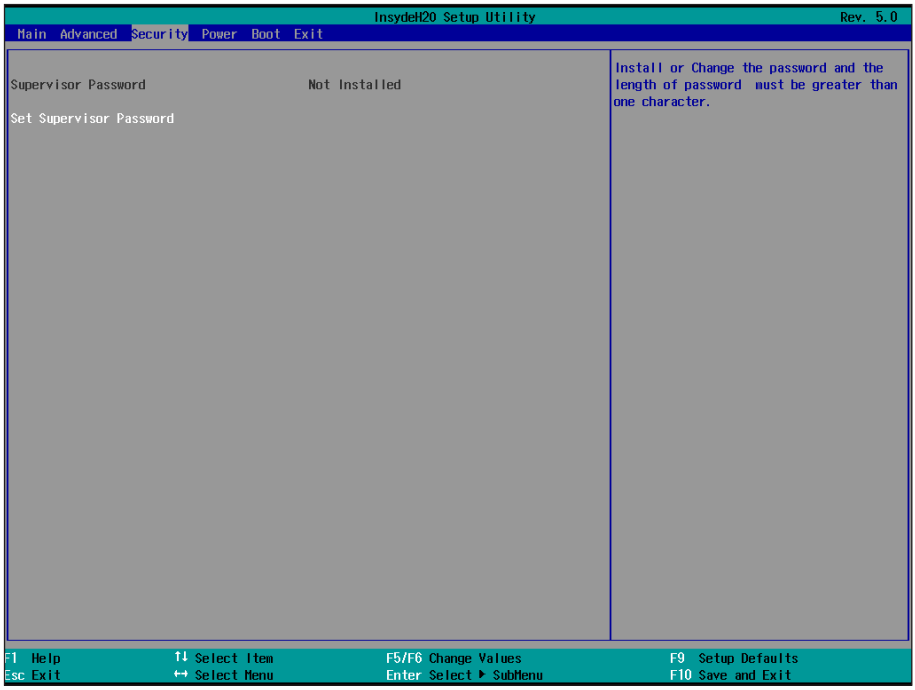
### 3.2.8. SIO FINTEK71869E

Configures SIO by the following settings:

| Setting | Description |
|---|---|
| **Power Loss mode** | Set the state of Power Loss mode<br>Options are Keep last state/ Bypass mode/ Always On(default)/Always Off |
| **Serial Port A** | ▸ Serial Port A<br>Enables/disables the Serial port.<br>▸ Base I/O Address<br>Setup the Base I/O Address of the Serial Port.<br>▸ Interrupt<br>Setup the Interrupt of the Serial Port |
| **Serial Port B** | ▸ Serial Port B<br>Enables/disables the Serial port.<br>▸ RS-232/RS-485 Setting<br>Set the mode of Serial port. Options are RS232 (default), RS485<br>▸ Base I/O Address<br>Setup the Base I/O Address of the Serial Port.<br>▸ Interrupt<br>Setup the Interrupt of the Serial Port |

## 3.3. Security

The **Security** menu sets up the password for the system's administrator account. Once the administrator password is set up, this BIOS Setup utility is limited to access and will ask for the password each time any access is attempted.

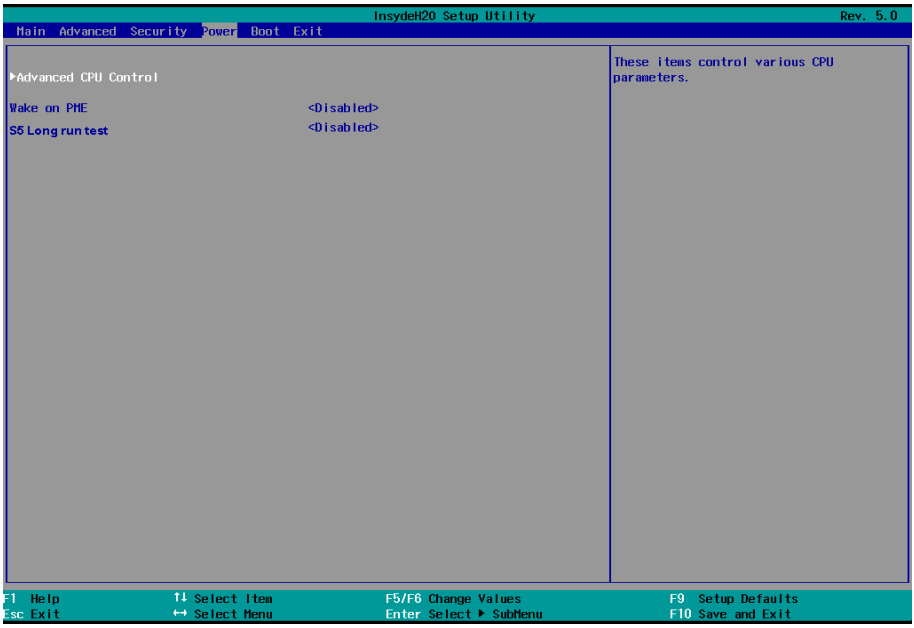



The featured setting is:

| Setting | Description |
|---|---|
| **Set Supervisor Password** | To set up an administrator password:<br>1. Select **Set Supervisor Password**. An **Create New Password** dialog then pops up onscreen.<br>2. Enter your desired password that is no less than 3 characters and no more than 20 characters.<br>3. Hit [Enter] key to submit. |

## 3.4. Power

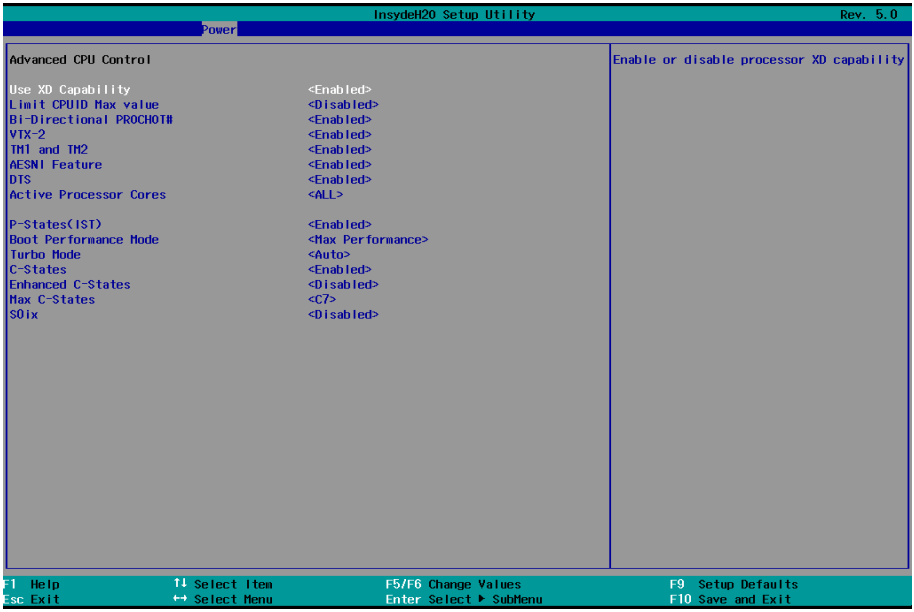
The **Power** menu sets up the power option of system




The featured setting is:

| Setting | Description |
|---|---|
| **Advanced CPU Control** | See 3.4.1 Advanced CPU Control on page 51. |
| **Wake on PME** | Enables or diables Wake on PME.<br>Determines the action taken when the system power is off and a PCI Power Management Enable wake up event occurs. |
| **S5 Long run test** | If enabled, force the system to enable RTC S5 wake up, even if OS disable it. Support ipwrtest to do RTC S5 wakeup.<br>Options are Enabled/Disabled. |

### 3.4.1 Advanced CPU Control

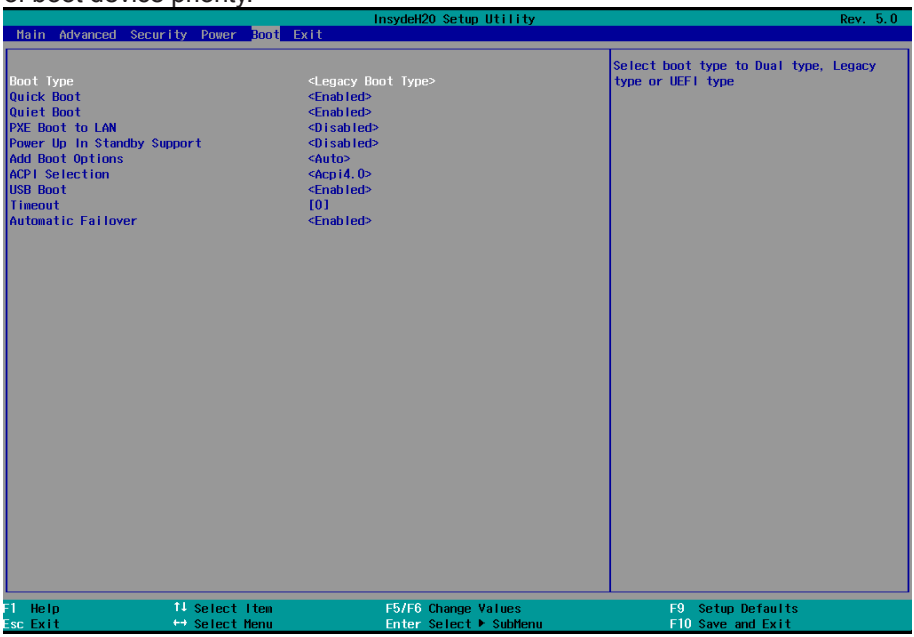



| Setting | Description |
|---|---|
| **Use XD Capability** | Enables or disables processor XD capability. |
| **Limit CPUID Max value** | Sets whether the processor should limit the maximum CPUID input value to 03h when the operating system queries it upon startup.<br>▸ Select **Enabled** to allow a processor with Intel® Hyper-Threading technology to work with an operating system that doesn't support it.<br>▸ **Disabled** is the default. |
| **Bi-Directional PROCHOT#** | When a processor thermal sensor trips(either core), the PROCHOT# will be driven. If Bi-Directional is enable, external agents can drive PROCHOT# to throttle. |
| **VTX-2** | Enables/disables the CPU's VTX-2 function. |
| **TM1 and TM2** | Enable/disables TM1/TM2 |
| **AESNI Feature** | Enable/disables AESNI |
| **DTS** | Enable/disables CPU Digital Thermal Sensor function. |
| **Active Processor Cores** | Set the Number of cores to enable in each processor package. Options are ALL/1 |
| **P-States(IST)** | Enables/disables processor performance states (P-States) |

| | |
|---|---|
| **Boot Performance Mode** | Select the performance state that BIOS will set before OS handoff |
| **Turbo Mode** | Enables/disables processor Turbo mode (EMTTM enabled is required) |
| **C-States** | Enables/disables processor idle power saving states (C-states) |
| **Enhanced C-States** | Enables/disables P-state transitions to occur in combination with C-states. |
| **Max C-States** | Set the Max CPC state C7/C6/C1 |
| **S0ix** | Enables/disables the platform to configure S0ix support. |

## 3.5. Boot

The **Boot** menu configures how to boot up the system such as the configuration of boot device priority.



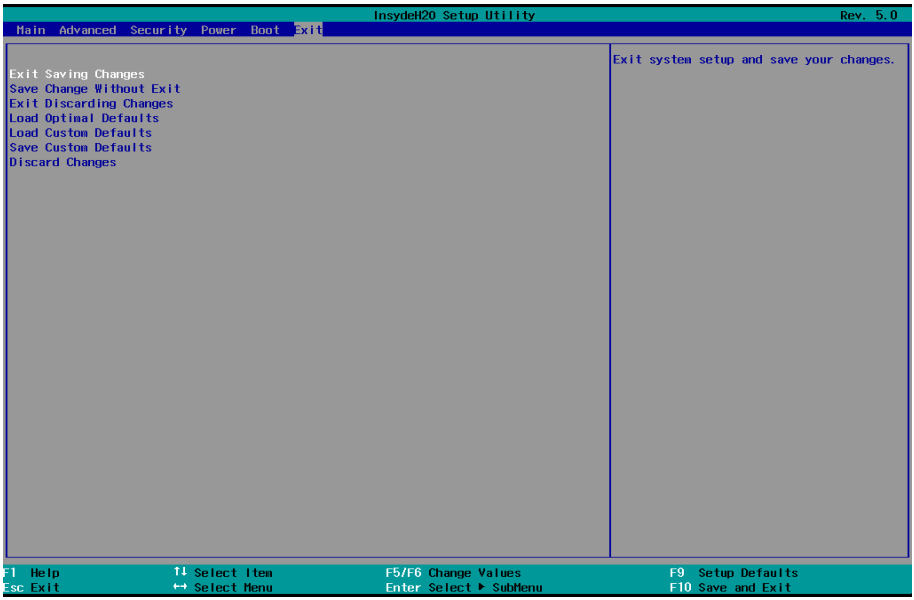

The featured settings are:

| Setting | Description |
|---|---|
| **Quick Boot** | Allow InsydeH20 to Skip certain tests while booting . This will descrese the time need to boot the system. |
| **Quiet Boot** | Disables or enables booting in text mode. |
| **PXE boot to LAN** | Disables or enables PXE boot to LAN. |
| **Power Up In Standby Support** | Disable or enable Power Up In Standby Support. |
| **Add Boot Option** | Position in Boot Order for Shell, Network and Removables. Options are First, Last, and Auto. |
| **APCI Selection** | Select boot to Acpi 3.0/Acpi 1.0B<br>Options are Acpi 1.0B/Acpi 3.0/Acpi 4.0/Acpi 5.0 |

| | |
|---|---|
| **USB Boot** | Disables or enables booting to USB boot devices. |
| **Timeout** | Set the waiting seconds before booting the default boot selection |
| **Automatic Failover** | Enables/disables the Automatic Failover. |

## 3.6. Exit

The **Save & Exit** menu features a handful of commands to launch actions from the BIOS Setup utility regarding saving changes, quitting the utility and recovering defaults.




The features settings are:

| Setting | Description |
|---|---|
| **Exit Saving Changes** | Saves the changes and quits the BIOS Setup utility. |
| **Save Changes Without Exit** | Save Changes but does not quit the BIOS. |
| **Exit Discard Changes** | Quits the BIOS Setup utility without saving the change(s). |
| **Load Optimal Defaults** | Restores all settings to defaults.<br>▶ This is a command to launch an action from the BIOS Setup utility rather than a setting. |
| **Load Custom Default** | Load custome default values |
| **Save Custom Default** | Save current setting as custome default |
| **Discard Changes** | Discard all changes without Exit. |

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# Appendices

## Appendix A. Watchdog Timer (WDT) Setting

The application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT timeout, the functional normal system will reload the WDT. The WDT never time-out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time-out and auto-reset the system to avoid abnormal operation.

This computer supports 255 levels watchdog timer by software programming I/O ports.

Below is an program example to disable and load WDT.

**Sample Codes:**

```
/*-----  Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

unsigned char sioIndex  = 0x2E;                                  /* or index = 0x4E */
unsigned char sioData   = 0x2F;                                  /* or data  = 0x4F */

/*-----  routing, sub-routing -----*/
void main()
{
        outportb(sioIndex, 0x87);                                /* Enable Super I/O */
        outportb(sioIndex, 0x87);

        outportb(sioIndex, 0x07);                                /* Select logic device
- WDT */
        outportb(sioData,  0x07);

        outportb(sioIndex, 0x30);                                /* Enable WDT */
        outportb(sioData,  0x01);

        outportb(sioIndex, 0xF0);                                /*   Enable   WDTRST#
Output */
        outportb(sioData,  0x80);

        outportb(sioIndex, 0xF6);                                /*  Set  WDT  Timeout
value */
        outportb(sioData,  0x05);

        outportb(sioIndex, 0xF5);                                /*  Set  Configure  and
Enable WDT timer, Start countdown */
        outportb(sioData,  0x32);

        outportb(sioIndex, 0xAA);                                /* SIO - Disable */
}
```

## Appendix B. Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 6Eh.

```
/*-----        Include Header Area -----*/
#include “math.h”
#include “stdio.h”
#include “dos.h”

#define     sioIndex                    0x2E                    /* or 0x4E */
#define     sioData                     0x2F                    /* or 0x4F */

/*-----        routing, sub-routing -----*/
void main()
{
   int iData;

   SioGPIOMode(0x0F);
   delay(2000);

    SioGPIOData(0x05);
    delay(2000);

   iData = SioGPIOStatus();
   printf(“ Input : %2x \n”,iData);
   delay(2000);

    SioGPIOData(0x0A);
    delay(2000);

   iData = SioGPIOStatus();
   printf(“ Input : %2x \n”,iData);
   delay(2000);
}

void SioGPIOMode(int iMode)
{
   outportb(sioIndex,0x87);                                 /* Enable Super I/O */
   outportb(sioIndex,0x87);

   outportb(sioIndex,0x07);                                 /* Select logic device – GPIO */
   outportb(sioData, 0x06);

   outportb(sioIndex,0x30);                                 /* Enable GPIO */
   outportb(sioData, 0x01);

   outportb(sioIndex,0xC0);                                 /* GPIO3 0~7 - Output Enable */
   outportb(sioData,iMode);

    outportb(sioIndex,0xAA);                                /* Disable Super I/O */
```

```
}


void SioGPIOData(int iData)
{
   outportb(sioIndex,0x87);                    /* Enable Super I/O */
   outportb(sioIndex,0x87);

   outportb(sioIndex,0x07);                    /* Select logic device – GPIO */
   outportb(sioData, 0x06);

   outportb(sioIndex,0xC1);                    /* GPIO3 0~7 - Output Data */
   outportb(sioData,iData);

    outportb(sioIndex,0xAA);                   /* Disable Super I/O */
}


int SioGPIOStatus()
{
    int iStatus;

   outportb(sioIndex,0x87);                    /* Enable Super I/O */
   outportb(sioIndex,0x87);

   outportb(sioIndex,0x07);                    /* Select logic device – GPIO */
   outportb(sioData, 0x06);

    outportb(sioIndex,0xC2);                   /* GPIO3 0~7 - Status */
   iStatus = inportb(sioData);

    outportb(sioIndex,0xAA);                   /* Disable Super I/O */

    return iStatus;
}
```