



### DESCRIPTION

The EVQ6615-QK-00A is an evaluation board designed to demonstrate the capabilities of the MPQ6615-AEC1, an H-bridge DC motor driver.

The MPQ6615-AEC1 operates from an input voltage ( $V_{IN}$ ) up to 40V. The H-bridge consists of four N-channel power MOSFETs. The internal charge pump generates the gate driver supply voltages for the high-side MOSFETs (HS-FETs), and a trickle charge circuit maintains sufficient gate driver voltages for 100% duty cycle operation.

The current flowing through the two  $S_x$  outputs is sensed by the internal current-sensing circuits. Each phase has an output pin ( $S_{Ox}$ ) that sources or sinks a current proportional to each phase's output current ( $I_{OUT}$ ). Only the

current flowing through the low-side MOSFET (LS-FET) is sensed. This current is sensed in both the forward and reverse directions.

Internal safety features include over-current protection (OCP), under-voltage lockout (UVLO) protection, and thermal shutdown.

The input control signals for the MPQ6615-AEC1 are applied through the connector on the board.

The MPQ6615-AEC1 is designed to drive brushed DC motors, door lock and latch motors, and seat actuators. The MPQ6615-AEC1 is available in a TQFN-26 (6mmx6mm) package with wettable flanks, and it is AEC-Q100 qualified.

### PERFORMANCE SUMMARY

Specifications are at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Parameters	Conditions	Value
Input power voltage ( $V_{IN}$ ) range		4.75V to 40V
Maximum continuous output current ( $I_{OUT}$ )		8A
VREF voltage ( $V_{REF}$ )		3.3V or 5V

## EVQ6615-QK-00A EVALUATION BOARD



LxWxH (5.08cmx5.08cmx4.2cm)

Board Number	MPS IC Number
EVQ6615-QK-00A	MPQ6615GQKTE-AEC1

## QUICK START GUIDE

The EVQ6615-QK-00A evaluation board is easy to set up and use to evaluate the performance of the MPQ6615-AEC1. For proper measurement equipment set-up, refer to Figure 1 on page 4 and follow the steps below:

1. Connect the input voltage ( $4.75V \leq V_{IN} \leq 40V$ ) and input ground to the VIN and VIN\_GND connectors, respectively.
2. Connect the 3P3 voltage ( $V_{3P3} = 3.3V$  or  $5V$ ) and input ground to the 3P3 and 3P3\_GND connectors, respectively.
3. Set the SW1 pin to position 1 (top side) to enable the chip.
4. To set the current-sense output reference voltage, connect the VREF voltage ( $V_{REF} = 3.3V$  or  $5V$ ) and input ground to the VREF connector and VREF\_GND connectors, respectively.
5. Select the over-current protection (OCP) mode and input mode via the SW2 pin (see Table 1).

**Table 1: Selecting the OCP Mode (Set via SW2)**

OCMD	OCP Mode
Open or drive logic high	Retry
GND	Latch off

6. Set the input mode via SW3 and SW4 (see Table 2, Table 3, and Table 4).

**Table 2: Input Logic for INM[1:0] = 00 (Set via SW3 and SW4)**

ENx	PWMx	Sx
High	High	$V_{IN}$
High	Low	GND
Low	High or low	Hi-Z

**Table 3: Input Logic for INM[1:0] = 01 (Set via SW3 and SW4)**

ENBL	DIR	BRK	BMOD	SA	SB
Low	High or low	High or low	High or low	Hi-Z	Hi-Z
High	High or low	High	Low	GND	GND
High	High or low	High	High	$V_{IN}$	$V_{IN}$
High	Low	Low	High or low	GND	$V_{IN}$
High	High	Low	High or low	$V_{IN}$	GND

**Table 4: Input Logic for INM[1:0] = 10 (Set via SW3 and SW4)**

INHx	INLx	Sx
Low	Low	Hi-Z
Low	High	GND
High	Low	$V_{IN}$
High	High	Hi-Z

7. Attach the input control signals generated by the external controller to the ENx and PWMx connectors.

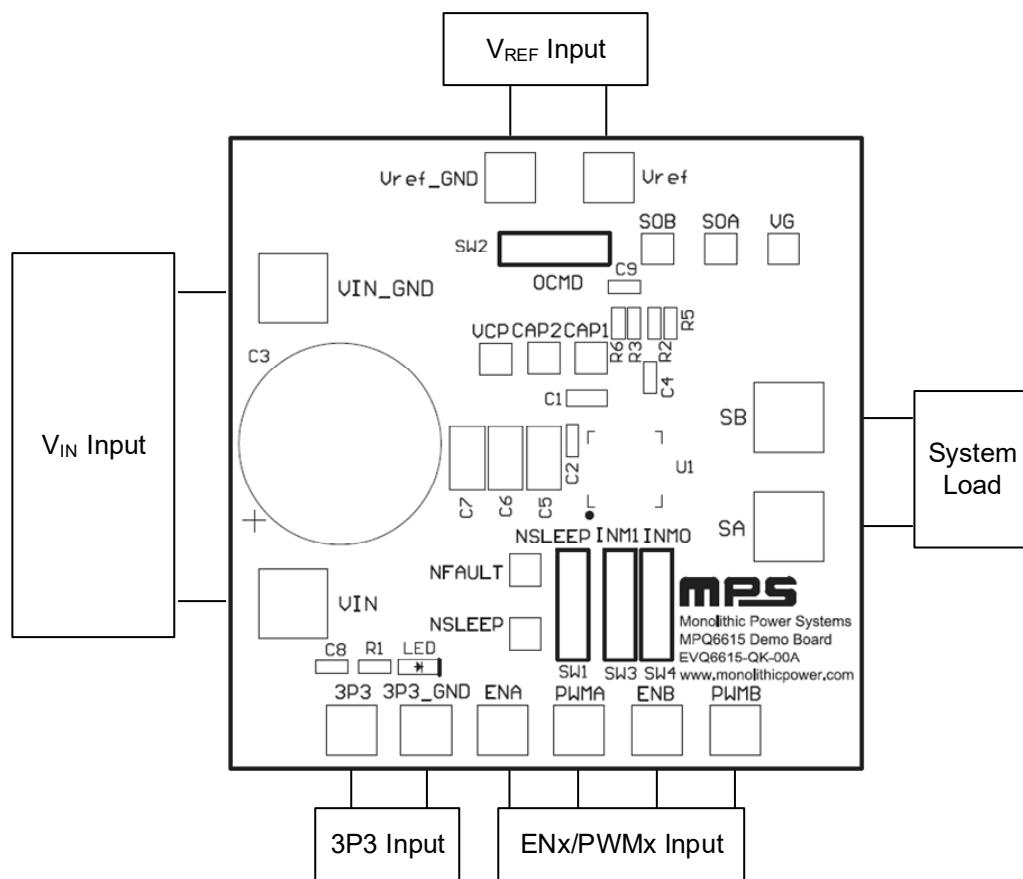


Figure 1: Measurement Equipment Set-Up for the MPQ6615GQKTE-AEC1

## EVALUATION BOARD SCHEMATIC

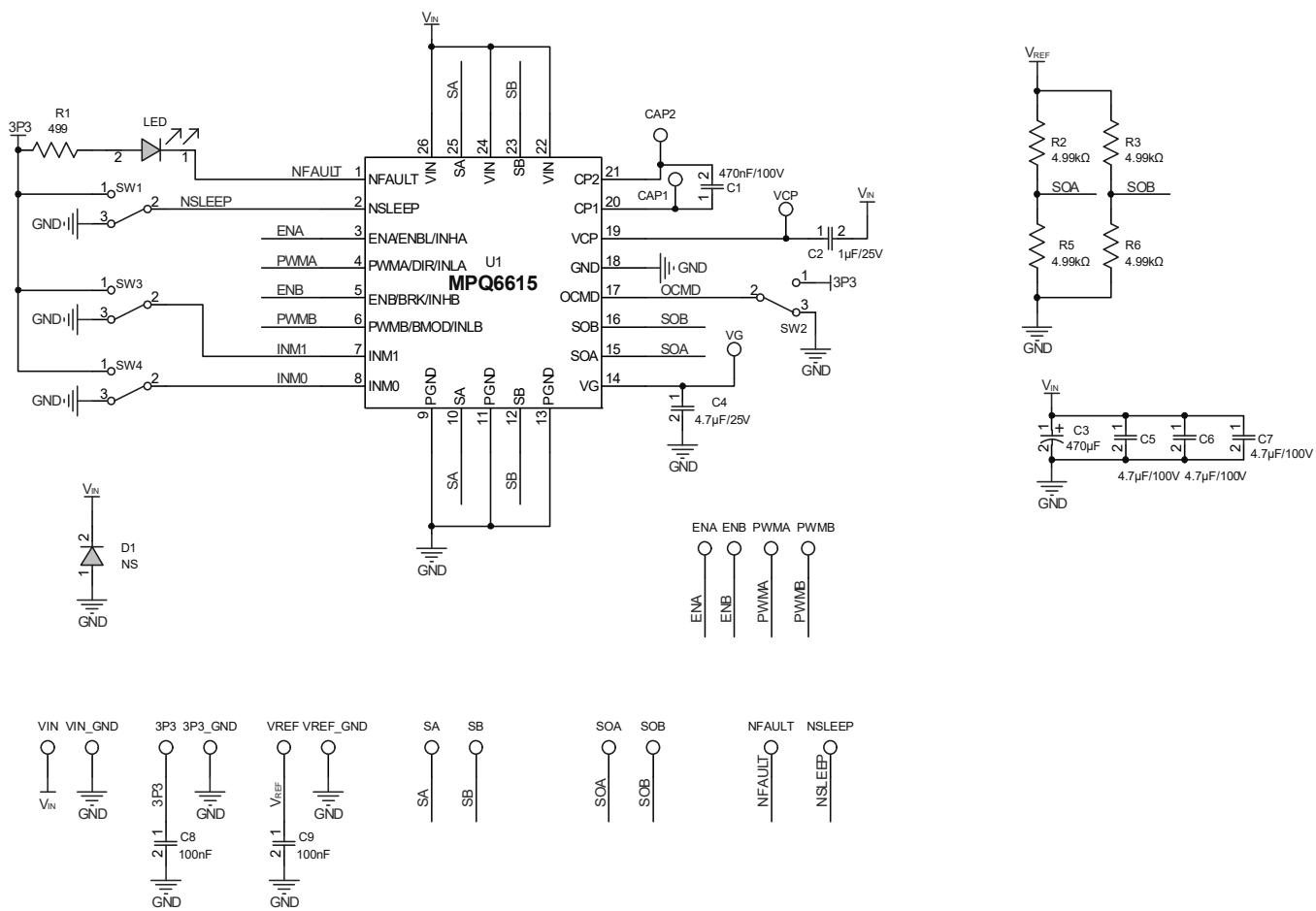


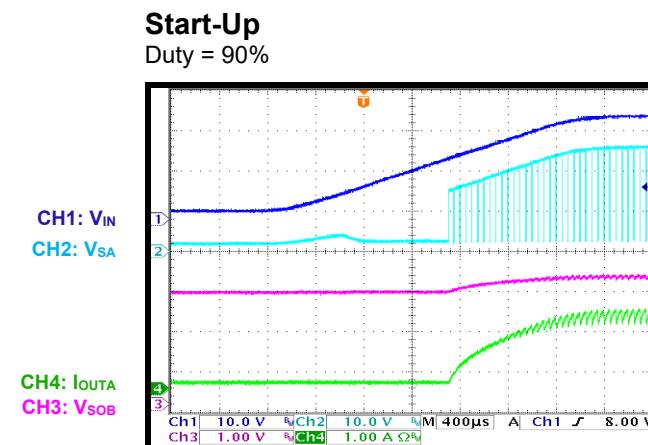
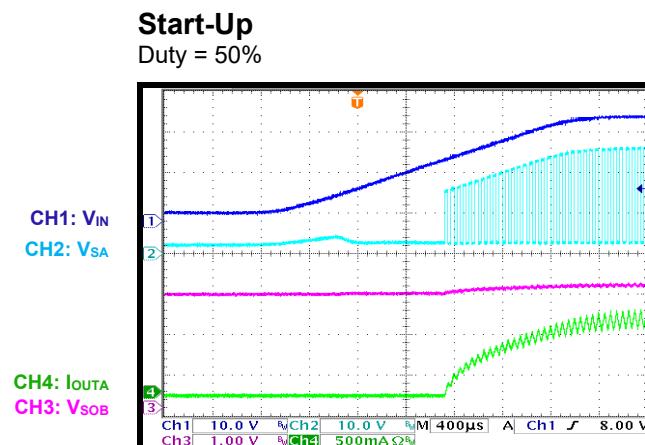
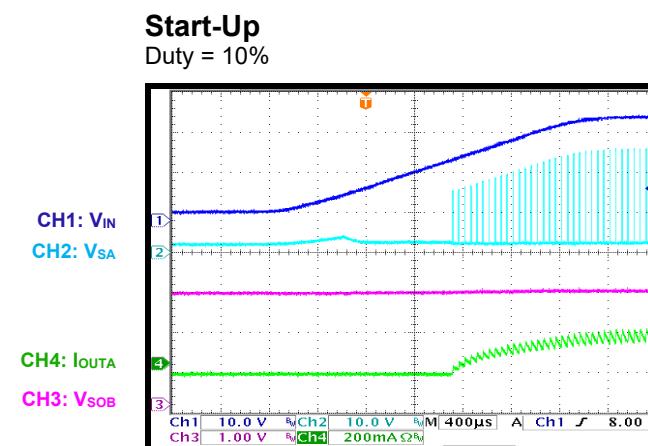
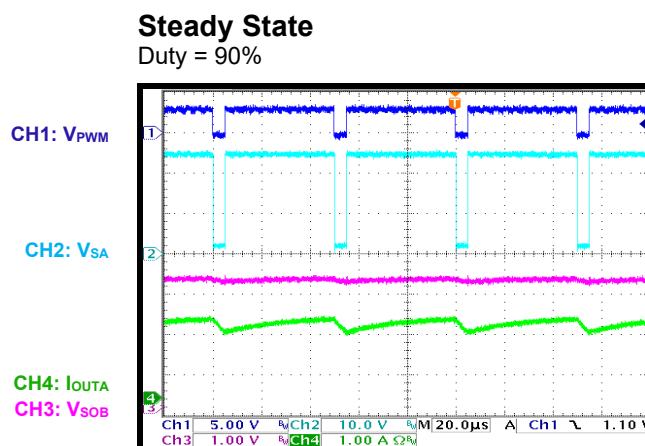
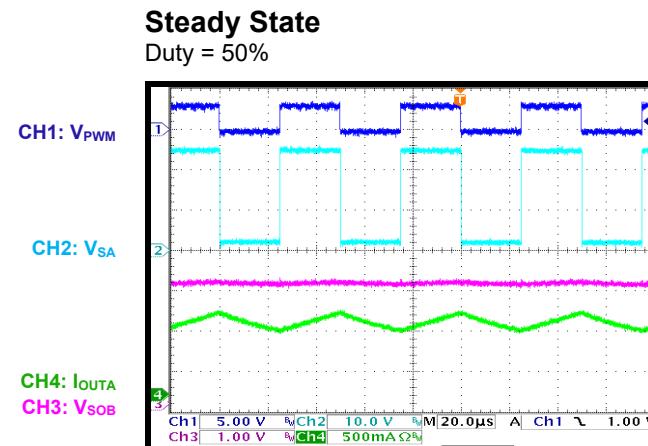
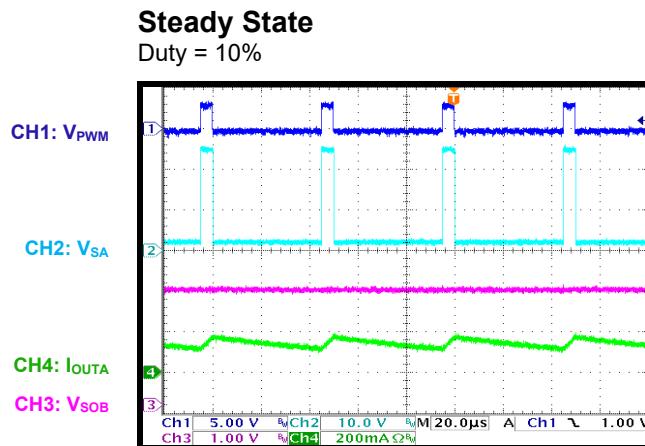
Figure 2: Evaluation Board Schematic

## EVQ6615-QK-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R1	499	Film resistor, 1%	0603	Yageo	RC0603FR-07499RL
4	R2, R3, R5, R6	4.99kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-074K99L
1	C1	470nF	Ceramic capacitor, 100V, X7R	0805	Murata	GRM21BR72A474KA73L
1	C2	1μF	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E105KA12D
1	C3	470μF	Electrolytic capacitor, 100V	DIP	Jianghai	CD263-100V470
1	C4	4.7μF	Ceramic capacitor, 25V, X6S	0603	Murata	GRM188C81E475KE11D
3	C5, C6, C7	4.7μF	Ceramic capacitor, 100V, X8L	1210	Murata	GCM32DL8EL475KE07L
2	C8, C9	100nF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	LED	2.6V	Red LED	0805	Bai Hong	BL-HUE35A-AV-TRB
1	U1	MPQ6615	40V, H-bridge DC motor driver, AEC-Q100 qualified	TQFN-26 (6mmx 6mm)	MPS	MPQ6615GQKTE-AEC1
1	D1	NS				
4	SW1, SW2, SW3, SW4	2.54mm	Button	DIP	Wurth	450301014042
8	CAP1, CAP2, VCP, VG, NFAULT, NSLEEP, SOA, SOB	1mm	Test point, yellow	DIP	Any	
4	VIN, VIN_GND, SA, SB	2mm	Connector	DIP	Any	
8	3P3, 3P3_GND, VREF, VREF_GND, ENA, ENB, PWMA, PWMB	1mm	Connector	DIP	Any	

## EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $V_{INM0} = V_{INM1} = 0V$ ,  $V_{ENA} = V_{ENB} = 5V$ ,  $f_{PWMA} = 20kHz$ ,  $V_{PWMB} = 0V$ ,  $V_{REF} = 5V$ , current-sense resistor divider =  $5k\Omega$ ,  $T_A = 25^\circ C$ , resistor + inductance:  $10\Omega + 2mH$ , unless otherwise noted.

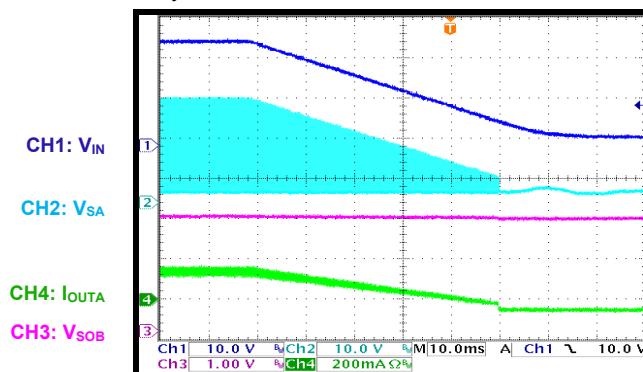


## EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $V_{INM0} = V_{INM1} = 0V$ ,  $V_{ENA} = V_{ENB} = 5V$ ,  $f_{PWMA} = 20kHz$ ,  $V_{PWMB} = 0V$ ,  $V_{REF} = 5V$ , current-sense resistor divider =  $5k\Omega$ ,  $T_A = 25^\circ C$ , resistor + inductance:  $10\Omega + 2mH$ , unless otherwise noted.

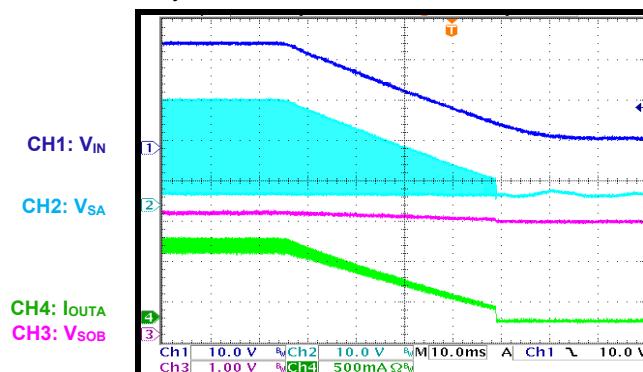
### Shutdown

Duty = 10%



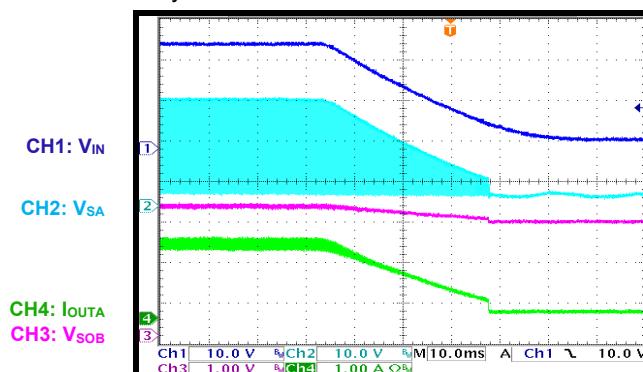
### Shutdown

Duty = 50%



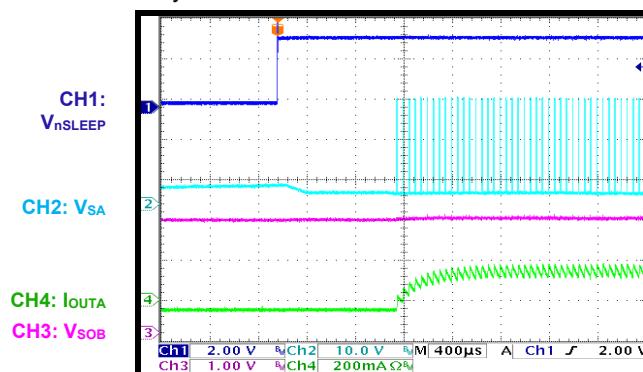
### Shutdown

Duty = 90%



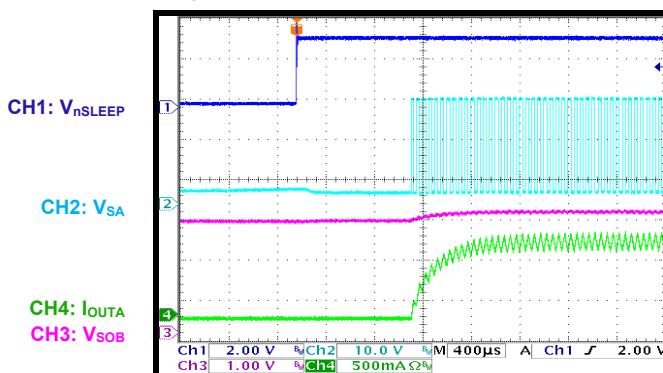
### Sleep Recovery

Duty = 10%



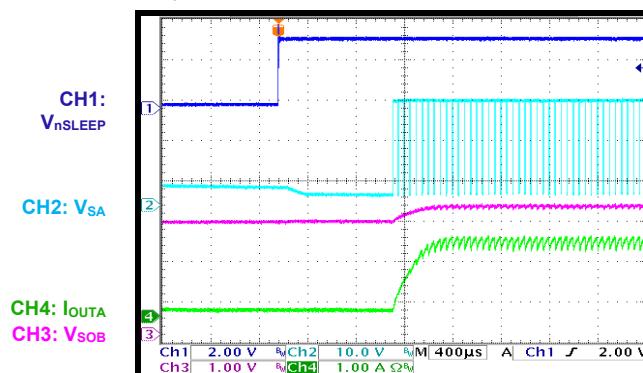
### Sleep Recovery

Duty = 50%



### Sleep Recovery

Duty = 90%

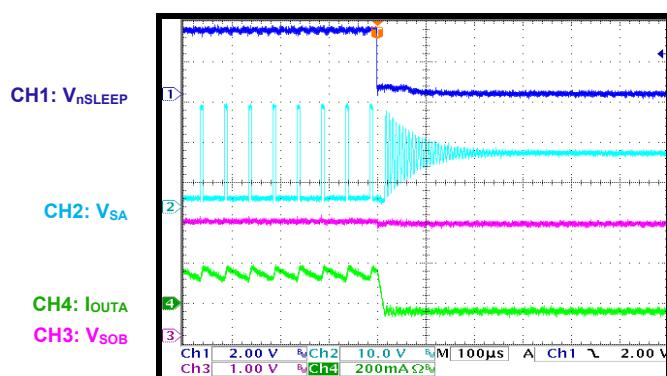


## EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $V_{INM0} = V_{INM1} = 0V$ ,  $V_{ENA} = V_{ENB} = 5V$ ,  $f_{PWMA} = 20kHz$ ,  $V_{PWMB} = 0V$ ,  $V_{REF} = 5V$ , current-sense resistor divider =  $5k\Omega$ ,  $T_A = 25^\circ C$ , resistor + inductance:  $10\Omega + 2mH$ , unless otherwise noted.

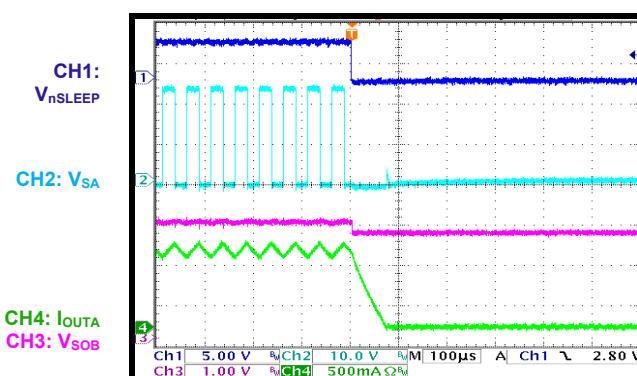
### Sleep Entry

Duty = 10%



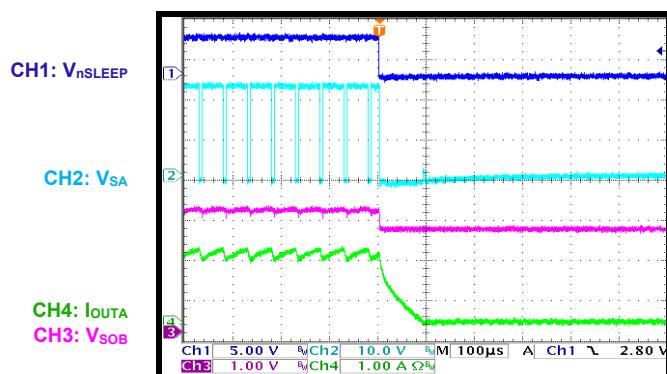
### Sleep Entry

Duty = 50%



### Sleep Entry

Duty = 90%



## PCB LAYOUT

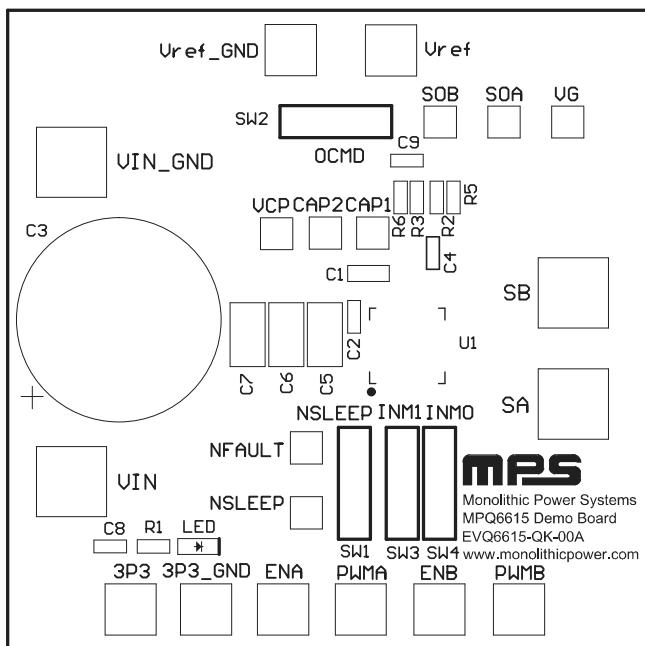


Figure 3: Top Silk

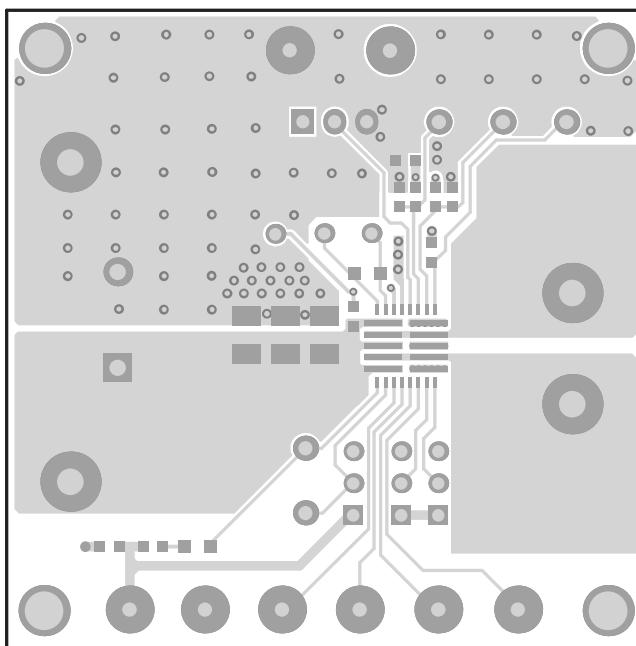


Figure 4: Top Layer

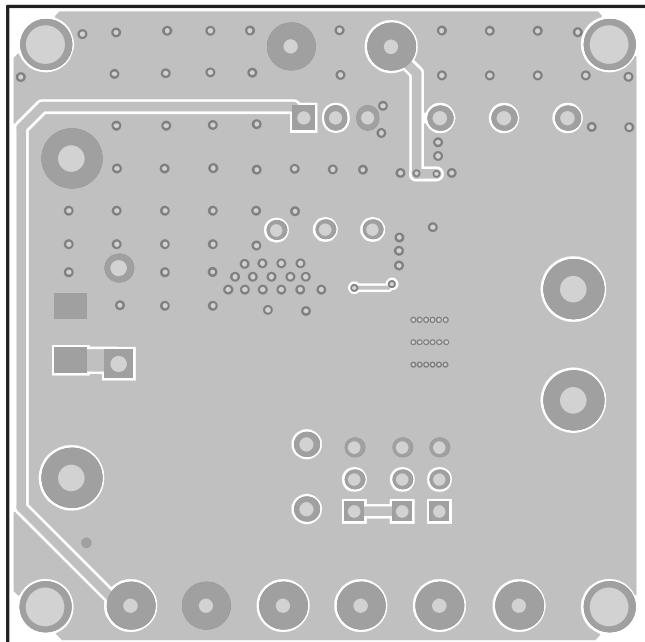


Figure 5: Bottom Layer

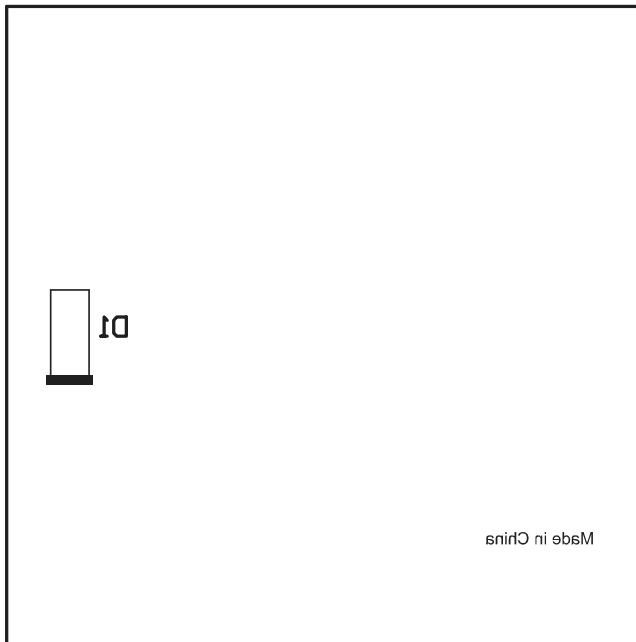


Figure 6: Bottom Silk

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	06/26/2023	Initial Release	-

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