EVM3824C-PA-01A

6V, 2A, Ultra-Small, Low-Noise, Single-Ouput Step-Down Power Module Evaluation Board

DESCRIPTION

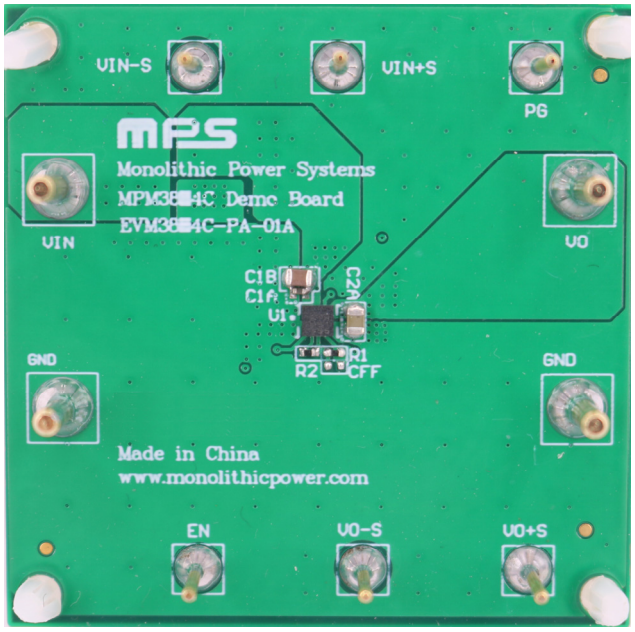
The EVM3824C-PA-01A is an evaluation board designed to demonstrate the capabilities of the MPM3824C, a high-efficiency, low-noise, single-output, step-down power module. The MPM3824C has a 1.25MHz fixed switching frequency (f_{SW}). The device's high f_{SW} and constant-on-time control (COT) control provide fast transient response, high efficiency, and easy loop stabilization. The MPM3824C is available in an ultra-small LGA-14 (2.5mmx2.5mmx1.2mm) package. For more information, refer to the MPM3824C datasheet.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		2.75V to 6V
Output voltage (V_{OUT})	V_{IN} = 2.75V to 6V, I_{OUT} = 0A to 2A	V_{OUT} = 1.2V
Maximum output current (I_{OUT})	V_{IN} = 2.75V to 6V	2A
Typical efficiency	V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A	85.3%
Peak efficiency	V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 1A	86.7%
Switching frequency (f_{SW})		1.25MHz

EVALUATION BOARD



LxWxH (5.1cmx5.1cmx1.6cm)

Board Number	MPS IC Number
EVM3824C-PA-01A	MPM3824CGPA

QUICK START GUIDE

The EVM3824C-PA-01A is easy to set up to evaluate the MPM3824C's performance. For proper measurement, equipment, and set-up, refer to Figure 1 and follow the guidelines below:

1. Preset the power supply between 2.75V and 6V (1), then turn off the power supply.
2. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
3. Connect the load terminals to: (2)
   a. Positive (+): VOUT
   b. Negative (-): GND
4. After making the connections, turn on the power supply. The board should start up automatically.
5. Check that the set output voltage (V_{OUT}) is flowing between VO+S and VO-S.
6. Once V_{OUT} is established, adjust the load within its operating range, then measure the efficiency, output voltage ripple (ΔV_{OUT}), input voltage ripple (ΔV_{IN}), and other parameters. (3)

Notes:

1) The input voltage (V_{IN}) should not exceed 6V.
2) The load is initially no load by default.
3) Do not use the oscilloscope's ground lead to measure ΔV_{OUT} or ΔV_{IN}.

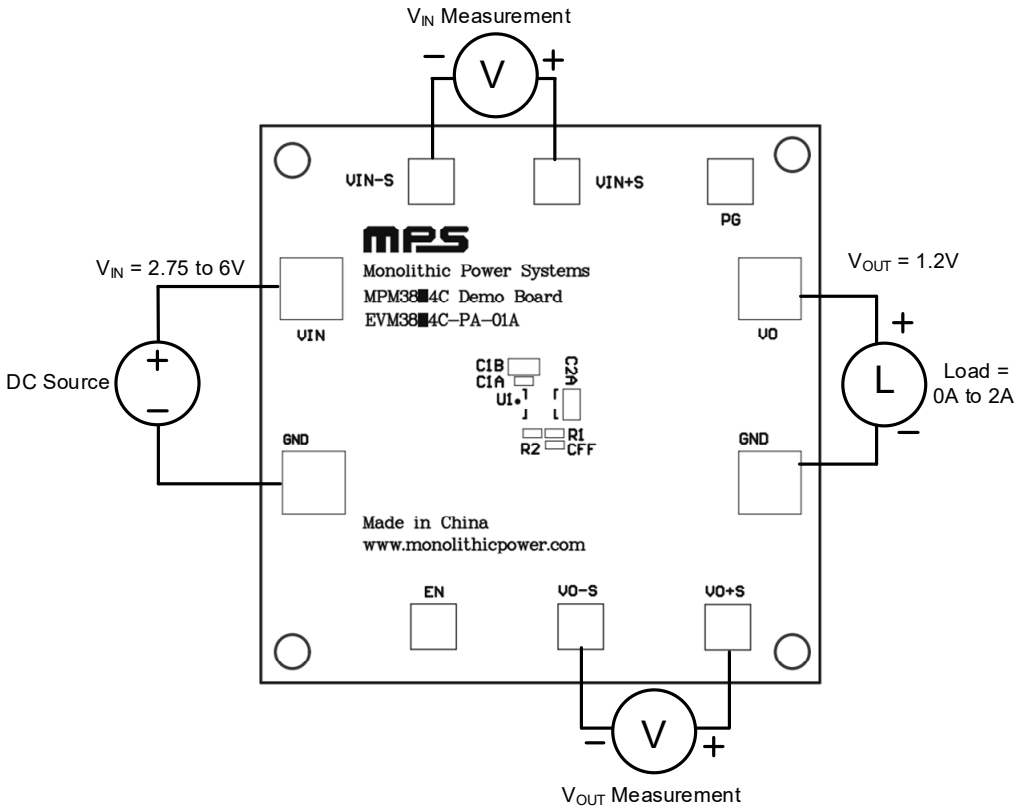


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

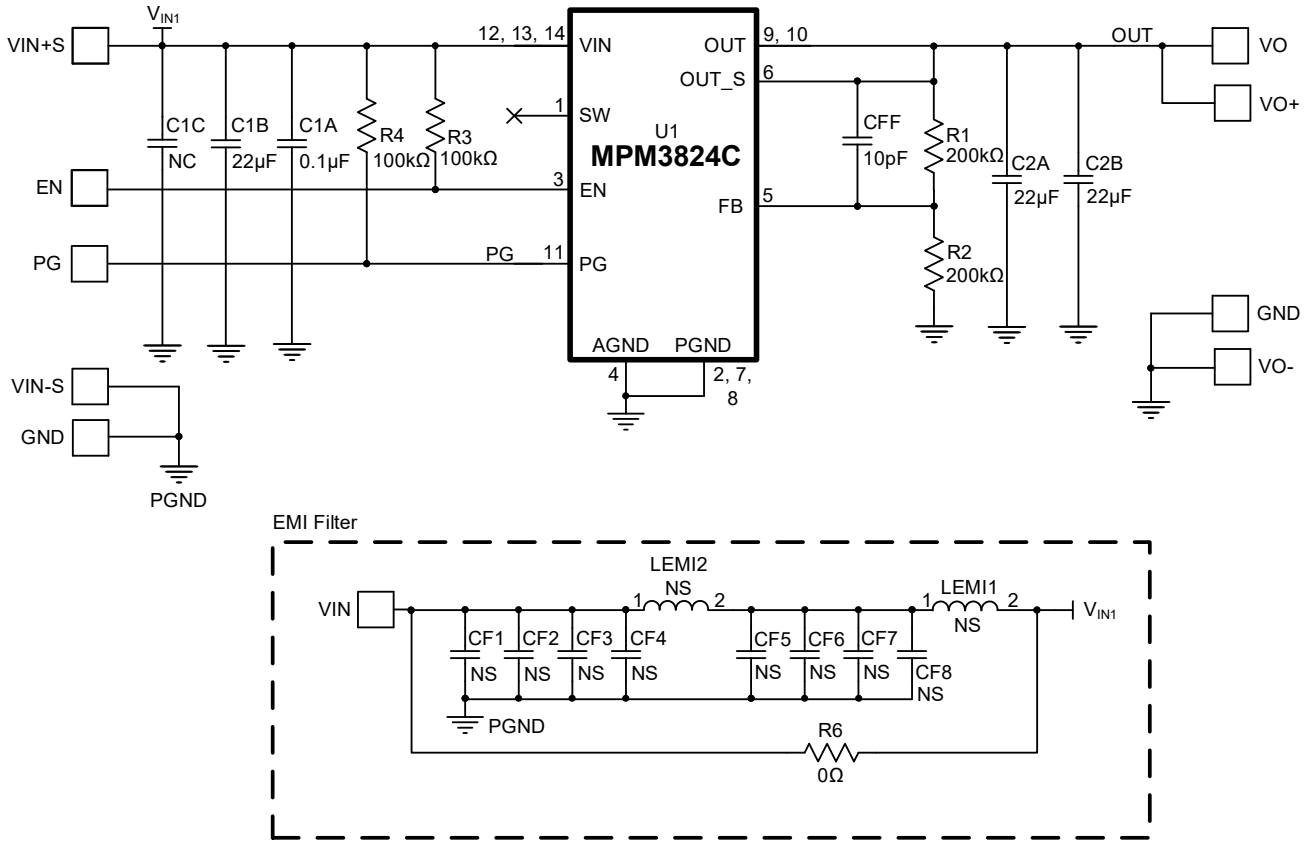


Figure 2: Evaluation Board Schematic

EVM3824C-PA-01A BILL OF MATERIALS

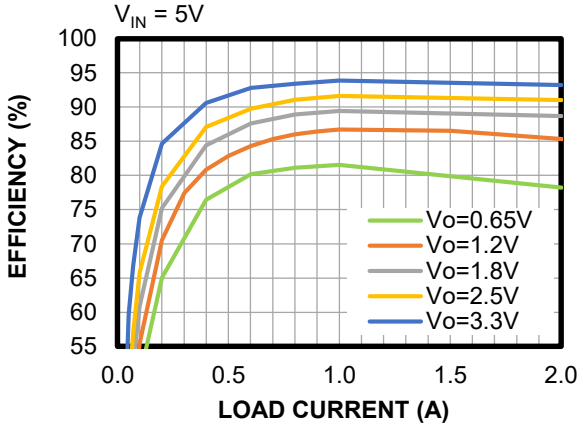
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1A	0.1µF	Ceramic capacitor, 10V, X7R	0402	TDK	C1005X7R1C104KT000E
2	C1B, C2A	22µF	Ceramic capacitor, 10V, X7R	0805	TDK	C2012X7R1C226MT000N
1	CFF	10pF	Ceramic capacitor, 10V, X7R	0402	TDK	C1005X7R1C100KT000E
2	R1, R2	200kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-07200KL
2	R3, R4	100kΩ	Film resistor, 1%	0402	Yageo	RC0603FR-07100KL
1	R6	0Ω	Film resistor, 1%	2512	Yageo	RC2512FK-070RL
6	VIN_S, VO_S, GND_S, GND_S, EN, PG	φ1	φ1 copper pin	DIP	Custom	
4	VIN, VO, GND, GND	Φ2	Φ2 copper pin	DIP	Custom	
1	U1	MPM3824C	Step-down power module, 6V, 2A	LGA-14 (2.5mmx 2.5mm)	MPS	MPM3824CGPA

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

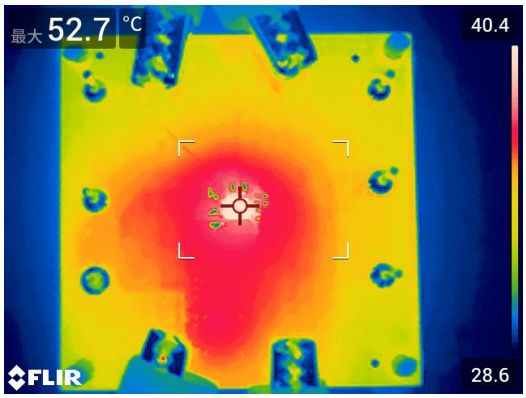
Efficiency vs. Load Current

V_{IN} = 5V



Thermal Performance

T_A = 28°C, I_{OUT} = 2A, t_{CASE} = 52.7°C, no forced airflow

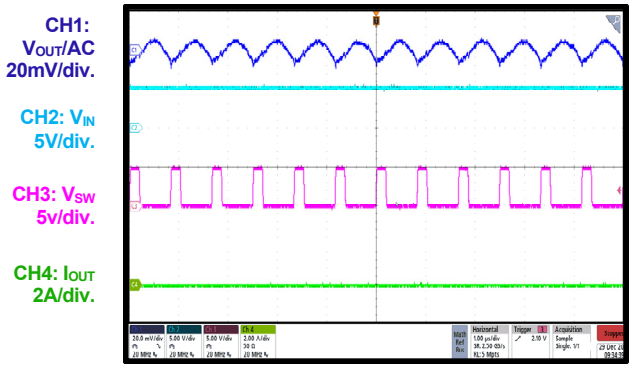


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

Steady State

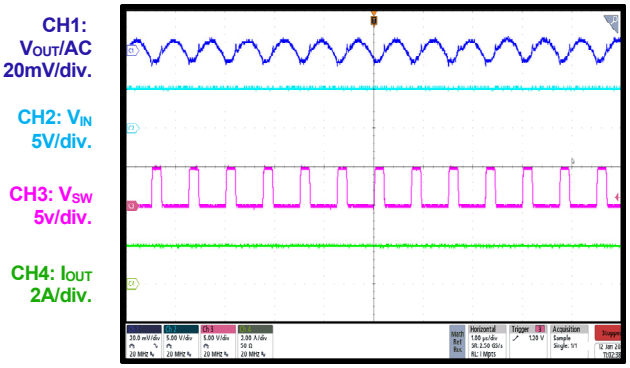
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



1µs/div.

Steady State

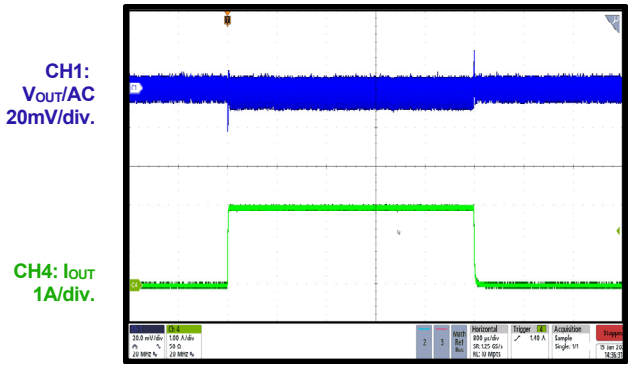
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



1µs/div.

Load Transient

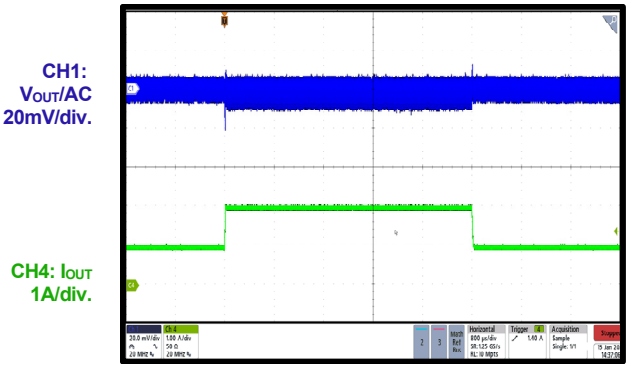
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A to 2A, 2.5A/µs, e-load



800µs/div.

Load Transient

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 1A to 2A, 2.5A/µs, e-load



800µs/div.

PCB LAYOUT

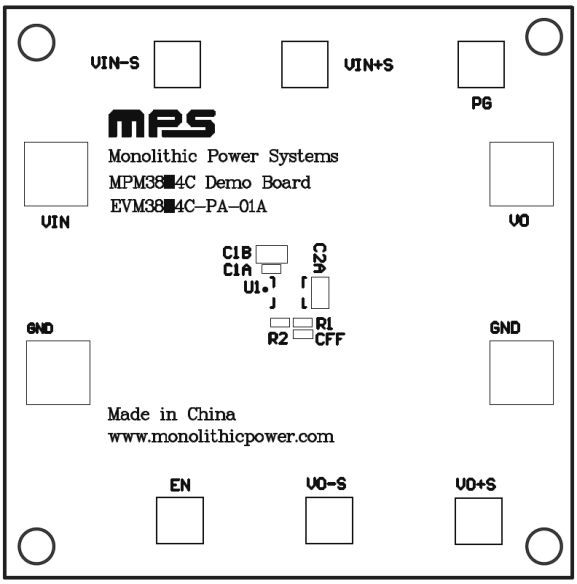


Figure 3: Top Silk

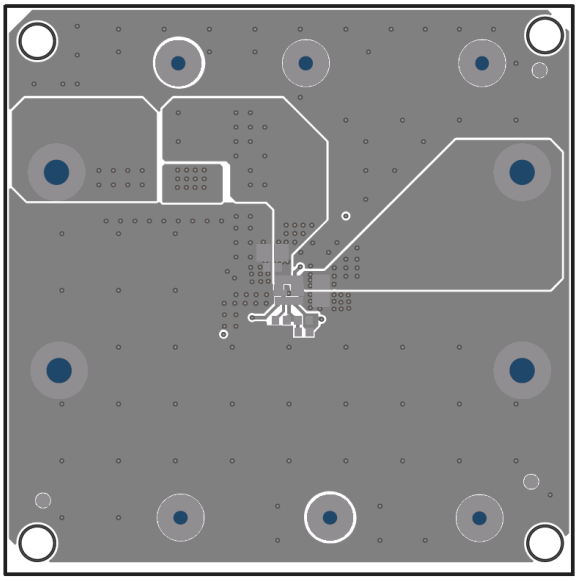


Figure 4: Top Layer

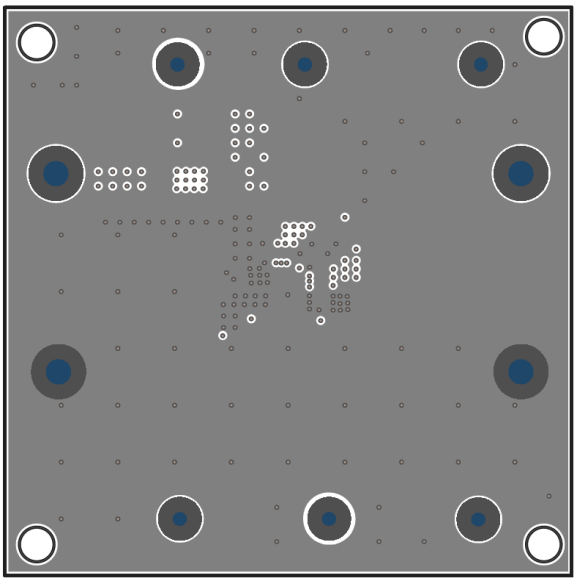


Figure 5: Mid-Layer 1

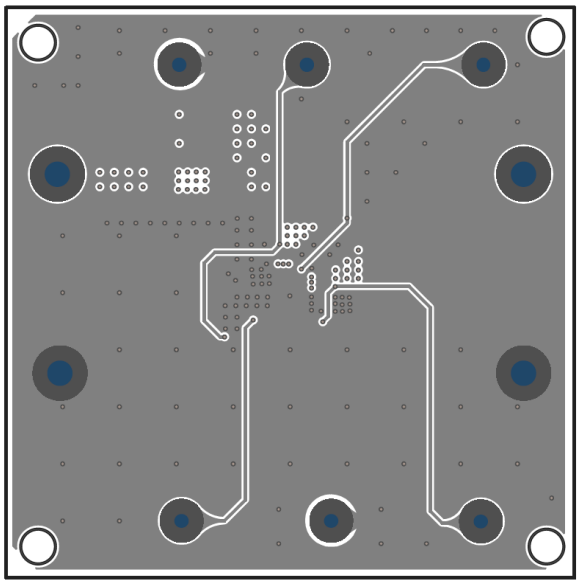


Figure 6: Mid-Layer 2

PCB LAYOUT *(continued)*

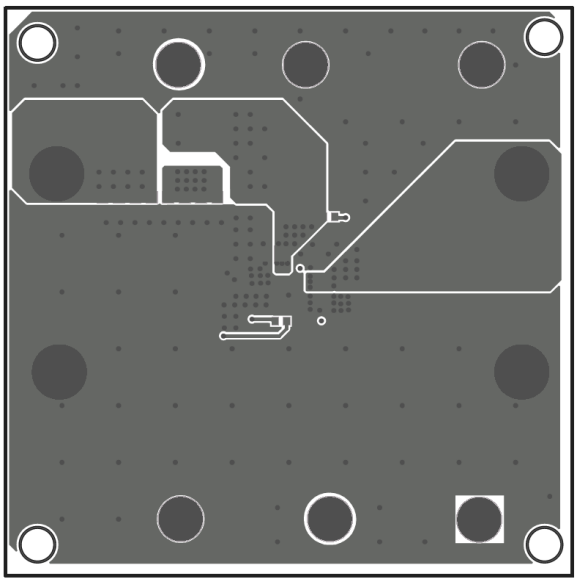


Figure 7: Bottom Layer

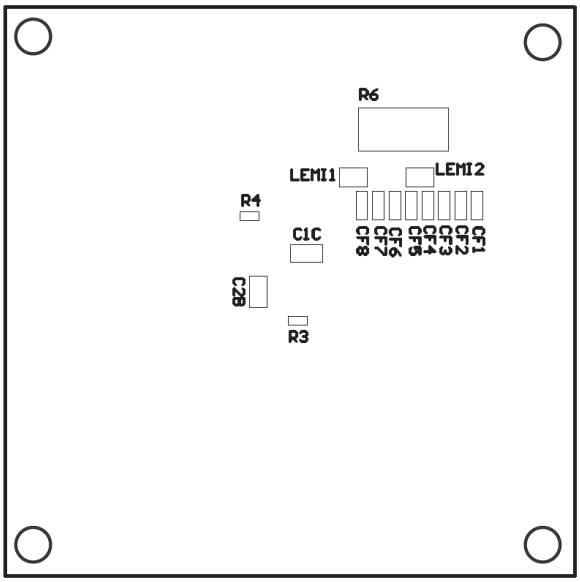


Figure 8: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	09/09/2021	Initial Release	-