



EVM3650C-QW-00A

17V, 6A, 1.2MHz, Ultra-Thin, Synchronous, Step-Down Power Module Evaluation Board

DESCRIPTION

The EVM3650C-QW-00A is an evaluation board designed to demonstrate the capabilities of the MPM3650C, a fully integrated, high-frequency, synchronous, rectified, step-down power module with an internal inductor. It offers a highly compact solution to achieve 6A of continuous output current (I_{OUT}) across a wide 2.75V to 17V input voltage (V_{IN}) range, with excellent load and line regulation. The MPM3650C offers synchronous operation for high efficiency across the I_{OUT} load range.

Constant-on-time (COT) control enables ultra-fast transient response and easy loop design, as well as very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MPM3650C is available in a QFN-24 (4mmx6mmx1.6mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	2.75 to 17	V
Output voltage	V_{OUT}	1	V
Output current	I_{OUT}	6	A

FEATURES

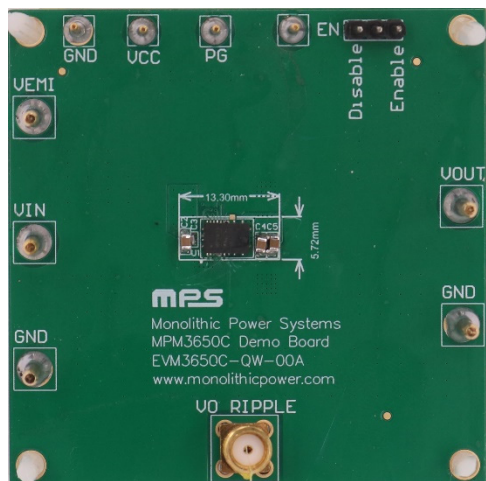
- Wide 2.75V to 17V Operating Input Voltage (V_{IN}) Range
- Output Current (I_{OUT}) for Different Output Voltage (V_{OUT}) Ranges:
 - 6A I_{OUT} for 0.6V to 1.8V V_{OUT}
 - 5A I_{OUT} for 1.8V to 3.3V V_{OUT}
- 3.3V Maximum V_{OUT}
- Forced Continuous Conduction Mode (CCM) for Low Output Voltage Ripple
- High-Efficiency Synchronous Operation
- Supports Pre-Biased Start-Up
- Fixed 1200kHz Switching Frequency (f_{SW})
- Externally Configurable Soft-Start Time (t_{SS})
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OVP) with Hiccup Mode
- Thermal Shutdown
- Available in a QFN-24 (4mmx6mmx1.6mm) Package

APPLICATIONS

- Field-Programmable Gate Array (FPGA) Power Systems
- Optical Modules
- Telecommunications
- Networking
- Industrial Equipment

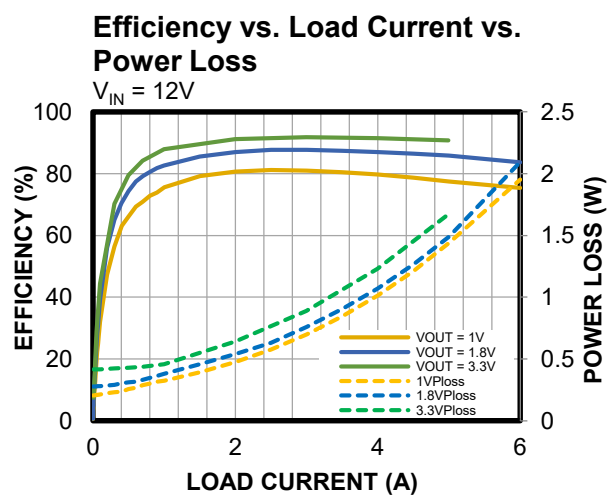
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EVM3650C-QW-00A EVALUATION BOARD



LxWxH (63.5mmx63.5mmx1.6mm)

Board Number	MPS IC Number
EVM3650C-QW-00A	MPM3650CGQY



QUICK START GUIDE

1. Preset the power supply between 2.75V and 17V.
2. Turn off the power supply.
3. Connect the power supply terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND
4. Connect load terminals ($\leq 6A$) to:
 - a. Positive (+): VOUT
 - b. Negative (-): GND
5. After making the connections, turn on the power supply. The board should start up automatically.

EVALUATION BOARD SCHEMATIC

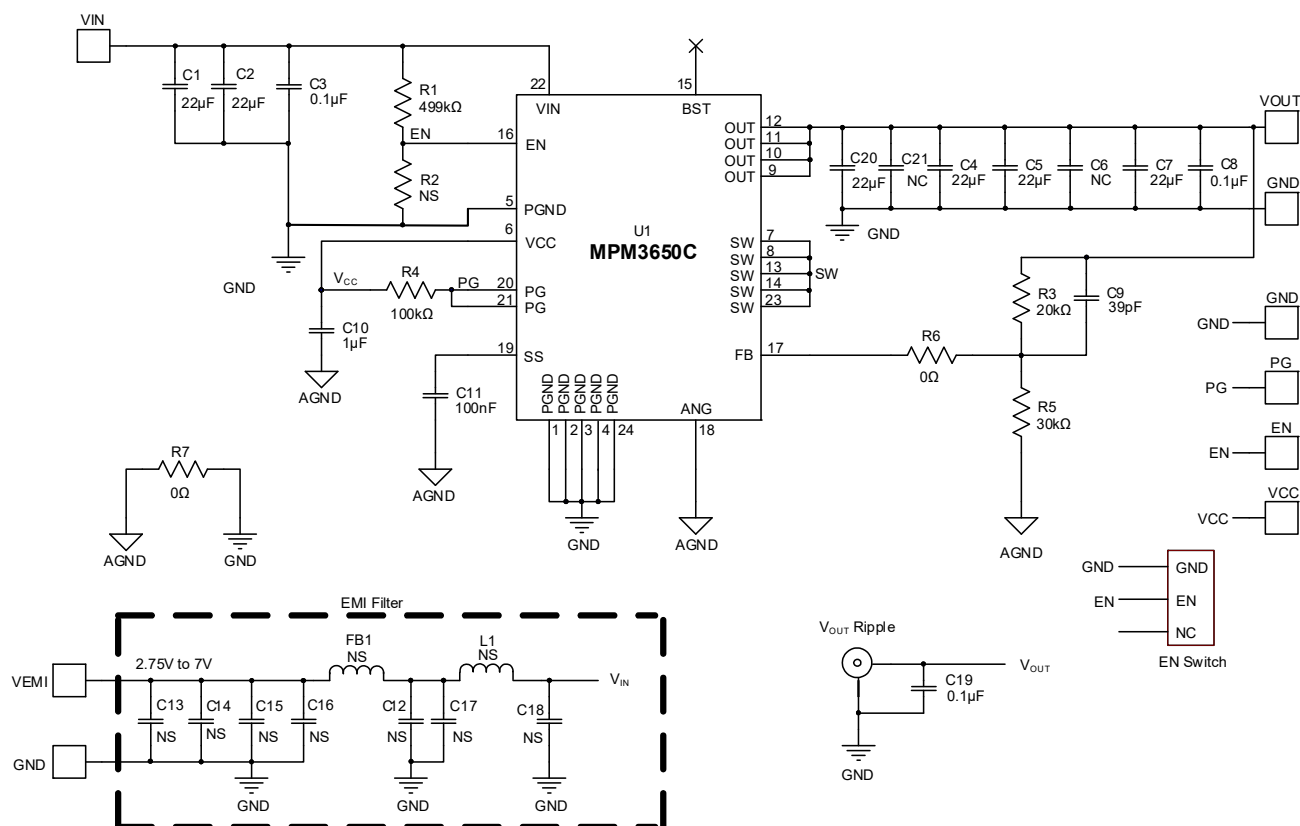


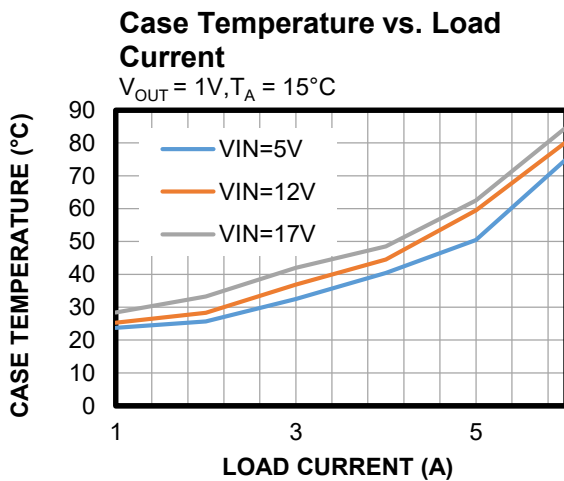
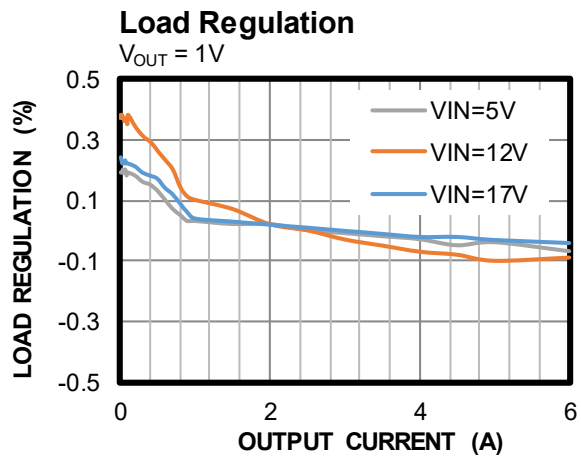
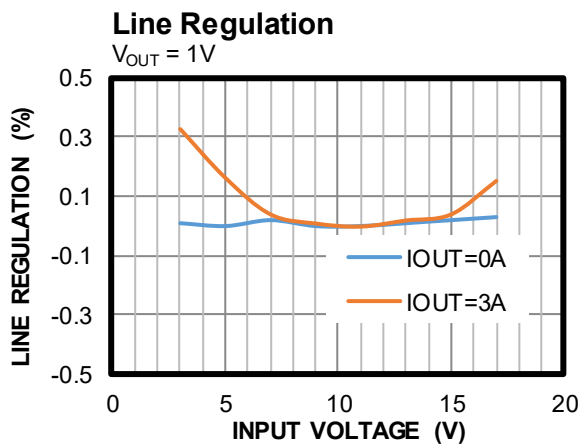
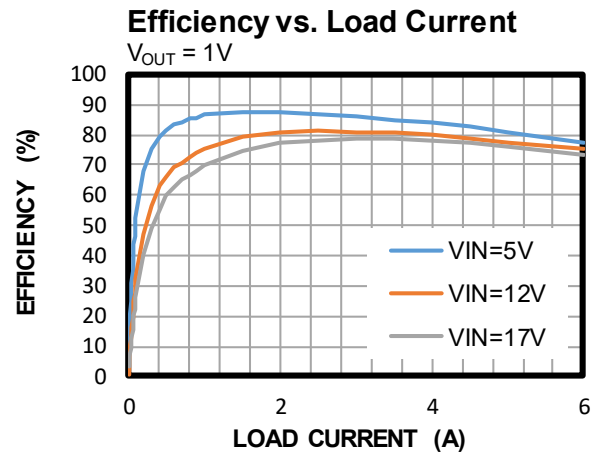
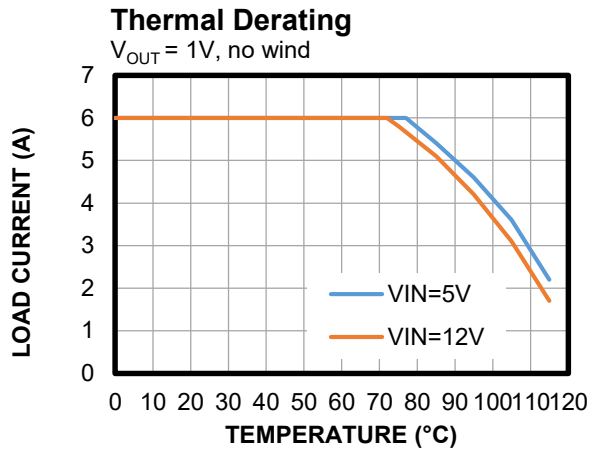
Figure 1: Evaluation Board Schematic

EVM3650C-QW-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
6	C1, C2, C4, C5, C20, C7	22 μ F	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
4	C3, C8, C11, C19	0.1 μ F	Ceramic capacitor, 25V, X5R	0402	Wurth	885012105018
1	C10	1 μ F	Ceramic capacitor, 25V, X5R	0402	Murata	GRM155R61E105KA12D
1	C9	39pF	Ceramic capacitor, 50V, C0G	0402	Murata	GRM1555C1H390JA01D
1	R1	499k Ω	Film resistor, 1%	0402	Yageo	RC0402FR-07499KL
1	R4	100k Ω	Film resistor, 1%	0402	Yageo	RC0402FR-07100KL
2	R7, R6	0 Ω	Film resistor, 1%	0402	Yageo	RC0402FR-070RL
1	R3	20k Ω	Film resistor, 1%	0402	Yageo	RC0402FR-0720KL
1	R5	30k Ω	Film resistor, 1%	0402	Yageo	RC0402FR-0730KL
1	EN	2.54mm	3-pin, single-row, straight socket header	DIP	Wurth	61300311821
0	V _{OUT} ripple	NS				
5	VIN, VEMI, GND, GND, VOUT	Φ 2.0	2 copper pins	DIP	Custom	
4	EN, GND, VCC, PG	Φ 1.0	1 copper pin	DIP	Custom	
1	U1	MPM3650C	Step-down power module, 17V, 6A, 1.2MHz	QFN-24 (4mmx 6mm)	MPS	MPM3650CGQW

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board, $V_{IN} = 12V$, $V_{OUT} = 1V$, $T_A = 25^{\circ}C$, unless otherwise noted.



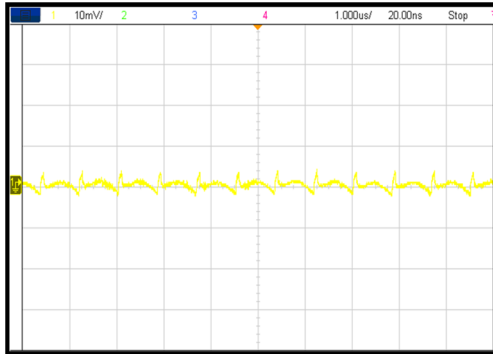
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board, $V_{IN} = 12V$, $V_{OUT} = 1V$, $T_A = 25^\circ C$, unless otherwise noted.

V_{OUT} Ripple

 $I_{OUT} = 0A$

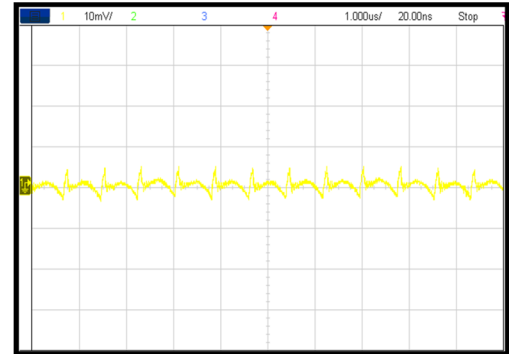
CH1:
 V_{OUT}/AC
10mV/div.



V_{OUT} Ripple

 $I_{OUT} = 6A$

CH1:
 V_{OUT}/AC
10mV/div.

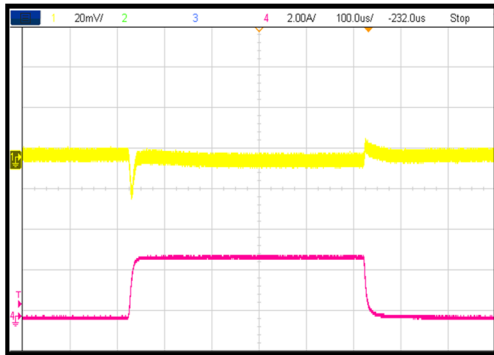


Load Transient

 $I_{OUT} = 0A$ to 3A

CH1:
 V_{OUT}/AC
20mV/div.

CH4: I_{OUT}
2A/div.

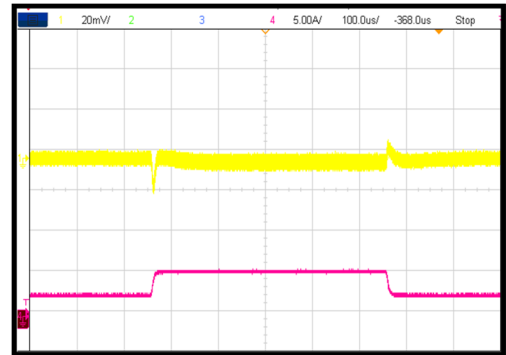


Load Transient

 $I_{OUT} = 3A$ to 6A

CH1:
 V_{OUT}/AC
20mV/div.

CH4: I_{OUT}
5A/div.



Start-Up through V_{IN}

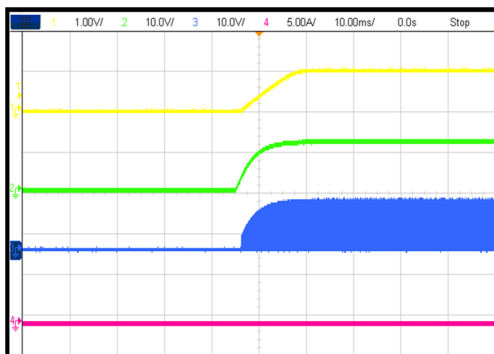
 $I_{OUT} = 0A$

CH1: V_{OUT}
1V/div.

CH2: V_{IN}
10V/div.

CH3: V_{SW}
10V/div.

CH4: I_{OUT}
5A/div.



Start-Up through V_{IN}

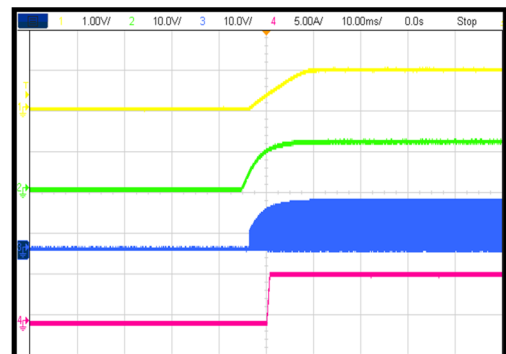
 $I_{OUT} = 6A$

CH1: V_{OUT}
1V/div.

CH2: V_{IN}
10V/div.

CH3: V_{SW}
10V/div.

CH4: I_{OUT}
5A/div.



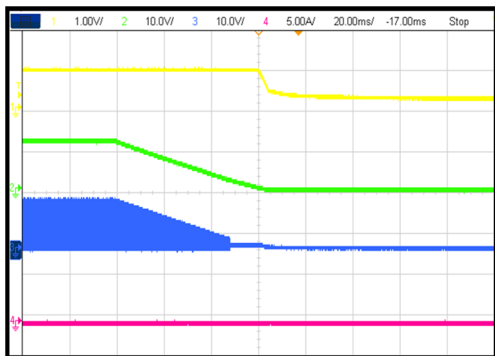
EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board, $V_{IN} = 12V$, $V_{OUT} = 1V$, $T_A = 25^{\circ}C$, unless otherwise noted.

Shutdown through VIN

 $I_{OUT} = 0A$

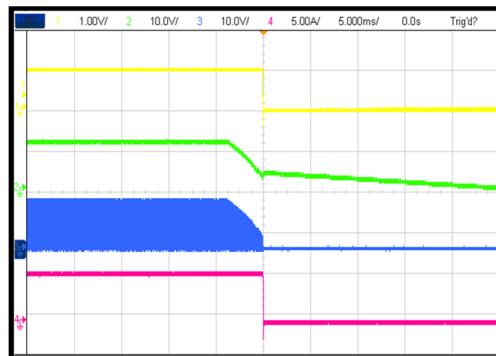
CH1: V_{OUT}
1V/div.
CH2: V_{IN}
10V/div.
CH3: V_{SW}
10V/div.
CH4: I_{OUT}
5A/div.



Shutdown through VIN

 $I_{OUT} = 6A$

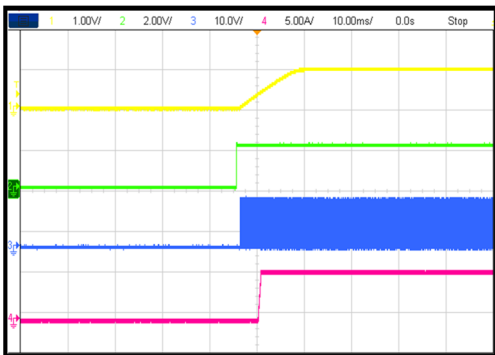
CH1: V_{OUT}
1V/div.
CH2: V_{IN}
10V/div.
CH3: V_{SW}
10V/div.
CH4: I_{OUT}
5A/div.



Start-Up through EN

 $I_{OUT} = 0A$

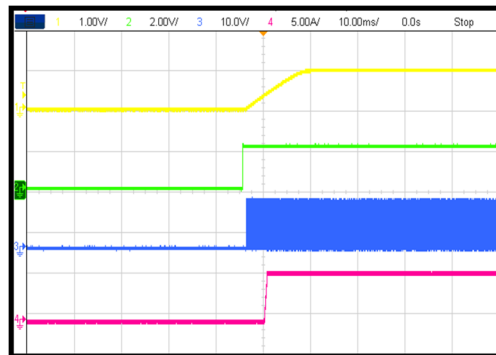
CH1: V_{OUT}
1V/div.
CH2: V_{EN}
2V/div.
CH3: V_{SW}
10V/div.
CH4: I_{OUT}
5A/div.



Start-Up through EN

 $I_{OUT} = 6A$

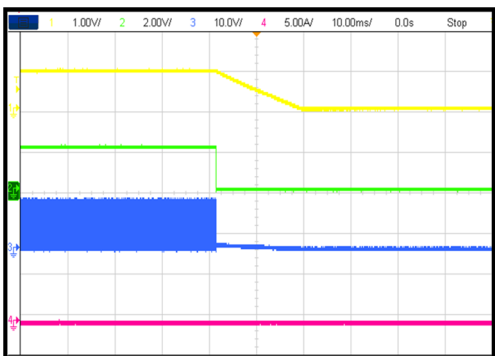
CH1: V_{OUT}
1V/div.
CH2: V_{EN}
2V/div.
CH3: V_{SW}
10V/div.
CH4: I_{OUT}
5A/div.



Shutdown through EN

 $I_{OUT} = 0A$

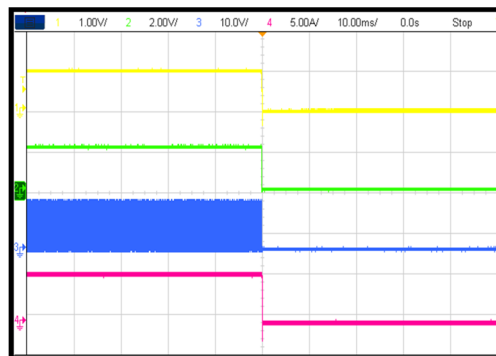
CH1: V_{OUT}
1V/div.
CH2: V_{EN}
2V/div.
CH3: V_{SW}
10V/div.
CH4: I_{OUT}
5A/div.



Shutdown through EN

 $I_{OUT} = 6A$

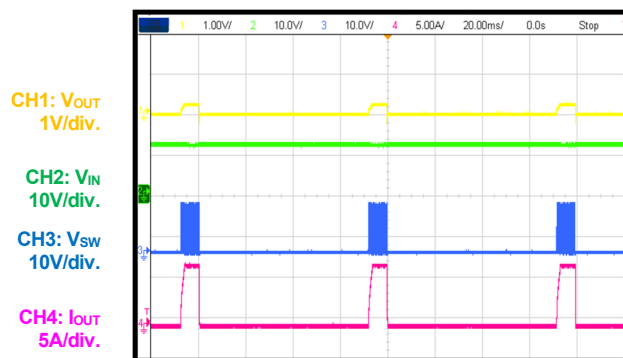
CH1: V_{OUT}
1V/div.
CH2: V_{EN}
2V/div.
CH3: V_{SW}
10V/div.
CH4: I_{OUT}
5A/div.



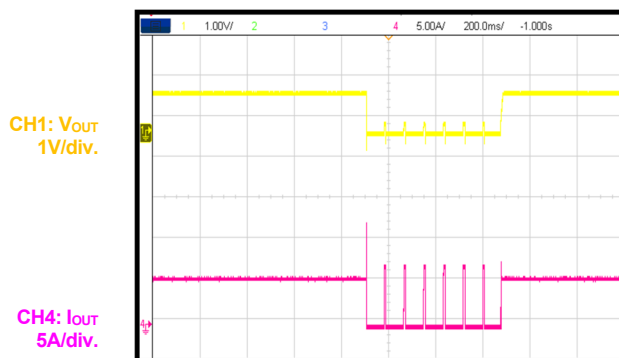
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board, $V_{IN} = 12V$, $V_{OUT} = 1V$, $T_A = 25^{\circ}C$, unless otherwise noted.

SCP Steady State



SCP Entry and Recovery



The diagram illustrates the layout of the MPM3650C Demo Board. Key components and their locations are marked with labels and corresponding square boxes:

- Top Row:** GND, VCC, PG, EN, Disable, Enable.
- Left Side:** VEMI, VIN, GND.
- Right Side:** VOUT, GND.
- Bottom:** VO RIPPLE.

A central component is shown with dimensions: 13.30mm in width and 5.72mm in height. The component is labeled with 'MPS' and 'C4C8'.

Figure 2: Top Silk

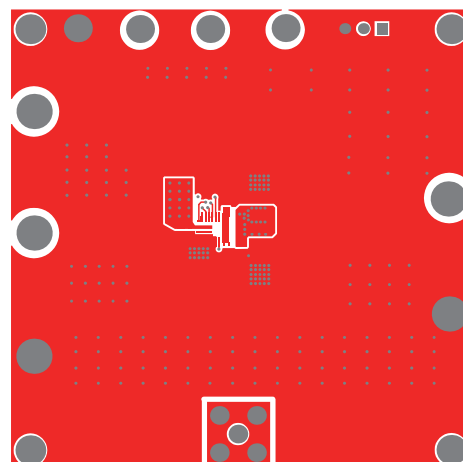


Figure 3: Top Layer

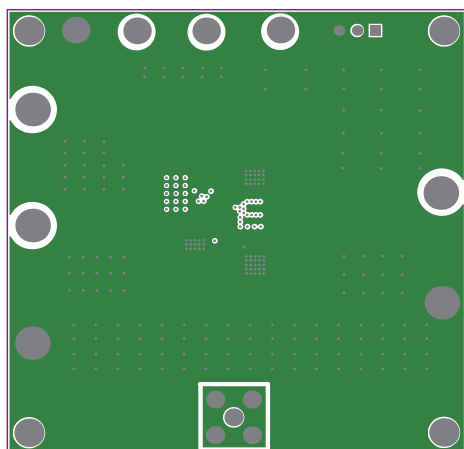


Figure 4: Mid-Layer 1

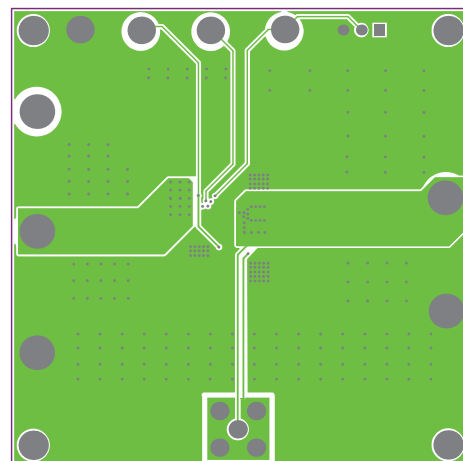


Figure 5: Mid-Layer 2

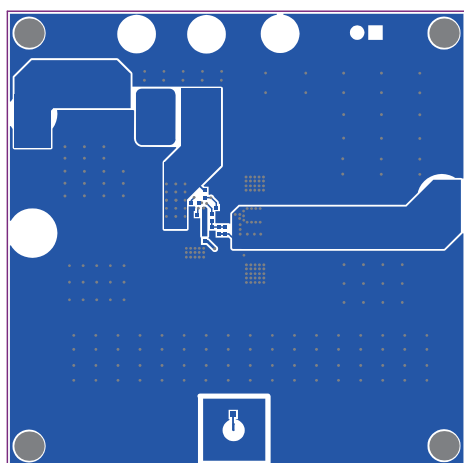


Figure 6: Bottom Layer

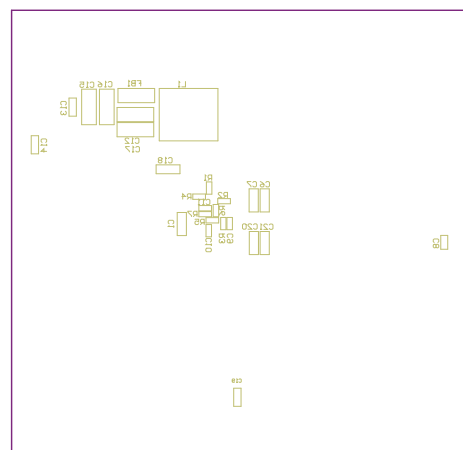


Figure 7: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	08/05/2021	Initial Release	-

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