EVL8853-Q-00A

High-Efficiency, 4A, 18V, Synchronous Step-Down Converter with I²C Interface Evaluation Board

DESCRIPTION

The EVL8853-Q-00A is an evaluation board designed to demonstrate the capabilities of the MP8853, a high efficiency, synchronous step-down converter with an I²C interface.

The MP8853 is a high-frequency, synchronous rectified, step-down, switch-mode converter with an I²C interface. The MP8853 offers a fully integrated solution that achieves up to 4A of continuous output current (I_{OUT}), with excellent load and line regulation across a wide input supply range. The output voltage (V_{OUT}) can be controlled on the fly via the I²C interface. The reference voltage (V_{REF}) can be adjusted from 0.6V to 1.108V in 4mV steps. The voltage slew rate, frequency, current limit, hiccup/latch-off protection, enable, and power-save mode (PSM) are also selectable via the I²C interface.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good (PG) pin indicates whether V_{OUT} is in the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

It is recommended to read the datasheet for the MP8853 prior to making any changes to the EVL8853-Q-00A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		2.85V to 18V
Output voltage (V_{OUT})	V_{IN} = 2.85V to 18V, I_{OUT} = 0A to 4A	V_{OUT} = 1V
Maximum output current (I_{OUT})	V_{IN} = 2.85V to 18V	4A
Typical efficiency	V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 4A	88.9%
Peak efficiency	V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 2.5A	89.7%
Switching frequency (f_{SW})		500kHz

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

EVALUATION BOARD

LxWxH (6.35cmx6.35cmx2cm)

Board Number	MPS IC Number
EVL8853-Q-00A	MP8853GQ

QUICK START GUIDE

The EVL8853-Q-00A evaluation board is easy to set up and use to evaluate the performance of the MP8853. For proper measurement equipment set-up, refer to Figure 1 and follow the steps below:

1. Preset the power supply to 12V, then turn off the power supply. (1)
2. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
3. Connect the load terminals to:
   a. Positive (+): VOUT
   b. Negative (-): GND
4. After making the connections, turn on the power supply. The board should automatically start up.
5. To use the enable (EN) function, apply a digital input to the EN pin. Drive EN above 1.3V to turn on the regulator, or below 0.9V to turn it off.
6. To configure the MP8853 registers, connect the SCL, SDA and GND to a computer via the USB to I²C interface communication kit, and run the MP8853 GUI software (Virtual Bench Pro). (2)

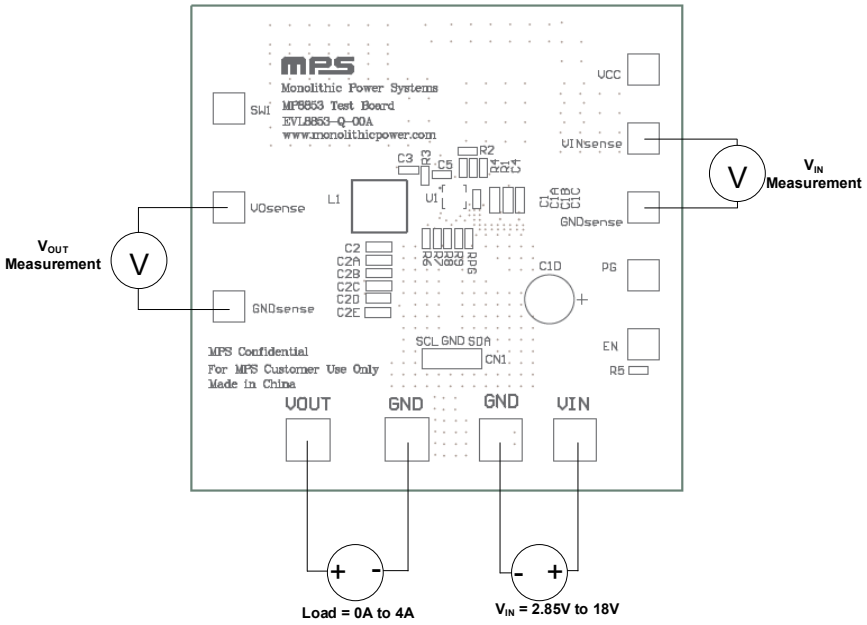


Figure 1: Measurement Equipment Set-Up (3)

Notes:

1) Ensure that V_{IN} does not exceed 18V.
2) The GUI installation file (Virtual Bench Pro) and supplemental documents can be downloaded from the MPS website.
3) When measuring the output or input voltage ripple, do not use the long ground lead on the oscilloscope probe.

EVALUATION BOARD SCHEMATIC

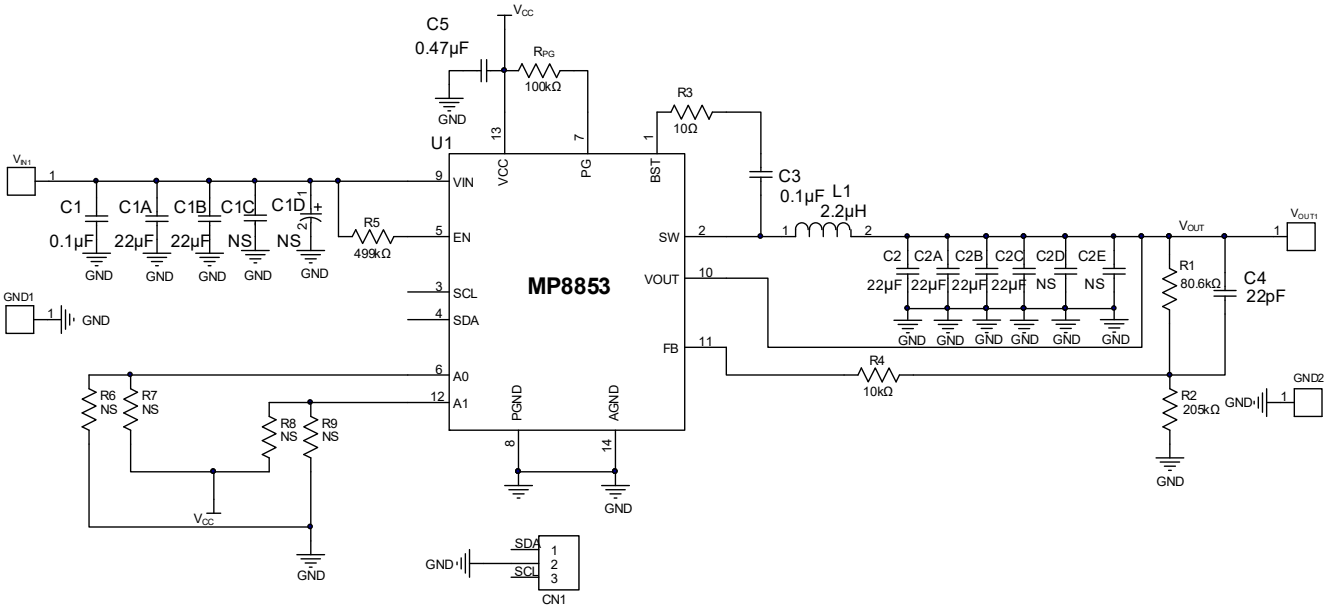


Figure 2: Evaluation Board Schematic

EVL8853-Q-00A BILL OF MATERIALS

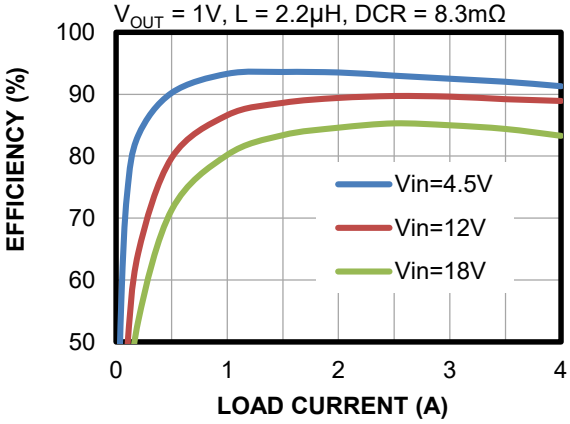
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R1	80.6kΩ	Film resistor, 1%	0603	RoyalOhm	RC0603FR-0780K6L
1	R2	205kΩ	Film resistor, 1%	0603	RoyalOhm	RL0603FR-07205KL
1	R3	10Ω	Film resistor, 1%	0603	RoyalOhm	RC0603FR-0710RL
1	R4	10kΩ	Film resistor, 1%	0603	RoyalOhm	RL0603FR-0710KL
1	R5	499kΩ	Film resistor, 1%	0603	RoyalOhm	RL0603FR-07499KL
0	R6, R7, R8, R9	NS				
1	RPG	100kΩ	Film resistor, 1%	0603	RoyalOhm	RL0603FR-07100KL
2	C1, C3	0.1μF	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E104KA01D
2	C1A, C1B	22μF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
4	C2, C2A, C2B, C2C	22μF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
0	C1C, C1D, C2D, C2E	NS				
1	C4	22pF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM1885C1H220JA01D
1	C5	0.47μF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C474KA88D
1	CN1	3 pins	3-pin connector	DIP	Any	
1	L1	2.2μH	Inductor, D_{CR} = 8.3mΩ	SMD	MPS	MPL-AL6050-2R2
1	U1	MP8853	Step-down converter with I^2C interface	QFN-14 (3mmx 3mm)	MPS	MP8853GQ

EVB TEST RESULTS

V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

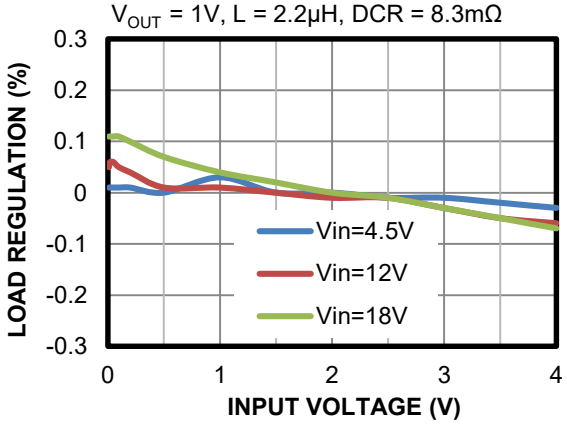
Efficiency vs. Load Current

V_{OUT} = 1V, L = 2.2µH, DCR = 8.3mΩ



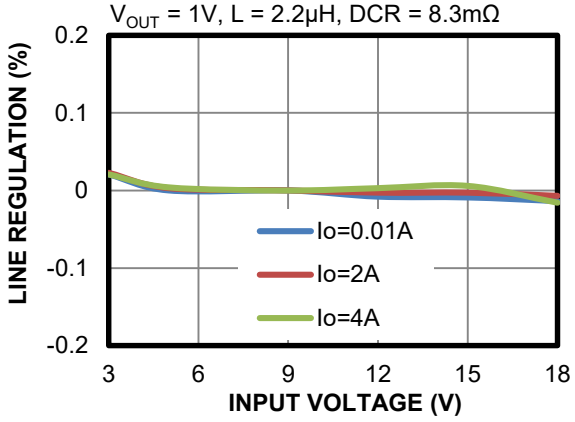
Load Regulation

V_{OUT} = 1V, L = 2.2µH, DCR = 8.3mΩ

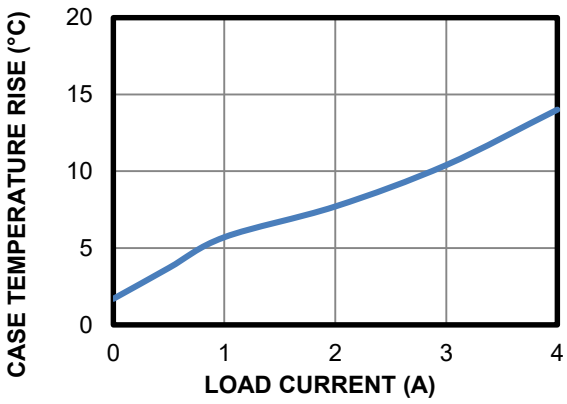


Line Regulation

V_{OUT} = 1V, L = 2.2µH, DCR = 8.3mΩ

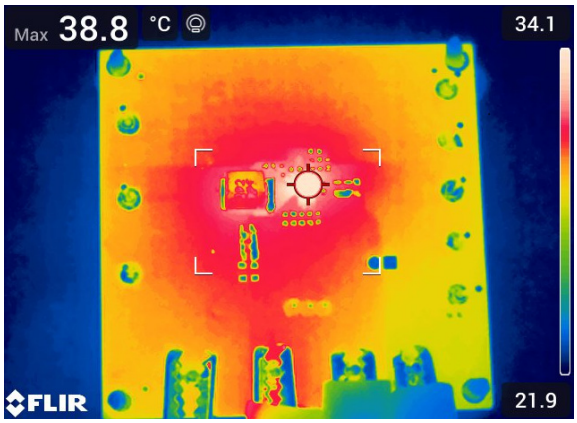


Case Temperature Rise vs. Load Current



Thermal Performance

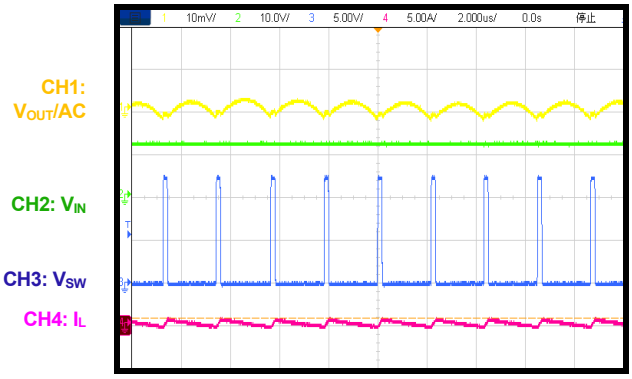
I_{OUT} = 4A, no forced airflow, T_{CASE} = 38.8°C



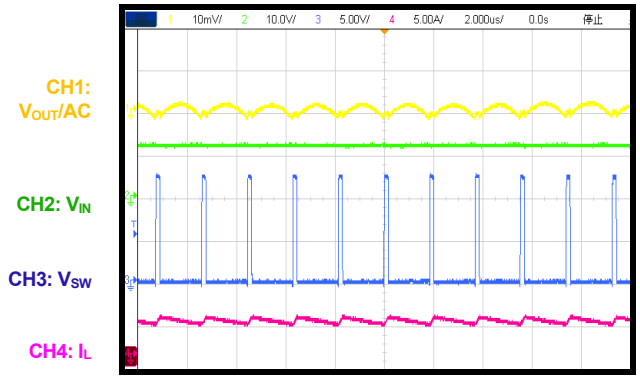
EVB TEST RESULTS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

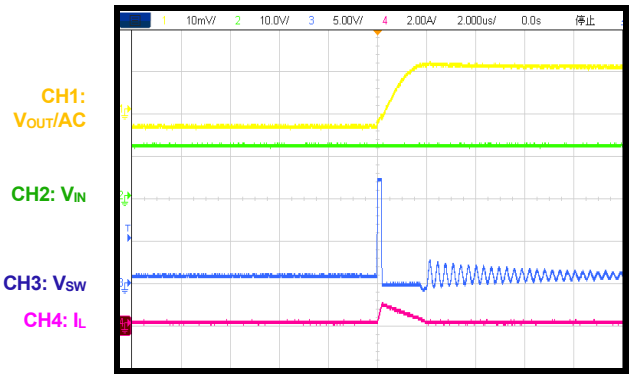
Steady State
I_{OUT} = 0A



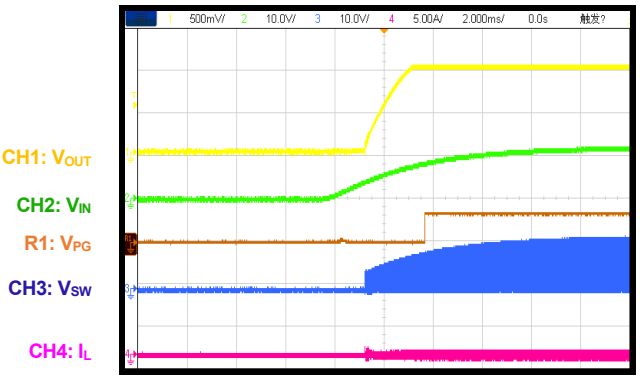
Steady State
I_{OUT} = 4A



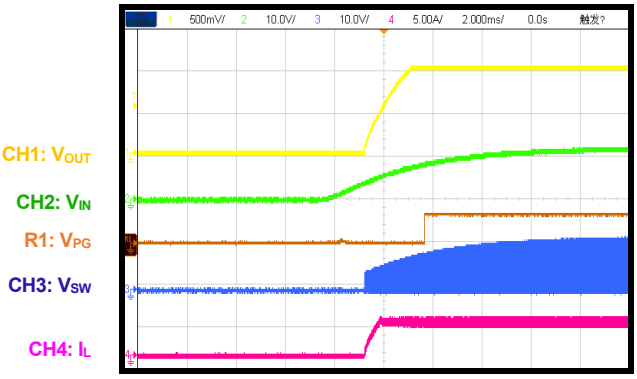
Steady State, PFM
I_{OUT} = 0A



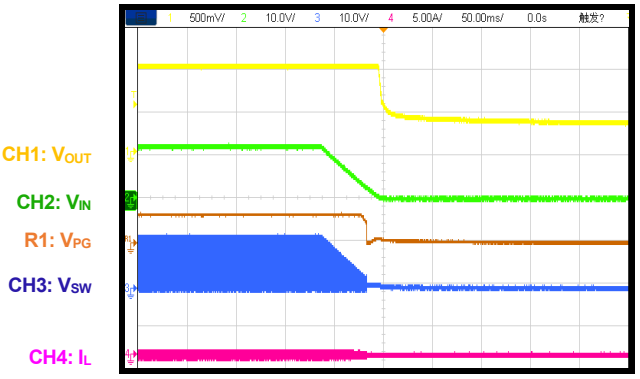
Input Power Start-Up
I_{OUT} = 0A



Input Power Start-Up
I_{OUT} = 4A



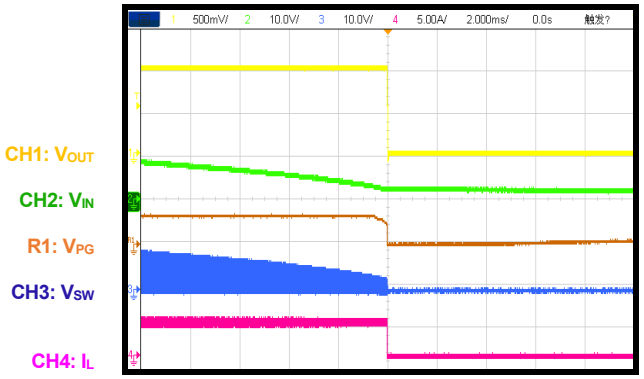
Input Power Shutdown
I_{OUT} = 0A



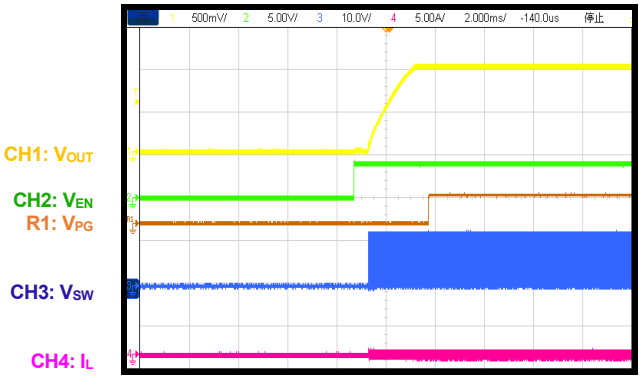
EVB TEST RESULTS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

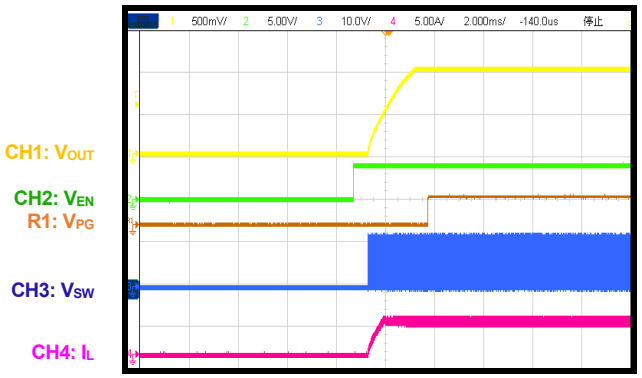
Input Power Shutdown
I_{OUT} = 4A



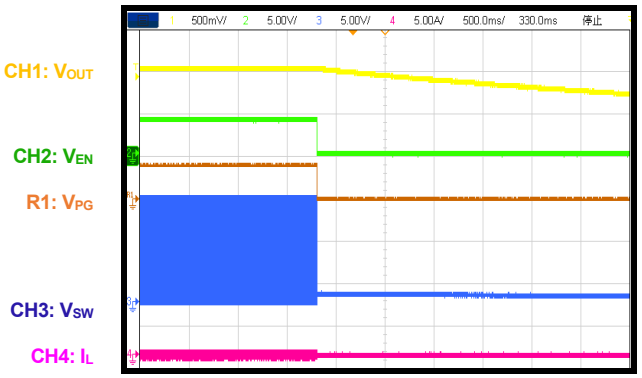
Start-Up through EN
I_{OUT} = 0A



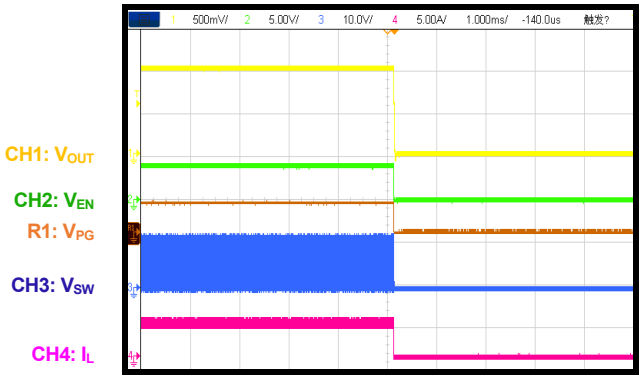
Start-Up through EN
I_{OUT} = 4A



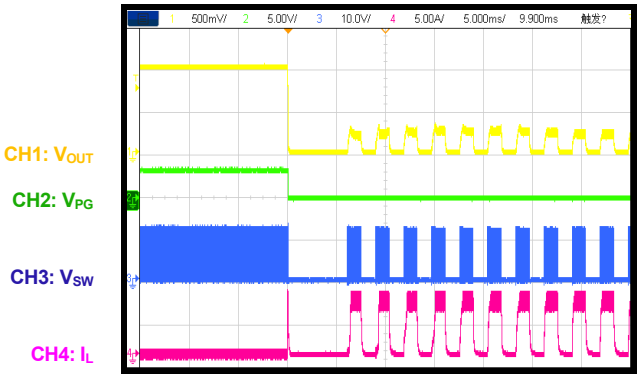
Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 4A



SCP Entry
I_{OUT} = 0A

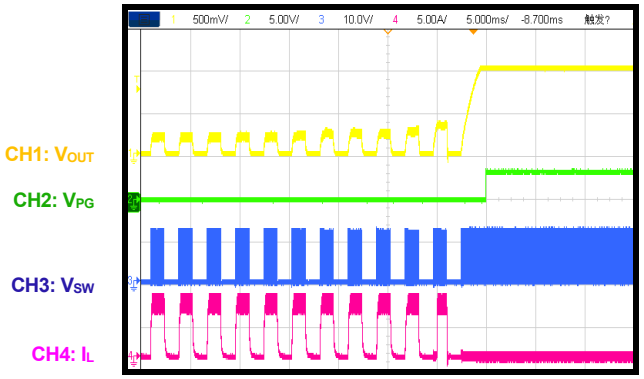


EVB TEST RESULTS *(continued)*

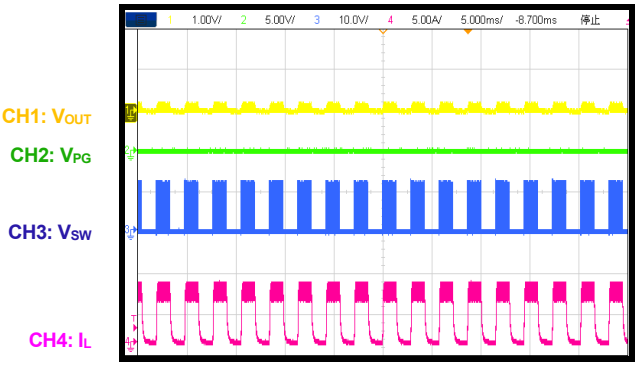
V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

SCP Recovery

I_{OUT} = 0A

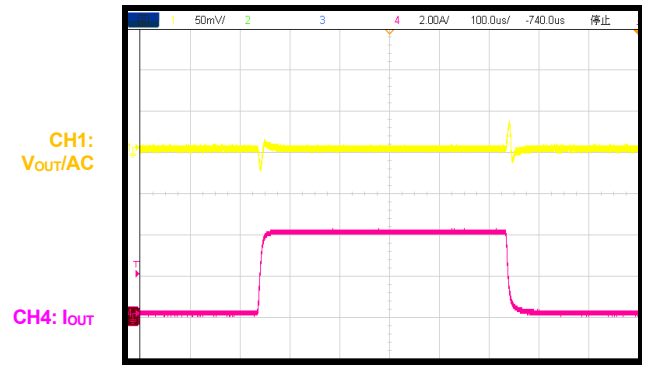


SCP Steady State



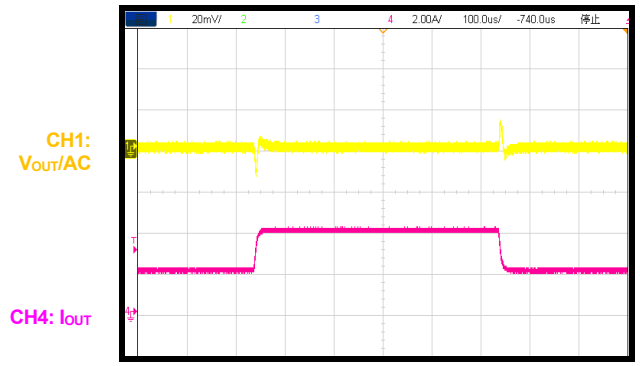
Load Transient

I_{OUT} = 0A to 4A, 2.5A/µs with e-load



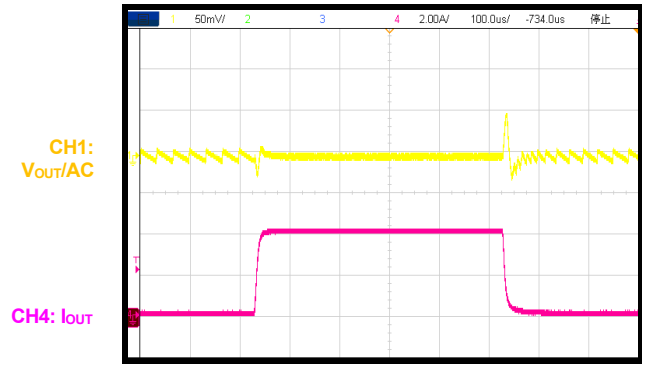
Load Transient

I_{OUT} = 2A to 4A, 2.5A/µs with e-load



Load Transient, PFM

I_{OUT} = 0A to 4A, 2.5A/µs with e-load



PCB LAYOUT

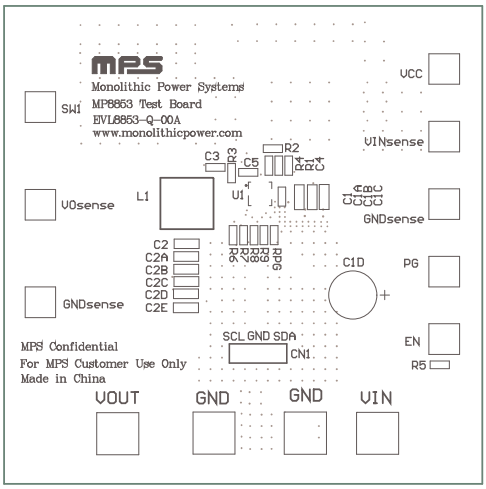


Figure 3: Top Silk

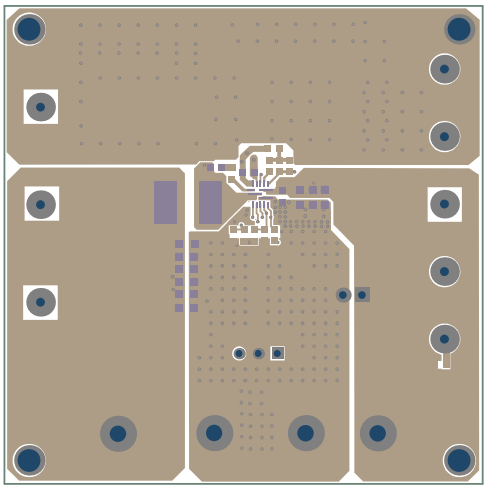


Figure 4: Top Layer

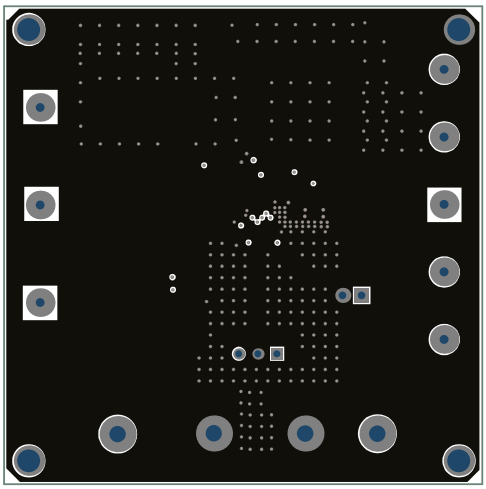


Figure 5: Mid-Layer 1

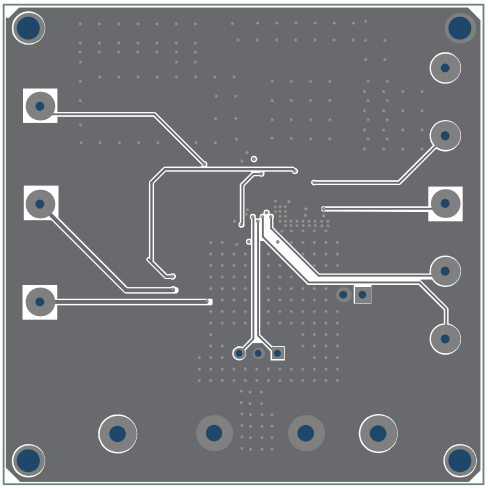


Figure 6: Mid-Layer 2

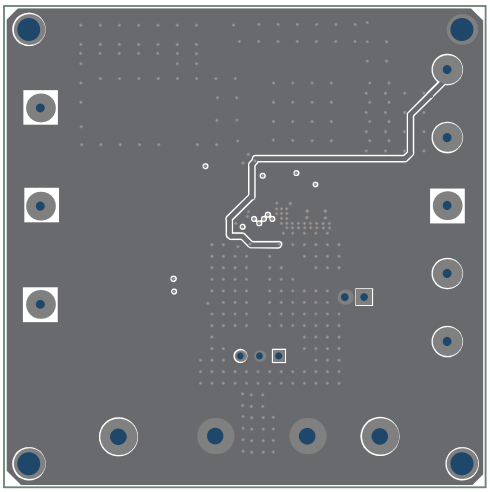


Figure 7: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/22/2024	Initial Release	-