EVL3439-C-00A

5.2V, 3A Dual-Phase Boost Converter with Output Disconnect and I²C Interface Evaluation Board

DESCRIPTION

The EVL3439-C-00A is an evaluation board designed to demonstrate the capabilities of the MP3439, a high-efficiency, synchronous, dual-phase boost converter with output disconnect function.

The MP3439 adopts constant-off-time control topology to provide fast transient response. The integrated synchronous MOSFETs disconnect the output from the input during shutdown. Dual-phasing switching with high frequency enables a small-sized power solution for up to 3A of load current from a 1-cell lithium battery.

The MP3439 features an I²C interface to configure the output voltage (V_{OUT}), current limit, and light-load operation mode. The MP3439 is available in a WLCSP-20 package.

It is recommended to read the MP3439 datasheet prior to making any changes to the EVL3439-C-00A.

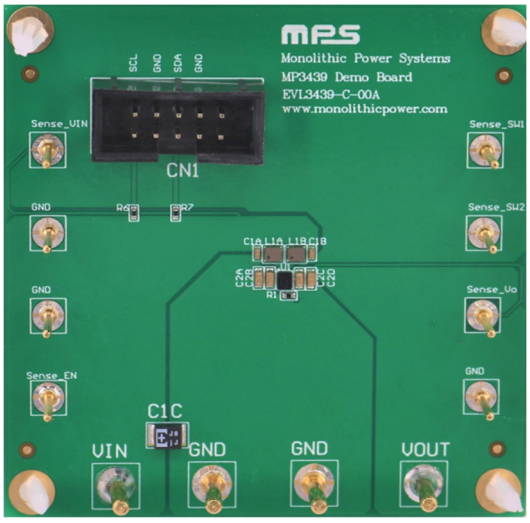
PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		2.7V to 5V
Output voltage (V_{OUT})		5.2V
Maximum output current (I_{OUT})		3A
Full load efficiency	V_{IN} = 4.2V, V_{OUT} = 5.2V, I_{OUT} = 3A, f_{SW} = 2MHz	95.2%
Switching frequency (f_{SW})		2MHz

MPL Optimized Performance with MPS Inductor MPL-AT2010 Series

EVALUATION BOARD



LxWxH (6.3cmx6.3cmx0.6cm)
2 Layers, 1oz/1oz

Board Number	MPS IC Number
EVL3439-C-00A	MP3439GC-0000

QUICK START GUIDE

The EVL3439-C-00A evaluation board is easy to set up and use to evaluate the performance of the MP3439. For proper measurement equipment set-up, refer to Figure 1 and follow the steps below:

1. Preset the power supply (V_{IN}) between 2.7V and 5V, then turn off the power supply.
2. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
3. Connect the load terminals to:
   a. Positive (+): VOUT
   b. Negative (-): GND
4. After making the connections, turn on the power supply.
5. Check for the proper output voltage (V_{OUT}) between the Sense_Vo to GND terminals.
6. The default V_{OUT} is 5.2V. If a different value is desired, configure V_{OUT} to a value between 5V and 5.5V via the I²C interface.
7. Once the proper V_{OUT} is established, adjust the load within the operating range, then measure the efficiency, output ripple voltage, and other parameters.
8. After completing all tests, adjust the load to 0A, then turn off the input power supply.

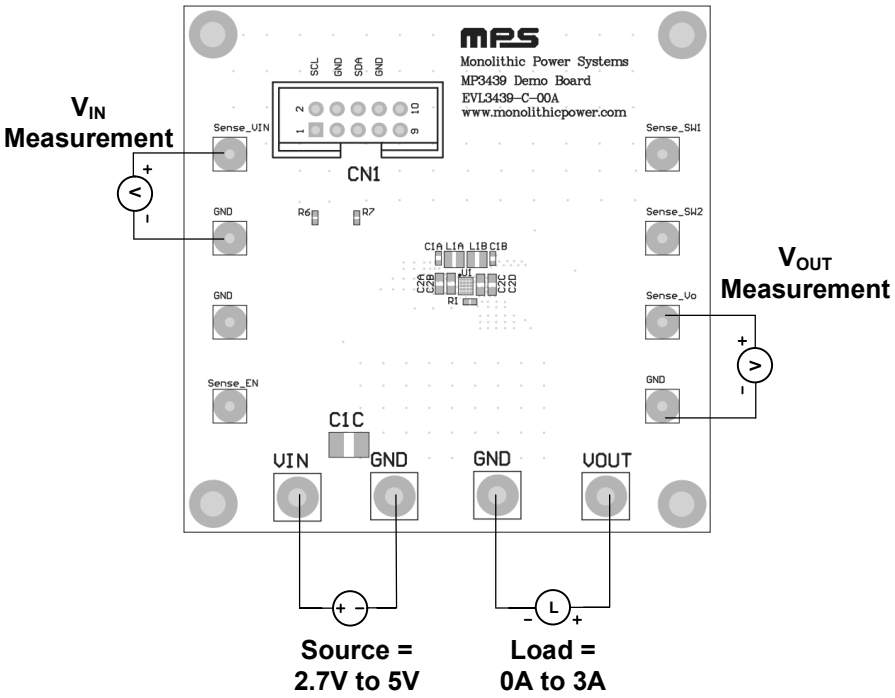


Figure 1: Proper Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

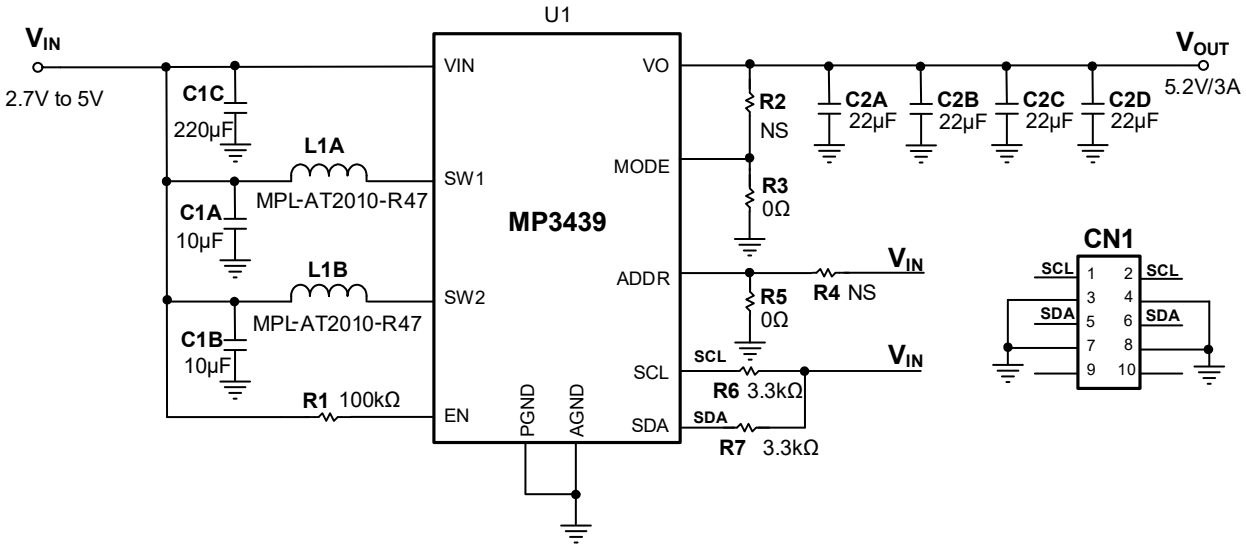


Figure 2: Evaluation Board Schematic

EVL3439-C-00A BILL OF MATERIALS

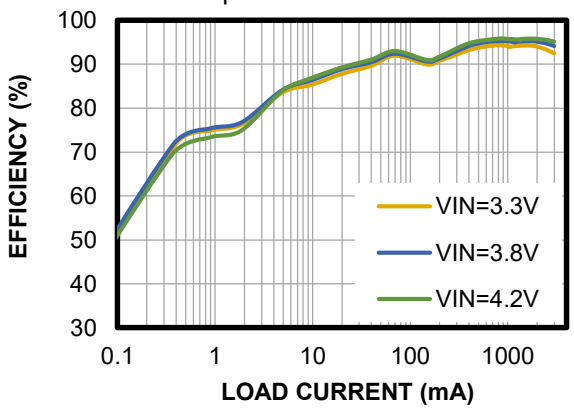
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	C1A, C1B	10µF	Ceramic capacitor, 6.3V, X5R	0402	Murata	GRM155R60J106ME44D
1	C1C	220µF	Polymer capacitor, 6.3V	SMD	Panasonic	6TPE220MAPB
4	C2A, C2B C2C, C2D	22µF	Ceramic capacitor, 10V, X5R	0603	Murata	GRM188R61A226ME15D
1	R1	100kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-07100KL
2	R3, R5	0Ω	Film resistor, 1%	0402	Yageo	RC0402FR-070RL
2	R6, R7	3.3kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-073K3L
2	R2, R4	NC				
1	CN1	10 pins	10-pin I²C connector	DIP	Wurth	612010235121
2	L1A, L1B	0.47µH	Inductor, R_{DC} = 27mΩ, I_{SAT} = 5.7A	SMD	MPS	MPL-AT2010-R47
1	U1	MP3439	5.2V, 3A, dual-phase boost converter	WLCSP-20 (1.75mmx 2.1mm)	MPS	MP3439GC-0000

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 3.8V, V_{OUT} = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

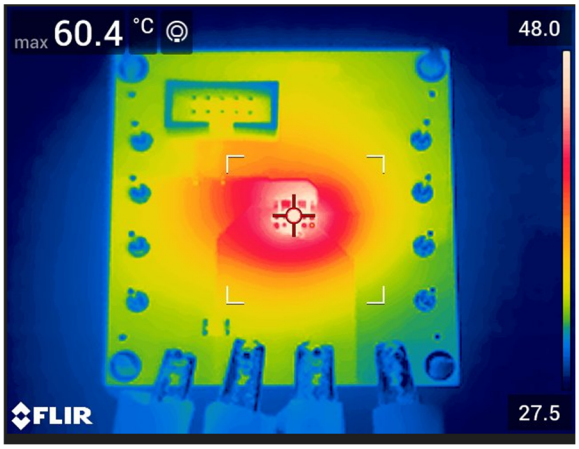
Efficiency vs. Load Current

Pulse-skip mode



Thermal Performance

V_{IN} = 3.8V, I_{OUT} = 3A, T_A = 28°C, no forced airflow

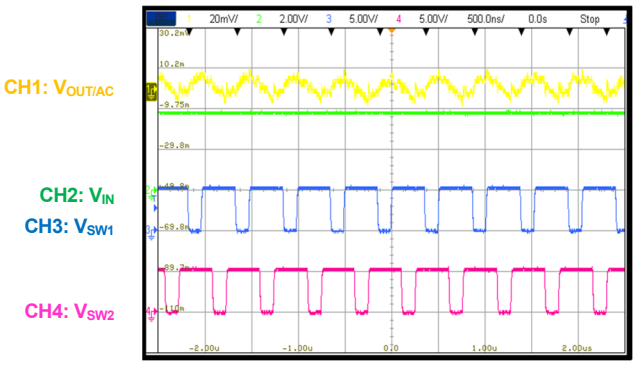


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 3.8V, V_{OUT} = 5.2V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

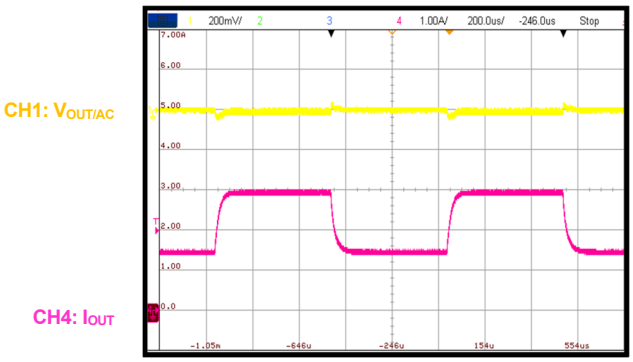
Steady State

I_{OUT} = 3A



Load Transient

I_{OUT} = 1.5A to 3A, I_{RAMP} = 25mA/µs



PCB LAYOUT

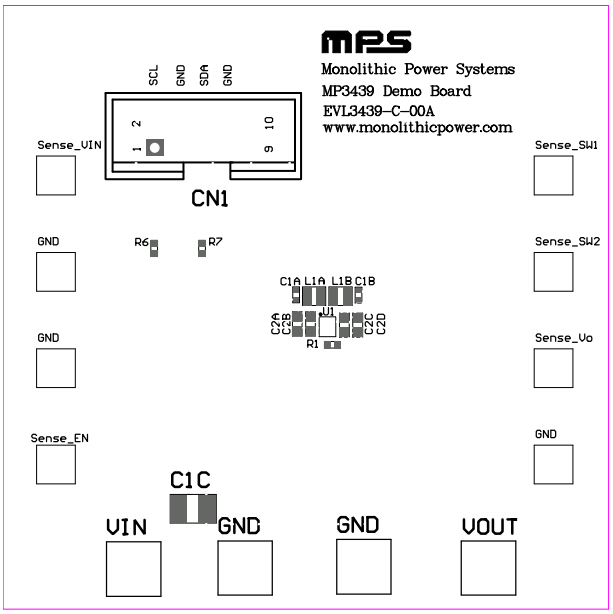


Figure 3: Top Silk

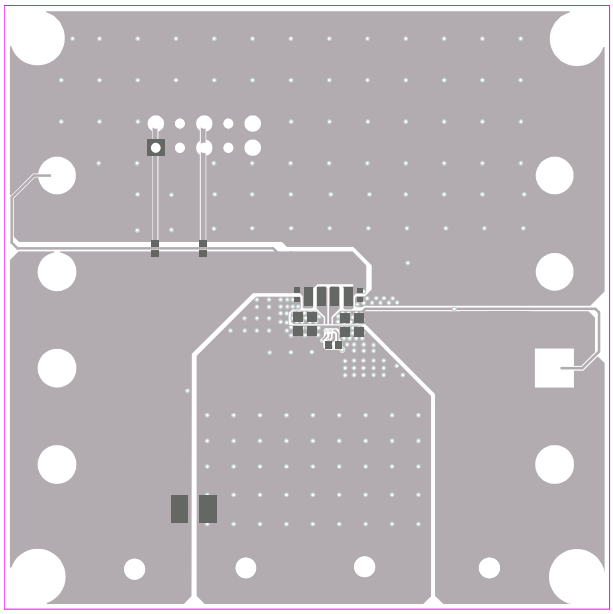


Figure 4: Top Layer

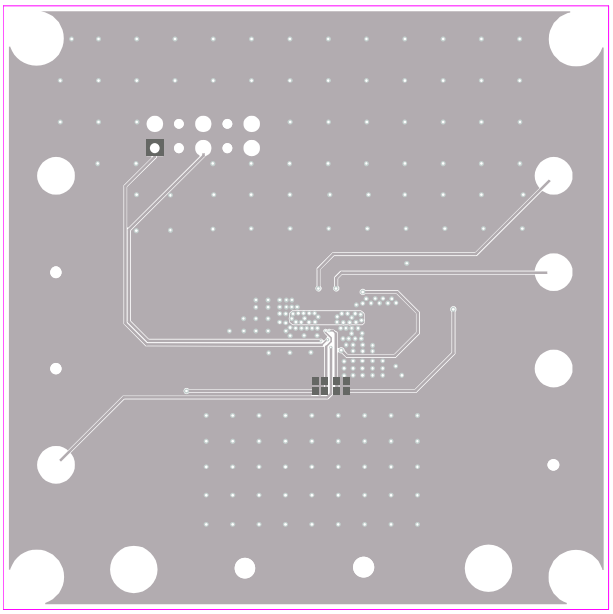


Figure 5: Bottom Layer

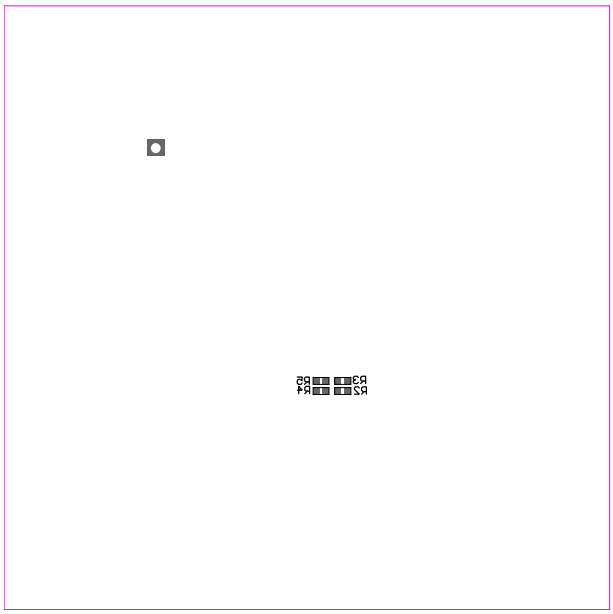


Figure 6: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/30/2023	Initial Release	-