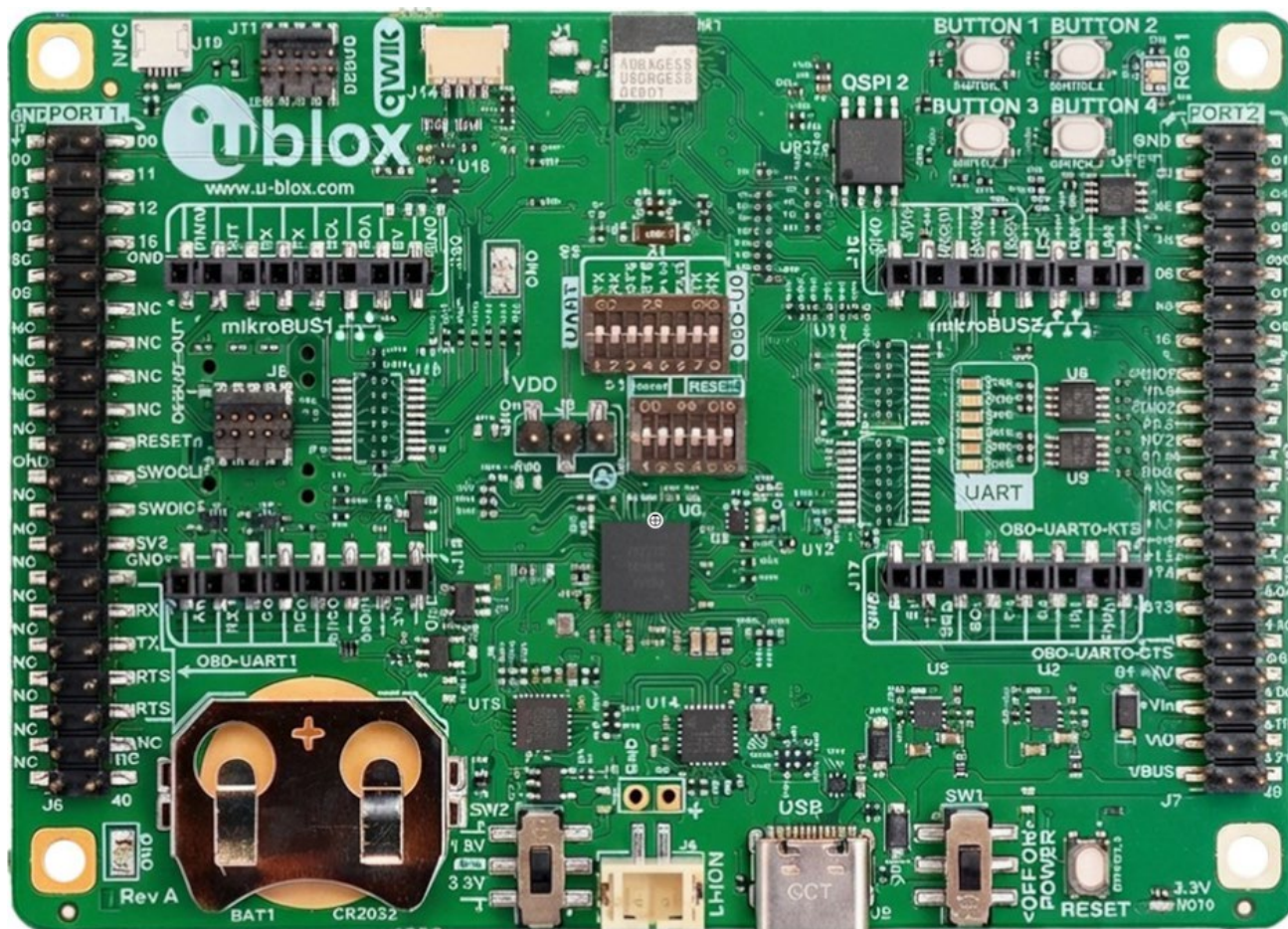


EVK-ANNA-B50

Evaluation kit for ANNA-B50 series modules

User guide



Abstract

The document describes how to set up and use the EVK-ANNA-B50 evaluation kits for prototyping ANNA-B50 Open CPU, Bluetooth LE applications. It also describes the different options for debugging and testing applications using the ANNA-B50 modules using the development capabilities included in the evaluation board.

Document information

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Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
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Mass production/ End of life	Production information	The document contains the final product specification.

This document applies to the following products:

Product name	Document status
EVK-ANNA-B505	Advance Information

-  For information about the hardware, software, and status of the available product types, see the ANNA-B50 datasheet [\[1\]](#).
-  The EVK-ANNA-B505 can be used to test both the ANNA-B505 and the ANNA-B501 modules.

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Contents

Document information	2
Contents	3
1 Product Description	5
1.1 Kit includes	6
1.2 Key features	6
1.3 Block diagram	7
2 Setting up the evaluation board	8
2.1 Powering up	8
2.2 COM port driver installation	8
2.3 Software development	8
3 Board configuration	9
3.1 Powering options	10
3.1.1 USB	10
3.1.2 Li-Ion battery or external supply 3.5 to 6 V	11
3.1.3 Coin cell battery	11
3.1.4 External supply, 1.7 – 3.5 V	11
3.2 Selecting the module supply voltage	12
3.3 Measuring current consumption	12
3.3.1 Current-sensing header	12
3.3.2 Using an ammeter	13
3.3.3 Using a voltmeter	13
3.3.4 Using an external power supply or power analyzer	13
4 Interfaces and peripherals	14
4.1 Buttons and LEDs	14
4.1.1 Reset	15
4.1.2 Buttons	15
4.1.3 LEDs	16
4.2 COM USB interface	16
4.3 UART connections	16
4.4 32.768 kHz low-frequency clock	16
4.5 Debug	17
4.5.1 External debugging	17
4.5.2 On Board debugger chip	17
4.6 QSPI external flash memory	18
4.7 NFC connector	18
4.8 Qwiic interface	19
4.9 mikroBUS sockets	19
4.10 Multipurpose GPIO header and Test Points	21
Appendix	25
A Schematics	25

B	Configuration possibilities for mikroBUS sockets	26
B.1	mikroBUS socket 1	26
B.2	mikroBUS socket 2	26
C	Modifying EVK to use U.FL connector	27
D	Glossary	28
	Related documentation	29
	Revision history	29
	Contact.....	30

1 Product Description

The EVK-ANNA-B50 evaluation kit provides a versatile development platform for the ANNA-B50 series modules, for quick prototyping of a variety of low-powered Internet of Things (IoT) applications supporting Bluetooth® Channel Sounding, and 802.15.4-2020 standards such as Thread®, Matter™, and Zigbee®.

The stand-alone ANNA-B50 module, included in the kit, is based on the Nordic Semiconductor nRF54L15 chipset, which features an Arm® Cortex®-M33 microcontroller with scalable memory configurations of 1.5 MB non-volatile memory (NVM), up to 256 kB RAM, and 128 MHz system clock. All features supported in the ANNA-B50 series modules are easily accessible from the Evaluation Kit (EVK).

[Table 1](#) describes the available evaluation kits.

Evaluation kit	Description	Suitable for
EVK-ANNA-B505	Evaluation kit (EVK) for evaluation of the ANNA-B505 or ANNA-B501 Open CPU modules. The default EVK configuration is to use the internal PCB trace antenna of ANNA-B505. To evaluate the external antenna of ANNA-B501 a hardware modification of the EVK is required.	ANNA-B505, ANNA-B501

Table 1: Available ANNA-B50 evaluation kits

 Refer to appendix [Modifying EVK to use U.FL connector](#) for instructions on how to modify the EVK-ANNA-B505 evaluation board to evaluate ANNA-B501 with an external antenna via a U.FL connector.

[Figure 1](#) shows the top view of the evaluation board.

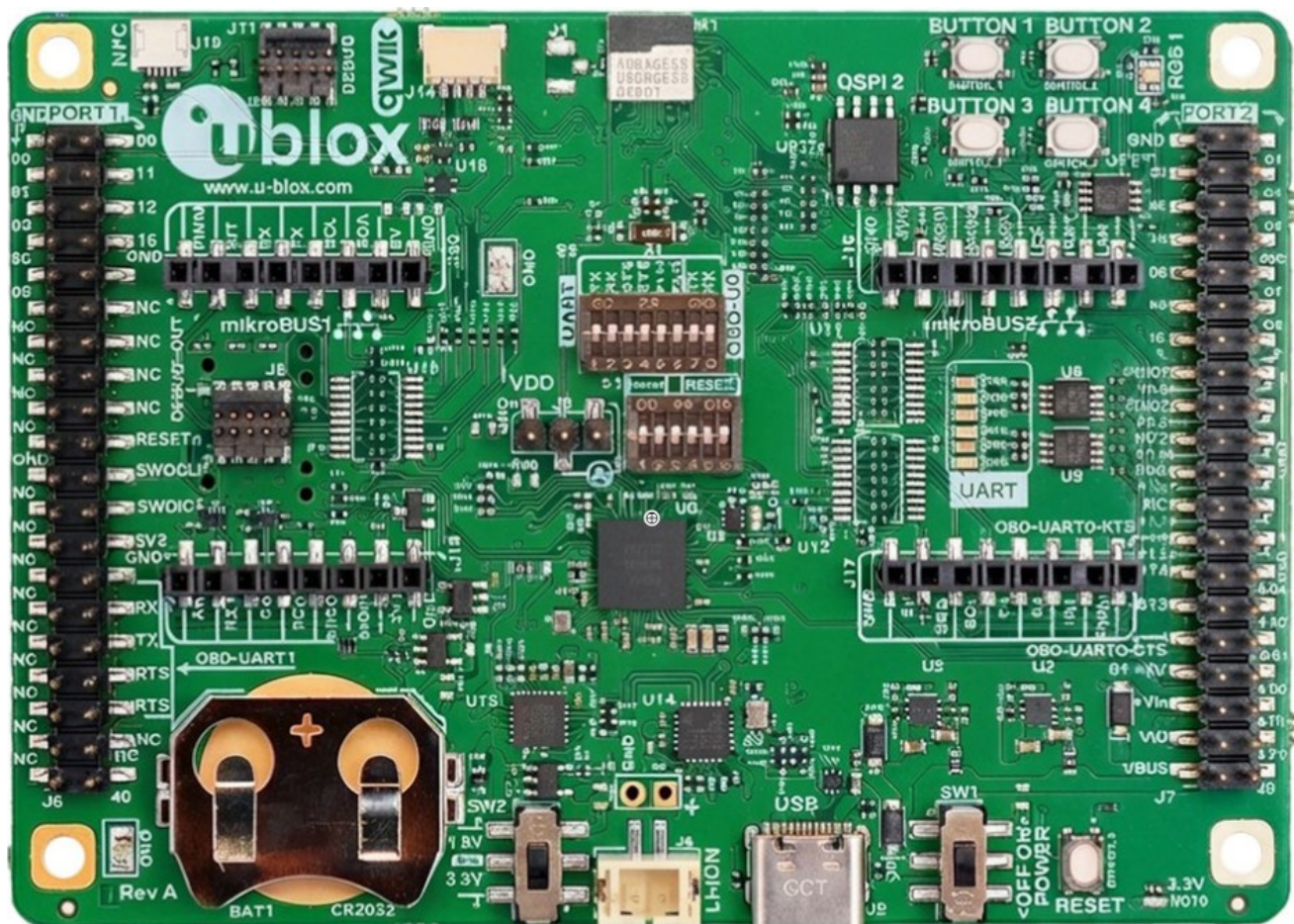


Figure 1: EVK-ANNA-B505 evaluation board (top view)

1.1 Kit includes

EVK-ANNA-B505

- Evaluation board with ANNA-B505 module (for evaluation of both ANNA-B501 and ANNA-B505)
- USB-C to USB-A cable
- NFC antenna

1.2 Key features

EVK-ANNA-B505 provide:

- Evaluation board for evaluation of ANNA-B501 or ANNA-B505 modules
- Module supply voltage of 3.3 V or 1.8 V
- COM ports and debug ports over USB
- 32x GPIOs accessible on pin sockets and test points
- An on-board SEGGER J-link OB programmer/debugger, with external Debug-out option
- Buttons and status LEDs for user interaction
- 2x mikroBUS™ compatible pin sockets. Visit the MikroE website [\[4\]](#) for more information
- SOIC-8 external flash memory
- 32.768 kHz crystal
- USB peripheral connector
- Power input through USB-C, pin sockets, Li-ion, or coin cell battery
- Current measurement access points from pin headers and jumpers
- NFC connector
- QWIIC® connector through level shifter

Figure 2 shows the major interfaces and internal connections supported on the EVK.



2 Setting up the evaluation board

Follow the instructions in this section to power up the EVK and prepare it for PC communication and software development.

 The EVK is delivered without any software and the software must be developed by the user. For more information, see [Software development](#).

2.1 Powering up

 For EVKs with U.FL connector: Before powering up the board, make sure to connect the 2.4 GHz antenna to the U.FL antenna connector **J1**. Failing to do so can cause module malfunction.

1. Insert the USB cable to a PC and connect it to the type-c connector, **J2**, on the EVK.
2. Set the power switch, **SW1**, to ON.

The green status LED (**D19**) and OBD chip status LED (**D16**) are lit when the EVK has powered up correctly.

 Further powering options for current measurement and use of other power sources are described in [Powering options](#).

2.2 COM port driver installation

The host operating system installs the correct COM port drivers automatically. The drivers need to be installed only when you connect the unit to a new computer for the first time. For more information about the COM ports and their configuration, see the FTDI FT231XQ-R Datasheet [\[2\]](#).

Windows OS automatically assigns three COM ports to the unit:

- “USB Serial Port” - the module's main UART used for serial communication by default.
- “JLink CDC UART Port” - Onboard Debugger (OBD) ports, UART0 and UART1. See also [Schematics](#).

To view the assigned COM ports on Windows open **Device Manager** and view the assigned COM ports.

2.3 Software development

The Open CPU architecture of ANNA-B50 series modules allows integrators to develop and run their applications on the built-in Arm® Cortex®-M33 core. For development, u-blox recommends the Nordic Semiconductor nRF Connect SDK, [\[5\]](#) which includes the Zephyr Real-Time Operating System (RTOS), the MCUboot secure bootloader, and Nordic Semiconductor's nrfxlib device drivers for the nRF54L15 and peripherals. See also the ANNA-B50 system integration manual [\[2\]](#).

3 Board configuration

The EVK is equipped with several connectors for power (**J2**, **J4**, and **J5**) and antenna (**J1**). It also supports connections for current measurement (**J3**), several I/O interfaces for mikroBUS Click add-on boards (**J17-J20**), flash and debug ports (**J9** and **J11**), multi-purpose GPIOs (**J7** and **J8**), and extended I2C communication (**J14**).

Figure 3 shows available connectors on the EVK.

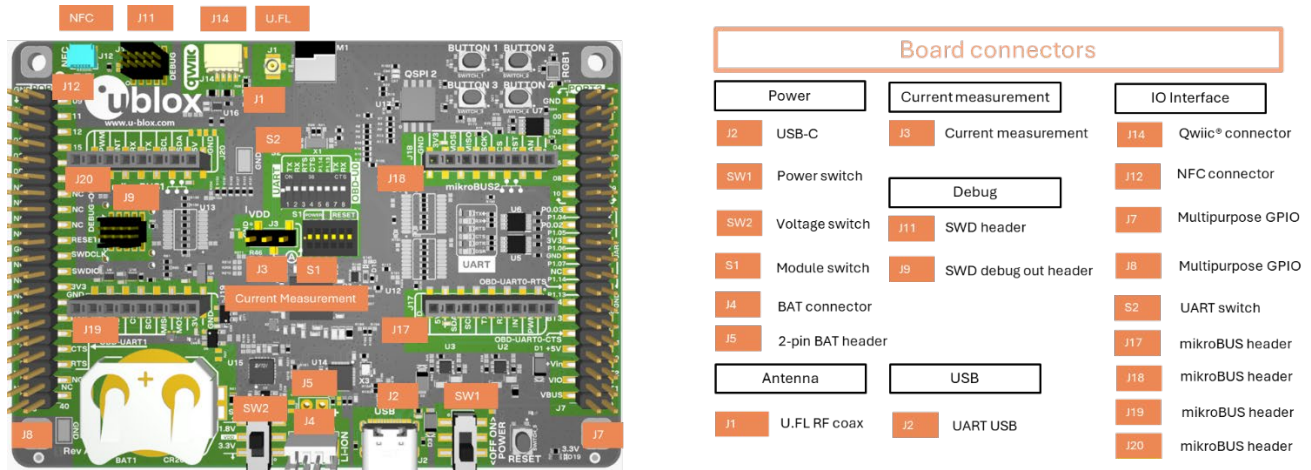


Figure 3: Available connectors on EVK. The U.FL connector is only available after hardware modification.

Table 2 describes the connectors supported by the EVK, as shown in Figure 3.

Connector	Function	Description
J1	2.4 GHz RF antenna connector	U.FL coaxial connector for antennas or RF equipment (not mounted by default, but can be mounted by the user to evaluate ANNA-B501)
J2	Power supply, COM port and debug USB	Main USB connector for programming, debugging, and communication with the module. This is the primary connector for powering the entire board.
J3	Current consumption header	Pin header for measuring the current consumption across the input voltage (VDD) of the module
J4	Li-Ion battery connector	2-pin JST Li-Ion battery power from the Li-Ion rechargeable battery
J5	Generic 2-pin header	2.54 mm, 2-pin header for connecting a battery without a standard JST connector. Not mounted by default.
J7	Generic 40-pin header	2.54 mm 40-pin header connected to multipurpose GPIOs on the module
J8	Generic 40-pin header	2.54 mm 40-pin header connected to multipurpose GPIOs on the module
J9	Cortex Debug connector	10-pin, 50 mil pitch connector that can be used to connect external target to the OBD. The board supports the SWD debug interface.
J11	Cortex Debug connector	10-pin, 50 mil pitch connector for connecting external debuggers to the NORA module. The module supports the SWD debug interface.
J12	NFC connector	5-pin connector compatible with the NFC
J14	QWIIC connector	4-pin connector compatible with the Qwiic connect system for extending the I2C interface – as defined by SparkFun Electronics
J17, J18	mikroBUS connector	mikroBUS socket 2 for hosting mikroBUS add-on boards on the module
J19, J20	mikroBUS connector	mikroBUS socket 1 for hosting mikroBUS add-on boards on the module
S1	Dual switch	DIP switch/SIP switch for disconnecting the module VDD
SW1	Power ON switch	Main power switch
SW2	Voltage mode for the module	1.8 V or 3.3 V select
BAT1	Coin cell holder	CR2032 Coin cell battery holder

Table 2: EVK connector description

3.1 Powering options

Power to the EVK can be supplied in several ways:

- +5 V USB connector (**J2**)
- 3.5 – 6 V power source to pin header (**J7** pin 35)
- 3.5 – 6 V Li-ion battery to the battery connectors (**J4** or **J5**)
- Coin cell battery in battery connector (**BAT1**)

The USB type C connector is only capable of handling 5 V input. The 12 V voltage rail is disabled. Each of the power supply sources are distributed throughout the EVK, as shown in [Figure 4](#).

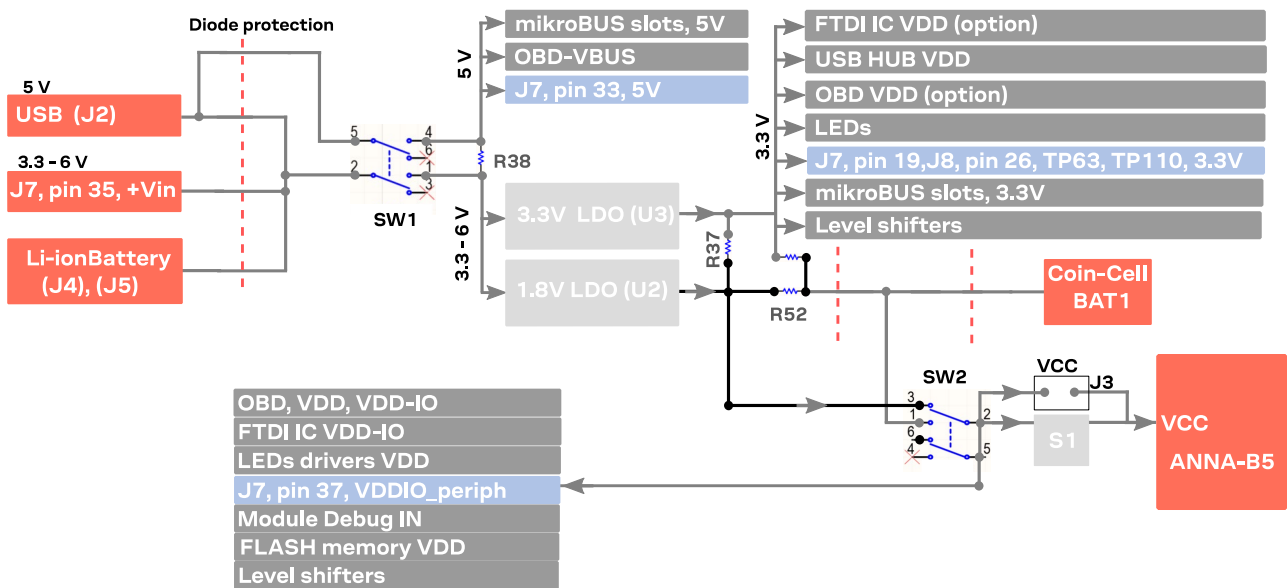


Figure 4: power net distribution block diagram .

- Coin cell battery (**BAT1**) only powers the module.
- All supplies are protected by reverse voltage diodes and can be connected simultaneously.

3.1.1 USB

1. Connect the USB Type-C connector to **J2**
2. Turn on the power switch, SW1

[Figure 5](#) shows the power set-up for using the EVK with a USB connector.

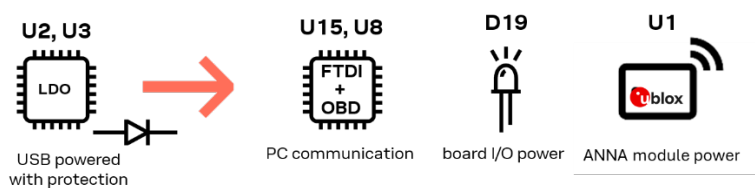


Figure 5: Configuration for using the EVK with a battery

3.1.2 Li-Ion battery or external supply 3.5 to 6 V

1. Connect a battery or external power source through connectors **J4** or **J5**.
2. Turn on the power switch (**SW1**).

PC communication between the EVK and the module can be made through the USB connector (**J2**).

Figure 6 shows the configuration for using the EVK with a battery or external power supply.

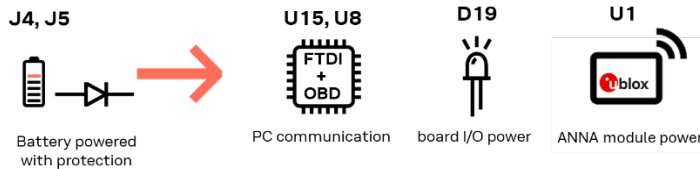


Figure 6: Configuration for using the EVK with a battery or other power source

3.1.3 Coin cell battery

1. Set **SW2** to the 3.3 V position
2. Disconnect the Peripherals' voltage supply by setting position 2 (left side) on switch **S1** to off
3. The coin cell battery will only supply power to the module, and the OBD chip will not be powered.
4. FTDI chip and UART LEDs can be disconnected from the module by turning off switch **S2**.
5. Insert a coin cell battery to battery connector (**BAT1**)

Figure 7 shows the configuration for using the EVK with a coin cell battery.

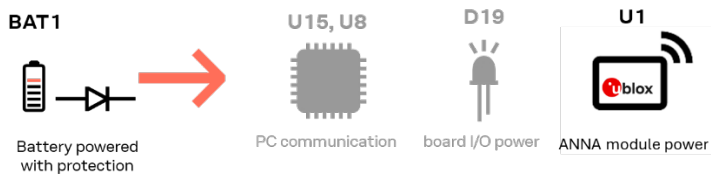


Figure 7: EVK coin cell battery configuration

3.1.4 External supply, 1.7 – 3.5 V

When measuring current consumption or performing other characterization measurements on the module, it is useful to power the module from an external source, such as a lab power supply. In such cases, connect the power supply for the module to **VDD (J3 pin 2)** and **GND (J3 pin 1)**. If the OBD chip will not be powered, refer to the section [Coin cell battery](#) for how to configure the reset.

Figure 8 shows the optional jumper connections for supplying the module with an external supply.

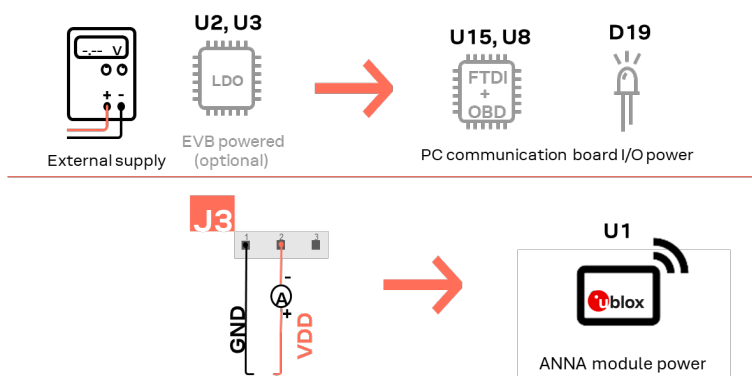


Figure 8: External power supply option

3.2 Selecting the module supply voltage

The EVK supports both 1.8 V and 3.3 V supply voltage to the module.

To select either 1.8 V or 3.3 V for the module and other peripherals, set switch (**SW2**) as shown in [Figure 9](#).

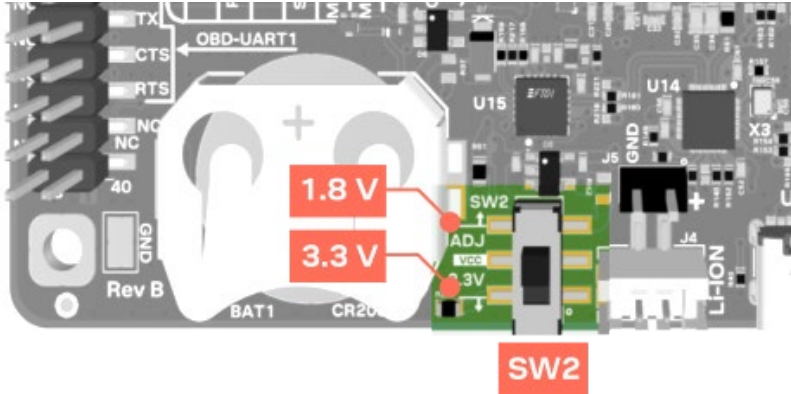


Figure 9: Voltage switch SW2

3.3 Measuring current consumption

Before making current consumption measurements, review the available [Powering options](#) to find out which module signals must be isolated for your chosen power configuration.

3.3.1 Current-sensing header

The evaluation board provides a 3-pin header with 2.54 mm pitch, **J3**, for power consumption measurement of the module's **VDD** supply. The current can be measured either with ammeter or voltage meter as described in [Using an ammeter](#) and [Using a voltmeter](#).

R46, which is intended to be mounted when measuring the current with a voltage meter, is connected between J3 pin 2 and 3.

[Figure 10](#) shows the EVK current-sensing header circuits.

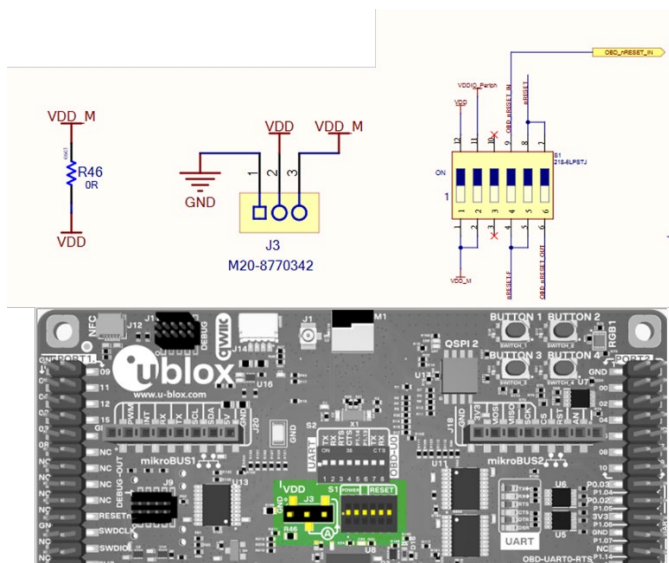


Figure 10: Current-sensing header circuits

3.3.2 Using an ammeter

To measure the current, connect the ammeter in series with the power source between **pin 2** and **3** of **J3**. In this way, the current is measured when the module is supplied from either the onboard regulator or an external supply, as shown in [Figure 11](#). Ensure that switch **S1** is in the off position for positions 1, 2, 4, and 6. **S1** is shown in [Figure 10](#) above.

3.3.3 Using a voltmeter

The EVK must be modified before the module current can be measured with a voltmeter.

To modify the board, solder low-resistance, high-tolerance, 0603-sized resistors to the footprint labeled **R46**, as shown in [Figure 11](#). This resistor replaces the jumpers and any current running through it produces a voltage across its terminals. Measure this voltage with the voltmeter and calculate the current using Ohm's law. Ensure that switch **S1** is in the off position for both channels.

3.3.4 Using an external power supply or power analyzer

Connect the terminals of the instrument to the EVK pins, as shown in [Figure 11](#). An ammeter can also be added in series. Ensure that switch **S1** is in the off position for both channels.

When using a power analyzer that both provides supply voltage and measures current, ensure that other EVK peripherals and components are disconnected from this supply. Failure to do so will introduce measurement errors – even if the other components are supplied with the same voltage level from another LDO or source.

To reduce leakage current, use a second external power channel to supply EVK peripherals. This second channel must also be used to enable PC communication.

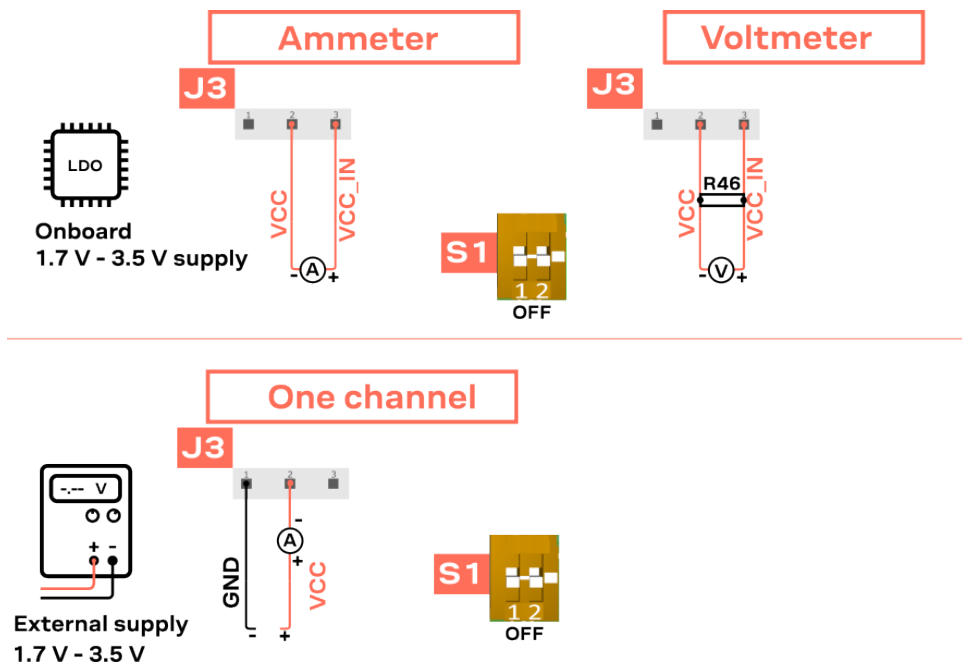


Figure 11: Options for measuring module current consumption

4 Interfaces and peripherals

Design files for the EVK PCB are available from your local [u-blox support team](#).

4.1 Buttons and LEDs

Figure 12 shows the position of the push buttons and LEDs on the evaluation board.

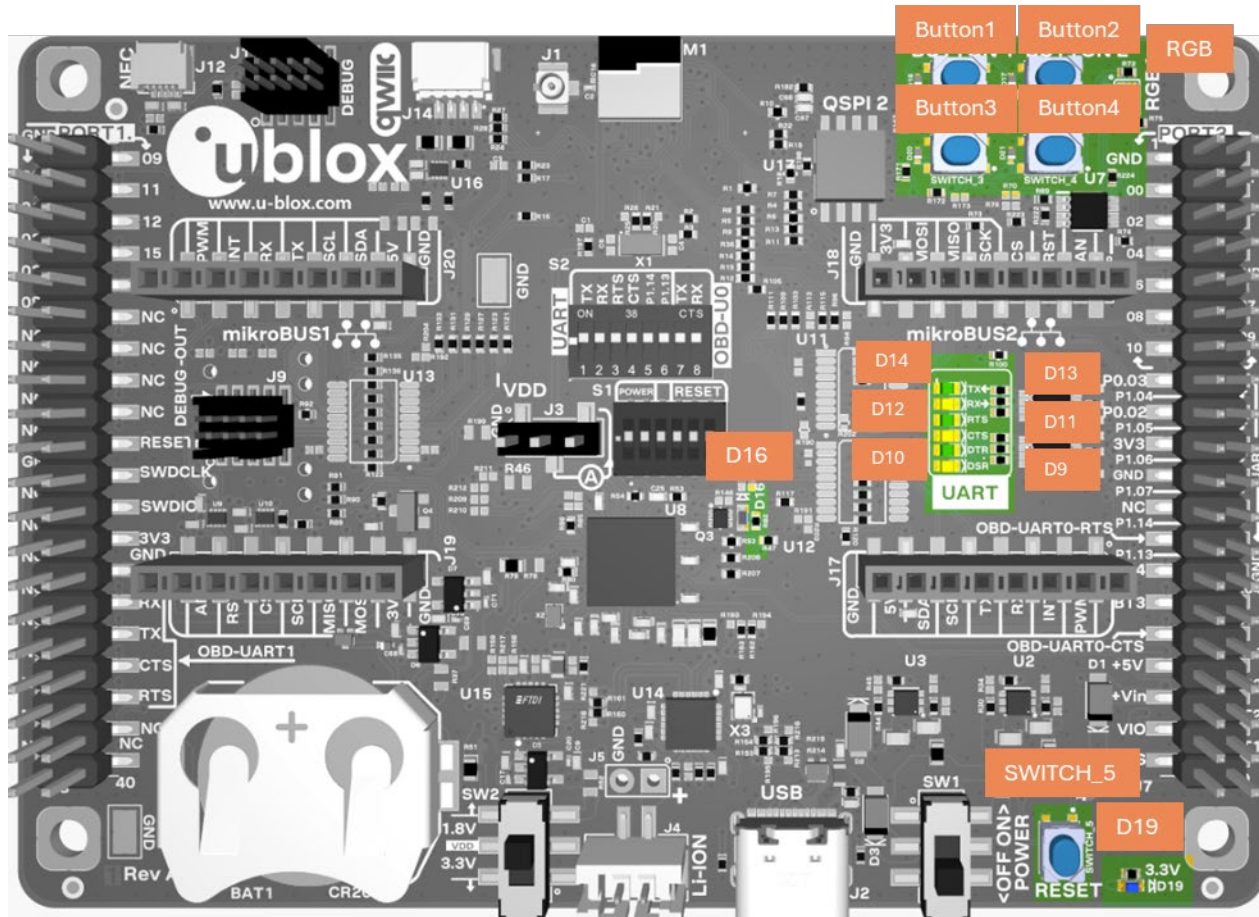


Figure 12: Evaluation board – showing position of the push buttons and LEDs

4.1.1 Reset

Press the **RESET** Button (**SWITCH_5**) to set **nRESET** low and reset the module.

nRESET is also available on:

- Module debug-in connector: **J11** pin 10, where **nRESET** resets the module.
- mikroBUS: **J18** pin 2. Output
- mikroBUS: **J19** pin 2. Output
- Pin header: **J8** pin 20, where **nRESET** is an input signal.

The module can also be reset through the OBD chip. Set S1 switch 6 in ON state to enable reset from OBD chip.

4.1.2 Buttons

In addition to the **RESET** button, the evaluation board also supports four user buttons (**Button1**, **Button2**, **Button3** and **Button4**) that are active-low and connect to GND when pressed. The functionality of these buttons is controlled by the system software through the GPIO interface.

The four user buttons also have an optional connection to the pin headers through the resistors described in [Table 3](#). Each button is associated with specific connections and components.

 For proper operation, the internal pull-up resistor of each GPIO pin must be enabled.

Figure 13 shows the schematics for the four user buttons.

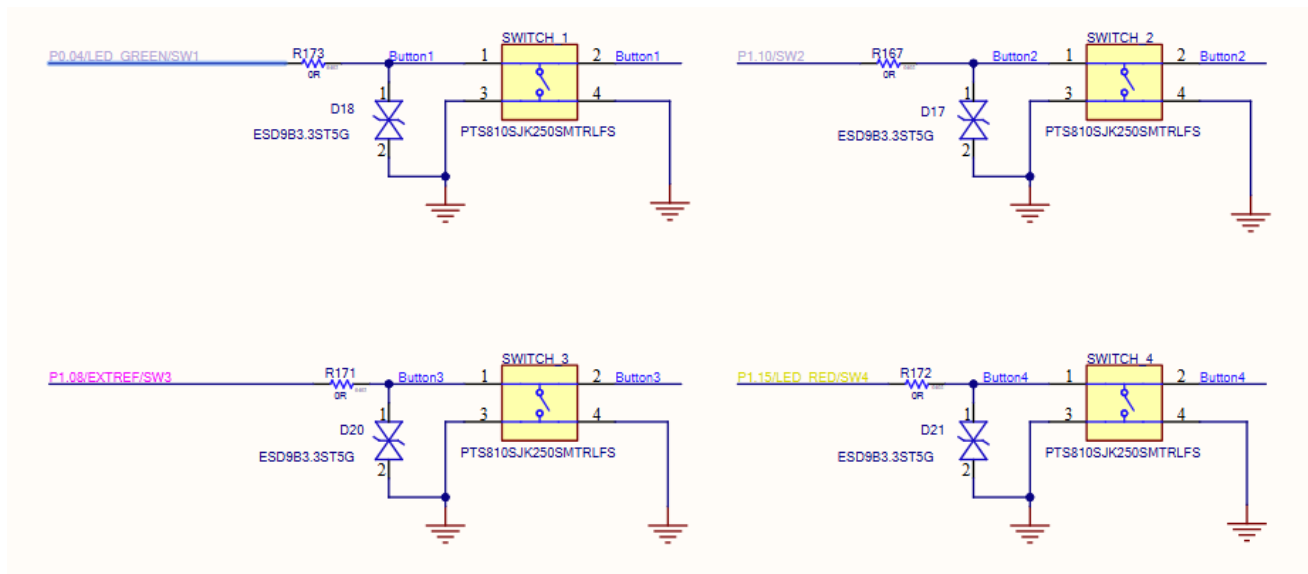


Figure 13: Four user buttons – schematics

Name	Switch	Pin	Pin header	Function
Button 1	SWITCH_1	P0.04	J7-pin 30	No predefined function (software controlled)
Button 2	SWITCH_2	P1.10	J7-pin 32	No predefined function (software controlled)
Button 3	SWITCH_3	P1.08	J8-pin 11	No predefined function (software controlled)
Button 4	SWITCH_4	P1.15	J8-pin 8	No predefined function (software controlled)

Table 3: User button components

4.1.3 LEDs

The EVK includes eight status LEDs and one RGB status LED:

- **Power status (D19):** Indicates the **+3.3V** power on the board when lit (green)
- **Power and activity status (D16):** Indicates the output of the voltage follower circuit and the OBD activity (green).
- **UART1 status (D9-D14):** Indicates UART1 signal status under GPIO control.
- **System status (RGB1):** Powered by **+3V3** and turned on by setting the associated GPIO low.

[Table 4](#) describes the association between each RGB LED and the respective GPIO.

RGB LED	Default GPIO
Red	P2.09
Green	P2.07
Blue	P1.09

Table 4: RGB LED associated signals

4.2 COM USB interface

Three COM ports are available for connecting the PC via the USB connector:

- USB serial port for the main UART
- Two CDC UART ports

4.3 UART connections

Switch **S2** connects FTDI chip to the module UART1 and pin header and OBD chip to the module UART0 if set ON. If switched OFF the corresponding UART signal is only connected between pin header and ANNA-B5.

- **S2 – OFF.** UART0 and UART1 connected from ANNA-B5 to pin header
- **S2 – ON.** UART0 connected from ANNA-B5 to pin header and OBD chip. UART1 connected from ANNA-B5 to pin header and FTDI chip

Module pin name	Pin	Pin socket
UART1-TxD	P1.04	J7-16
UART1-RxD	P1.05	J7-18
UART1-CTS	P1.07	J7-22
UART1-RTS	P1.06	J7-20
UART0-TxD	P0.00	J7-36
UART0-RxD	P0.01	J7-34

Table 5: UART pins and socket header connections

4.4 32.768 kHz low-frequency clock

The EVK has a 32.768 kHz crystal (**X1**), which is connected to the module. This provides an external crystal option to source the RTC clock.

Loading capacitors for the oscillator circuit of the module are internal to the nRF54L15. The capacitance is set by software between 4 pF and 18 pF in 0.5 pF steps [\[2\]](#).

The EVK also provides an option to use external capacitors in positions **C4** and **C5**.

If an internal low-frequency clock source is used, you can disconnect the circuit by removing resistors **R20** and **R25**, as shown in [Figure 14](#).

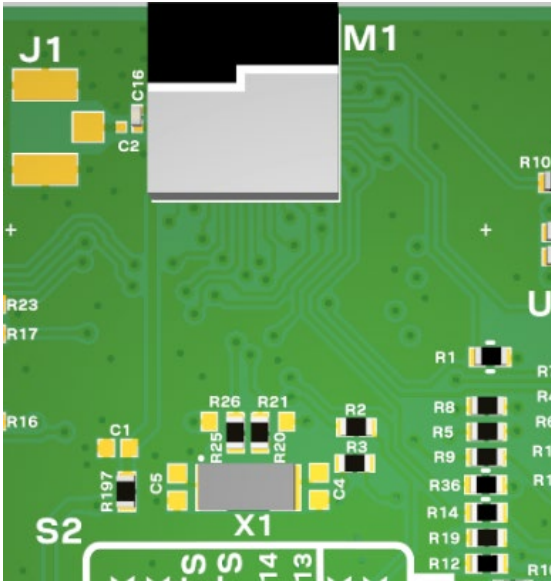


Figure 14: PCB placement of crystal X1 and capacitors C4 and C5.

- ✎ The internal load capacitance of the low-frequency oscillator must be set according to u-blox board configuration settings, which are described in the u-blox openCPU GitHub repository [7].

4.5 Debug

4.5.1 External debugging

The module supports firmware programming and debugging through its SWD interface, which includes two external interfaces for connecting a debug unit:

- **J11** is implemented through a 10-pin connector.
- **J13** is implemented through a 10-pin needle adapter. **J13** is not enabled by default. To enable **J13** mount 0402 0Ω resistor in positions **R164**, **R165**, and **R166**.

- ✎ The external debugger requires the installation of Nordic nRF Command Line Tools [6] and SEGGER J-Link debugger application.

4.5.2 On Board debugger chip

The EVK includes an nRF5340 onboard debugger chip (OBD), **U8**. The OBD can be programmed through the connector **J10**.

The OBD also supports a debug-out function for using the EVK for debugging other boards based on Nordic Semiconductor SoCs through the header **J9**.

4.6 QSPI external flash memory

Figure 15 shows the schematic of the external SOIC-8, 64 Mbit, Quad SPI Flash circuit and its implementation on the EVK board.

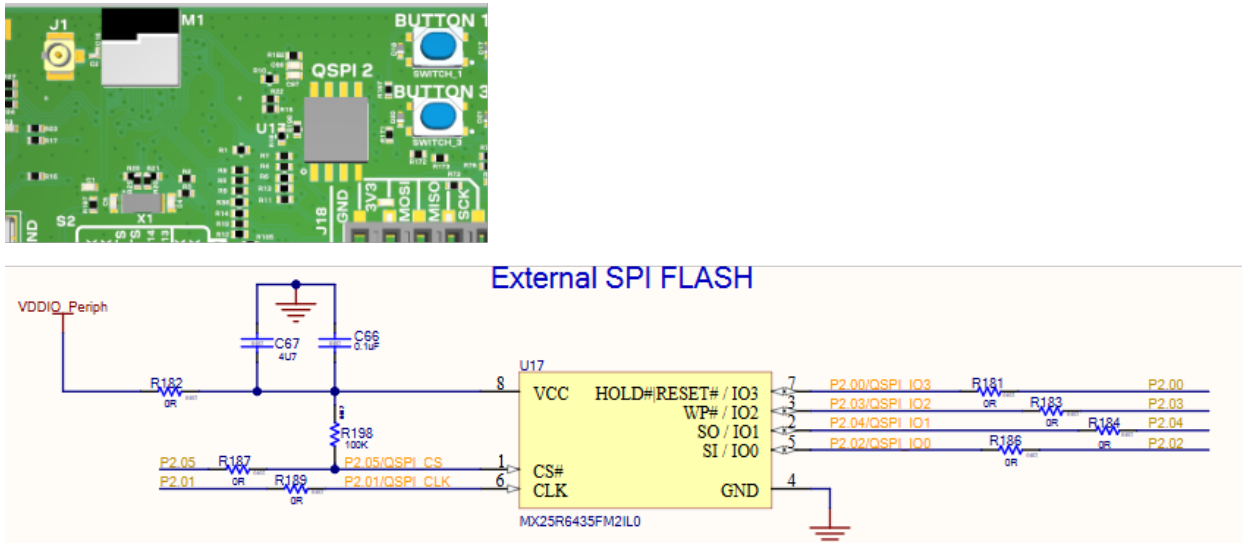


Figure 15: Quad SPI Flash EVK – EVK board view (top) and schematic (below)

Table 6 shows the SPI functions for corresponding nRF54L15 GPIOs and module pins.

Interface function	Resistor (0 Ω)	Module pin	Interface IC function
QSPI-CS	R187	P2.05	FLASH chip select
QSPI-CLK	R189	P2.01	SPIO clock
QSPI-IO3	R181	P2.00	SPI Input/Output 3
QSPI-IO2	R183	P2.03	SPI Input/Output 2
QSPI-IO1	R184	P2.04	SPI Input/Output 1
QSPI-IO0	R185	P2.02	SPI Input/Output 0

Table 6: Quad SPI interface signal overview for external flash

The resistors are placed under the QSPI memory.

To connect the module pins to pin header J7 remove the QSPI memory and mount the resistors listed in Table 6.

4.7 NFC connector

Connect the NFC antenna through connector **J12**. The tuning capacitors mounted on the EVK. To use the supplied NFC antenna, select **C62** and **C63**.

The values of **C62** and **C63** might need to be changed if a different antenna is used.

The NFC antenna can be connected in both directions to **J12**.

By default, the module pins **P1.02** and **P1.03** are configured for NFC use. By modifying the population of **R55**, **R56**, and the value of the PADCONFIG register, these pins can also be used for digital GPIO.

Figure 16 shows the schematic for the NFC connector.

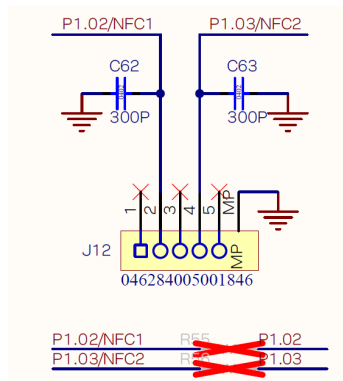


Figure 16: NFC connector J12

Table 7 describes the NFC pin configuration.

Mode	R55 (0 Ω)	R56 (0 Ω)	NFCPINS UICR register
NFC (default)	Mount	Mount	0xFFFFFFFF (enable protection, use as NFC)
GPIO	No Mount	No Mount	0xFFFFFFFFE (disable protection, use as GPIO)

Table 7: NFC pins configuration

4.8 Qwiic interface

The module I2C bus is available for connecting other peripherals over the I2C bus through a Qwiic interface (J14), as shown in Figure 3.

Table 8 shows the Qwiic interface pin configuration.

J14	Qwiic pin	Module pin	Function	Remarks
1	GND	GND	GND	
2	3.3 VDC	3V3	Power	On-board generated voltage
3	SDA	P0.02	SDA	High-speed I2C data
4	SCL	P0.03	SCL	High-speed I2C clock

Table 8: Qwiic pin configuration

4.9 mikroBUS sockets

The EVK has two standard mikroBUS compatible sockets. Figure 17, Table 9 and Table 10 show the pin designations for the mikroBUS1 and mikroBUS2 connectors.

mikroBUS1 (J19, J20)	Module
Analog	P1.14
Reset	nRESET, P1.15
SPI chip select	P2.07
SPI clock	P2.06
SPI MISO	P2.09
SPI MOSI	P2.08
PWM output	P1.00
Interrupt	P1.01
UART RX	P1.02
UART TX	P1.03
I2C Clock	P0.03
I2C Data	P0.02
5 V	5 V – On board generated voltage
3.3 V	3.3 V – On board generated voltage

Table 9: mikroBUS1 pin out

mikroBUS2 (J17 and J18)	Module
Analog	P1.13
Reset	nRESET, P1.08
SPI chip select	P2.10
SPI clock	P2.06
SPI MISO	P2.09
SPI MOSI	P2.08
PWM output	P1.15
Interrupt	P0.04
UART RX	P0.01
UART TX	P0.00
I2C Clock	P0.03
I2C Data	P0.02
5V	5V – On board generated voltage
3.3V	3.3V – On board generated voltage

Table 10: mikroBUS2 pin out

- Several module GPIOs can be accessed through multiple connectors, mikroBUS, and pin headers.
- Make sure that the module GPIOs are not simultaneously connected to more than one peripheral.

Figure 17 shows the pin out of the mikroBUS connectors.

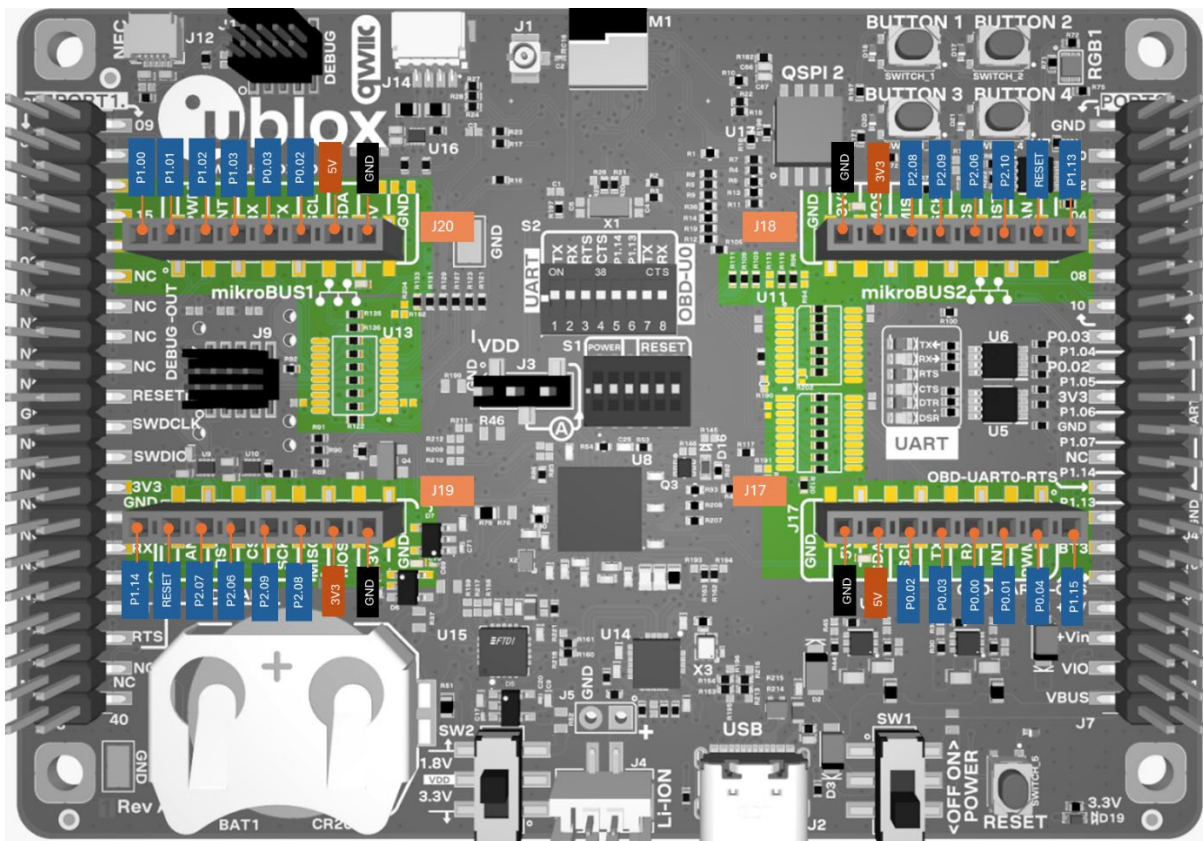


Figure 17: mikroBUS1 and mikroBUS2 pins

Refer to appendix [Configuration possibilities for mikroBUS](#) for information about different possible HW configurations.

4.10 Multipurpose GPIO header and Test Points

The EVK includes pin headers (**J7** and **J8**) and test points (TP) to access the GPIOs on the module, as shown in [Figure 18](#) and [Figure 19](#).

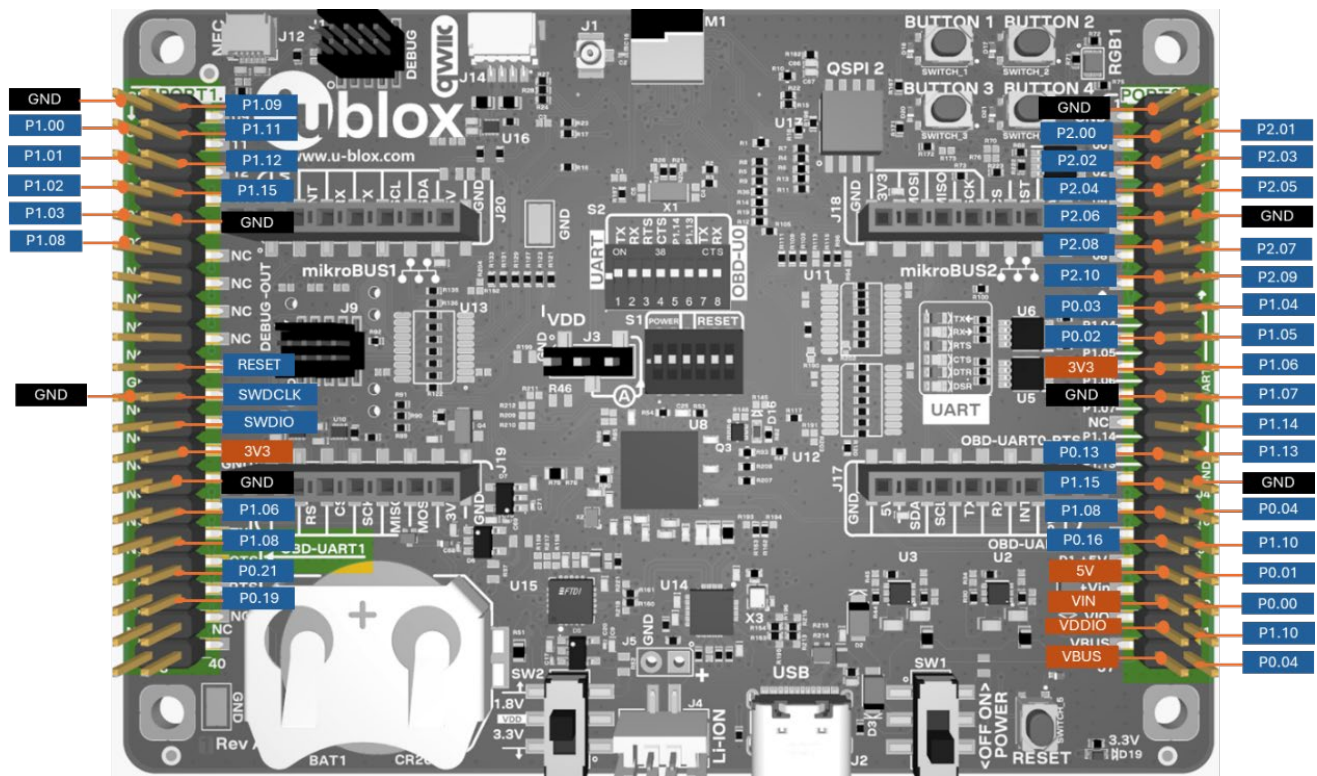


Figure 18: Pin headers J7, and J8 signaling and board view

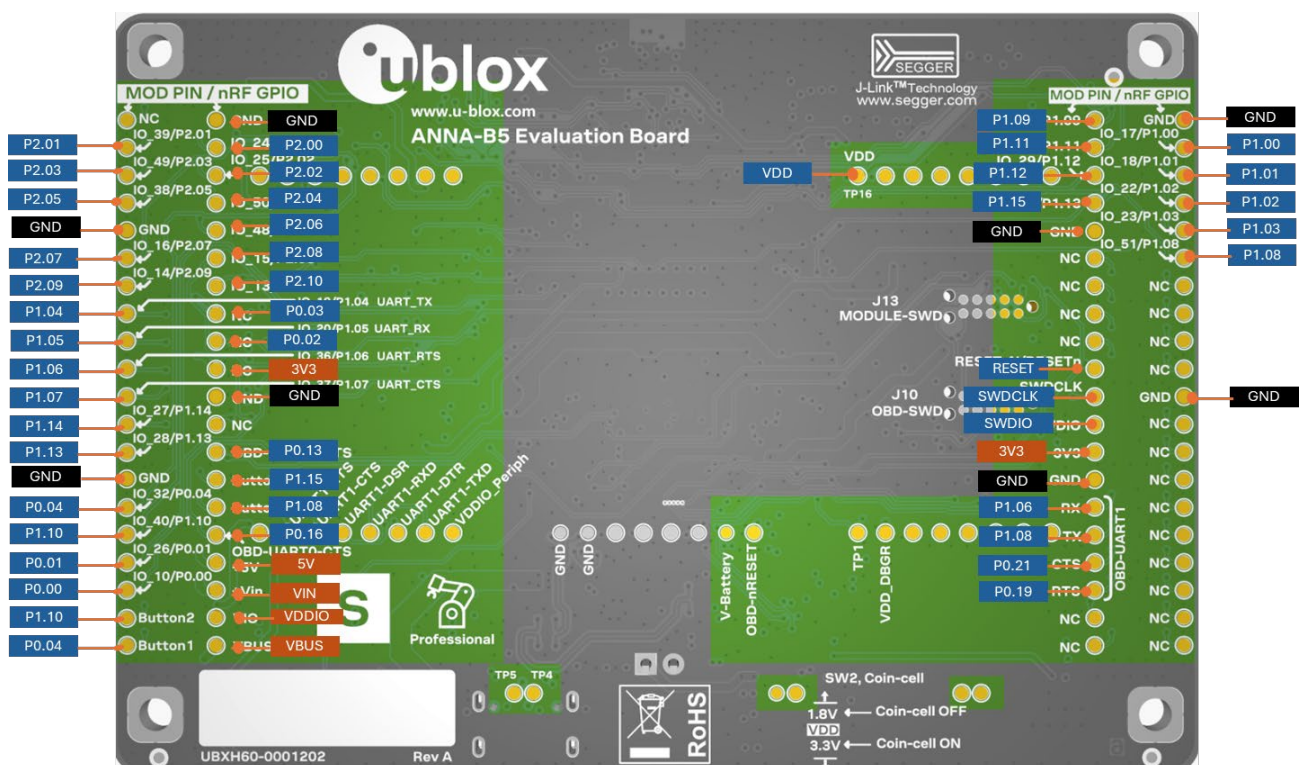


Figure 19: Test point signaling and board view

Table 11 describes the **J7** and **J8** header pins, their function, and respective Test Points (TP).

Pin	TP	Pad	Module function	I/O ¹	Description	nRF54L15 function	Remarks
J7-1	TP48		GND		GND		
J7-2	TP45	NC					
J7-3	TP46	24	QSPI_D3	I/O	GPIO, SPIM_DCX, UARTE_RXD, QSPI_D3	P2.00	
J7-4	TP47	39	QSPI_CLK	I/O	GPIO, SPIM_SCK, SPIS_SCK, QSPI_SCK	P2.01	Clock Pin, FLPR
J7-5	TP49	25	QSPI_D0	I/O	GPIO, SPIM_MOSI, SPIS_MISO, UARTE_TXD, QSPI_D0, Serial wire output SWO	P2.02	FLPR, Trace
J7-6	TP50	49	QSPI_D2	I/O	GPIO, QSPI_D2	P2.03	FLPR
J7-7	TP51	50	QSPI_D1	I/O	GPIO, SPIM_MISO, SPIS_MOSI, UARTE_CTS, QSPI_D1	P2.04	FLPR(QSPI)
J7-8	TP52	38	QSPI_CS	I/O	GPIO, SPIM_CS, SPIS_CS, UARTE_RTS, QSPI_CS	P2.05	FLPR
J7-9	TP53	48	SPI_SCK	I/O	GPIO, SPIM_SCK, SPIS_SCK; TRACE_CLK	P2.06	Trace, Clock Pin, FLPR
J7-10	TP56		GND		GND		
J7-11	TP54	15	SPI_MOSI	I/O	GPIO, TRACE DATA [1], SPIM_MOSI, SPIS_MISO, UARTE_TXD	P2.08	Trace, FLPR
J7-12	TP55	16	SPI_DCX	I/O	GPIO, TRACEDATA [0], Serial wire output (SWO), SPIM_DCX, UARTE_RXD	P2.07	Trace, SWO, FLPR
J7-13	TP57	13	SPI_CS	I/O	GPIO, TRACEDATA [3], SPIM_CS, SPIS_CS, UARTE_RTS	P2.10	Trace, FLPR
J7-14	TP58	14	SPI_MISO	I/O	GPIO, TRACE DATA [2], SPIM_MISO, SPIS_MOSI, UARTE_CTS	P2.09	Trace, FLPR
J7-15	TP59	47			I2C_SCL	P0.03	GRTC, Clock Pin
J7-16	TP60	19	UART_TXD	I/O	GPIO	P1.04	Clock Pin, AIN0
J7-17	TP61	11			I2C_SDA	P0.02	
J7-18	TP62	20	UART_RXD	I/O	GPIO	P1.05	AIN1
J7-19	TP63				+3.3V		
J7-20	TP64	36	UART_RTS	I/O	GPIO	P1.06	AIN2
J7-21	TP68	GND			GND		
J7-22	TP65	37	UART_CTS	I/O	GPIO	P1.07	AIN3
J7-23	TP66	NC					
J7-24	TP67	27	WAKE_HOST	I/O	GPIO	P1.14	AIN7
J7-25	TP69				OBD-UART0-RTS		
J7-26	TP70	28	WAKE_UP	I/O	GPIO, GRTC PWM output	P1.13	AIN6
J7-27	TP71	31			Button 4	P1.15	
J7-28	TP74	GND			GND		
J7-29	TP72	51			Button 3	P1.08	Clock Pin
J7-30	TP73	32	GPIO	I/O	LED_GREEN/SW1	P0.04	Clock Pin, GRTC

¹ I/O notations: I=Input, O=Output, I/O=Input or Output, PU=Pull Up, PD=Pull Down, D=Default, PP=Push-Pull, OD=Open Drain, AI/AO=Analog Input/Output, NC=Not Connected

Pin	TP	Pad	Module function	I/O ¹	Description	nRF54L15 function	Remarks
J7-31	TP75				OBD-UART0-CTS		
J7-32	TP76	40	GPIO	I/O	SW2	P1.10	
J7-33	TP77				+5V		
J7-34	TP78	26	GPIO	I/O	GPIO, D_RX	P0.01	
J7-35	TP79				+Vin		
J7-36	TP80	10	GPIO	I/O	GPIO, D_TX	P0.00	
J7-37	TP81	VDD			VDD		
J7-38	TP82	40			Button 2	P1.10	
J7-39	TP83				VBUS		
J7-40	TP84		32		Button 1	P0.04	Clock Pin, GRTC
J8-1	TP88	GND			GND		
J8-2	TP85	33	GPIO	I/O	LED_BLUE	P1.09	
J8-3	TP86	17	XTAL_32K	I/O	GPIO, 32.768 kHz crystal connection	P1.00	AIN
J8-4	TP87	30		I/O	GPIO	P1.11	AIN4, clock pin
J8-5	TP89	18	XTAL_32K	I/O	GPIO, 32.768 kHz crystal connection	P1.01	AIN
J8-6	TP90	29		I/O	GPIO	P1.12	AIN5, clock pin
J8-7	TP91	22	NFC1	I/O	GPIO	P1.02	NFC Input
J8-8	TP92	28	GPIO	I/O	GPIO	P1.13	AIN6
J8-9	TP93	23	NFC2	I/O	GPIO	P1.03	Clock Pin, NFC
J8-10	TP96	GND			GND		
J8-11	TP94	51	GPIO/SW3	I/O	GPIO	P1.08/EXTREF	AN, clock pin (GRTC HF clock output), External reference for SAADC
J8-12	TP95	NC					
J8-13	TP97	NC					
J8-14	TP98	NC					
J8-15	TP99	NC					
J8-16	TP100	NC					
J8-17	TP101	NC					
J8-18	TP102	NC					
J8-19	TP103	NC					
J8-20	TP104	12	nRESET	I	RESET	RESET	
J8-21	TP108	GND					
J8-22	TP105	41	SWDCLK	Debug	Serial wire debug clock	SWDCLK	
J8-23	TP106	NC					
J8-24	TP107	42	SWDIO	Debug	Serial wire debug I/O	SWDIO	
J8-25	TP109	NC					
J8-26	TP110				+3.3V		
J8-27	TP111	NC					
J8-28	TP114	GND			GND		
J8-29	TP112	NC					
J8-30	TP113				OBD-UART1-RX		
J8-31	TP115	NC					

Pin	TP	Pad	Module function	I/O ¹	Description	nRF54L15 function	Remarks
J8-32	TP116				OBD-UART1-TX		
J8-33	TP117	NC					
J8-34	TP118				OBD-UART1-CTS		
J8-35	TP119	NC					
J8-36	TP120				OBD-UART1-RTS		
J8-37	TP121	NC					
J8-38	TP122	NC					
J8-39	TP123	NC					
J8-40	TP124	NC					

Table 11: Pin headers J7, J8

[Table 12](#) describes the additional Test Points (TP) on the EVK.

TP	Connection
TP1	Battery voltage level
TP2-TP3	NC
TP4	USB-n
TP5	USB-p
TP6-TP15	NC
TP16	Module VDD
TP17	NC
TP18-TP25	NC
TP26	UART1-TXD
TP27	UART1-DSR
TP28	VDDIO
TP29	UART1-RXD
TP30	UART1-DTR
TP31	UART1-CTS
TP32-TP35	NC
TP36	OBD-RESET
TP37	OBD-RESET-Pulled up (option)
TP38	GND
TP39	NC
TP40-TP41	NC
TP43	OBD-VDD
TP44	GND
TP125-TP126	NC

Table 12: Additional test points

Appendix

A Schematics

The schematics of the EVK are available in PDF format in GitHub [\[8\]](#) together with other hardware design files.

B Configuration possibilities for mikroBUS sockets

B.1 mikroBUS socket 1

The configuration possibilities for the mikroBUS socket 1 are described in [Table 13](#).

mikroBUS	nRF Pin	Default Function		Pin Type	Required patching
M1-AN	P1.14	Connected to FTDI chip as UART1-DTR	Channel sounding (possible option)	AN	Recommended to turn off switch S2 12-5
M2-RESET					None
M2-RESET	P1.15	Button 4, mikroBUS2_PWM			double-check Button 4 status, slot 2 connection, Remove R112, mount R115 with 0R 0402
M1-CS	P2.07	RGB-G, SWD-SWO			Remove R93, and R74
M1-CLK	P2.06	Shared between slot 1 and slot 2		clock pin	None, just double-check slot 2 connection
M1-MISO	P2.09	Shared between slot 1 and slot 2			Can disconnect RGB-R, remove R69
M1-MOSI	P2.08	Shared between slot 1 and slot 2			None, just double-check slot 2 connection
M1-PWM	P1.00	LFXO-XL1			Disconnect LFXO by removing R25
M1-INT	P1.01	LFXO-XL2			Disconnect LFXO by removing R20
M1-RX	P1.02	NFC1			Check NFC connection, can remove C62
M1-TX	P1.03	NFC2		clock pin	Check NFC connection, can remove C63
M1-SCL	P0.03	QWIIC connector, Shared between slot 1 and slot 2		clock pin	None, just double-check QWIIC connector, and slot 2 connection
M1-SDA	P0.02	QWIIC connector, Shared between slot 1 and slot 2			None, just double-check QWIIC connector, and slot 2 connection

Table 13 mikroBUS socket 1 configuration options.

B.2 mikroBUS socket 2

The configuration possibilities for the mikroBUS socket 2 are described in [Table 14](#).

mikroBUS	nRF Pin	Default Function	Other option	Pin Type	Required re-work
M2-AN	P1.13	Connected to FTDI chip as UART1-DSR	Channel sounding (possible option)	AN	Recommended to turn off switch S2 11-6
M2-RESET					None
M2-RESET	P1.08			clock pin	Remove R96, mount R94 with 0R 0402
M2-CS	P2.10				None
M2-CLK	P2.06	Shared between slot 1 and slot 2		clock pin	None, just double-check slot 1 connection
M2-MISO	P2.09	RGB-R, Shared between slot 1 and slot 2			Can disconnect RGB-R, remove R69
M2-MOSI	P2.08	Shared between slot 1 and slot 2			None, just double-check slot 1 connection
M2-PWM	P1.15	Button 4, shared between slot 1 and slot 2			None, just double-check Button 4 status, slot 1 connection
M2-INT	P0.04	Button 1		clock pin	None, just double-check Button 1 status, or remove R173
M2-RX	P0.01	OBD-UART0-RX			Recommended to turn off switch S2 9-8
M2-TX	P0.00	OBD-UART0-TX			Recommended to turn off switch S2 10-7
M2-SCL	P0.03	QWIIC connector, Shared between slot 1 and slot 2		clock pin	None, just double-check QWIIC connector, and slot 1 connection
M2-SDA	P0.02	QWIIC connector, Shared between slot 1 and slot 2			None, just double-check QWIIC connector, and slot 1 connection

Table 14 mikroBUS socket 2 configuration options.

C Modifying EVK to use U.FL connector

To use a U.FL connector on the EVK two modifications need to be done:

1. Mount a U.FL connector on position J1
2. Twist or replace the 15 pF capacitor C16 to C2



Figure 20 Unmodified EVK (left) and EVK with U.FL connector mounted (right)

D Glossary

Abbreviation	Definition
CPU	Central Processing Unit
CTS	Clear To Send
DC	Direct Current
DC-DC	DC to DC converter
DFU	Device Firmware Update
EVK	Evaluation Kit
FICR	Factory Information Configuration Register
GPIO	General Purpose Input / Output
LDO	Low Drop-Out voltage regulator
LE	Low Energy
LED	Light Emitting Diode
LF	Low Frequency
LiPo	Lithium-Polymer battery
NC	Not Connected
NCS	nRF Connect SDK
NFC	Near-Field Communications
OBD	On board debugger
QSPI	Quad Serial Peripheral Interface
RC	Resistor-Capacitor network
RTS	Request To Send
RXD	Receive data signal
SIG	Special Interest Group
SoC	System on Chip
SPI	Serial Peripheral Interface
TXD	Transmit data signal
UICR	User Information Configuration Register
USB	Universal Serial Bus

Table 15: Explanation of the abbreviations and terms used

Related documentation

- [1] ANNA-B50 data sheet, [UBXDOC-465451970-3932](#)
- [2] ANNA-B50 system integration manual, [UBXDOC-465451970-3933](#)
- [3] FTDI FT231XQ-R Datasheet, [FT231X \(ftdichip.com\)](#)
- [4] Mikroe, <https://www.mikroe.com/mikrobus>
- [5] Nordic Semiconductor [nRF Connect SDK](#)
- [6] Nordic nRF command line tool <https://www.nordicsemi.com/Products/Development-tools/nrf-command-line-tools/download>
- [7] u-blox open CPU GitHub repository, <https://github.com/u-blox/u-blox-sho-OpenCPU/>
- [8] u-blox HW design GitHub repository, https://github.com/u-blox/evk_designs_sho_altium

 For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	26-Sep-2025	Iber, mape	Initial release for EVK-ANNA-B5
R02	4-May-2026	mape	Added appendix Modifying EVK to use U.FL connector . Minor readability changes throughout the document.

Contact

u-blox AG

Address: Zürcherstrasse 68
8800 Thalwil
Switzerland

For further support and contact information, visit us at www.u-blox.com/support.