One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the ADuM6420A/ADuM6421A/ADuM6422A Quad-Channel Isolators with Integrated DC-to-DC Converter

FEATURES

- *iso*Power integrated, isolated dc-to-dc converter
- Meets CISPR 32/EN 55032, Class B emission limits
- On-board 6 V to 9 V LDO power supply that provides 5 V to the V_{DDP} pin
- 5 V input operation and selectable 3.3 V or 5 V isolated dc-to-dc converter output
- Screw terminal connectors for the following
  - LDO power supply
  - 5 V direct power supply
  - Off board PDIS control
  - Isolated output supply

EVALUATION KIT CONTENTS

- EVAL-ADuM6421ARNZ, includes the ADuM6421ABRNZ5
- EVAL-ADuM6421AURNZ, requires the ADuM6420A, ADuM6421A, or ADuM6422A to be ordered separately

DOCUMENTS NEEDED

- ADuM6420A/ADuM6421A/ADuM6422A data sheet

GENERAL DESCRIPTION

The ADuM6420A/ADuM6421A/ADuM6422A devices integrate four *i*Coupler® on-off keying (OOK) digital isolation channels and *i*Coupler chip scale *iso*Power® transformer technology.

This *i*Coupler transformer technology enables a small form factor integrated, reinforced isolated signal and power solution, in applications requiring up to 500 mW of isolated power.

Available dc-to-dc converter supply configurations and maximum available power at the elevated ambient temperatures are specified in the ADuM6420A/ADuM6421A/ADuM6422A data sheet.

The ADuM6420A/ADuM6421A/ADuM6422A devices provide regulated, isolated power that meets CISPR 32/EN 55032, Class B limits at full load on a 2-layer printed circuit board (PCB) with ferrite beads. Radiated emissions test plots of the EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ are provided in Figure 4 and Figure 5. All devices in the family include the same isolated dc-to-dc converter and are differentiated by directional digital channel configurations.

The EVAL-ADUM6421ARNZ includes the ADuM6421ABRNZ5 quad-channel digital isolator with integrated, isolated dc-to-dc converter. Alternatively, the EVAL-ADUM6421AURNZ leaves the isolator position unpopulated to support evaluation of the ADuM6420A, ADuM6421A, or ADuM6422A.

Full specifications for the ADuM6420A/ADuM6421A/ADuM6422A are available in the ADuM6420A/ADuM6421A/ADuM6422A data sheet, which must be consulted in conjunction with this user guide when using the evaluation boards.

TABLE OF CONTENTS

REVISION HISTORY

12/2019—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

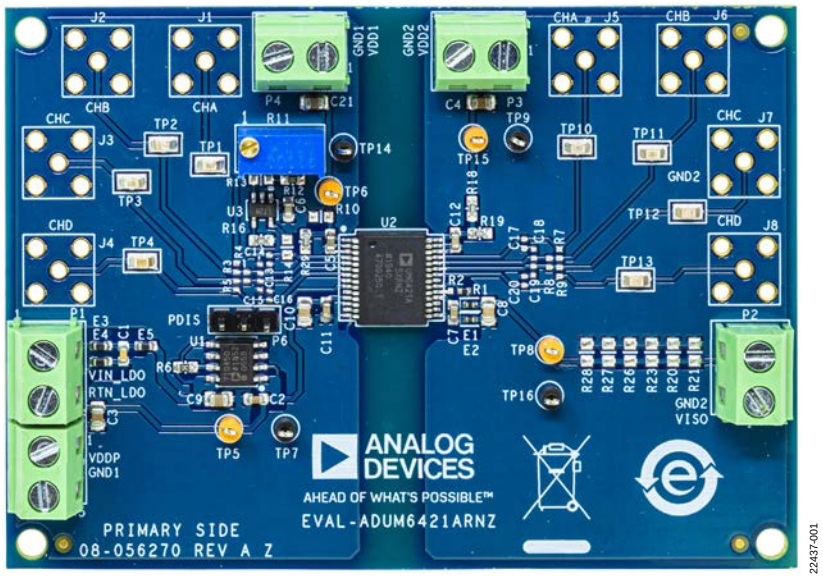

Figure 1. EVAL-ADUM6421ARNZ

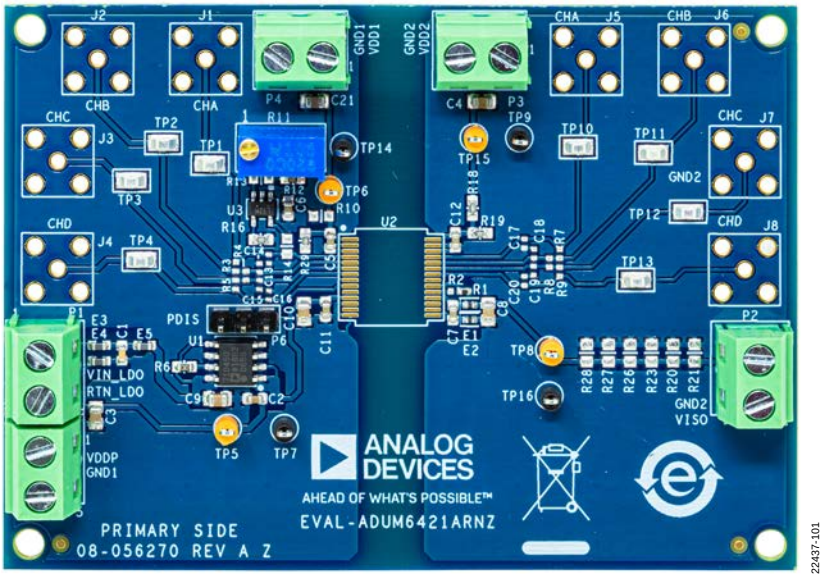

Figure 2. EVAL-ADUM6421AURNZ

EVALUATION BOARD HARDWARE

USING THE EVALUATION BOARD

Figure 1 and Figure 2 show the EVAL-ADUM6421ARNZ and EVAL-ADUM6421AURNZ, respectively. The ADuM6420A/ADuM6421A/ADuM6422A can be powered directly or by the on-board low dropout (LDO) regulator. Either power scheme can be used without modification to the evaluation boards. The LDO input supply and return, Pin 1 and Pin 2, respectively, of Screw Terminal P1 (marked VIN_LDO and RTN_LDO in Figure 6), requires a power supply voltage of 6 V to 9 V. The LDO supply input is filtered by a ferrite bead network. The LDO generates the required 5 V to the ADuM6420A/ADuM6421A/ADuM6422A V_{DDP} pin. A 9 V battery can power the evaluation boards (when testing for electromagnetic compatibility (EMC), for example). Alternatively, the ADuM6420A/ADuM6421A/ADuM6422A can be powered directly with a 5 V supply through Pin 1 of Screw Terminal P5 (marked VDDP in Figure 6).

In both power schemes, the power supply return connects to Pin 2 of Screw Terminal P1 or P5 (marked AGND1 in Figure 6).

The jumper on P6 must be installed to short Pin 3, pull the PDIS pin low, and enable the ADuM6420A/ADuM6421A/ADuM6422A when no external control signal is used.

Installing the jumper on P6 to short Pin 1 and Pin 2 pulls the PDIS pin high and disables the integrated dc-to-dc converter. The V_{ISO} supply pin output voltage is set to 5.0 V or 3.3 V by installing a 0 Ω resistor in the R1 pull-up position or a 0 Ω resistor in the R2 pull-down position, respectively.

LAYOUT RECOMMENDATIONS FOR EMC

Isolators are constructed with split paddles to galvanically isolate the primary and secondary sides of the devices. The ADuM6420A/ADuM6421A/ADuM6422A feature a split in the secondary side lead frame paddle, which can be used in conjunction with ferrite beads for lower radiated emissions. On the primary side, the dc-to-dc converter and digital isolator share a paddle. However, on the secondary side, isolated power and signal paths are galvanically separated from each other. The isolated supply and return paths must be externally routed to the signal isolation input supply pins, which provide a place to insert the ferrite beads.

The EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ provide an example of recommended layout practices using ferrite beads. To pass CISPR 32/EN 55032, Class B limits on a 2-layer PCB, the following layout guidelines are recommended:

- Place ferrite beads between the PCB trace or PCB plane connections, V_{ISO} (Pin 18), and GND_{ISO} (Pin 17).
- Connect the V_{ISO} load (shown in Figure 6) using a PCB trace. Do not connect the V_{ISO} load to a power plane.
- Ensure that V_{ISO} (Pin 18) is connected through the E2 ferrite bead before connecting to the V_{ISO} load, as shown in Figure 3.
- Ensure that GND_{ISO} (Pin 17) is connected by a trace to the GND_{ISO} pins (Pin 15 and Pin 19) on the inside (device side) of the C7 100 nF capacitor.
- Ensure that the C4 capacitor is connected between V_{ISO} (Pin 18) and GND_{ISO} (Pin 17) on the device side of the E1 ferrite bead and E2 ferrite bead.
- Ensure that there is a keep out area in the PCB layout around E1 and E2, as shown in Figure 3.
- Place the power delivery circuit close to the ADuM6420A/ADuM6421A/ADuM6422A to ensure the V_{DDP} trace is as short as possible. The EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ PCB has a power delivery circuit located on the PCB with a short trace from the ADP7104ARDZ-5.0 regulator output (U1) to V_{DDP} (Pin 11). This layout example minimizes the loop area in which high frequency flows. An increase in the loop area results in an increase in the emissions levels.
- Use Murata BLM18HE152SN1D ferrite beads (0603 size) for E3, E4, and E5 to improve emissions. Other ferrite beads can be used for E3, E4, and E5. However, the ferrite beads must be 0603 size due to the input power requirements.

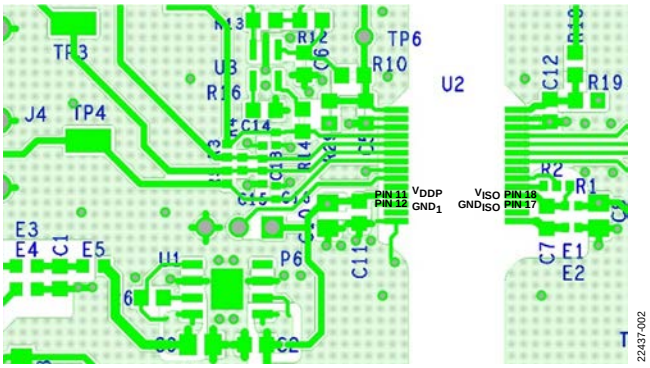

Figure 3. Layout Notes for EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ

CISPR 32/EN 55032 RADIATED EMISSIONS TEST RESULTS

The EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ have been tested to pass the CISPR 32/EN 55032, Class B standard.

The EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ were configured and tested with 5.0 V power supplied to the V_{DDP} pin from the ADP7104ARDZ-5.0 regulator output. The ADP7104ARDZ-5.0 regulator input is supplied from a standard 9 V battery. V_{ISO} can be loaded with six 300 Ω, 0805 size, surface-mount device (SMD) resistors in parallel for a total load of 50 Ω or 100 mA load at 5 V.

Measurements carried out according to the CISPR 32/EN 55032, Class B standard in a 10 meter semianechoic chamber from 30 MHz to 1 GHz are shown in Figure 4 and Figure 5. Figure 4 shows the results of the peak horizontal scan (the worst case) from 30 MHz to 1 GHz with 100 mA, 5 V output. Figure 5 shows the results of the peak horizontal scan (the worst case) from 30 MHz to 1 GHz with 50 mA, 5 V output, and 5 Mbps signal on Channel A, Channel B, Channel C, and Channel D. Table 1 shows the tabulated quasi peak (QP) results. These results show that the ADuM6420A/ADuM6421A/ADuM6422A emissions are below CISPR 32/EN 55032, Class B limits when tested on a 2-layer PCB with the use of ferrite beads. When tested with 5 V supplies, a 100 mA load, and a data rate of 0 Mbps on Channel A, Channel B, Channel C, and Channel D, the quasi peak margin limit is −3.6 dBµV/m. When tested with 5 V supplies, a 50 mA load, and a data rate of 5 Mbps on Channel A, Channel B, Channel C, and Channel D, the quasi peak margin limit is −6.0 dBµV/m.

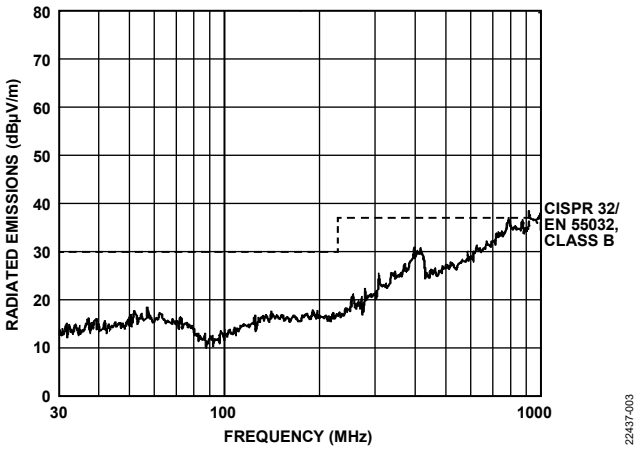

Figure 4. Peak Horizontal Scan from 30 MHz to 1 GHz with 100 mA, 5 V Output, 0 Mbps Signals on Channel A, Channel B, Channel C, and Channel D

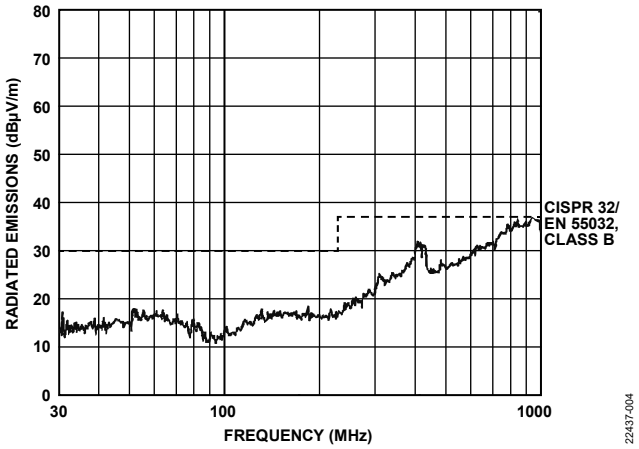

Figure 5. Peak Horizontal Scan from 30 MHz to 1 GHz with 50 mA, 5 V Output, and 5 Mbps Signals on Channel A, Channel B, Channel C, and Channel D

Table 1. ADuM6421A Test Results (QP Measurements)

Frequency (MHz)	QP Level (dBµV/m)	Limit CISPR 32/ EN 55032, Class B (dBµV/m)	QP Margin from limit CISPR 32/EN 55032, Class B (dBµV/m)	Antenna Position	Antenna Height (meters)	5 V In, 5 V Out Output Current (mA)	Data Rate Channel x[1] (Mbps)	Pass or Fail
307.22	27.3	37	−9.7	Horizontal	3.5	100	0	Pass
397.09	30.2	37	−6.8	Horizontal	2.5	100	0	Pass
417.90	26.5	37	−10.5	Horizontal	2.5	100	0	Pass
791.47	32.0	37	−5.0	Horizontal	1.0	100	0	Pass
919.07	33.4	37	−3.6	Horizontal	1.0	100	0	Pass
183.22	13.3	30	−16.7	Horizontal	3.0	50	5	Pass
310.90	28.0	37	−14.8	Horizontal	3.0	50	5	Pass
410.68	28.5	37	−8.5	Horizontal	2.0	50	5	Pass
429.56	27.8	37	−9.2	Horizontal	2.0	50	5	Pass
847.03	31.0	37	−6.0	Horizontal	1.0	50	5	Pass

[1] Where x stands for Channel A, Channel B, Channel C, or Channel D.

EVALUATION BOARD SCHEMATIC AND ARTWORK

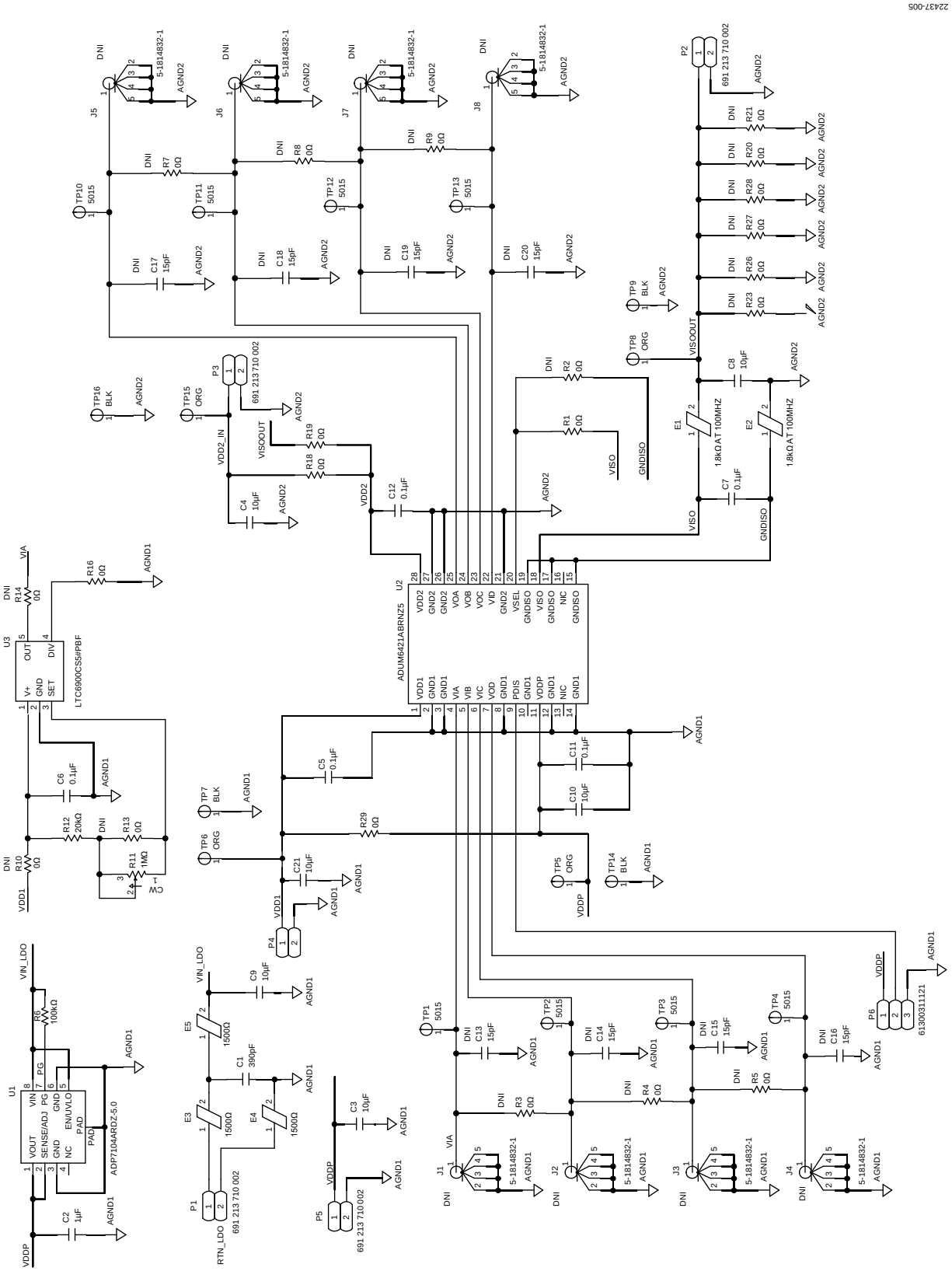

Figure 6. EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ Schematic

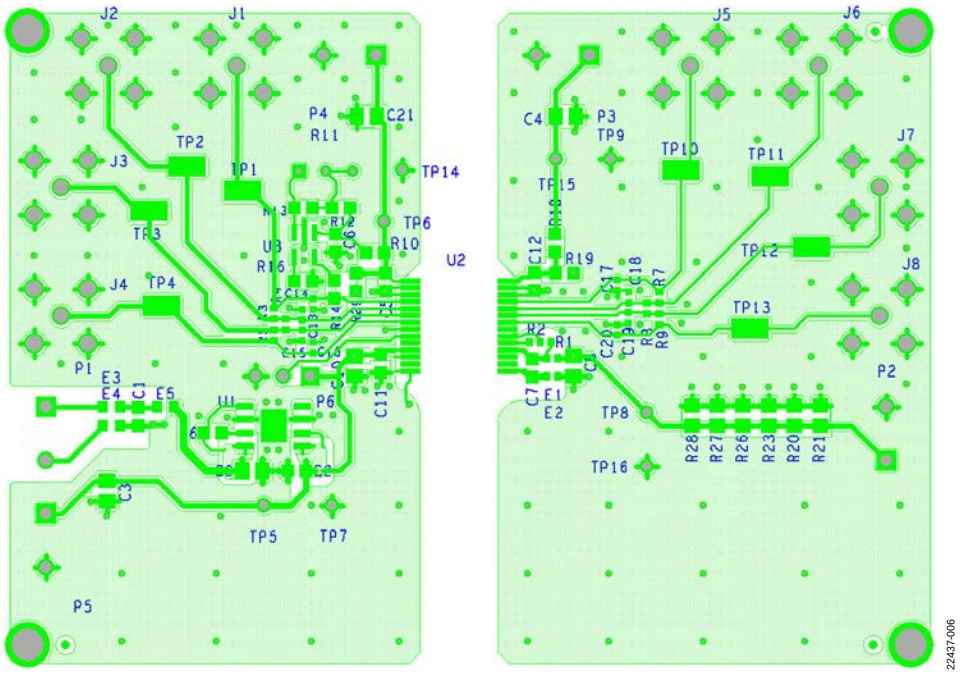

Figure 7. EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ Top Layer

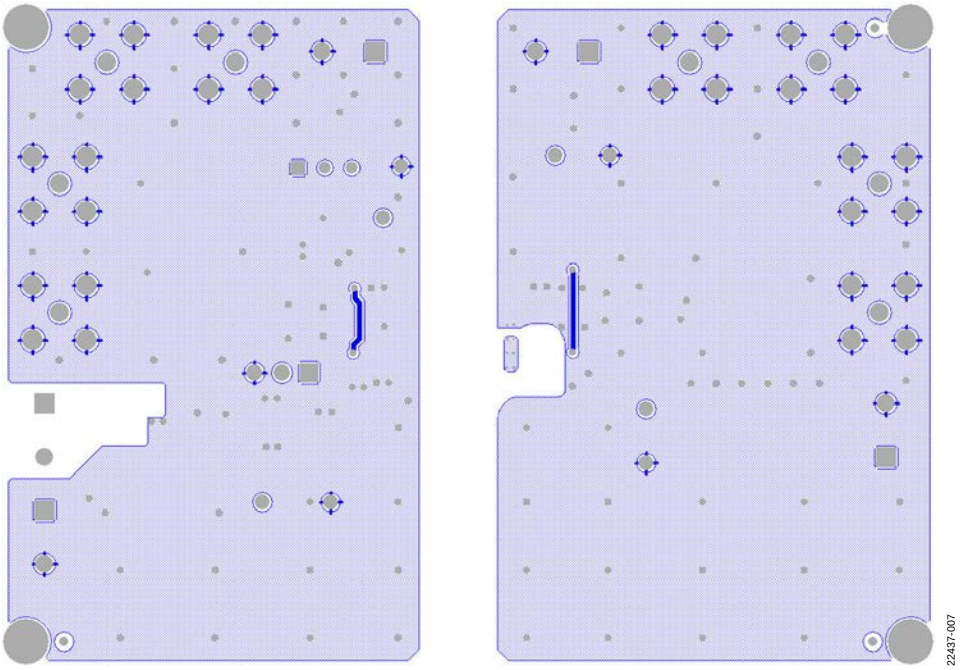

Figure 8. EVAL-ADUM6421ARNZ/EVAL-ADUM6421AURNZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Manufacturer	Part Number
U2	Quad-channel isolator with integrated dc-to-dc converter	Analog Devices	ADuM6421ABRNZ5
U1	20 V, 500 mA, low noise, complimentary metal-oxide semiconductor (CMOS) LDO	Analog Devices	ADP7104ARDZ-5.0
U3	Low power, 1 kHz to 20 MHz resistor set SOT-23 oscillator	Analog Devices	LTC6900CS5#PBF
C1	Capacitor, X7R, 16 V, 390 pF, 0603	AVX Corp	0603YC391KAT2A
C2	Capacitor, X7R, 10 V, 1 µF, 0603	Würth Elektronik	885012206076
C3, C4, C8 to C10, C21	Capacitors, X7R, 10 µF, 10 V, 0805	Würth Elektronik	885012207026
C5 to C7, C11, C12	Capacitors, X7R, 0.1 µF, 0603	Wurth Elektronik	885012206046
E3, E4, E5	Ferrite beads, 1500 Ω, 0603	Murata	BLM18HE152SN1D
E1, E2	Ferrite beads, 1.8 kΩ at 100 MHz, 0402	Taiyo Yuden	BKH1005LM182-T
Jumper	100 mil (2.54 mm) jumper	Amphenol ICC (FCI)	65474-001LF
P6	PCB connector, unshrouded header, 6 mm post height, 2.54 mm pitch	Würth Elektronik	61300311121
P1, P2, P3, P4, P5	Connectors, PCB, terminal blocks, horizontal cable entry, 5 mm pitch	Würth Elektronik	691 213 710 002
R11	Variable resistor, 1 MΩ trimming potentiometer, ½ W	Bourns	3296W-1-105LF
R12	Resistor, 20.0 kΩ, 0603	Panasonic	ERJ-3EKF2002V
R6	Resistor, 100 kΩ, 0603	Panasonic	ERJ-3EKF1003V
R1	Resistor, 0 kΩ, 0402	Panasonic	ERJ-2GE0R00X
R16, R18, R19, R29	Resistors, 0 kΩ, 0603	Panasonic	ERJ-3GEY0R00V
TP1 to TP4, TP10 to TP13	Connectors, PCB test point	Keystone Electronics	5015
TP7, TP9, TP14, TP16	Connectors, PCB test point, black	Vero Technology	20-2137
TP5, TP6, TP8, TP15	Connectors, PCB test point, orange	Keystone Electronics	5003

RELATED LINKS

Resource	Description
AN-1349	PCB implementation guidelines to minimize radiated emissions on the ADM2582E/ADM2587E RS-485/RS-422 transceivers
AN-0971	Recommendations for control of radiated emissions with *iso*Power devices

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG22437-0-12/19(0)

www.analog.com