EVAL-ADuM4136EBZ User Guide
UG-1019

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Evaluation Board for the ADuM4136 *i*Coupler, Dual-Supply, High Voltage, Isolated IGBT Gate Driver

FEATURES

- 4 A peak drive output capability
- Output power device resistance: <1 Ω
- Desaturation protection
  - Isolated fault output
- Soft shutdown on fault
- Isolated fault and ready functions
- Low propagation delay: <50 ns
- Operating temperature range: −40°C to +125°C
- Output voltage range to 35 V
- Output and input undervoltage lockout (UVLO) Pad placement for multiple switch types Screw terminals for easy connectivity
- Jumpered enable/disable

EVALUATION KIT CONTENTS

- EVAL-ADuM4136EBZ evaluation board

EQUIPMENT NEEDED

- Suggested test equipment
  - Primary side power supply: 0 V to 6 V at 100 mA
  - Secondary side supply: 0 V to 35 V at 250 mA
  - Optional secondary supply: 0 V to 15 V at 250 mA
  - Square wave generator: 0 V to 5 V

GENERAL DESCRIPTION

The EVAL-ADuM4136EBZ evaluation board supports the ADuM4136 single-channel gate driver, which is specifically optimized for driving insulated gate bipolar transistors (IGBTs). Analog Devices, Inc., *i*Coupler® technology provides isolation between the input signal and the output gate driver.

The ADuM4136 provides operation with voltages of up to 35 V. With a dual-rail supply, the negative rail can go as low as −15 V, providing robust turn off of the IGBT.

The EVAL-ADuM4136EBZ evaluation board facilitates testing of the desaturation circuitry with pads available for standard desaturation detection. The evaluation board has layout locations for three different types of discrete switches, allowing for a wide range of device testing. Screw terminals provide easy access to supplying the secondary side with either a single or dual supply.

For complete information about the ADuM4136, refer to the product data sheet that should be consulted in conjunction with this user guide when using the evaluation board.

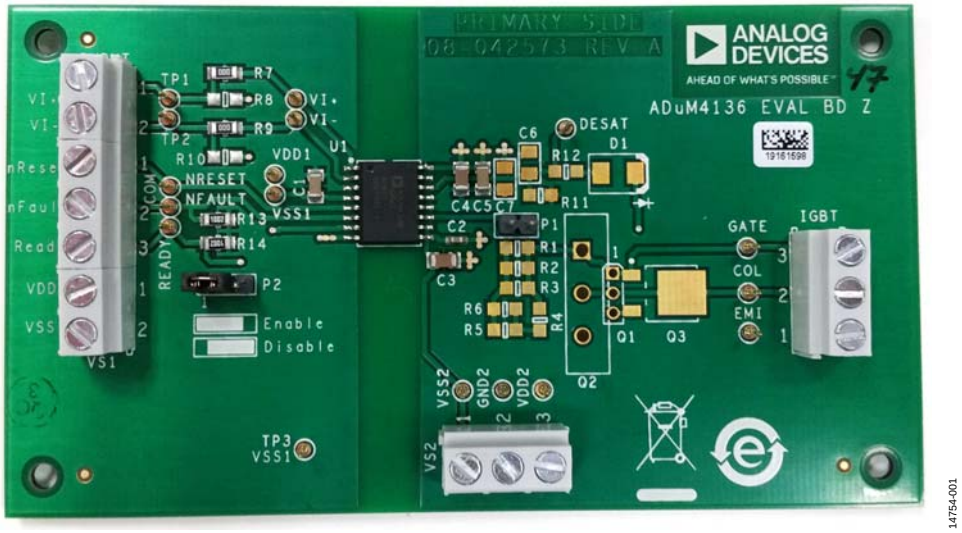

Figure 1. Picture of the EVAL-ADuM4136EBZ in Stock Configuration

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REVISION HISTORY

7/2016—Revision 0: Initial Version

SETTING UP THE EVAL-ADUM4136EBZ

INITIAL CONFIGURATION

Before the first use, certain steps must be completed to prepare the board for operation. In the stock configuration, the R1 to R6 resistors are not placed. These are the locations of the series external resistors for the charging and discharging paths to V_{OUT_ON} and V_{OUT_OFF}. It is recommended to use 1206 surface-mount resistors with values between approximately 1 Ω and 10 Ω, depending on the load being driven. An actual IGBT or MOSFET can be placed in the provided landing patterns to the right of P1. P1 allows shorting across the series external resistors to observe overshoot and/or allow the user to probe voltage to quantify peak currents.

In the stock configuration, the desaturation circuitry is left open. Before the first use, if desaturation functionality is not used, it is recommended to short the DESAT pin to ground, either by a wire or by placing a 0 Ω resistor in the C6 component pad. Failure to do so results in a desaturation fault being observed on the first rising edge of the output.

If the desaturation circuitry is tested, an IGBT or MOSFET must be added to the circuit to allow for the DESAT pin to be pulled down during on times, preventing the desaturation fault. Additionally, C6 (C_{BLANK}), R12 (R_{BLANK}), and D1 must have the appropriate components placed. For details about sizing, refer to the ADuM4136 data sheet. R11 is provided to allow extra DESAT pin blanking current by means of an external pull-up resistor. C7 can provide decoupling for this external pull-up current source, if desired.

R13 and R14 come with 10 kΩ resistors in place. These resistors provide pull-ups to the READY and $\overline{\text{FAULT}}$ pins. P2 allows for easy enabling and disabling of the device by means of jumper pins. A silkscreen reminder is included to show which pins to short to enable or disable the device. R8 and R10 allow for easy placement of 50 Ω terminating resistors, if desired.

Pins accompany the screw terminals. The user can decide which connection mechanism to use. Do not leave VSS2 floating. It must always be at or less than the potential of GND2. Shorting VSS2 and GND2 is a valid operating point.

During operation, if a fault is seen, the $\overline{\text{FAULT}}$ pin is brought low. In this case, the device can be reset by either powering down VDD1 to GND1 and powering back up, or by bringing the $\overline{\text{RESET}}$ pin low then high again. The easiest way to toggle $\overline{\text{RESET}}$ is to remove the jumper on P3 from Pin 2 and Pin 3 and then replace it. An internal pull-down resistor brings $\overline{\text{RESET}}$ low on its own.

PAD LAYOUT FOR THE DEVICE UNDER TEST (DUT)

Figure 4 shows the top layer artwork for the dual-gate driver circuit.

- U1 is the footprint for the ADuM4136.
- C1, C2, and C5 are 0.1 µF bypass capacitors; C3 and C4 are 10 µF bypass capacitors. C7 is provided as an extra space in case more decoupling is desired. C6 allows for a desaturation blanking capacitor to be placed.
- Q1, Q2, and Q3 can be populated with TO-252 MOSFETs or IGBTs with the pinout shown in Figure 2.
- R1 to R6 are gate resistors that control the edges of the outputs. By default, no resistors are installed; these resistors must be populated with low value 1206 resistors, generally in the 1 Ω to 10 Ω range.

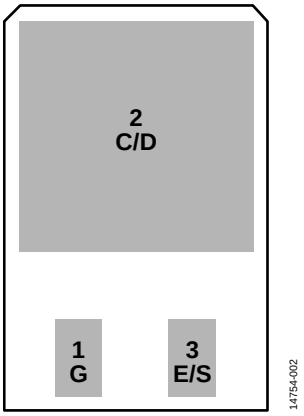

Figure 2. IGBT/MOSFET Footprint

POWER CONNECTIONS

Follow these steps to connect the ADuM4136 evaluation board to the power supply:

1. Connect the 5 V or 3.3 V input supply with the positive terminal on VDD1 and the ground on VSS1.
2. Connect the ADuM4136 VDD2 supply voltage (12 V to 35 V) to the VDD2 pin and its return to the VSS2 pin.

VSS1 and VSS2 are functionally isolated. The emitter/source of the IGBT/MOSFET is tied to GND2.

INPUT/OUTPUT CONNECTIONS

The VI+ and VI− pins are complementary metal oxide semiconductor (CMOS) inputs. R8 and R10 are provided in case the user needs to terminate the inputs with a 50 Ω load.

R7 and R9 are provided to add damping, if needed. However, in most cases, the 0 Ω resistors in the stock configuration can remain on R7 and R9.

The ADuM4136 evaluation board comes with screw terminals for both the input and output connections. These terminals are to facilitate connection options but are not the best option for high performance transient testing. The best measurements performed on the load, whether it is an IGBT or MOSFET or a load capacitor, come from small loop measurements performed right at the load. Using the screw terminals as either the sensing node or for the connection of the load often results in overshoot being observed during measurement.

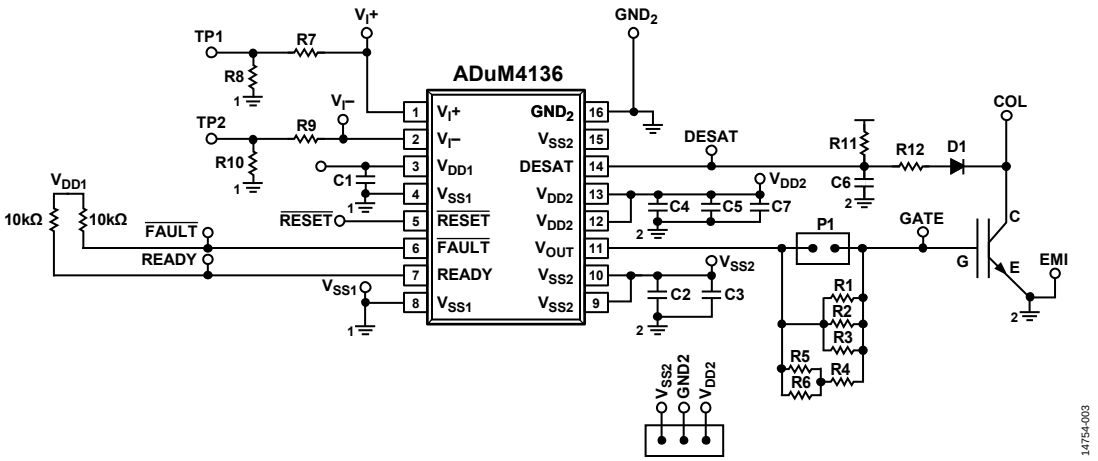

Figure 3. Schematic of the EVAL-ADuM4136EBZ

BILL OF MATERIALS

Table 1. Bill of Materials for Stock Board

Reference	Part
R13, R14	Resistor, 10 kΩ, 1206
R7, R9	Resistor, 0 Ω, 1206
U1	ADuM4136
C1, C5	Capacitor, 0.1 µF, 25 V, 10%, 1206
C3, C4	Capacitor, 10 µF, 50 V, 10%, 1206
C2	Capacitor, 0.1 µF, 25 V, 10%, 0402
R1 to R6, R11, R12, C6, C7, D1, R8, R10	Not installed

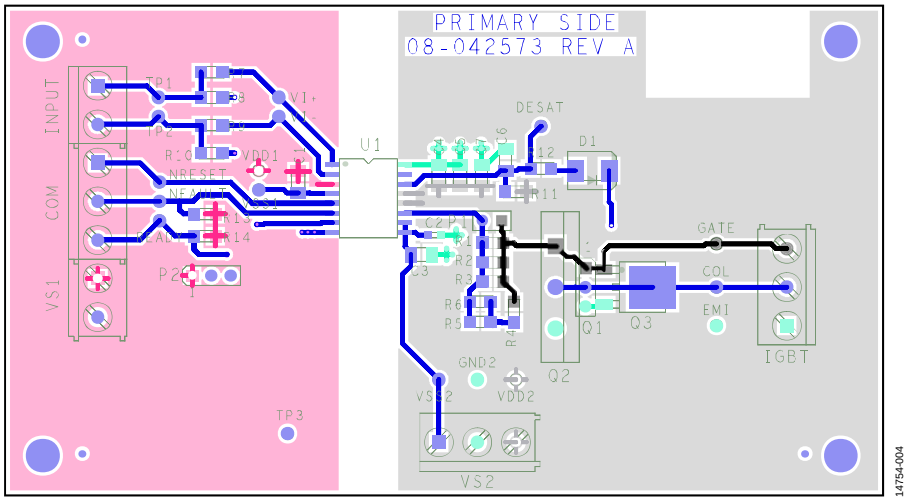

Figure 4. EVAL-ADuM4136EBZ Evaluation Board Top Layer

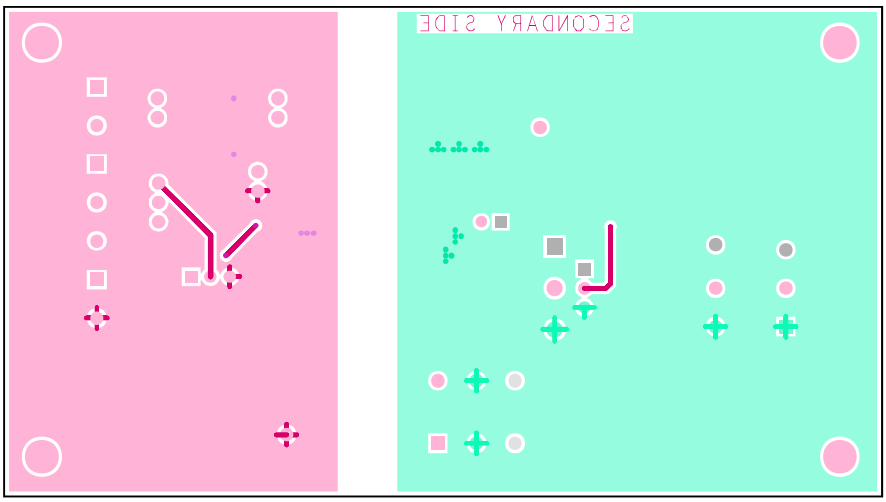

Figure 5. EVAL-ADuM4136EBZ Evaluation Board Bottom Layer

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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