EV6603-V-00A

55V, 5A, Dual Full-Bridge Motor Driver Evaluation Board

DESCRIPTION

The EV6603-V-00A is an evaluation board designed to demonstrate the capabilities of the MP6603, a dual full-bridge motor driver with a built-in, microstepping translator.

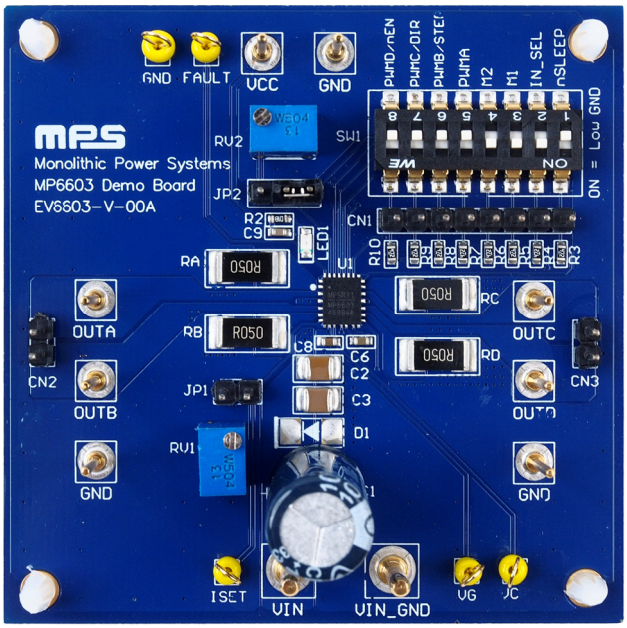
The MP6603 operates from a supply voltage of up to 55V, and it can deliver a motor current up to 5A. It can drive one or two DC motors or a bipolar stepper motor in full-, half-, quarter-, and eighth-step modes by setting M2 and M1. The input control signals for the MP6603 are applied through the CN1 connector or generated on the board.

The MP6603 is available in a QFN-25 (4mmx5mm) package. It is recommended to read the MP6603 datasheet prior to making any changes to the evaluation board.

PERFORMANCE SUMMARY

Parameters	Conditions	Value
Input voltage (V_{IN}) range		8V to 55V
Maximum output current (I_{OUT_MAX})		5A
VCC voltage (V_{CC})		3.3V or 5V

EVALUATION BOARD



LxW (6.5cmx6.5cm)

Board Number	MPS IC Number
EV6603-V-00A	MP6603GV

QUICK START GUIDE

For proper measurement equipment set-up, refer to Figure 3 on page 4 and follow the guidelines below:

1. Connect the input voltage (8V ≤ V_{IN} ≤ 55V) and input ground to the VIN and GND connectors, respectively.
2. Connect the VCC voltage (V_{CC}, 3.3V or 5V) and VCC ground to the VCC and GND connectors, respectively.
3. Set the input control and logic signal through the CN1 connector via the external microcontroller unit (MCU), or manually through SW1. Manual action requires an external 3.3V or 5V V_{CC} to act as a pull-up power supply.
4. The MP6603 features two configurable input modes. The IN_SEL pin configures the input interface. To drive a DC motor with a pulse-width modulation (PWM) input interface, set IN_SEL = GND. To drive a stepper motor with an indexer interface, set IN_SEL = V_{CC}. The evaluation board's JP2 must be set accordingly. Figure 1 shows the set-up for a PWM input. Figure 2 shows the set-up for an indexer interface.

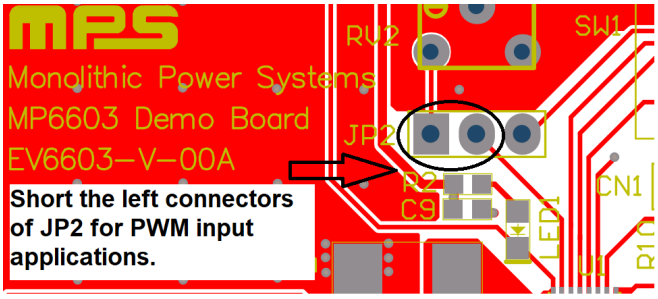


Figure 1: Set-Up JP2 for PWM Input

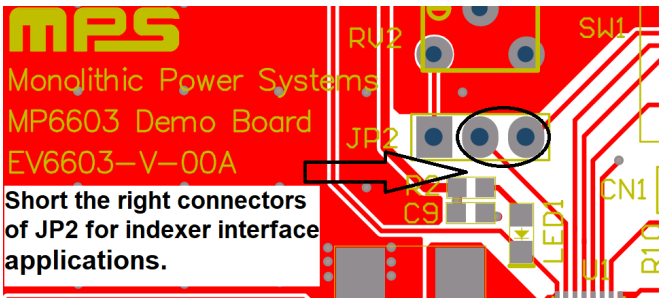


Figure 2: Set-Up JP2 for Indexer Interface

5. If IN_SEL = GND, the MP6603 supports a PWM input interface, which has four different modes for different applications, to drive DC brush motors or other loads. The motor current can be regulated by applying external PWM signals on the input pins: PWM_A, PWM_B, PWM_C, and PWM_D. Table 1 shows the mode selections when IN_SEL = GND.

Table 1: Mode Selection for PWM Input Control

Mode	M2	M1	Outputs	Current Limit
1	0	0	4 x half bridges, OUT_X = PWM_X	Yes
2	0	1	4 x half bridges, OUT_X = PWM_X	No
3	1	0	2 x full bridges	Yes
4	1	1	Parallel full bridge	Yes

For mode 1 and 2, each half-bridge input PWM signal controls the corresponding half bridge, such that OUT_x = PWM_x.

In mode 3, PWM_A and PWM_B control the half-bridges A and B, respectively. Meanwhile, PWM_C and PWM_D control the half-bridges C and D, respectively. Table 2 shows the logic truth table for PWM_A and PWM_B. Table 3 shows the logic truth table for PWM_C and PWM_D.

Table 2: Input Logic Truth Table (Mode 3)

PWM_A (DIR)	PWM_B (nENBL)	OUT_A	OUT_B	Function (DC Motor)
High	Low	High	Low	Forward
Low	Low	Low	High	Reverse
High	High	Low	Low	Brake
Low	High	Hi-Z	Hi-Z	Coast

Table 3: Input Logic Truth Table (Mode 3)

PWM_C (DIR)	PWM_D (nENBL)	OUT_C	OUT_D	Function (DC Motor)
High	Low	High	Low	Forward
Low	Low	Low	High	Reverse
High	High	Low	Low	Brake
Low	High	Hi-Z	Hi-Z	Coast

Mode 4 is parallel full-bridge mode. PWM_A controls both half-bridges A and B, while PWM_B controls both half-bridges C and D. The PWM_C and PWM_D pins are the enable control pins. Bridges A and B are synchronized internally (even during cycle-by-cycle current limiting (CBC)), and so are bridges C and D. OUT_A and OUT_B should be connected together, and OUT_C and OUT_D should be connected together. Table 4 shows the logic truth table for OUTA/B. Table 5 shows the logic truth table for OUTC/D.

Table 4: Input Logic Truth Table for Mode 4

PWM_A (PWM for OUT_A and OUT_B)	PWM_C (nEN for OUT_A and OUT_B)	OUT_A/B
High	Low	High
Low	Low	Low
-	High	Hi-Z

Table 5: Input Logic Truth Table for Mode 4

PWM_B (PWM for OUT_C and OUT_D)	PWM_D (nEN for OUT_C and OUT_D)	OUT_C/D
High	Low	High
Low	Low	Low
-	High	Hi-Z

6. If IN_SEL= V_{CC}, the MP6603 supports the indexer input interface. The step mode is determined by applying logic high and low voltages to the M1 and M2 pins (see Table 6 on page 4)

Table 6: Stepping Format

M2	M1	Step Mode
0	0	Full Step
0	1	Half-Step
1	0	Quarter-Step
1	1	Eighth-Step

Figure 3 shows the measurement equipment set-up.

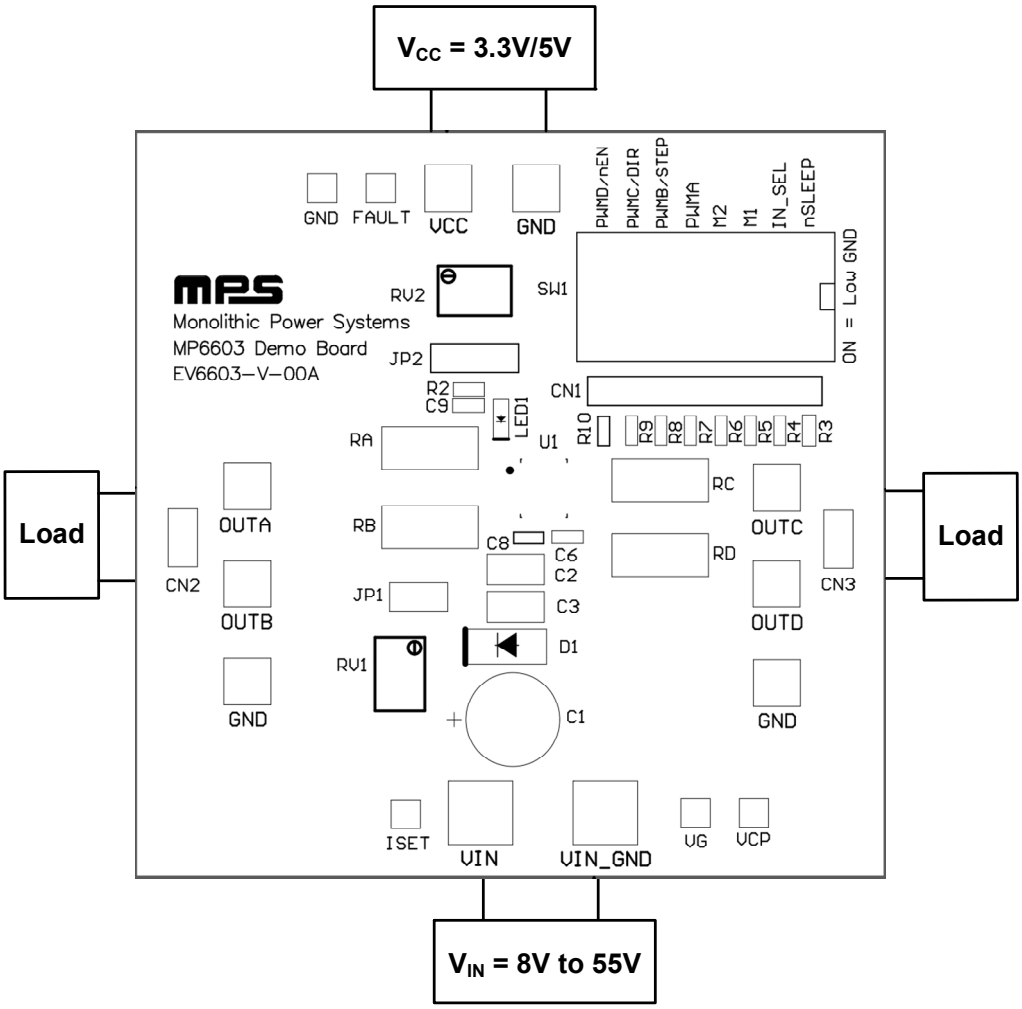


Figure 3: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

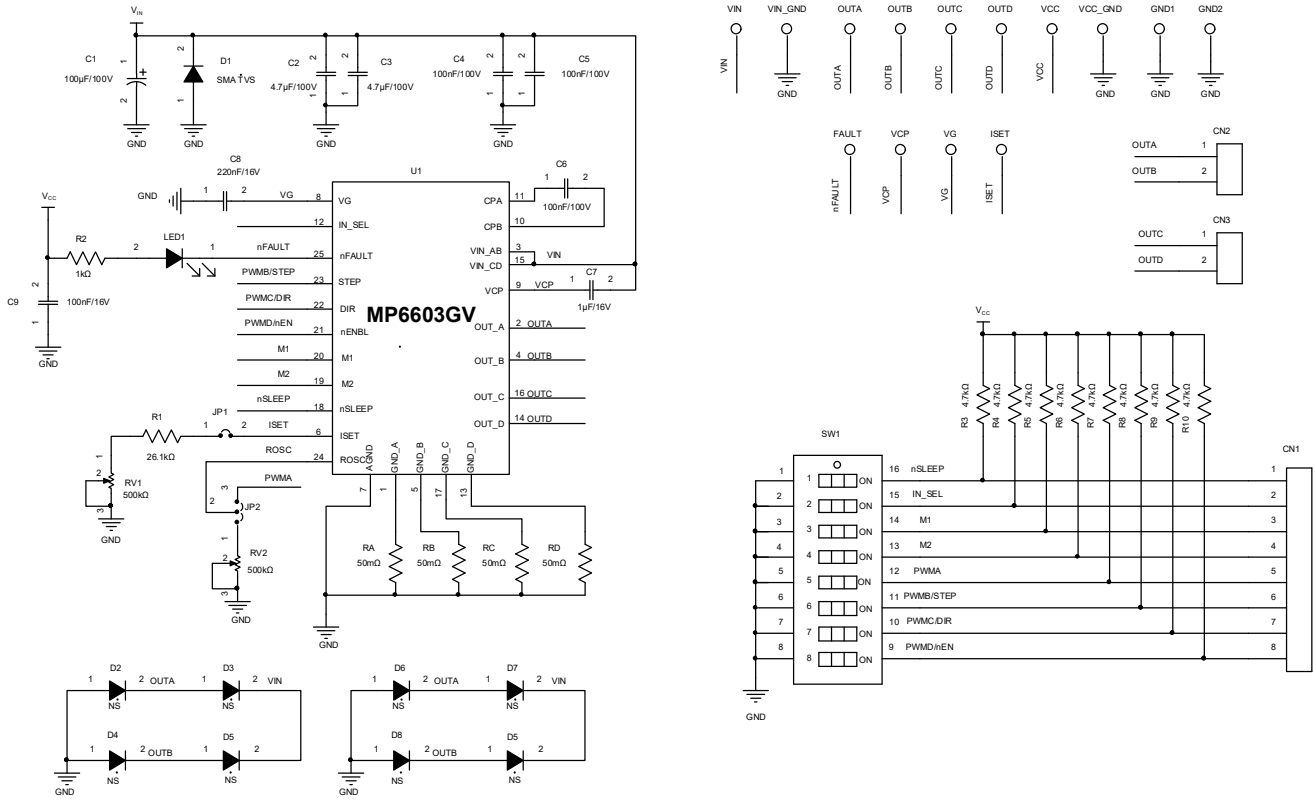


Figure 4: Evaluation Board Schematic

EV6603-V-00A BILL OF MATERIALS

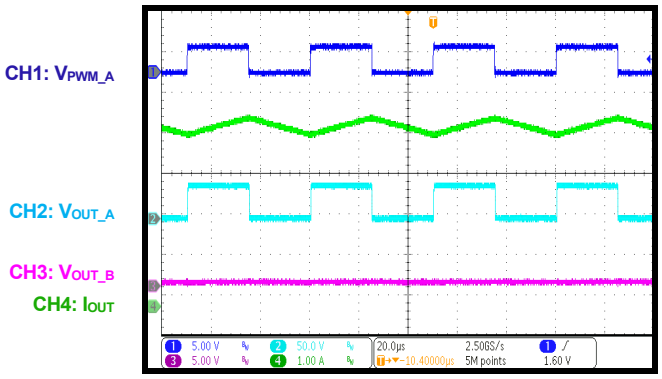
Qty	Designator	Value	Description	Package	Manufacture	Manufacturer PN
1	C1	100μF	Electrolytic capacitor, 100V	DIP	Jianghai	CD263-100V100
2	C2, C3	4.7μF	Ceramic capacitor, 100V, X8L	1210	Murata	GCM32DL8EL475KE07L
3	C4, C5, C6	100nF	Ceramic capacitor, 100V, X7R	0603	Murata	GRM188R72A104KA35D
1	C7	1μF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C105KA12D
1	C8	220nF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C224KA01D
1	C9	100nF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	R1	26.1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0726K1L
1	R2	1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071KL
8	R3, R4, R5, R6, R7, R8, R9, R10	4.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-074K7L
2	RV1, RV2	500kΩ	Square trimming potentiometer	DIP	Any	3266W-1-504LF
4	RA, RB, RC, RD	50mΩ	Film resistor, 1%	2512	Yageo	RL2512FK-070R05L
1	LED1	50mW	Red LED	0805	Baihong	BL-HUE35A-AV-TRB
1	SW1	25mA	8-bit dial switch	SMD	Wurth	418121270808
1	CN1	2.54mm	8-bit connector	DIP	Any	
3	JP1, CN2, CN3	2.54mm	2-bit connector	DIP	Any	
1	JP2	2.54mm	3-bit connector	DIP	Any	
2	JP1, JP2	2.54mm	Short jumper	DIP	Any	
1	D1	NS		SMA		
8	D2, D3, D4, D5, D6, D7, D8, D9	NS				
2	VIN, VIN_GND	2mm	Connector, φ = 2mm	DIP	Any	
8	VCC, VCC_GND, OUTA, OUTB, OUTC, OUTD, GND, GND	1mm	Connector, φ = 1mm	DIP	Any	
5	FAULT, VCP, VG, ISET, GND	Yellow	Test point	DIP	Any	
1	U1	MP6603	55V, 5A dual full-bridge motor driver	QFN-25 (4mmx5mm)	MPS	MP6603GV

EVB TEST RESULTS

V_{IN} = 40V, nSLEEP = 3.3V, T_A = 25°C, load = resistor + inductor between OUT_A and OUT_B, OUT_C and OUT_D, unless otherwise noted.

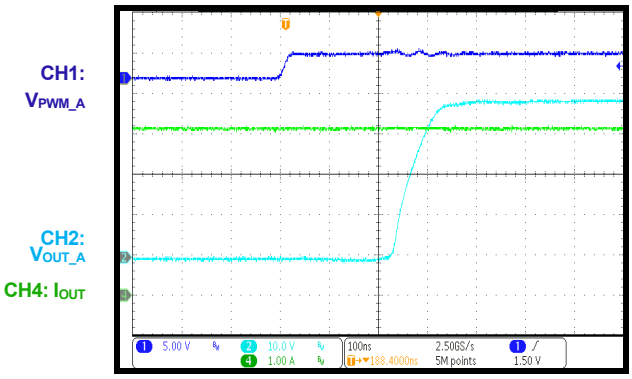
Steady State

IN_SEL = 0, M1 = 1,
M2 = 0 (4 x half-bridges PWM input)



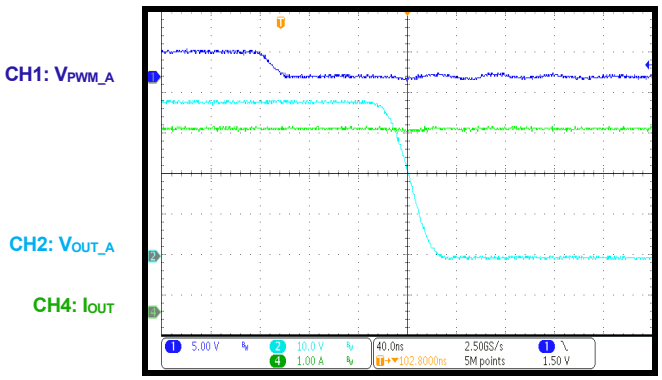
Steady State

IN_SEL = 0, M1 = 1, M2 = 0 (PWM_A to OUT_A)



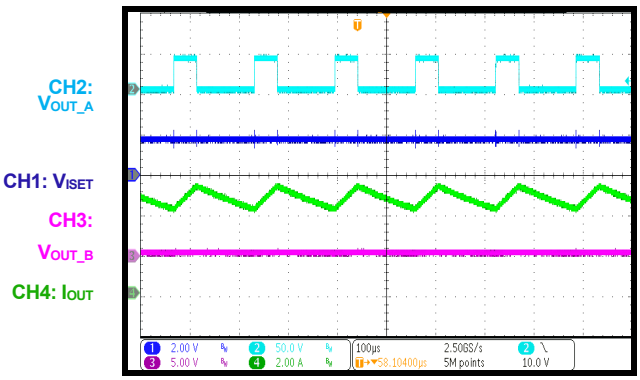
Steady State

IN_SEL = 0, M1 = 1, M2 = 0 (PWM_A to OUT_A)



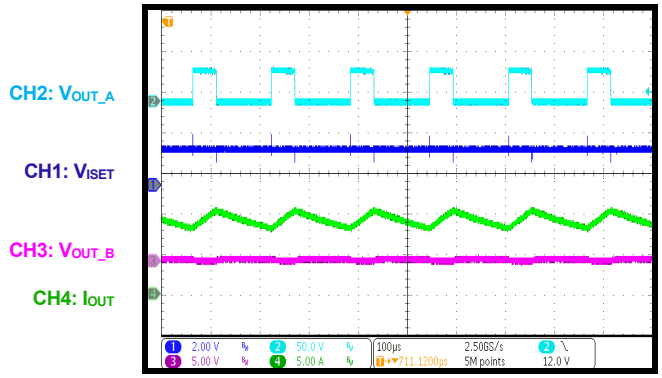
Steady State

IN_SEL = 0, M1 = 0, M2 = 0 (4 x half-bridges current limit)



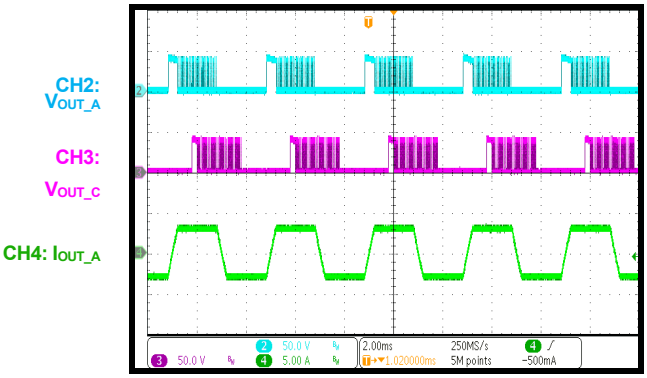
Steady State

IN_SEL = 0, M1 = 1, M2 = 1 (parallel full bridge)



Steady State

IN_SEL = 1, M1 = 0, M2 = 0 (full step)

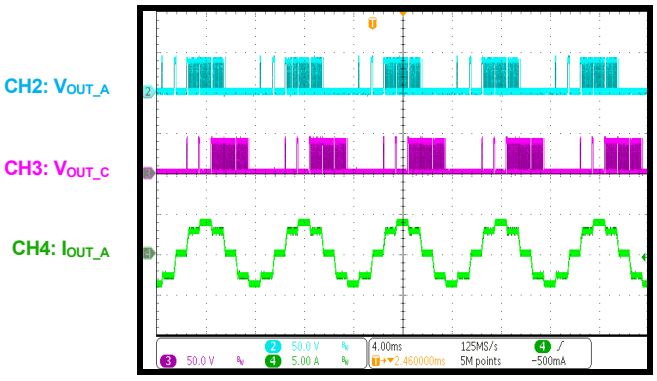


EVB TEST RESULTS *(continued)*

V_{IN} = 40V, nSLEEP = 3.3V, T_A = 25°C, load = resistor + inductor between OUT_A and OUT_B, OUT_C and OUT_D, unless otherwise noted.

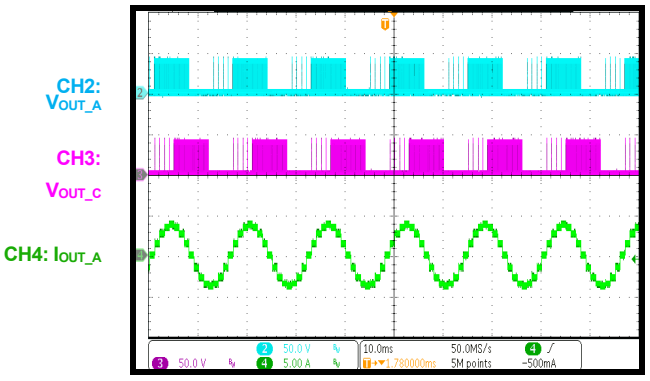
Steady State

IN_SEL = 1, M1 = 1, M2 = 0 (half-step)



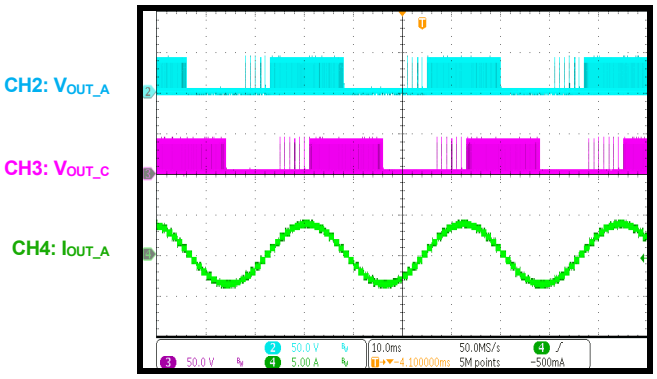
Steady State

IN_SEL = 1, M1 = 0, M2 = 1 (quarter-step)



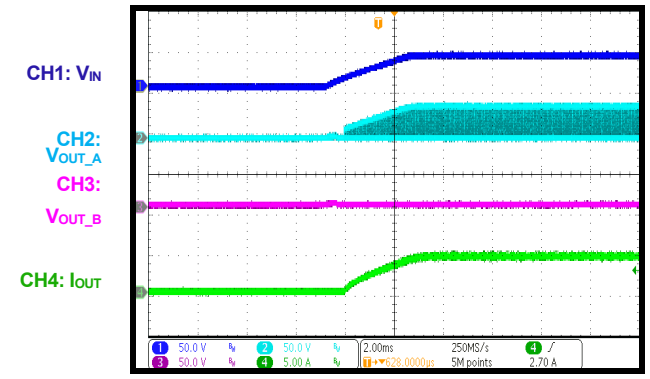
Steady State

IN_SEL = 1, M1 = 1, M2 = 1 (eighth-step)



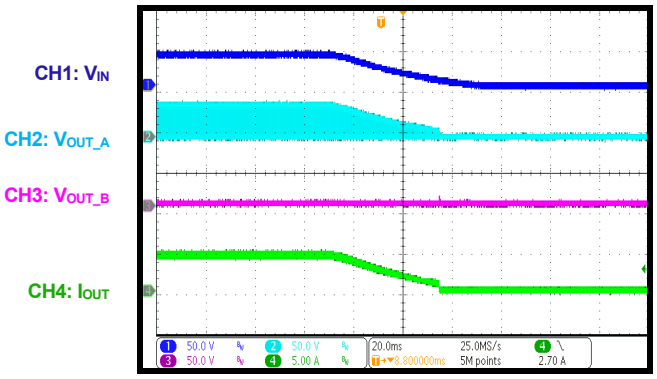
Power Ramping Up

IN_SEL = 0, M1 = 1, M2 = 0 (4 x half-bridges PWM input)



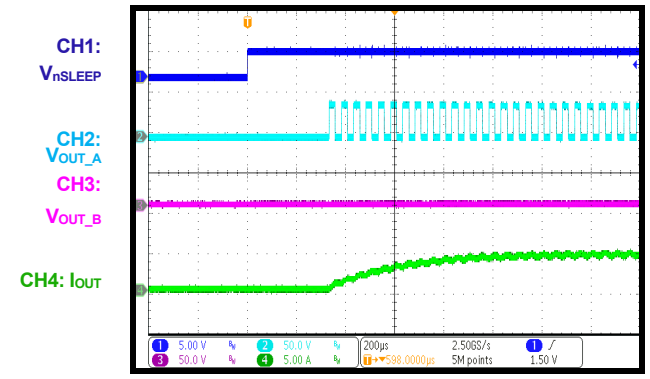
Power Ramping Down

IN_SEL = 0, M1 = 1, M2 = 0 (4 x half-bridges PWM input)



nSLEEP Mode Recovery

IN_SEL = 0, M1 = 1, M2=0 (4 x half-bridges PWM input)

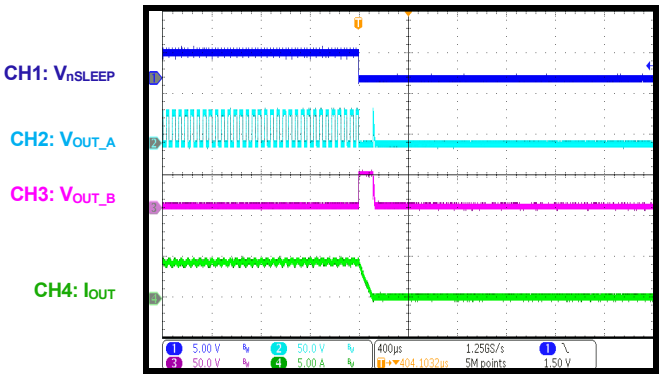


EVB TEST RESULTS *(continued)*

V_{IN} = 40V, nSLEEP = 3.3V, T_A = 25°C, load = resistor + inductor between OUT_A and OUT_B, OUT_C and OUT_D, unless otherwise noted.

nSLEEP Mode Entry

IN_SEL = 0, M1 = 1, M2 = 0 (4 x half-bridges PWM input)



PCB LAYOUT

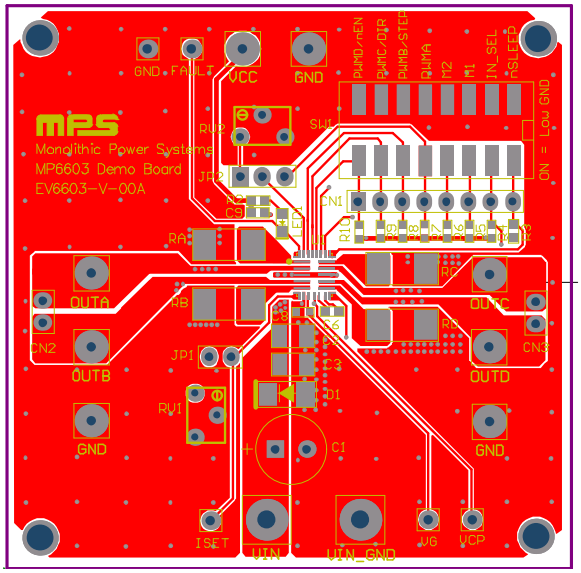


Figure 5: Top Silk

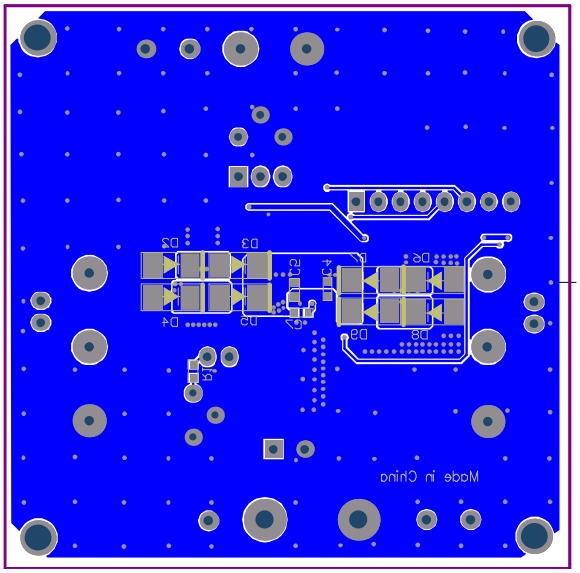


Figure 6: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/12/2024	Initial Release	-