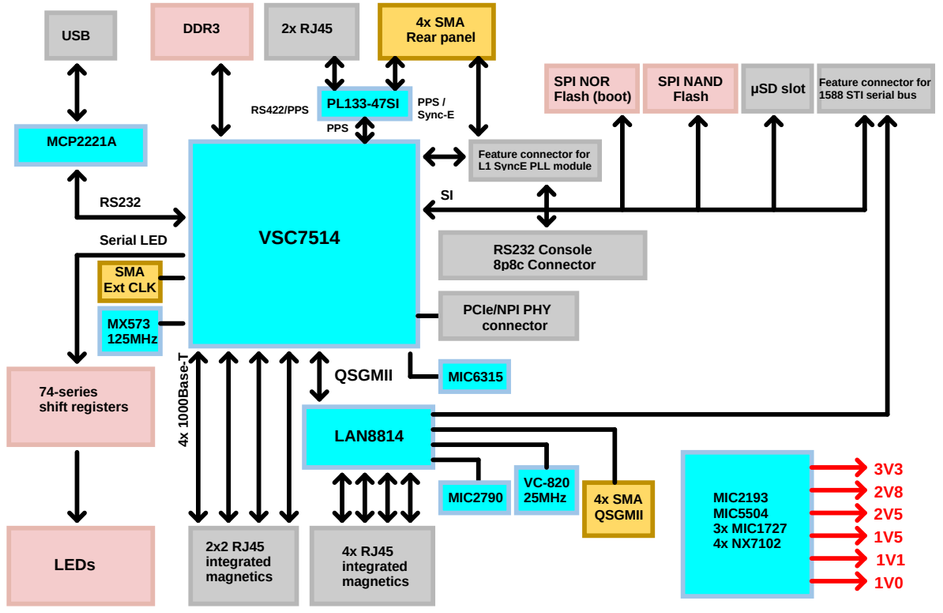
Table of Contents

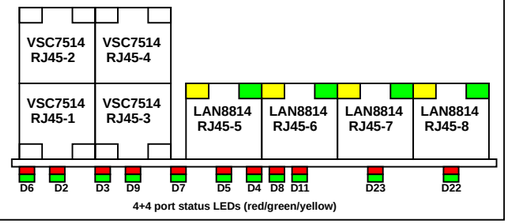
Revision History

Revision	Date	Revision Summary	Author
00C	11/11/2021	Import from Rev B	Arnaldo Cruz
01C	1/31/2022	U42 footprint change, silkscreen updates	Arnaldo Cruz
C0	2/04/2022	Release to manufacturing	Arnaldo Cruz
C1	5/17/2022	FB4 replaced with 100R, 22uF capacitor added in paralled with C118	Arnaldo Cruz

Block Diagram of LAN8814 Ethernet Evaluation Board

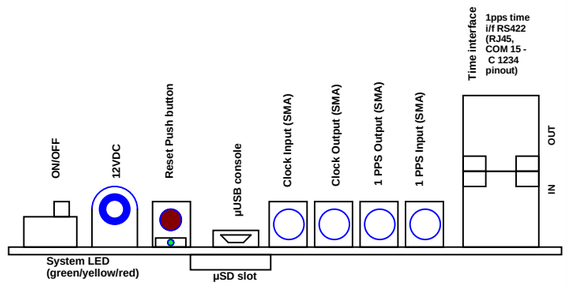


Front layout



4+4 port status LEDs (red/green/yellow)

Rear layout



Notes

1	All resistors are 1% unless specified otherwise
2	Shunt jumper default selections are marked with an asterisk [*].

Project Owner: Howard Hicks			
PCB Layout Contact: Arnaldo Cruz			
PartNumber: EV53D52A	Project Title: UNG8261 EVB-LAN8814	Variant: Standard	
Sheet Title: Table of Contents, History, Block Diagram			
Size: Tabloid	SCH #: EVB-LAN8814	Rev: C1	Date: 5/17/2022
	PCB #: UNG8261	Rev: C0	Sheet 1 of 6
File: 1 - TOC.SchDoc			

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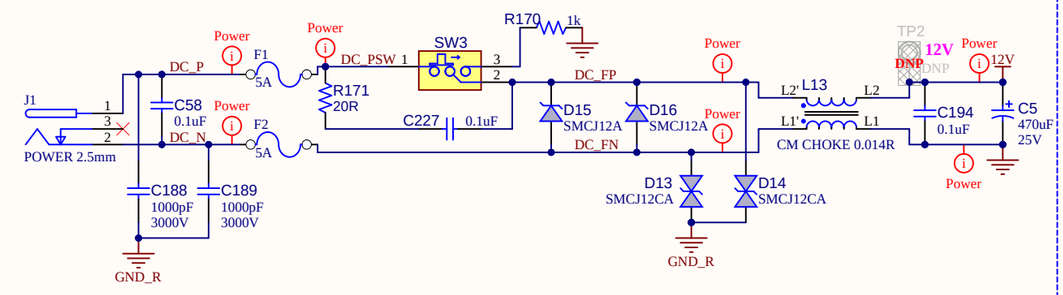
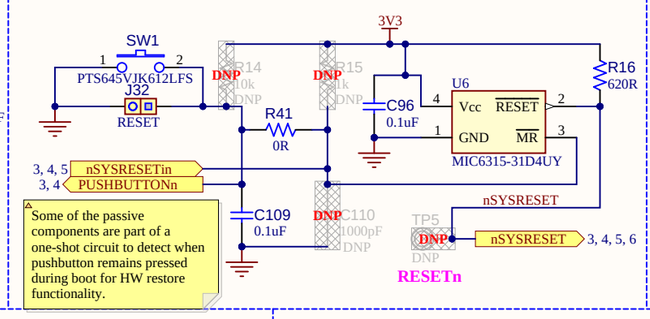
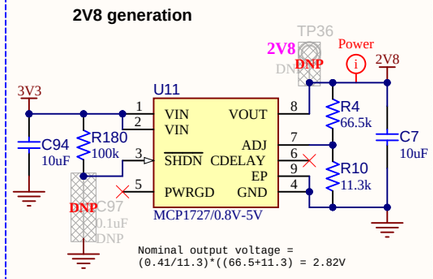
12VDC Jack, Fuses, Power Switch, Input Filtering



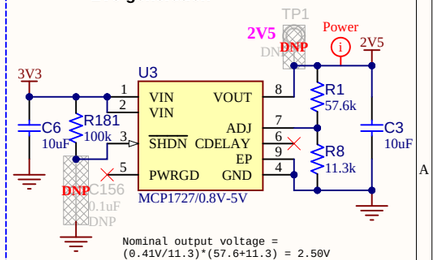
Reset generator



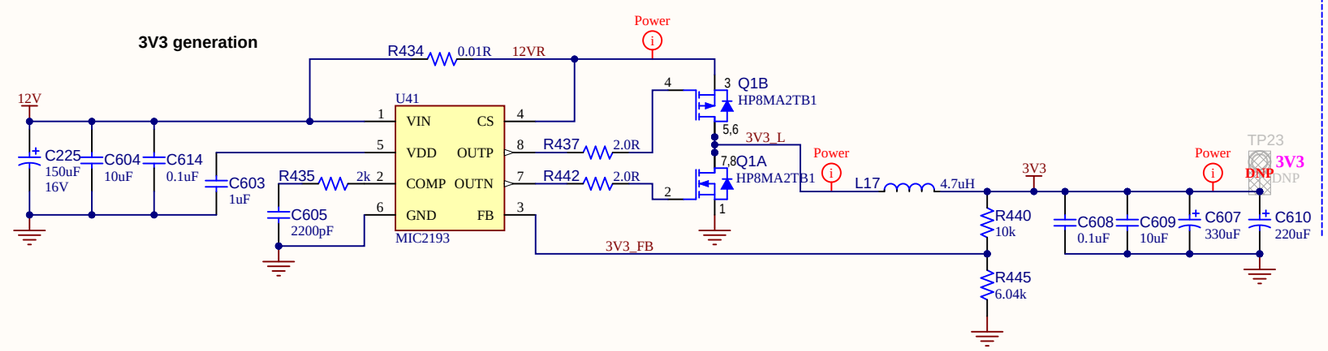
2V8 generation



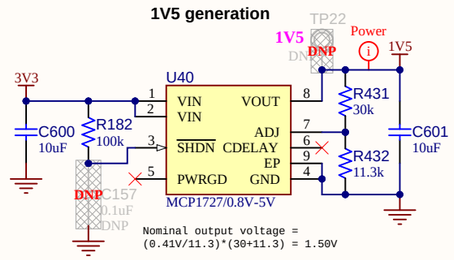
2V5 generation



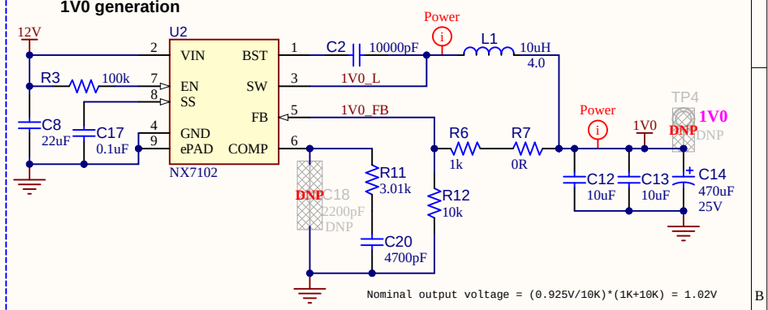
3V3 generation



1V5 generation

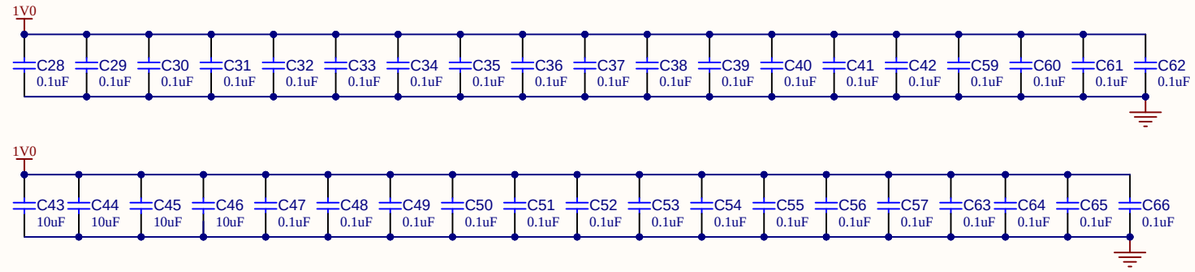


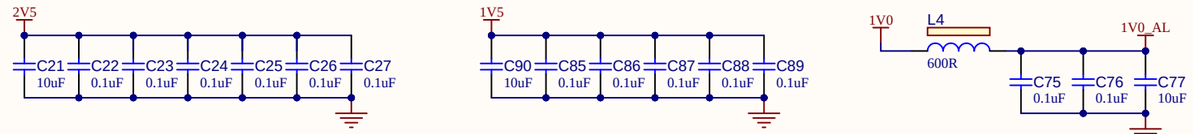
1V0 generation



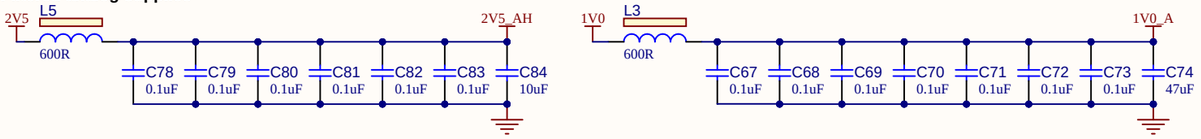
VSC7514 power/decoupling

Digital supplies

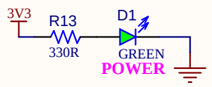




Filtered analog supplies



Power ON indicator

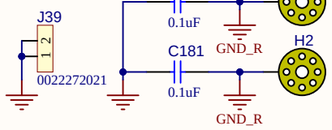


LABEL1

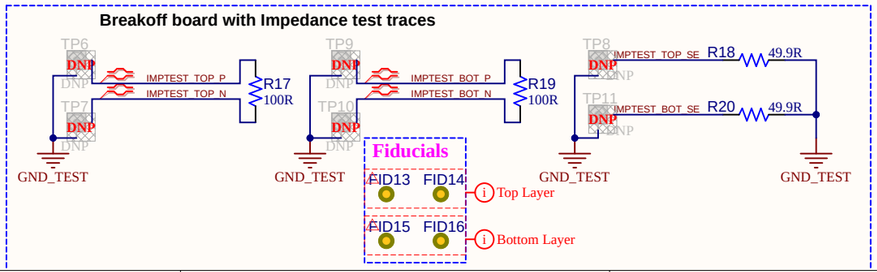
Product number/revision
Serial number

PCBA LABEL 18X6mm

Mounting holes



Breakoff board with Impedance test traces



Project Owner: Howard Hicks			
PCB Layout Contact: Arnaldo Cruz			
PartNumber: EV53D52A	Project Title: UNG8261 EVB-LAN8814		Variant: Standard
Sheet Title: Power Input and DC-DC Converters			
Size: Tabloid	SCH #: EVB-LAN8814	Rev: C1	Date: 5/17/2022
	PCB #: UNG8261	Rev: C0	Sheet 2 of 6
File: 2 - Power Input, VSC7514 Regulators.SchDoc			

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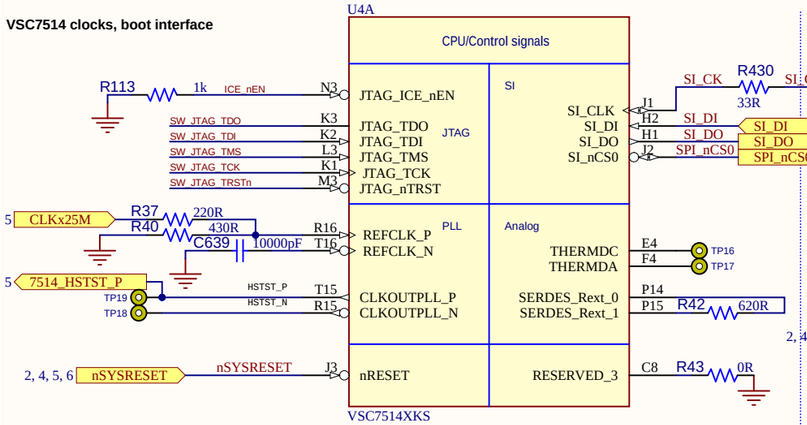
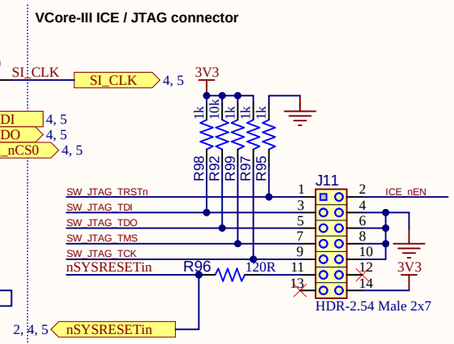
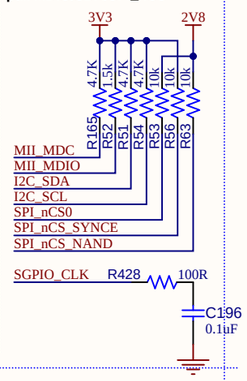
VSC7514 clocks, boot interface



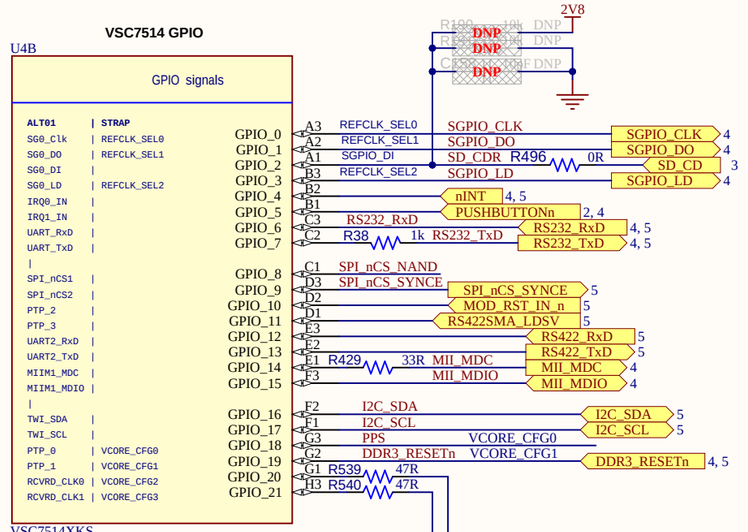
VCore-III ICE / JTAG connector



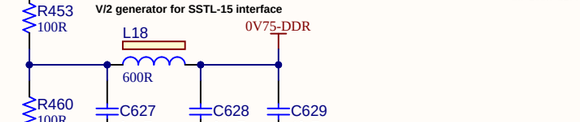
End termination of multidrop clocks, pull MDIO/SDA/SPI_nCS



VSC7514 GPIO

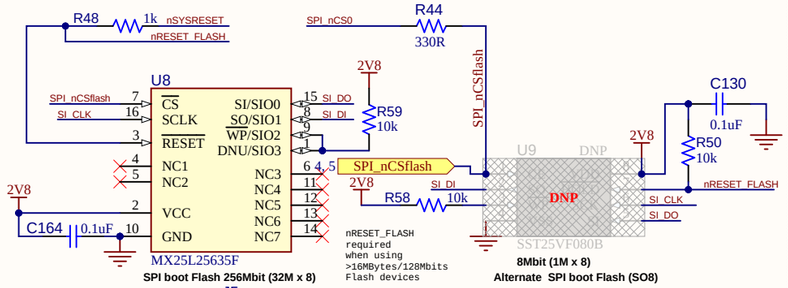


SPI Program



nSYSRESETin must be low during programming of SPI Flash, to output disable VSC7514 SI bus. nRESET_FLASH must be high during programming of SPI Flash, to enable SPI Flash which would otherwise be reset by nSYSRESET.

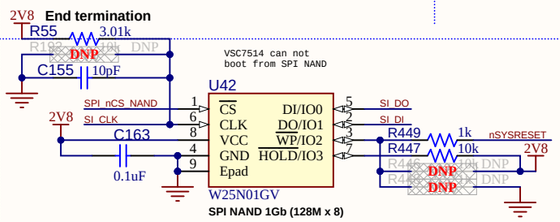
SPI boot Flash 256Mbit (32M x 8) / Alternate SPI boot Flash (SO8)



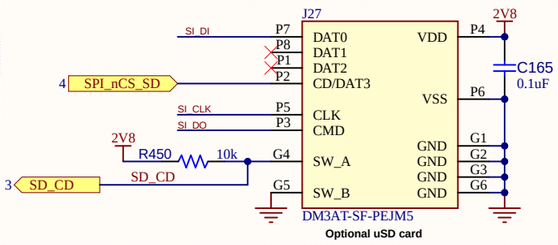
SPI boot Flash 256Mbit (32M x 8)

8Mbit (1M x 8) Alternate SPI boot Flash (SO8)

End termination



SPI NAND 1Gb (128M x 8)



Optional uSD card

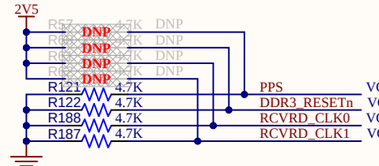
VSC7514 boot mode strapping

VCore_Cfg[3:0]	VCore-III CPU Behavior
0 0 0 0	MIPS (or 8051 boots) from SI interface. The MIPS is Little Endian.
0 0 0 1	8051 IROM boot. Reserved for port-bringup.
0 0 1 0	8051 IROM boot. Reserved for port-bringup.
0 0 1 1	8051 IROM boot. Reserved for port-bringup.
0 1 0 0	8051 IROM boot. Reserved for port-bringup.
0 1 0 1	8051 IROM boot. Reserved for port-bringup.
0 1 1 0	8051 IROM boot. Reserved for port-bringup.
0 1 1 1	8051 IROM boot. Reserved for port-bringup.
1 0 0 0	8051 IROM boot. NPI:1G FDX NoFC, VRAP.
1 0 0 1	8051 IROM boot. PCIe
1 0 1 0	No boot. SI slave and MIIM slave @ address 0 (GPIO alternative).
1 0 1 1	No boot. SI slave and MIIM slave @ address 31 (GPIO alternative).
1 1 0 0	MIPS or 8051 boots from SI interface. The MIPS is Big Endian.
1 1 0 1	Reserved.
1 1 1 0	8051 boots from SI interface (the MIPS is disabled).
1 1 1 1	No boot. SI slave is enabled.

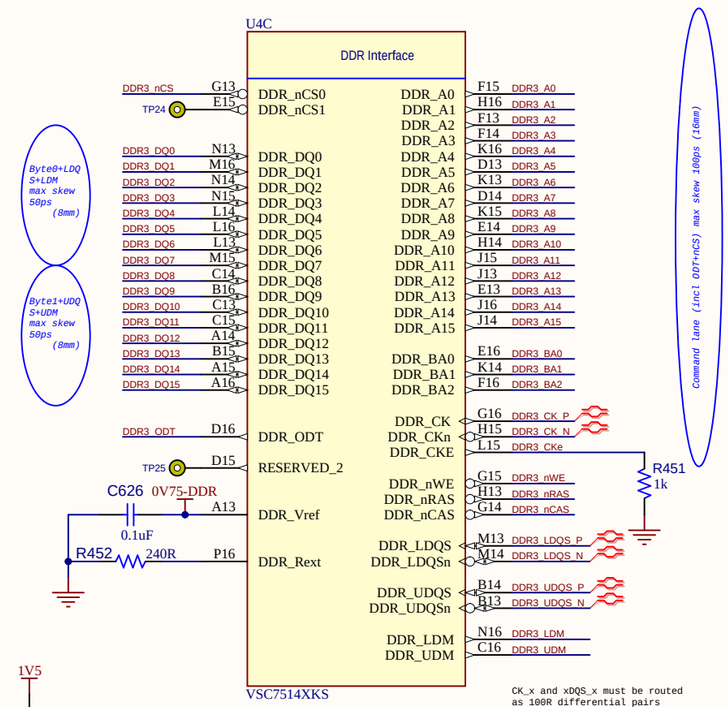
VSC7514 PLL strapping

REFCLK_SEL[2:0]	Frequency	Comment
0 0 0	125MHz	The default mode. Normal operation mode with 125MHz
0 0 1	156.25MHz	Normal operation mode with 156.25MHz ref clock
0 1 0	250MHz	Normal operation mode with 250MHz ref clock
0 1 1	N/A	Reserved
1 0 0	25MHz	Normal operation mode with 25MHz ref clock
1 0 1	N/A	Reserved
1 1 0	N/A	Reserved
1 1 1	N/A	Reserved

Due to VSC7514 jitter requirements, don't use 25MHz REFCLK as base for QSGMII

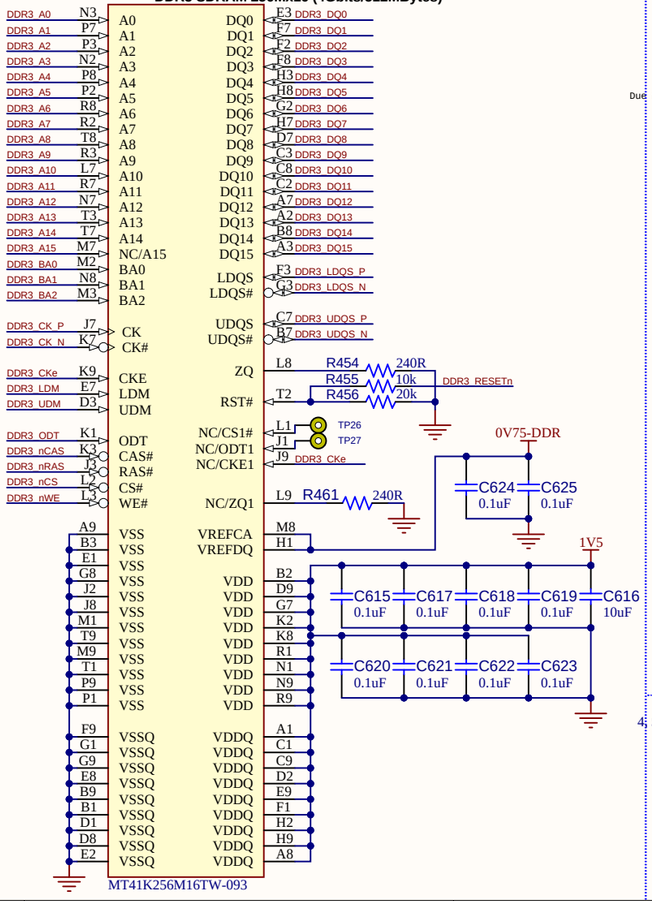


VSC7514 DDR3 RAM Interface

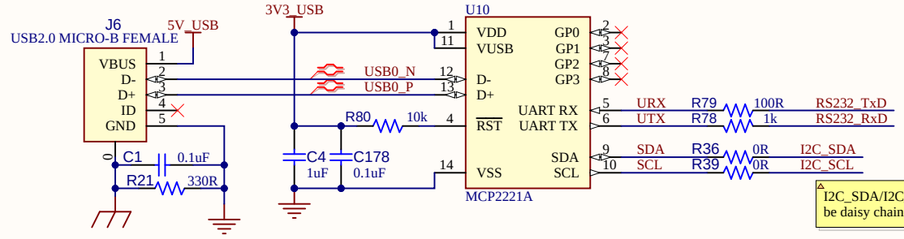


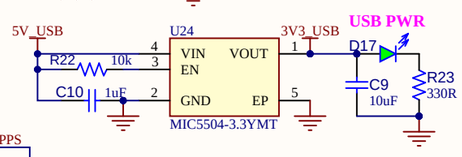
V/2 generator for SSTL-15 interface

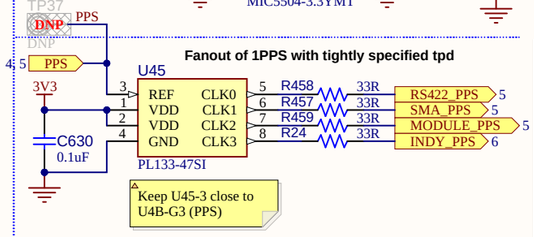
DDR3 SDRAM 256Mx16 (4Gbits/512MBytes)



UART/USB connection







Project Owner: Howard Hicks			
PCB Layout Contact: Arnaldo Cruz			
PartNumber: EV53D52A	Project Title: UNG8261 EVB-LAN8814	Variant: Standard	
Sheet Title: VSC7514 Memory, USB			
Size: Tabloid	SCH #: EVB-LAN8814	Rev: C1	Date: 5/17/2022
	PCB #: UNG8261	Rev: C0	Sheet 3 of 6
File: 3 - VSC7514 Memory, GPI.SchDoc			

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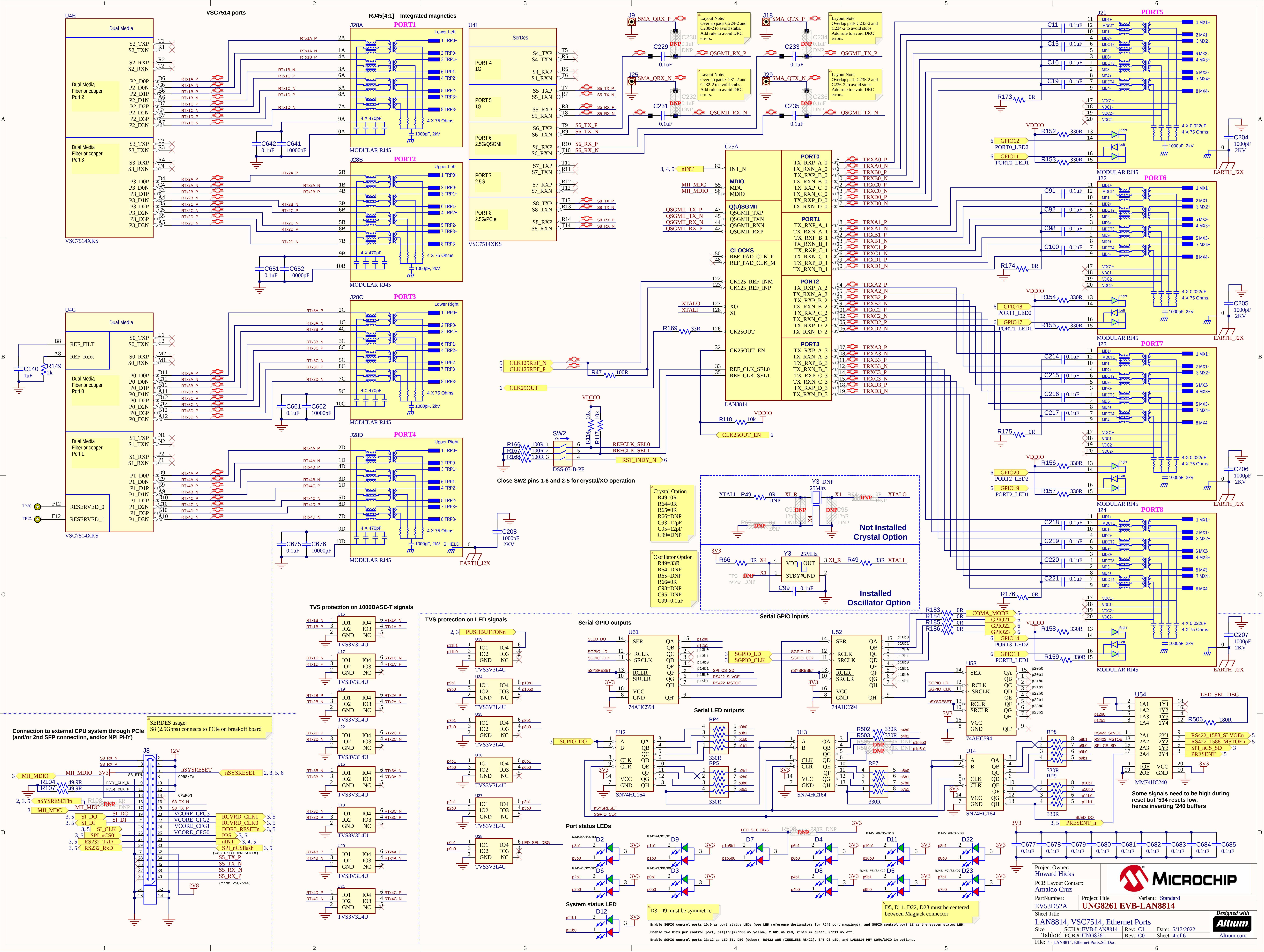

VSC7514 ports
RJ45[4:1] Integrated magnetics
Dual Media
SerDes
PORT1
PORT2
PORT3
PORT4
PORT5
PORT6
PORT7
PORT8
MODULAR RJ45
VSC7514XKS
LAN8814
Layout Note: Overlap pads C229-2 and C230-2 to avoid stubs. Add rule to avoid DRC errors.
Layout Note: Overlap pads C233-2 and C234-2 to avoid stubs. Add rule to avoid DRC errors.
Layout Note: Overlap pads C231-2 and C232-2 to avoid stubs. Add rule to avoid DRC errors.
Layout Note: Overlap pads C235-2 and C236-2 to avoid stubs. Add rule to avoid DRC errors.
Close SW2 pins 1-6 and 2-5 for crystal/XO operation
Crystal Option R49=0R R64=0R R65=0R R66=DNP C93=12pF C95=12pF C99=DNP
Not Installed Crystal Option
Oscillator Option R49=33R R64=DNP R65=DNP R66=0R C93=DNP C95=DNP C99=0.1uF
Installed Oscillator Option
TVS protection on 1000BASE-T signals
TVS protection on LED signals
Serial GPIO outputs
Serial GPIO inputs
Serial LED outputs
SERDES usage: S8 (2.5Gbps) connects to PCIe on breakoff board
Connection to external CPU system through PCIe (and/or 2nd SFP connection, and/or NPI PHY)
Port status LEDs
System status LED
D3, D9 must be symmetric
D5, D11, D22, D23 must be centered between Magjack connector
Some signals need to be high during reset but '594 resets low, hence inverting '240 buffers
Enable SGPIO control ports 10:0 as port status LEDs (see LED reference designators for RJ45 port mappings), and SGPIO control port 11 as the system status LED.
Enable two bits per control port, bit[1:0]=2'b00 => yellow, 2'b01 => red, 2'b10 => green, 2'b11 => off.
Enable SGPIO control ports 23:12 as LED_SEL_DBG (debug), RS422_xOE (IEEE1588 RS422), SPI CS uSD, and LAN8814 PHY COMA/GPIO_in options.
Project Owner: Howard Hicks
PCB Layout Contact: Arnaldo Cruz
PartNumber: EV53D52A
Project Title UNG8261 EVB-LAN8814
Variant: Standard
Sheet Title LAN8814, VSC7514, Ethernet Ports
Size Tabloid
SCH #: EVB-LAN8814 Rev: C1
PCB #: UNG8261 Rev: C0
Date: 5/17/2022
Sheet 4 of 6
File: 4 - LAN8814, Ethernet Ports.SchDoc
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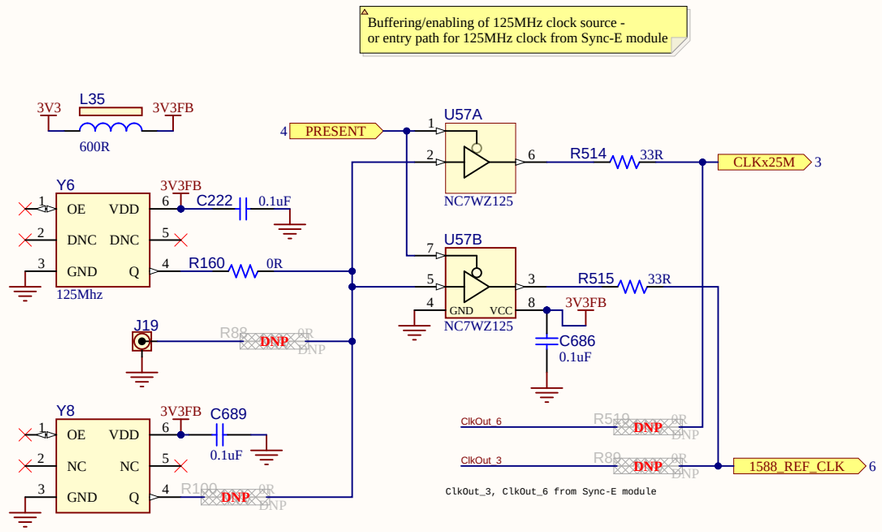
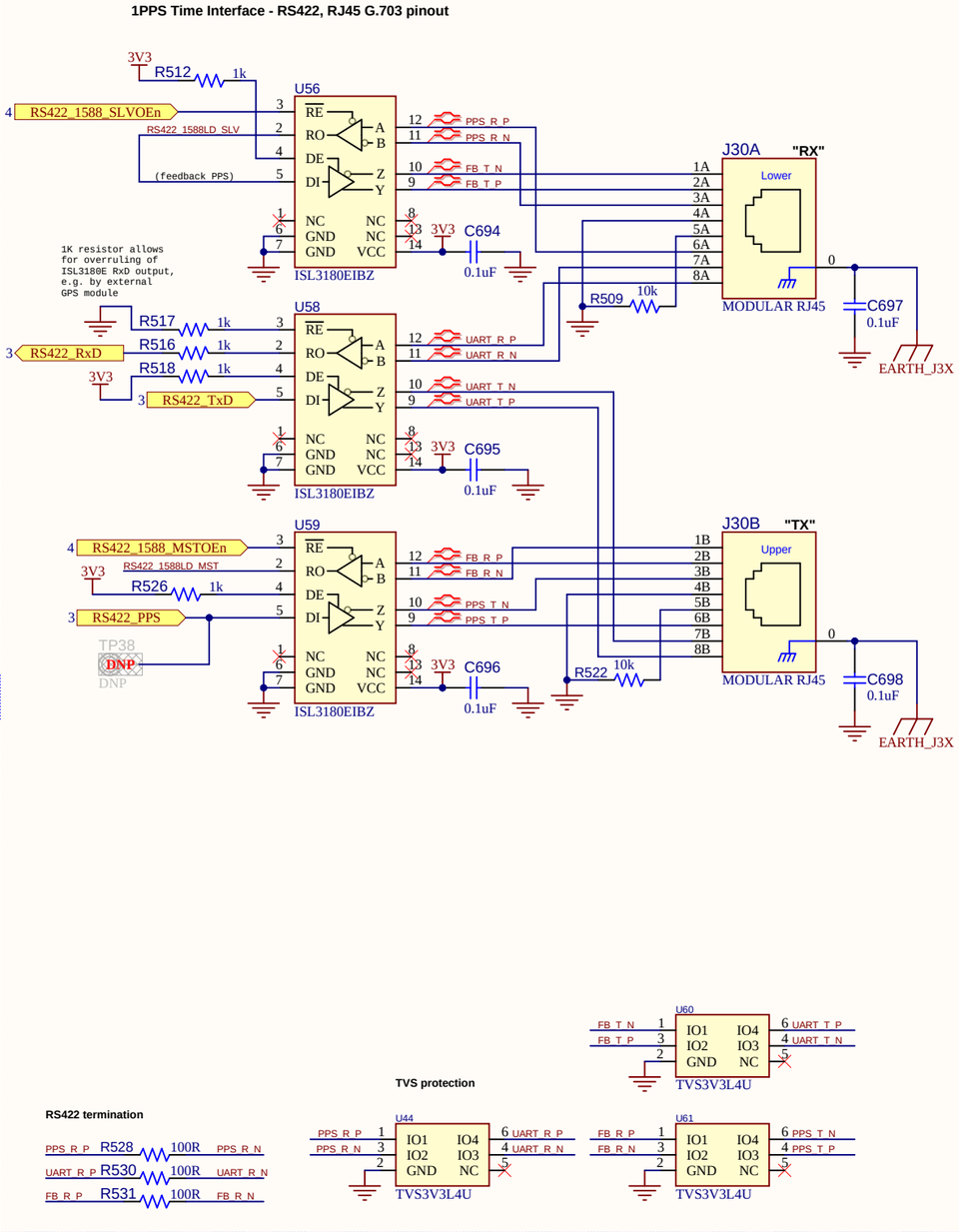
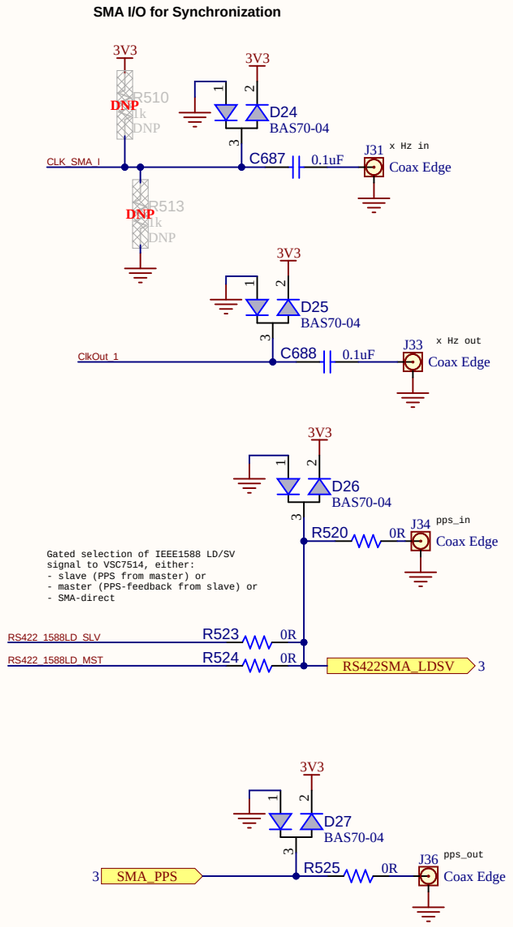
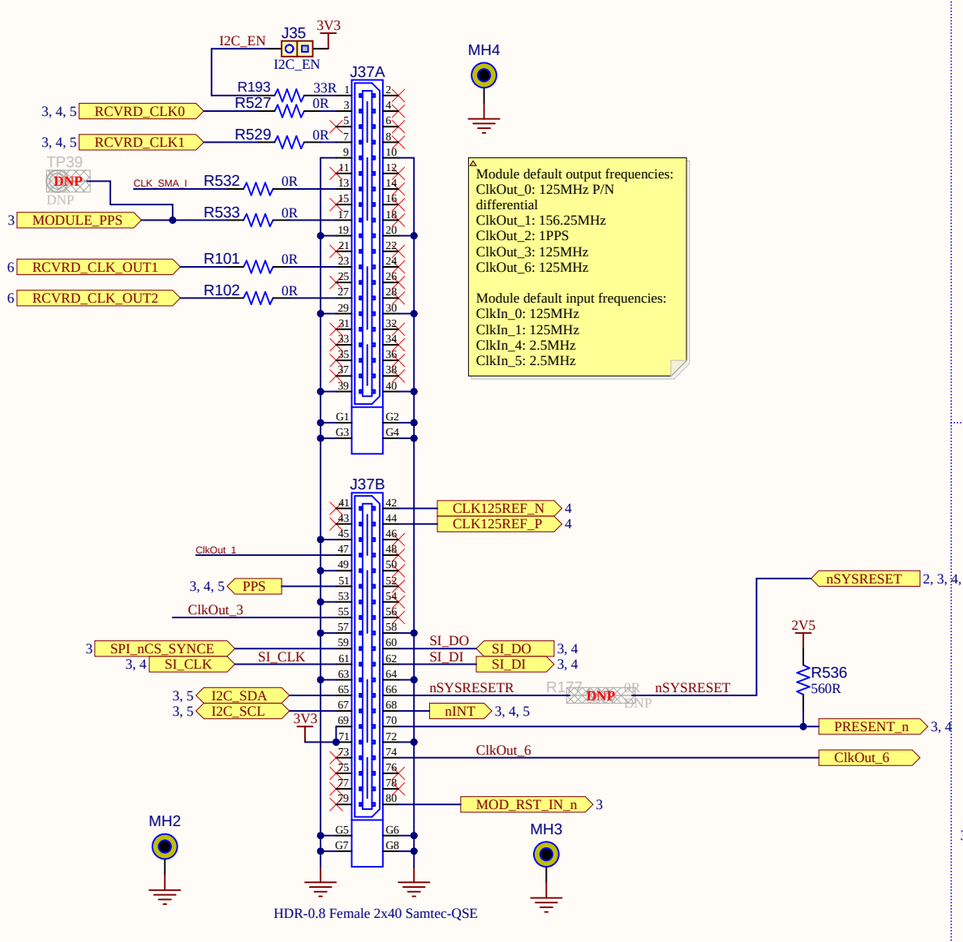
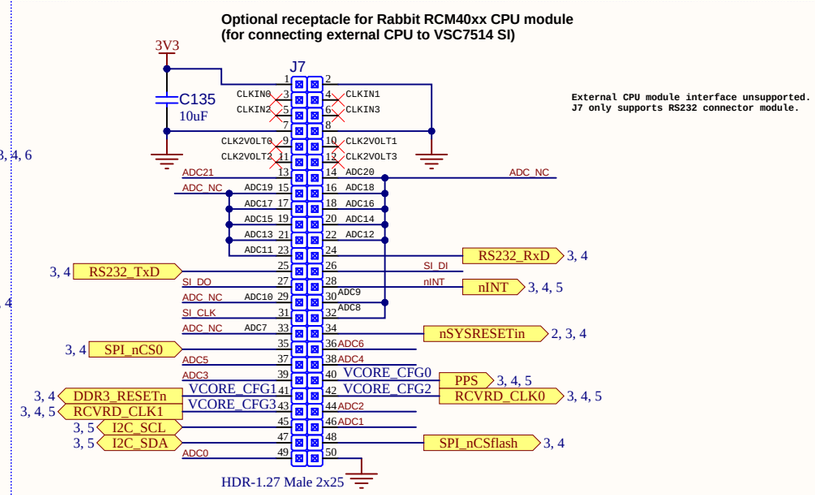
MICROCHIP

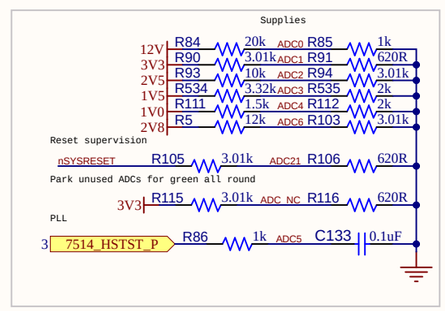






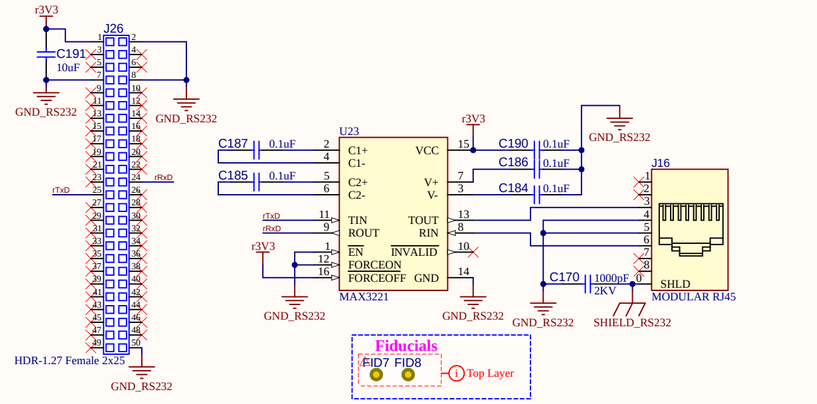




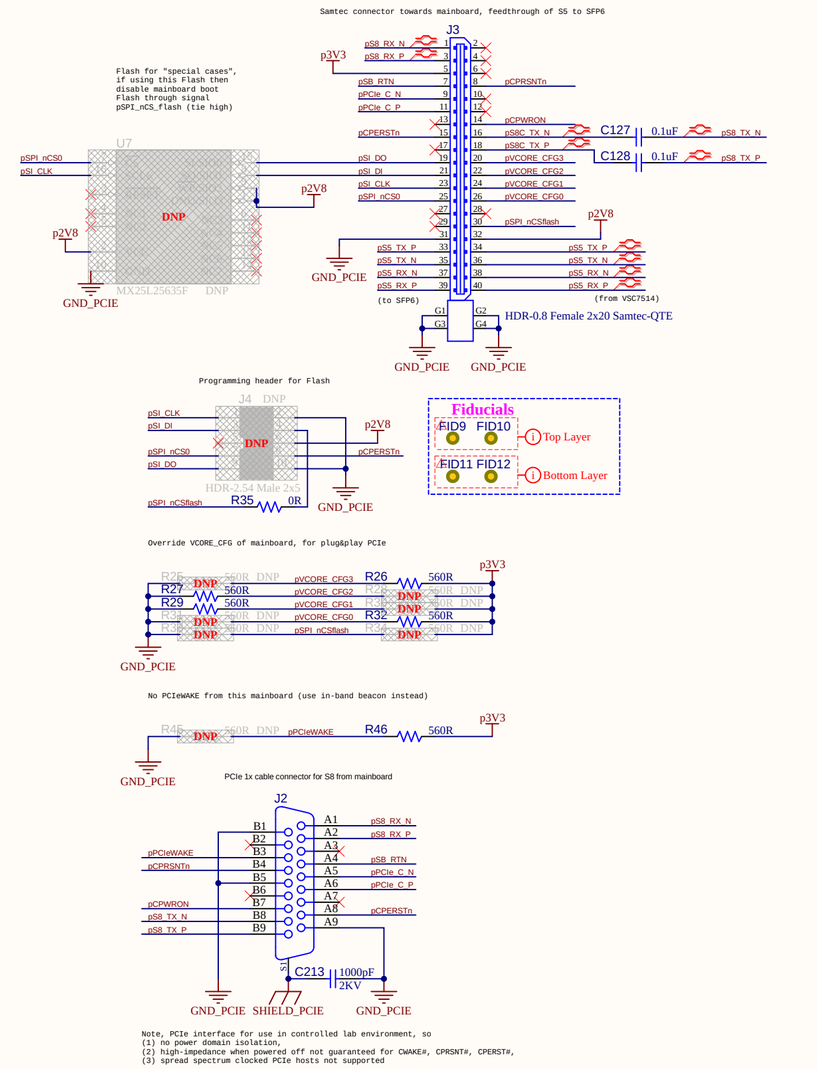


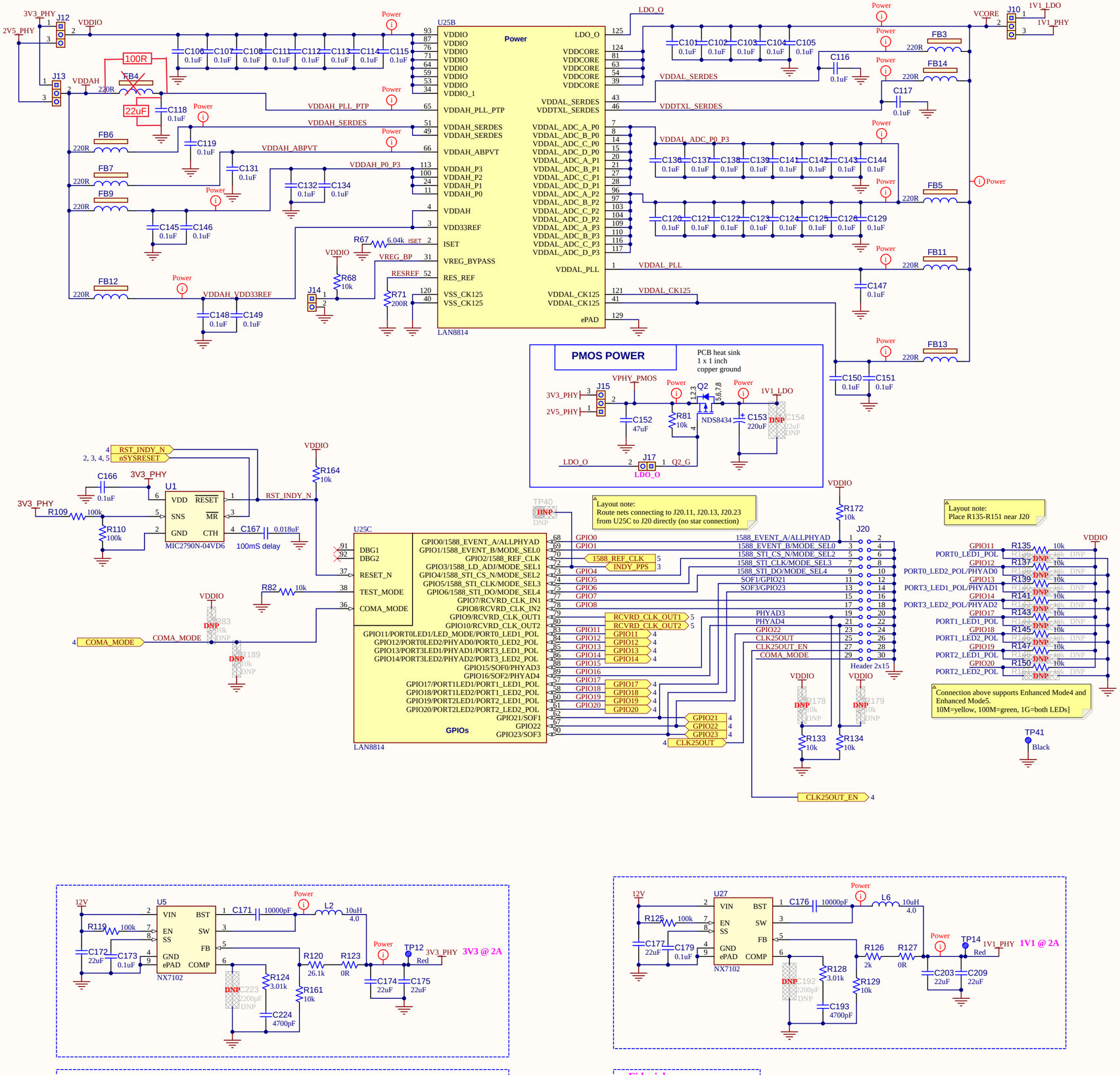
Project Owner: Howard Hicks		MICROCHIP
PCB Layout Contact: Arnaldo Cruz		
PartNumber: EV53D52A	Project Title: UNG8261 EVB-LAN8814	Variant: Standard
Sheet Title: Clocks, 1588, SyncE Connector		Designed with Altium
Size: Tabloid	SCH #: EVB-LAN8814 / PCB #: UNG8261	Rev: C1 / C0 — Date: 5/17/2022 — Sheet 5 of 6
File: 5 - Clocks, 1588, SyncE.SchDoc		Altium.com

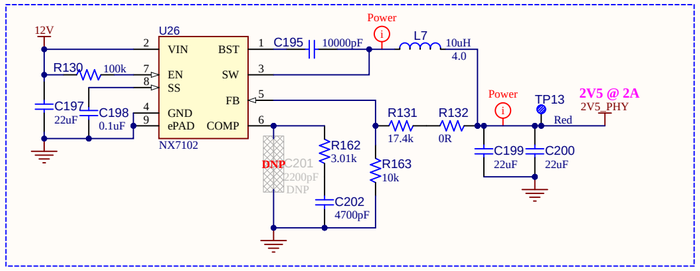
Breakoff board with RS232 port for old-school management

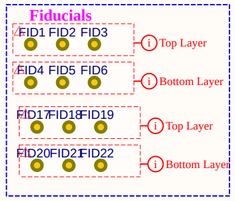


Breakoff board for connecting PCIe cable to mainboard S8 (SFP6 is 1Gbps S5)









Project Owner: Howard Hicks			
PCB Layout Contact: Arnaldo Cruz			
PartNumber: EV53D52A	Project Title: UNG8261 EVB-LAN8814	Variant: Standard	
Sheet Title: LAN8814 GPIOs, DC-DC Converters, Breakoffs			
Size: Tabloid	SCH #: EVB-LAN8814	Rev: C1	Date: 5/17/2022
	PCB #: UNG8261	Rev: C0	Sheet 6 of 6
File: 6 - LAN8814 GPIOs, Regulators, Breakoffs.SchDoc			

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