EV3921-U-00A

Single-Port, IEEE 802.3af/at PSE Controller for Power over Ethernet Evaluation Board

DESCRIPTION

The EV3921-U-00A is an evaluation board designed to demonstrate the capabilities of the MP3921, a single-port power-sourcing equipment (PSE) power controller for IEEE 802.3af/at-compliant power over Ethernet (PoE) applications.

The MP3921 provides all the functions of IEEE 802.3af/at, including detection, single-event and two-event classification, current limiting, and disconnected load detection. All the functions can be configured to work in automatic mode or software configuration mode via the I^{2}C.

The MP3921 features a 9-bit analog-to-digital converter (ADC) to monitor the current and voltage, a special I^{2}C interface for isolated controller communication, adjustable current limits, and configurable system functions. These features provide flexibility for PoE applications.

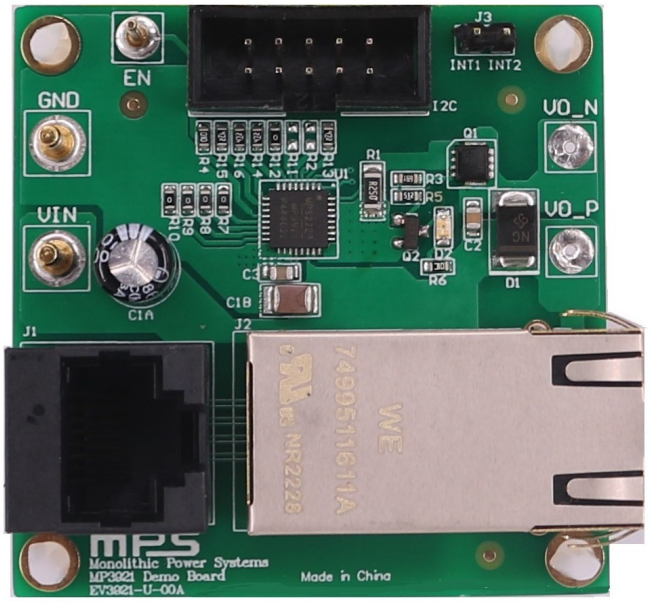
The MP3921 is available in a QFN-32 (5mmx5mm) package. It is recommended to read the MP3921 datasheet prior to making any changes to the EV3921-U-00A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		44V to 57V
Output voltage (V_{OUT})	V_{IN} = 44V to 57V	0V to 57V
Output power (P_{OUT})	V_{IN} = 44V to 57V	0W to 30W

EV3921-U-00A EVALUATION BOARD



LxWxH (5.1cmx5.1cmx2.3cm)

Board Number	MPS IC Number
EV3921-U-00A	MP3921GU

QUICK START GUIDE

The EV3921-U-00A evaluation board is easy to set up and use to evaluate the MP3921's performance. For proper measurement equipment set-up, refer to Figure 1 and follow the steps below:

1. Preset the power supply between 44V and 57V, then turn the power supply off.
2. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
3. After making the connections, turn the power supply on.
4. Connect the powered device (PD) to the RJ45 jack. The MP3921 starts up the PD automatically.

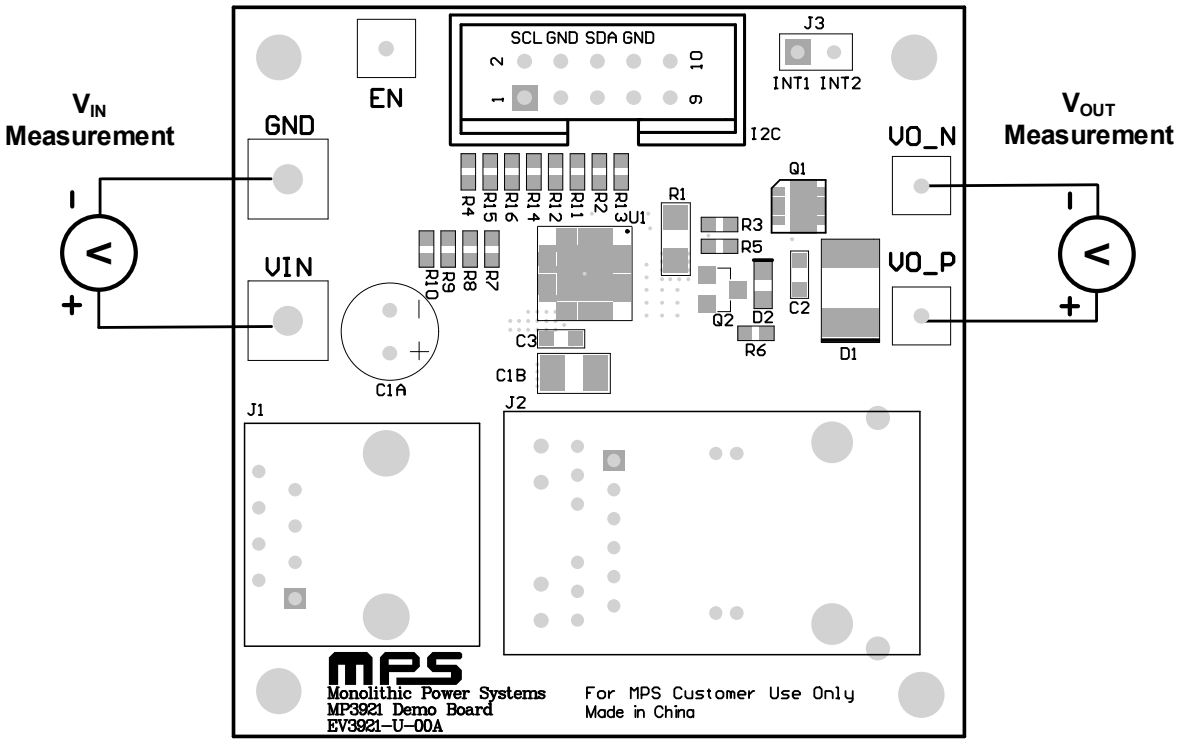


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

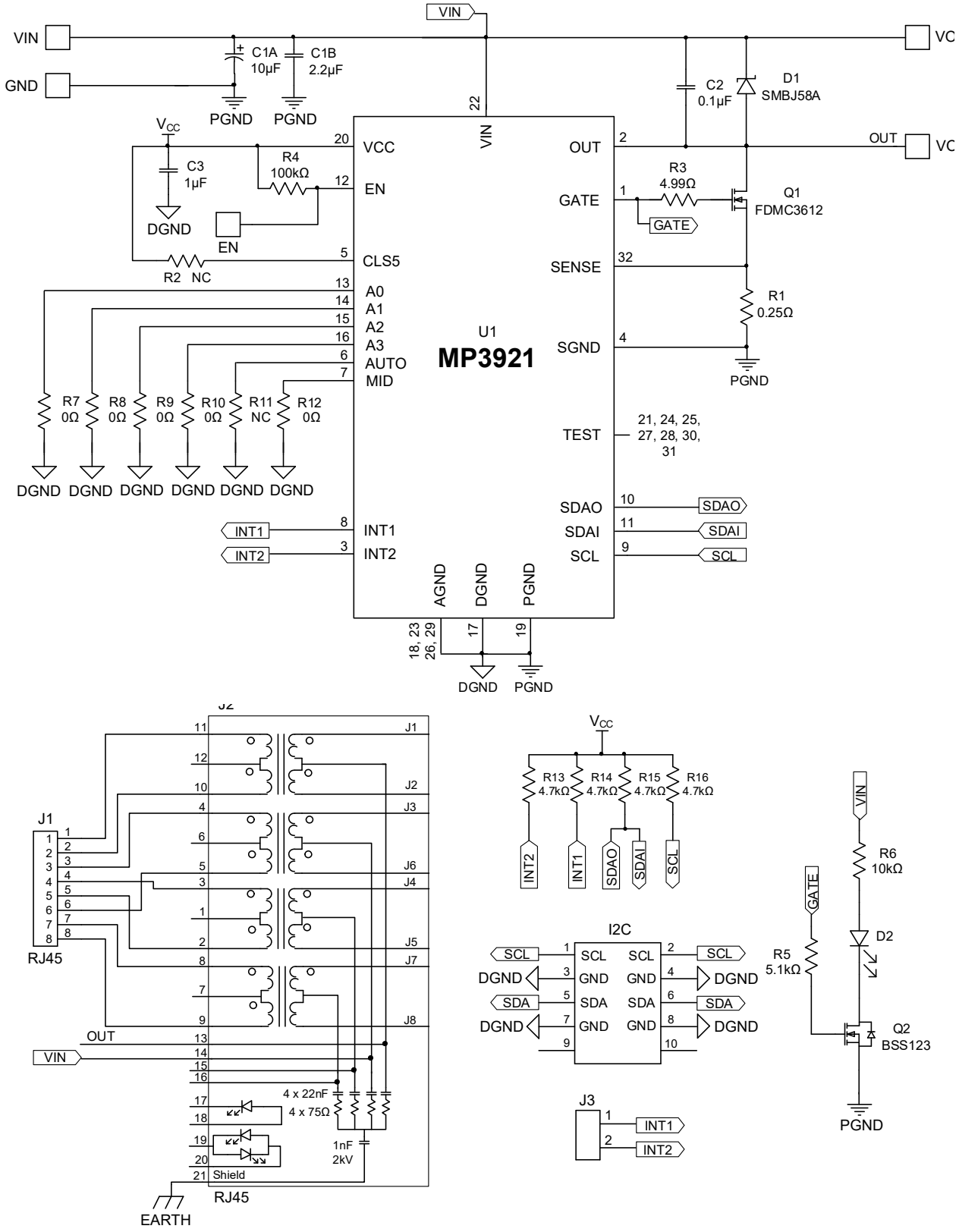


Figure 2: Evaluation Board Schematic

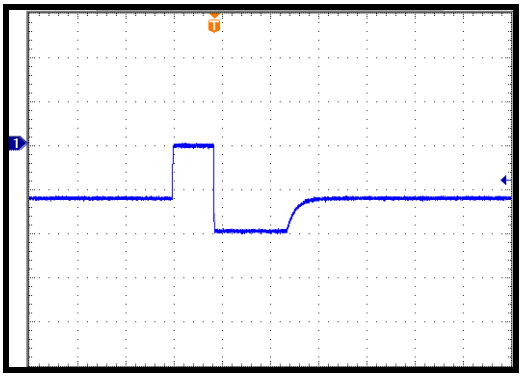
EV3921-U-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1A	10µF	Electrolytic capacitor, 100V, CD286	DIP	Jianghai	ECR2AGK100M063011
1	C1B	2.2µF	Ceramic capacitor, 100V, X7R	1210	TDK	C3225X7R2A225K230AB
1	C2	0.1µF	Ceramic capacitor, 100V, X7R	0805	TDK	C2012X7R2A104K125AA
1	C3	1µF	Ceramic capacitor, 10V, X7R	0805	Wurth	885012207022
2	R2, R11	NC				
1	D1	58V	TVS diode	SMB	Diodes, Inc.	SMBJ58A
1	D2	30mA	Red LED	0805	Wurth	150080RS75000
1	J1	1.5A	Jack modular connector (RJ45), female, WR-MJ, plastic	DIP	Wurth	615008138021
1	J2	600mA	Modular connector (RJ45), Int XFMR	DIP	Wurth	7499511611A
1	J3	2.54mm	Connector, 2-pin	DIP	Wurth	61300211121
1	I2C	2.54mm	I^2C connector, 10-pin	DIP	Wurth	612010235121
1	Q1	100V	N-channel MOSFET, 12A	Power-33-8	Fairchild	FDMC3612
1	Q2	100V	N-channel MOSFET, 170mA	SOT-23	Fairchild	BSS123
1	R1	0.25Ω	Film resistor, 1%	1206	Yageo	PT1206FR-070R25L
1	R3	4.99Ω	Film resistor, 1%	0603	Yageo	RC0603FR-074R99L
1	R4	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R5	5.1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-075K1L
1	R6	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
5	R7, R8, R9, R10, R12	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
4	R13, R14, R15, R16	4.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-074K7L
1	U1	MP3921	Single-port, IEEE 802.3af/at PSE controller	QFN-32 (5mmx5mm)	MPS	MP3921GU

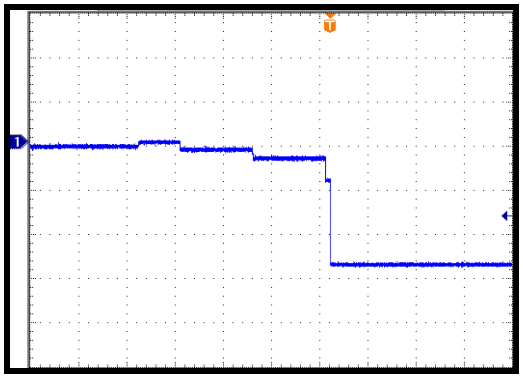
EVB TEST RESULTS

V_{IN} = 54V, set with a Class 4 PD load, T_A = 25°C, unless otherwise noted.

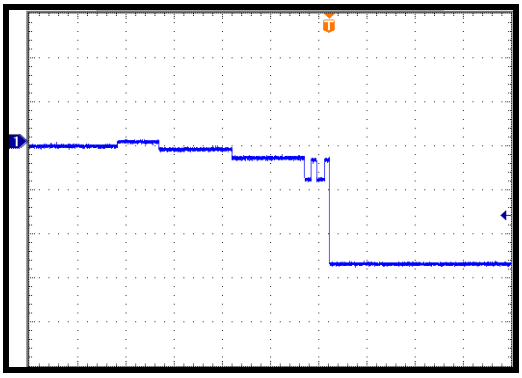
No PD Connection



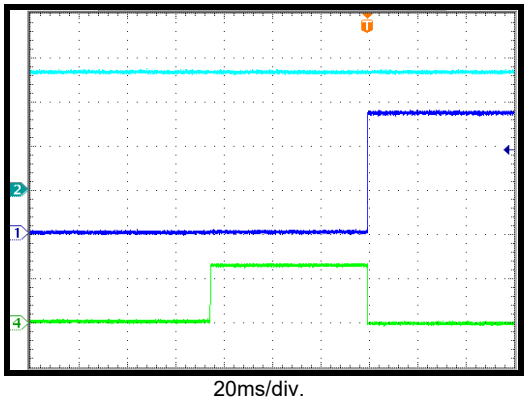
Class 0 to Class 3 PD Connection



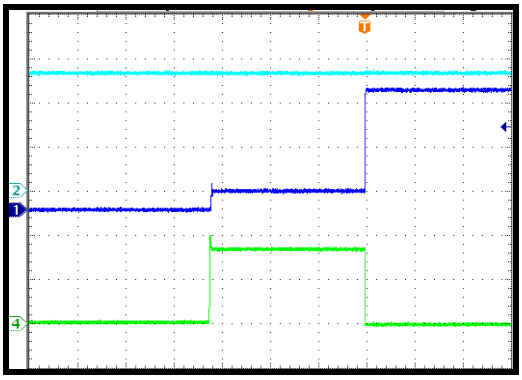
Class 4 PD Connection



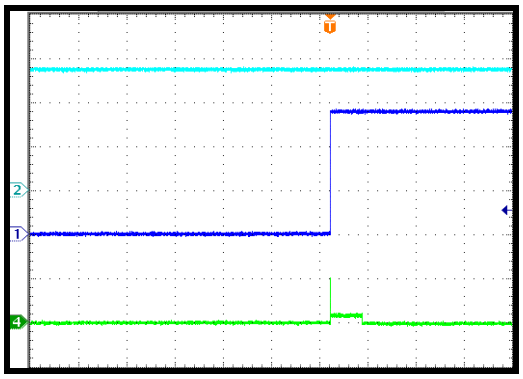
ICUT Triggered



ILIM Triggered



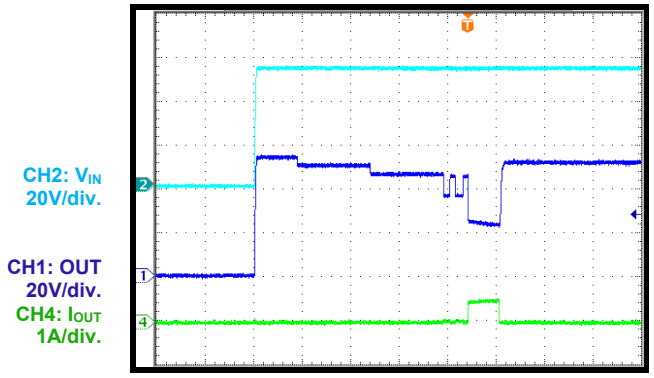
Output SCP Triggered



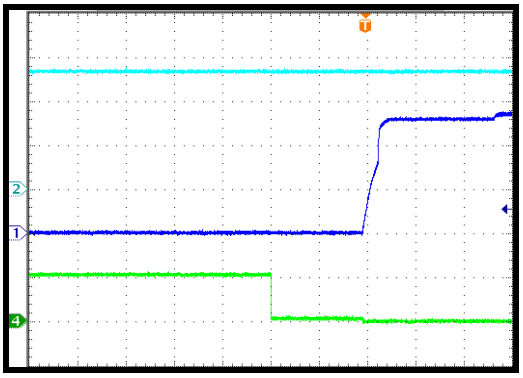
EVB TEST RESULTS *(continued)*

V_{IN} = 54V, set with a Class 4 PD load, T_A = 25°C, unless otherwise noted.

Inrush Current Limit Triggered



Output Disconnection Triggered



PCB LAYOUT

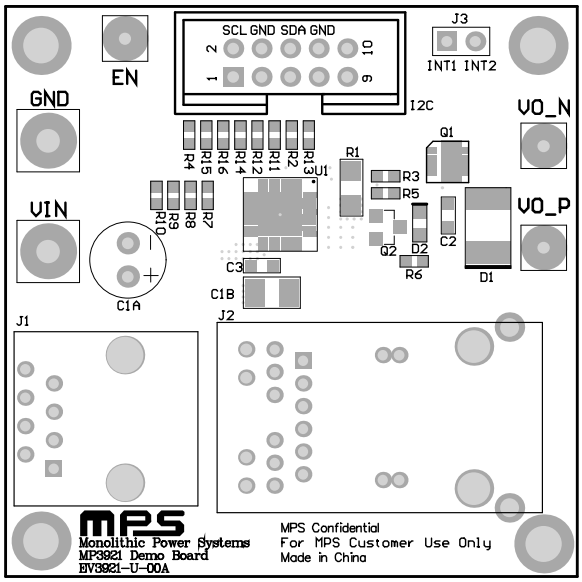


Figure 3: Top Silk

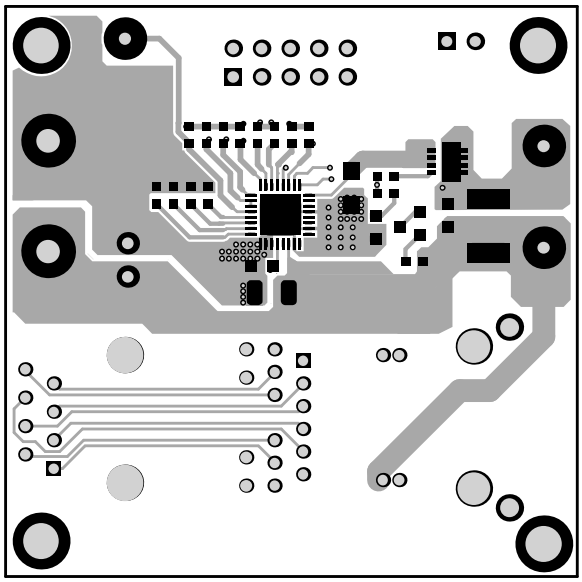


Figure 4: Top Layer

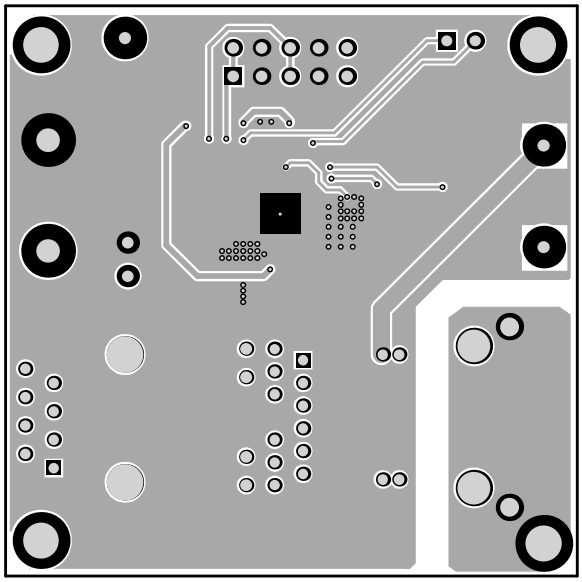


Figure 5: Bottom Layer

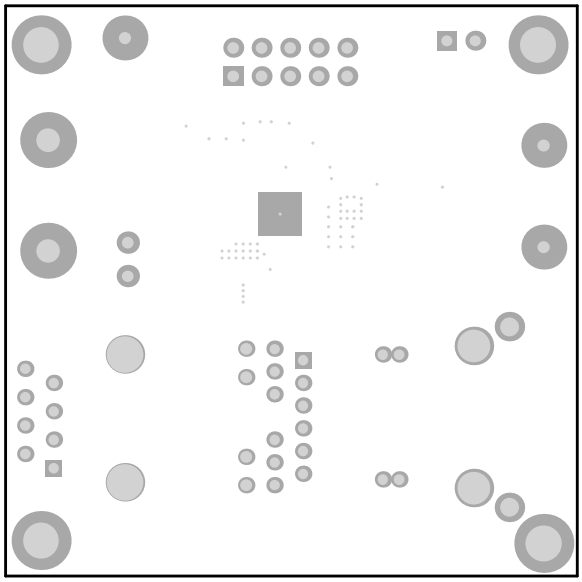


Figure 6: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/15/2024	Initial Release	-